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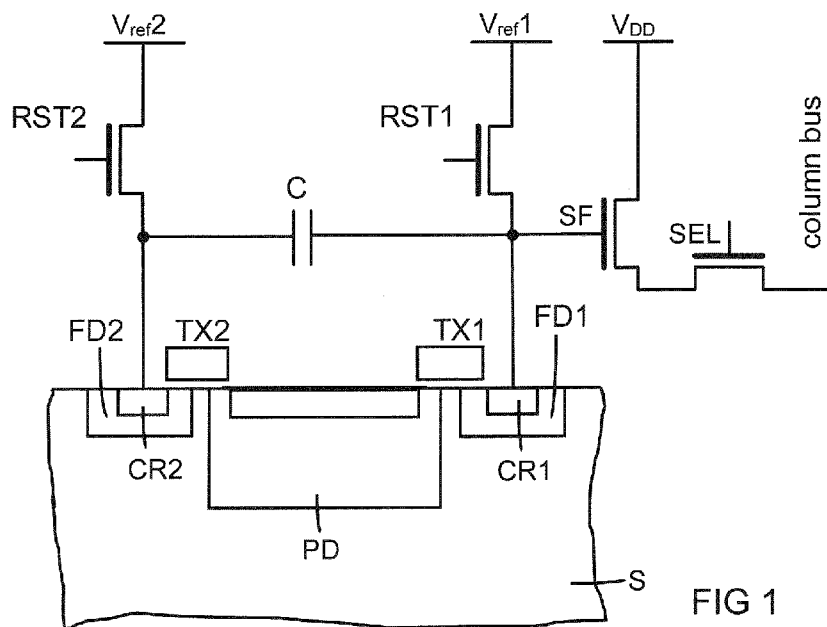


FIG 1

(57) Abstract: A photodetector (PD) in semiconductor material (S) is provided with a first transfer gate (TX1) between the photodetector and a first diffusion region (FD1) in the semiconductor material, a second transfer gate (TX2) between the photodetector (PD) and a second diffusion region (FD2) in the semiconductor material, a capacitor (C) connected between the first diffusion region (FD1) and the second diffusion region (FD2), a first switch (RST1) connected between the first diffusion region (FD1) and a first reference voltage (V_{ref1}), and a second switch (RST2) connected between the second diffusion region (FD2) and a second reference voltage (V_{ref2}).



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Description

PIXEL STRUCTURE, IMAGE SENSOR DEVICE AND SYSTEM WITH PIXEL
STRUCTURE, AND METHOD OF OPERATING THE PIXEL STRUCTURE

5

The present disclosure applies to the field of three-dimensional imaging, especially differential imaging.

Active stereovision systems make use of a projector and at
10 least one image sensor. Typically the projector projects a
structured light pattern that is composed of dots, lines or
other shapes which are projected on the scene by infrared
light, which may typically have a wavelength of 940 nm, for
instance. The pattern is then recorded by a global-shutter
15 two-dimensional image sensor including a two-dimensional
matrix of pixels. The image sensor may be optimized for a
good response at the used wavelength.

The light pattern can be projected by a strong light source,
20 such as a VCSEL (vertical-cavity surface-emitting laser)
during a short time. The maximum emitted light power is
constrained by eye safety limitations and by the maximal
power that can be output by the VCSEL at a specified duty
cycle. Usually short pulses of few microseconds to few
25 milliseconds are used. A pattern is created, e.g. by a mask,
which is projected by an optical system (e.g. a lens and/or an
optical diffractive element) onto the scene.

A two-dimensional camera records the projected pattern. The
30 position of the pattern as seen in the recorded image depends
on the distance of the objects to the camera and projector.
By triangulation the distance can be recorded. Other
computation techniques may involve deep learning, for example

in a case where the projected patterns changes appearance depending on object distance, thanks to some optical effect like focus distance or interference.

5 Some systems use two cameras and employ stereovision to make a depth map. A pattern is projected to create some contrast in the scene. This may be needed for objects without much texture, e.g. a painted wall. In those cases a flashed illumination is used.

10

In the above described stereovision and structured light cases, the light is pulsed and illuminated only during short time. The image sensor works in 'global shutter' mode. Before the flash, all pixels are reset and start integrating light.

15 Then the pattern is projected. After the light pulse, the exposure time stops. In the pixels, the signal from the photodiode is sampled on an in-pixel memory. That memory is then read out row-by-row after the exposure time. This is a typical way of operation of global shutter image sensors, in
20 so-called 'triggered global shutter mode'.

A rolling shutter pixel can instead be used. Because of the significantly larger contribution of background light to the captured signal, fast readout and off-chip data buffer
25 storage are required.

Background image subtraction can be used to improve the contrast in the image. A second image is captured with the same exposure time but without projected light. The
30 differential image is then calculated by software. The subtraction operation is preferably executed inside the pixel during the image acquisition phase. It is favourable if multiple image acquisitions can be accumulated in the pixel,

because a large amount of acquisition cycles enables to enhance the signal-to-noise ratio. After each image acquisition, the signal corresponding to the difference between the images with and without structured light projection remains stored in the pixel. Signals from successive subtraction operations are thus accumulated in the pixel.

US 8 569 671 B2 discloses a pixel comprising a photo-sensitive element for generating charges in response to incident radiation. A transfer gate is positioned between the photo-sensitive element and a sense node for controlling transfer of charges to the sense node. A reset switch is connected to the sense node for resetting the sense node to a predetermined voltage. A first buffer amplifier has an input connected to the sense node. A sample stage is connected to the output of the first buffer amplifier and is operable to sample a value of the sense node. A second buffer amplifier has an input connected to the sample stage. Control circuitry operates the reset switch and causes the sample stage to sample the sense node while the photo-sensitive element is being exposed to radiation. An array of pixels is synchronously exposed to radiation. Sampled values for a first exposure period can be read while the photo-sensitive element is exposed for a second exposure period.

It is an object of the present invention to provide improved differential imaging.

This object is achieved with the pixel structure for a semiconductor imaging device according to claim 1, the image sensor device with pixel array according to claim 9 the imaging system according to claim 10, and the method of

operating the pixel structure according to claim 13.

Embodiments and variants derive from the dependent claims.

The definitions as described above also apply to the

5 following description unless stated otherwise.

The pixel structure for a semiconductor imaging device comprises a photodetector in a semiconductor material, a first transfer gate between the photodetector and a first
10 diffusion region in the semiconductor material, a second transfer gate between the photodetector and a second diffusion region in the semiconductor material, a capacitor connected between the first diffusion region and the second diffusion region, a first switch connected between the first
15 diffusion region and a first reference voltage, and a second switch connected between the second diffusion region and a second reference voltage.

In an embodiment of the pixel structure, the photodetector is
20 a pinned photodiode in a substrate comprising the semiconductor material.

A buffer amplifier is connected to one of the diffusion regions to read out the pixel. In a further embodiment,
25 buffer amplifiers are connected to the first diffusion region and the second diffusion region. In such an embodiment there may also be an additional anti-blooming gate connected to the photodetector to avoid carriers flowing into the diffusion region after the exposures.

30

In a further embodiment, the first reference voltage and the second reference voltage are equal, in particular equal to a

supply voltage. The first reference voltage or the second reference voltage may be connected to a supply voltage.

In a further embodiment, a select transistor is connected to
5 a column bus. A source follower formed by a field-effect transistor can be connected to the select transistor, a gate of the source follower being connected to the first diffusion region. This is a possible way of implementing the buffer amplifier.

10

The image sensor device comprises a two-dimensional array of such pixel structures.

The imaging system including such an image sensor device
15 further comprises a light source synchronized to the image sensor device, the light source being configured to be active when the signal is acquired on the first diffusion region and not active when the signal is acquired on the second diffusion region. The light source may instead be configured
20 to be active when the signal is acquired on the second diffusion region and not active when the signal is acquired on the first diffusion region. In particular, the light source can be configured to project a pattern or sequence of patterns on a scene to be imaged.

25

The method of operating the pixel structure comprises discharging the capacitor by closing both the first switch and the second switch into a connecting state, acquiring a first signal on the photodetector and transferring the first
30 signal to the first diffusion region by a charge transfer pulse on the first transfer gate, while the second switch is closed in a connecting state, acquiring a second signal on the photodetector and transferring the second signal to the

second diffusion region by a charge transfer pulse on the second transfer gate, while the first switch is closed in a connecting state, and after acquisition of the signals, reading the pixel signal out from the first diffusion region while the second diffusion region is connected to the second reference voltage via the second switch.

In a variant of the method, the second transfer gate is at a higher electric potential than the first transfer gate during readout of the pixel signal.

Using the method, first and second signals can repeatedly be acquired and accumulated on the capacitor.

In a further variant of the method, the charge transfer pulse on the first transfer gate, the charge transfer pulse on the second transfer gate, or each of the charge transfer pulses is a multiple pulse, so that the corresponding transfer gate is pulsed several times during the same charge transfer operation.

The following is a detailed description of examples of the pixel structure in conjunction with the appended figures.

Figure 1 shows a pixel circuit including a schematical cross section of a pinned photodiode.

Figure 2 shows a circuit diagram of the pixel circuit according to Figure 1.

Figure 3 is a timing diagram for the pixel structure.

Figure 4 is a timing diagram according to Figure 3 for control of the maximal amount of stored charges.

5 Figure 5 is an alternative timing diagram according to Figure 3 for voltage control.

Figure 6 is an alternative timing diagram according to Figure 5 for repeated pulsing of the transfer gate(s).

10 Figure 7 is a layout example with a capacitor comprising interdigitated conductor tracks.

Figure 8 is a layout example with a plate capacitor.

15 Figure 9 is a layout example with a plate capacitor and both transfer gates on the same side.

Figure 1 shows an example of the pixel structure. The circuit of the pixel structure includes a schematical cross section of a semiconductor photodetector device, which can be used for the pixel structure. A photodetector PD, which may be a pinned photodiode, for example, is integrated in semiconductor material S, in particular in a semiconductor substrate, which may comprise silicon, for instance. The photodetector PD can be connected with a first diffusion region FD1 in the semiconductor material S via a first transfer gate TX1 and with a second diffusion region FD2 in the semiconductor material S via a second transfer gate TX2.

20
25
30 The diffusion regions FD1, FD2 may be arranged on opposite sides of the photodetector PD and may be provided with a first contact region CR1 and a second contact region CR2, respectively. The contact regions CR1, CR2 may have a higher

doping concentration to enable the formation of an ohmic contact for external electric connections.

Typically the substrate may be composed of a bulk silicon
5 wafer (e. g. p++ doped) with an epitaxial layer (e. g. p-,
 $5 \times 10^{14} \text{ cm}^{-3}$). The pinned photodiode may comprise a p++ shallow
surface implant and a deeper n-type implant. The first
contact region CR1 and the second contact region CR2 may be
highly doped (e. g. $5 \times 10^{19} \text{ cm}^{-3}$) n-type implants. They may be
10 surrounded by lower doped n-type implants, and may or may not
be located in a p-well area (which may be typically doped
with a doping concentration of about $1 \times 10^{17} \text{ cm}^{-3}$).

The diffusion regions FD1, FD2 are electrically connected
15 with each other via a capacitor C, which may typically have a
capacitance of about 15 fF, for instance. The first diffusion
region FD1 is also connected to a first reference voltage
 V_{ref1} via a first switch RST1, and the second diffusion region
FD2 is also connected to a second reference voltage V_{ref2} via
20 a second switch RST2. The first and second switches RST1,
RST2 can be field-effect transistors, for instance. The first
reference voltage V_{ref1} and the second reference voltage V_{ref2}
may be equal or different.

25 The first diffusion region FD1 is further connected to a
buffer amplifier. This could be a source follower SF as shown
in Figure 1. The first diffusion region FD1 may in this case
especially be connected to the gate of a further field-effect
transistor, for instance. The source follower SF connects a
30 supply voltage V_{DD} with a source/drain terminal of a select
transistor SEL. The other source/drain terminal of the select
transistor SEL is connected with a column bus for read-out.
The supply voltage V_{DD} may in particular be used as the first

reference voltage V_{ref1} and the second reference voltage V_{ref2} . The source follower SF and the select transistor SEL may also be integrated in the semiconductor material S. Alternatively to the source follower, a junction FET could be used, or a
5 differential amplifier configuration could be used.

Figure 2 shows a complete circuit diagram of the pixel circuit according to Figure 1. The node of the first diffusion region FD1 has a first parasitic capacitance Cfd1,
10 and the node of the second diffusion region FD2 has a second parasitic capacitance Cfd2. It is advantageous if the parasitic capacitances Cfd1, Cfd2 are equal and as small as possible. The capacitance of the capacitor C is considerably larger than the first and second parasitic capacitances Cfd1,
15 Cfd2. Typical values of the first and second parasitic capacitances Cfd1 and Cfd2 could be in the range from 1 fF to 4 fF. Techniques could be used to reduce the parasitic capacitances. Each of these parasitic capacitances Cfd1 and Cfd2 is composed of the junction capacitance of the diffusion
20 region, the gate-drain overlap capacitance of the transfer gates, the input capacitance of the buffer amplifier and the gate-drain overlap capacitance of the reset transistor. The overlap capacitances could be reduced by dedicated implant schemes, e. g. with modifications of dopant concentrations at
25 lightly doped drain areas (LDDs) located adjacent to the gate under the gate spacer region. The junction capacitance and junction sidewall capacitance in particular can be changed by reducing the doping of the p-well under the n+ diffusion area, or by using a moderately doped n-type diffusion
30 surrounding the higher doped n++ ohmic contact area. The latter is shown in Figure 1. The capacitance of the buffer amplifier can be reduced by the input transistor topology. E. g. a buried channel source follower or JFET could be used

with lower input capacitance. Both devices have the additional benefit that they have lower $1/f$ and random-telegraph-signal noise, which is also a benefit to reduce the read noise of the pixel.

5

Charges are dumped for successive frames consecutively on the first diffusion region FD1, while the second diffusion region FD2 is kept at the second reference voltage $V_{\text{ref}2}$ via the second switch RST2, and on the second diffusion region FD2, while the first diffusion region FD1 is kept at the first reference voltage $V_{\text{ref}1}$ via the first switch RST1. The reference voltages $V_{\text{ref}1}$ and $V_{\text{ref}2}$ are chosen such that the signal swing on nodes FD1 and FD2 can be maximized.

15 An image with active illumination (e. g. when a structured light pattern is projected) may be integrated using the first diffusion region FD1, while a background reference image may be integrated using the second diffusion region FD2. In this case the signal at the first diffusion region FD1 will drop faster than the signal at the second diffusion region FD2. After several acquisitions of illuminated and background reference images, as per the later described timing diagrams, where the illuminated image is always transferred to FD1 and the background reference voltage is always transferred to FD2, the voltage on FD1 will drop below $V_{\text{ref}1}$ and the voltage on FD2 will rise above $V_{\text{ref}2}$. It is then beneficial to use a low voltage for $V_{\text{ref}2}$ and a high voltage for $V_{\text{ref}1}$. It should be ensured that the voltage levels on FD1 and FD2 are always higher than the depletion voltage of the pinned photodiode at the moment that the respective transfer gate TX1 or TX2 is opened. This is needed to guarantee a charge transfer of all carriers from the photodiode to the nodes FD1 and FD2.

Figure 3 shows a timing diagram for this pixel structure. The operation of the pixel structure is synchronously performed with the operation of a structured-light projector for multiple image acquisitions in global shutter mode. A first
5 image is taken under structured-light conditions. The photocarriers from this image exposure are integrated on the photodiodes of the pixel. The photodiode is then read out by a charge transfer through the first transfer gate TX1 with the first switch RST1 in its disconnecting state and the
10 second switch RST2 in its connecting state, so that the signal is transferred to the first diffusion region FD1. The first diffusion region FD1 is thus floating when the first switch RST1 is in its disconnecting state. The diffusion region must be floating when the corresponding transfer gate
15 is operated. A further image is taken without structured light. The photocarriers are again integrated on the photodiode. The photodiode is then read out by a charge transfer through the second transfer gate TX2 with the first switch RST1 in its connecting state and the second switch
20 RST2 in its disconnecting state, so that the signal is transferred to the second diffusion region FD2.

The first and second switches RST1, RST2 are alternately operated to remove the common mode signal corresponding to
25 the background light. The first switch RST1 is in its connecting state only when the second switch RST2 is in its disconnecting state and vice versa, in order to prevent the capacitor C from being discharged. The driving circuits should guarantee that the RST1 and RST2 signals are non-
30 overlapping, in order to avoid this discharge. Only at the start of the image acquisition process, both switches are switched on together, in order to reset the capacitor C.

After the time period of exposure, the differential image is read out from the first diffusion region FD1 using the source follower SF and the select transistor SEL. For this purpose, the first switch RST1 is in its disconnecting state, and the
5 second switch RST2 is in its connecting state, so that the second diffusion region FD2 is at least approximately on the second reference voltage V_{ref2} , and the first diffusion region FD1 provides the stored signal. The voltage at the second transfer gate TX2 is higher than the voltage at the first
10 transfer gate TX1, and the second transfer gate TX2 is acting as anti-blooming drain during readout. When the photodetector PD saturates, excess charge is removed by means of the second transfer gate TX2 and the second switch RST2. Alternatively, the second transfer gate TX2 could be in a high state during
15 readout.

The pixel can also be operated as a standard rolling shutter pixel, by not clocking the transfer gate TX2 and the second switch RST2.

20

Figure 4 shows a further timing diagram. The timing according to this diagram allows to control the maximal amount of charges to be stored on the photodiode. This avoids overflow from the photodetector to the respective diffusion region.
25 This can especially be useful if the illumination is bright. Three distinct voltage levels will be needed for the transfer gate control line if this timing diagram is used: a high voltage to enable charge transfer; a low voltage to prohibit overflow of carriers in case when the photodiode is saturated
30 (under strong light conditions) and a middle voltage level to ensure that overflow of carriers at saturation flows thorough the transfer gate. The overflow should happen to the diffusion region where the respective RST switch is in its

connecting stage, so that this diffusion region is connected to its respective V_{ref} voltage. Figure 4 shows a particular instance of such timing, but slight modifications can be considered that still are according to the described operation.

Figure 5 shows a further timing diagram. This timing avoids excessive voltage at the second diffusion region FD2 by delaying the rising edge of the first switch RST1. The excessive voltage could otherwise cause leakage through the second switch RST2. The timing depends on the different dimensions of the components, including the full-well capacity of the photodiode PD, the capacitance of the capacitor C, and the parasitic capacitances Cfd1 and Cfd2.

The first transfer gate TX1 may be pulsed several times during the time period when the first switch RST1 is in its disconnecting state and the second switch RST2 in its connecting state, the signal corresponding to the first switch RST1 thus being low. And similarly the second transfer gate TX2 may be pulsed several times during the time period when the first switch RST1 is in its connecting state and the second switch RST2 is in its disconnecting state, the signal corresponding to RST2 thus being low. This multiple pulsing allows to transfer more carriers from the photodiode to the integration capacitor C. Using multiple transfers can reduce the attenuation caused by parasitic capacitances at the nodes formed by the first and second diffusion regions FD1, FD2. A corresponding time diagram is shown in figure 6.

Figures 7 and 8 show layout examples of the proposed pixel structure, in particular for backside-illuminated image sensor technologies.

Figure 7 shows an example with a capacitor formed by interdigitated conductor tracks, which can be produced in CMOS technology. For backside illumination, this capacitor
5 can be arranged on top of the photodetector PD, so that the incident light is not shielded by the conductor tracks. An optional reflector R can be provided at the bottom of the layers that are produced in the back end of line (BEOL).

10 Figure 8 shows an example with a plate capacitor comprising a sequence of a metal plate, a dielectric layer, and a further metal plate, in particular a metal-isolator-metal (MiM) capacitor, which is known per se. In the example shown in Figure 8, the capacitor C is formed by two individual
15 capacitors connected in anti-parallel fashion, in order to keep the parasitic capacitances of the bottom plate identical for the nodes of the first diffusion region FD1 and the second diffusion region FD2.

20 Other types of capacitors may be appropriate as well, depending on the individual application of the pixel structure. Examples are trench capacitors and polysilicon-insulator-polysilicon capacitors, which are known per se in semiconductor technology.

25 Figure 9 shows a structure according to Figure 8 with the difference that the transfer gates TX1, TX2 are located on the same side of the photodetector PD. This arrangement may be advantageous for a more symmetrical pixel layout.

30 Additionally, a separate anti-blooming gate or photodiode reset gate may be connected. It may also be possible to evacuate and overflow charges from the pinned photodiode via

a vertical anti-blooming structure. In that case the photodiode can be reset by a voltage pulse on the substrate under the photodiode.

5 The pixel can also include a sample stage behind the pixel source follower, especially as described in US 8 569 671 B2, for example. This enables various new readout modes. It allows to expose the next image during readout, for example. It can also be used to sample the initial reset level and
10 reduce the kTC noise of the pixel.

A two-dimensional array of pixel structures is especially suitable for an image sensor device. An imaging system including such an image sensor device may further comprise a
15 light source synchronized to the image sensor device. A light source L is schematically indicated in Figures 7 and 8. The light source can be configured to be active when the signal is acquired on the first floating diffusion FD1 and not active when the signal is acquired on the second floating
20 diffusion FD2, or vice versa. The light source can be used to project a pattern or a sequence of patterns.

In typical applications of the described pixel structure, difference signals are repeatedly obtained by detecting and
25 subtracting two frames, which may be an illuminated frame and a dark frame, for example. The difference signals are additively stored. Thus the signal-to-noise ratio is increase by charge accumulation. This enables to realize structured-light systems or stereovision with improved tolerance of
30 background light. The amount of accumulated photocharges is $d = \sum_{k=1}^n (q_{1,k} - q_{2,k})$, where $q_{1,k}$ and $q_{2,k}$ are the charges accumulated in the k-th time interval of exposure of frame number 1, which may be an illuminated frame, for example, and

frame number 2, which may be a dark frame. The duration of the corresponding time intervals can be different.

In embodiments of the pixel structure, more than two
5 different frames can be subtracted (e. g. for m different image acquisitions), by use of more than one capacitor in the pixel. Each of the frames $q_{i,k}$, $i = 1, 2, 3, \dots, m$, can have an exposure time that differs from the exposure times of the other frames. Such pixels allow to do charge arithmetic and
10 frame-to-frame calculations in the pixel.

It is advantageous that the subtraction operation can be executed inside the pixel during the image acquisition phase. It is also favourable that, after subtraction, successive
15 acquisitions can be accumulated in the pixel. This improves the saturation level that can be accumulated in the pixel. The described pixel structure allows a compact implementation, because it requires only one photodetector, one capacitor, two transfer gates, two reset switches, and a
20 source follower and select transistor in the pixel (6 transistors in total). It is compatible with backside illumination. Different timing allows to store a simple non-subtracted image with large full well charge.

25 The described image sensor can also be used in a camera system where an object is tracked. This object is illuminated by a flashed illumination or contains a flashed light source, which is synchronized to the images collected on FD1 or on FD2.

30

The described image sensor can also be used in a system where two structured light patterns are projected, and the first structured light pattern is integrated on FD1 while the

second structured light pattern is integrated on FD2. This can further enhance the information that can be extracted from the projected patterns. Such information could include depth information. This depth information could be calculated
5 from triangulation principles.

Similarly, the system could be operated with two light sources at two different wavelengths. E. g. for eye tracking applications, it is known that the eye reflects certain
10 wavelengths and absorbs other wavelengths, leading to a high contrast in a differential image which is the difference between these two images. The proposed image sensor pixel allows to generate such profile.

List of reference logograms

	C	capacitor
	Cfd1	first parasitic capacitance
5	Cfd2	second parasitic capacitance
	CR1	first contact region
	CR2	second contact region
	FD1	first diffusion region
	FD2	second diffusion region
10	L	light source
	PD	photodetector
	R	reflector
	RST1	first switch
	RST2	second switch
15	S	substrate
	SEL	select transistor
	SF	source follower
	TX1	first transfer gate
	TX2	second transfer gate
20	V _{DD}	supply voltage
	V _{ref1}	first reference voltage
	V _{ref2}	second reference voltage

Claims

1. A pixel structure for a semiconductor imaging device, comprising:
 - 5 a photodetector (PD) in a semiconductor material (S),
a first transfer gate (TX1) between the photodetector (PD)
and a first diffusion region (FD1) in the semiconductor
material,
a second transfer gate (TX2) between the photodetector (PD)
10 and a second diffusion region (FD2) in the semiconductor
material,
a capacitor (C) connected between the first diffusion region
(FD1) and the second diffusion region (FD2),
a first switch (RST1) connected between the first diffusion
15 region (FD1) and a first reference voltage (V_{ref1}), and
a second switch (RST1) connected between the second diffusion
region (FD2) and a second reference voltage (V_{ref2}).
2. The pixel structure according to claim 1, wherein
20 the photodetector (PD) is a pinned photodiode in a substrate
comprising the semiconductor material (S).
3. The pixel structure according to claim 1 or 2, further
comprising:
 - 25 buffer amplifiers connected to the first diffusion region
(FD1) and the second diffusion region (FD2).
4. The pixel structure according to one of claims 1 to 3,
wherein the first reference voltage (V_{ref1}) and the second
30 reference voltage (V_{ref2}) are equal.

5. The pixel structure according to claim 4, wherein the first reference voltage (V_{ref1}) and the second reference voltage (V_{ref2}) are equal to a supply voltage (V_{DD}).

5 6. The pixel structure according to one of claims 1 to 3, wherein the first reference voltage (V_{ref1}) or the second reference voltage (V_{ref2}) is connected to a supply voltage (V_{DD}).

10 7. The pixel structure according to one of claims 1 to 6, further comprising:
a select transistor (SEL) connected to a column bus.

8. The pixel structure according to claim 7, further
15 comprising:
a source follower (SF) formed by a field-effect transistor, which is connected to the select transistor (SEL), a gate of the source follower (SF) being connected to the first diffusion region (FD1).

20 9. An image sensor device comprising a two-dimensional array of pixel structures according to one of claims 1 to 8.

10. An imaging system including an image sensor device
25 according to claim 9, further comprising:
a light source (L) synchronized to the image sensor device, the light source (L) being configured to be active when the signal is acquired on the first diffusion region (FD1) and not active when the signal is acquired on the second
30 diffusion region (FD2), or vice versa.

11. The imaging system according to claim 10, wherein

the light source (L) is configured to project a pattern or sequence of patterns on a scene to be imaged.

12. A method of operating the pixel structure according to one of claims 1 to 8, comprising:

discharging the capacitor (C) by closing both the first switch (RST1) and the second switch (RST2) into a connecting state,

acquiring a first signal on the photodetector (PD) and transferring the first signal to the first diffusion region (FD1) by a charge transfer pulse on the first transfer gate (TX1), while the second switch (RST2) is closed in a connecting state,

acquiring a second signal on the photodetector (PD) and

transferring the second signal to the second diffusion region (FD2) by a charge transfer pulse on the second transfer gate (TX2), while the first switch (RST1) is closed in a connecting state, and

after acquisition of the signals, reading the pixel signal out from the first diffusion region (FD1) while the second diffusion region (FD2) is connected to the second reference voltage (V_{ref2}) via the second switch (RST2).

13. The method according to claim 12, wherein

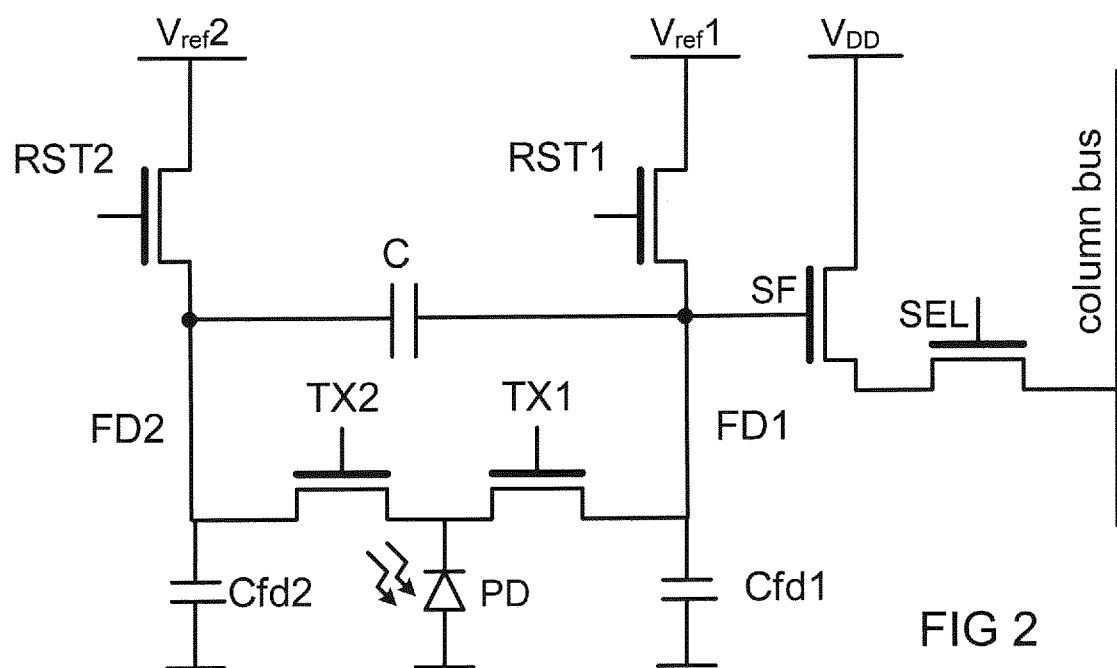
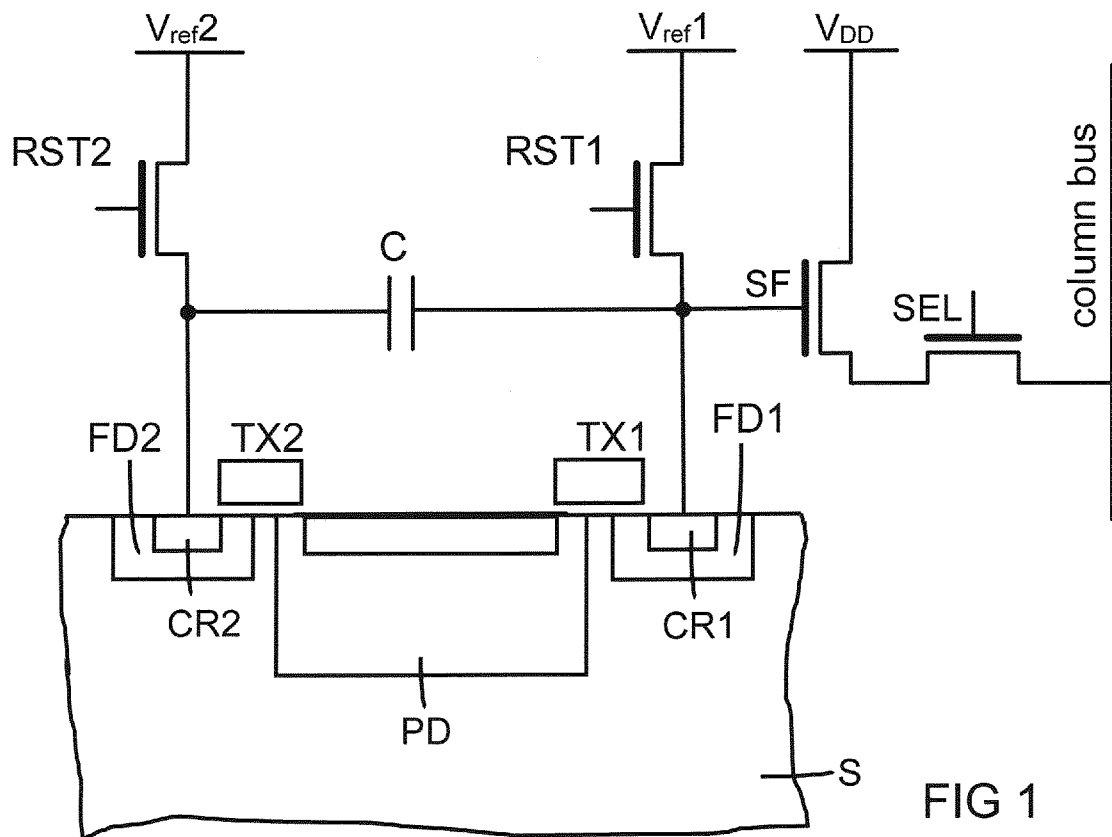
the second transfer gate (TX2) is at a higher electric potential than the first transfer gate (TX1) during readout of the pixel signal.

14. The method according to claim 12 or 13, wherein

first and second signals are repeatedly acquired and accumulated on the capacitor (C).

15. The method according to one of claims 12 to 14, wherein

at least one of the charge transfer pulse on the first transfer gate (TX1) and the charge transfer pulse on the second transfer gate (TX2) is a multiple pulse.



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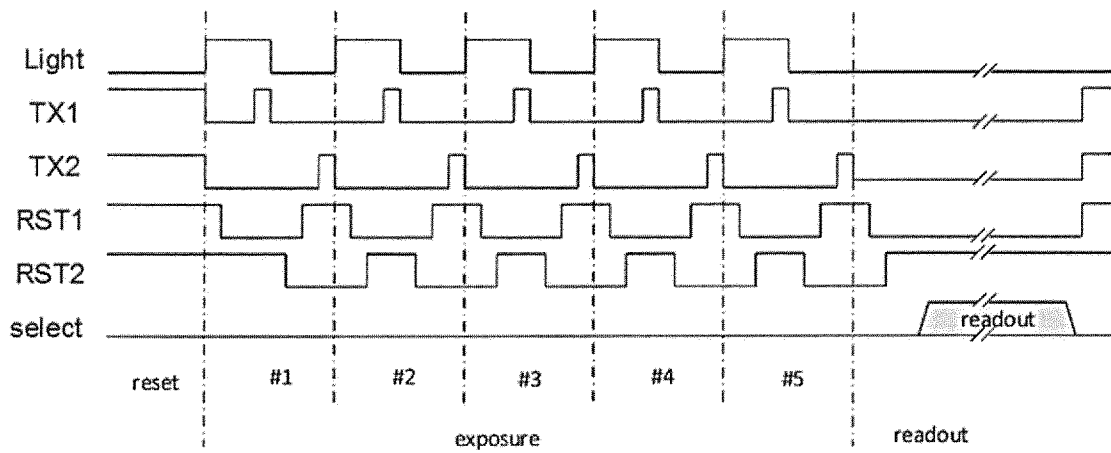


FIG 3

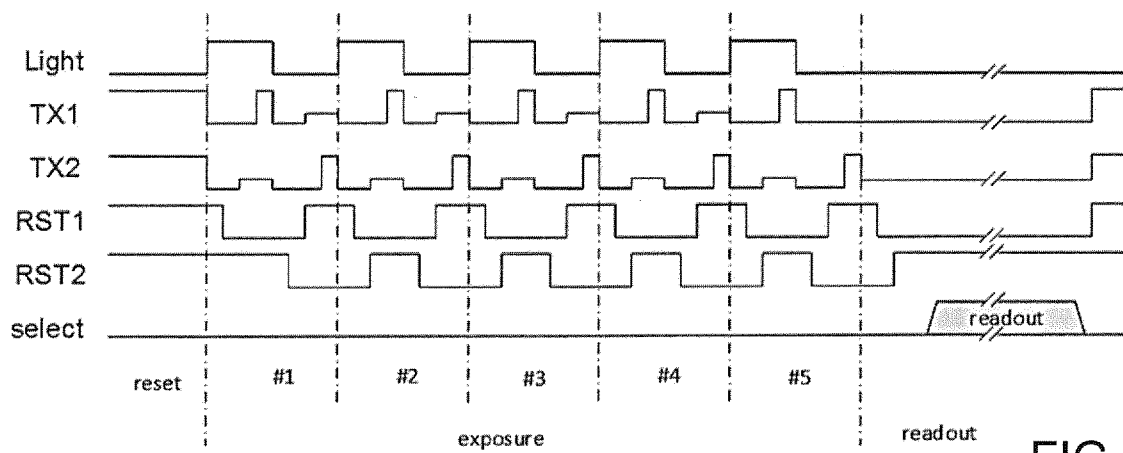


FIG 4

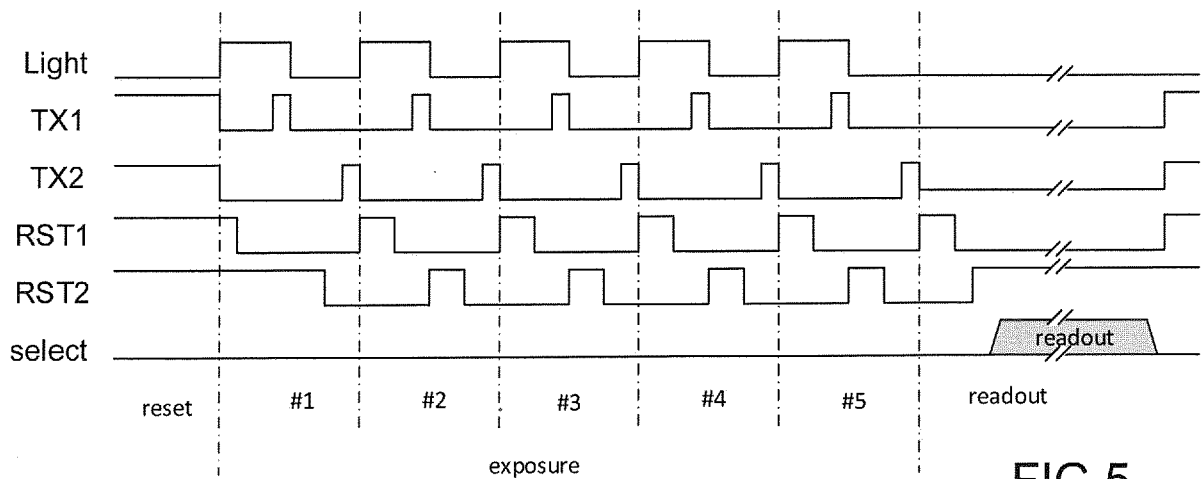


FIG 5

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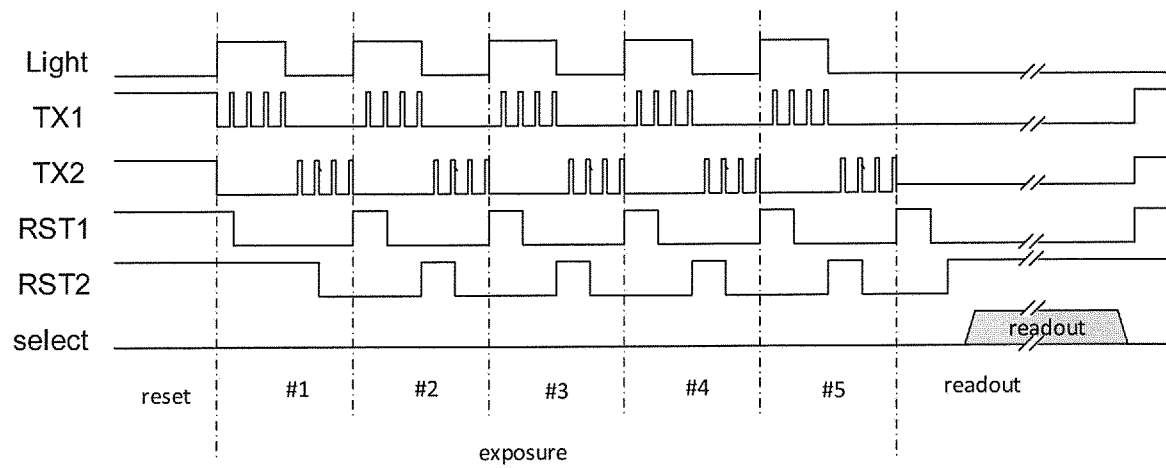


FIG 6

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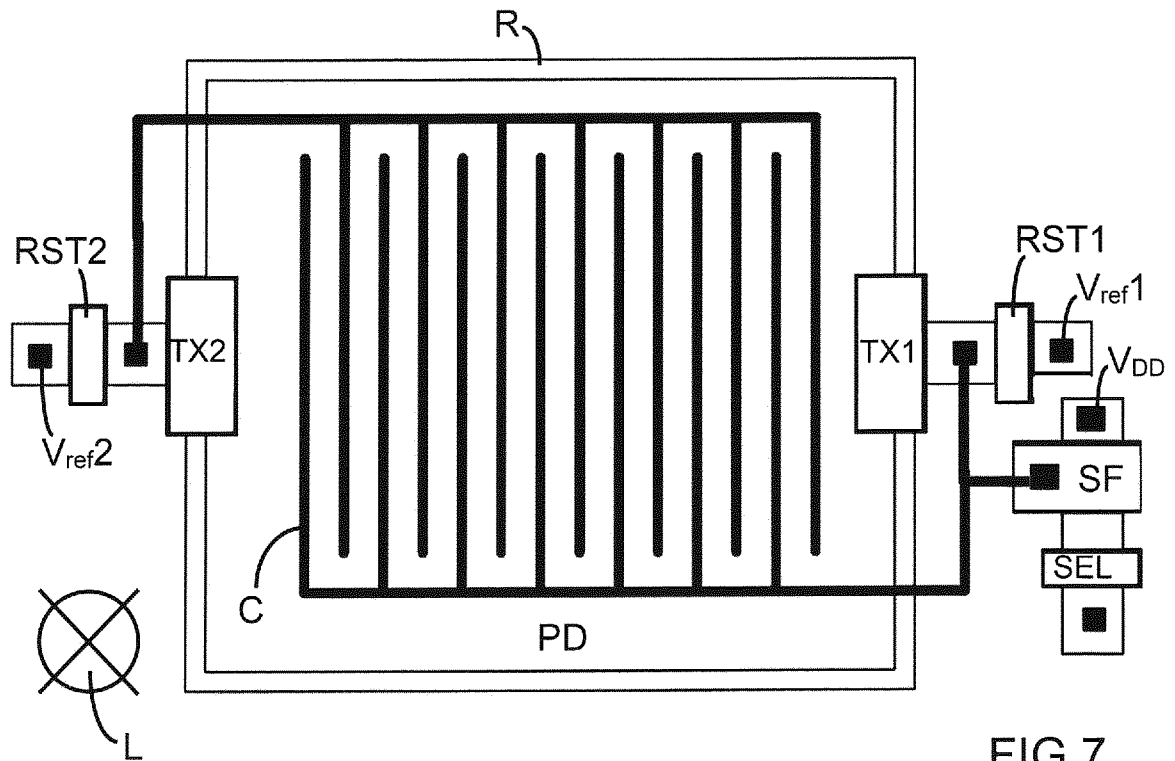


FIG 7

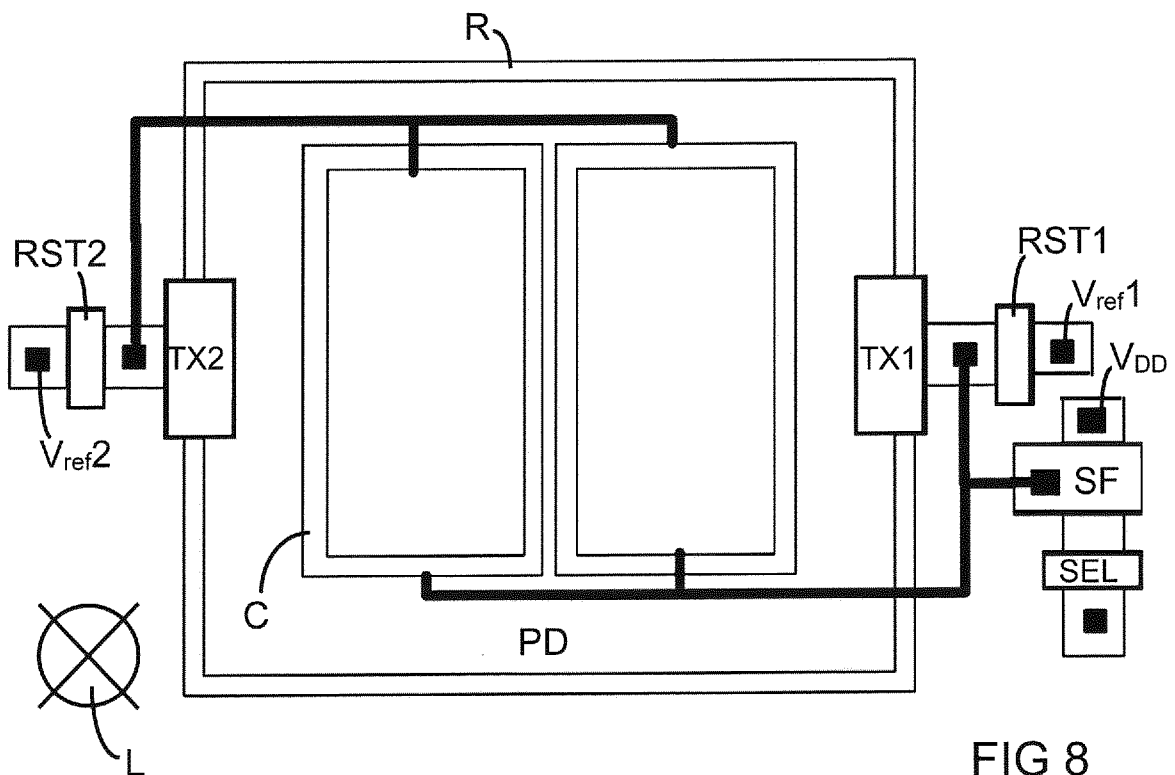


FIG 8

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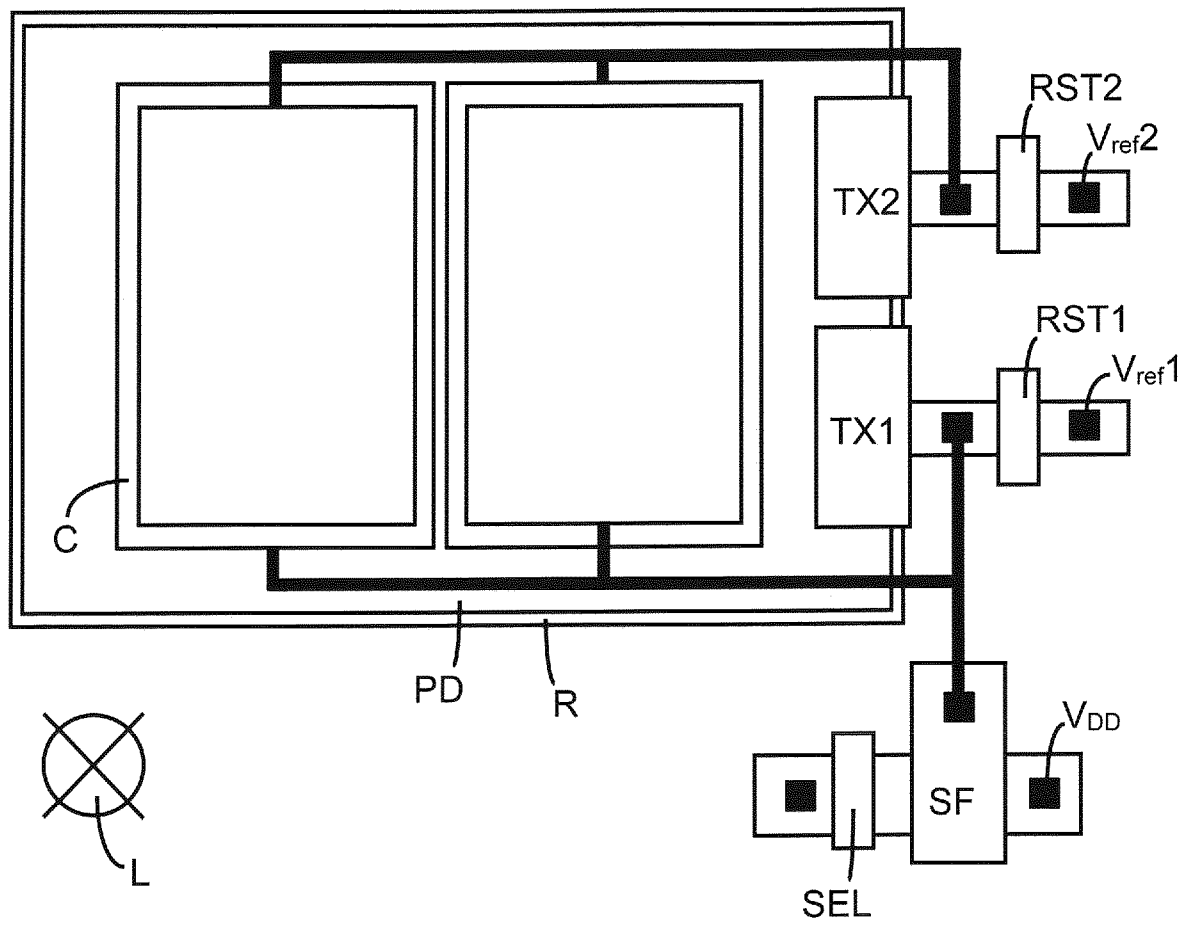


FIG 9

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2018/084188

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/3745 G01B11/25
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G01B H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

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X	US 2008/079833 A1 (ICHIKAWA MICHINORI [JP] ET AL) 3 April 2008 (2008-04-03) paragraph [0064] - paragraph [0088]; figures 6,12 -----	1-11
X	US 2004/013232 A1 (RAHN JEFFREY [US]) 22 January 2004 (2004-01-22) paragraph [0053] - paragraph [0054]; figure 6 -----	1-13
X	US 2010/308209 A1 (BUETTGEN BERHARD [CH] ET AL) 9 December 2010 (2010-12-09) column 37 - column 42; figure 1 ----- -/-	1-11



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

2 January 2019

Date of mailing of the international search report

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Penchev, Petyo

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2018/084188

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
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INTERNATIONAL SEARCH REPORT

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International application No

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