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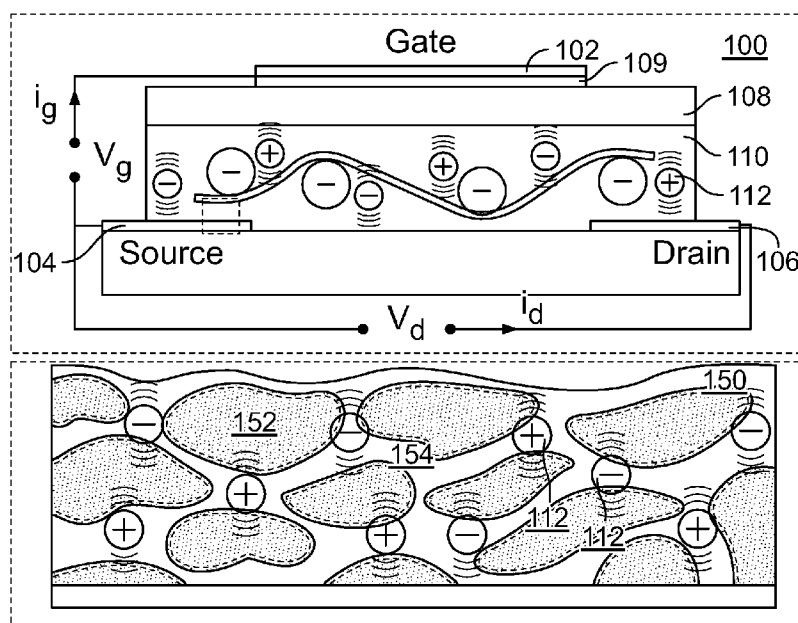


FIG. 1

(57) **Abstract:** An internal-ion gated electrochemical transistor is provided. In some embodiments, the internal-ion gated electrochemical transistor comprises: a gate electrode, a source electrode, and a drain electrode; a channel formed between the source electrode and the drain electrode, wherein the channel comprises a conducting polymer, wherein the channel serves as a reservoir of positively charged mobile ions; and an ion membrane between the channel and the gate electrode, wherein: in an off state, at least a subset of the positively charged mobile ions are ionically bonded to negatively charged ions of the conducting polymer, and wherein in an on state, at least a subset of the positively charged mobile ions are unbonded from the negatively charged ions of the conducting polymer to induce a current within the channel, and wherein at least one of the off state and the on state is actuated by application of a voltage to the gate electrode.



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## INTERNAL-ION GATED ELECTROCHEMICAL TRANSISTORS

### **Cross Reference to Related Applications**

[0001] This application claims the benefit of United States Provisional Application No. 62/784,315, filed December 21, 2018, and United States Provisional Application No. 62/952,692, filed December 23, 2019, each of which is hereby incorporated by reference herein in its entirety.

### **Technical Field**

[0002] The disclosed subject matter relates to internal-ion gated electrochemical transistors.

### **Background**

[0003] Electronic systems that can acquire, process, and interact with biological substrates are increasingly used to understand dynamic living organisms and treat human disease. These responsive systems are critical for establishing causality in complex experimental paradigms and have been shown to increase efficacy and tolerability of therapy for a range of disorders. Transistors are necessary components of these systems, forming the building blocks of circuits capable of performing specific operations such as signal amplification, filtering, detection of signal characteristics, and delivery of electrical or chemical stimulation. Prior attempts at providing transistors for such applications have been deficient in a variety of aspects.

[0004] Accordingly, it is desirable to provide new internal-ion gated electrochemical transistors.

### **Summary**

[0005] Internal-ion gated electrochemical transistors are provided.

[0006] In accordance with some embodiments of the disclosed subject matter, an internal-ion gated electrochemical transistor is provided, the internal-ion gated electrochemical transistor comprising: a gate electrode, a source electrode, and a drain electrode; a channel formed between the source electrode and the drain electrode, wherein the channel comprises a

material that includes a conducting polymer and a biocompatible solution, wherein the channel serves as a reservoir of positively charged mobile ions; and an ion membrane between the channel and the gate electrode, wherein: in an off state of the internal-ion gated electrochemical transistor, at least a subset of the positively charged mobile ions are ionically bonded to negatively charged ions of the conducting polymer, and wherein in an on state of the internal-ion gated electrochemical transistor, at least a subset of the positively charged mobile ions are unbonded from the negatively charged ions of the conducting polymer to induce a current within the channel, and wherein at least one of the off state and the on state of the internal-ion gated electrochemical transistor is actuated by application of a voltage to the gate electrode.

### **Brief Description of the Drawings**

[0007] Various objects, features, and advantages of the disclosed subject matter can be more fully appreciated with reference to the following detailed description of the disclosed subject matter when considered in connection with the following drawings, in which like reference numerals identify like elements.

[0008] FIG. 1 shows example schematic diagrams of a depletion mode internal-ion gated electrochemical transistor (d-IGT) in accordance with some embodiments of the disclosed subject matter.

[0009] FIG. 2 shows a top view of a d-IGT in accordance with some embodiments of the disclosed subject matter.

[0010] FIGS. 3A and 3B show output characteristics of a d-IGT in accordance with some embodiments of the disclosed subject matter.

[0011] FIGS. 4A and 4B show example schematic diagrams of a d-IGT operating under normal conditions and under high gate voltage conditions, respectively, in accordance with some embodiments of the disclosed subject matter.

[0012] FIGS. 5A, 5B, 5C, 5D, 5E, and 5F show example schematic diagrams for fabrication of a d-IGT in accordance with some embodiments of the disclosed subject matter.

[0013] FIGS. 5G and 5H show example schematic diagrams of a d-IGT in accordance with some embodiments of the disclosed subject matter.

[0014] FIG. 6 shows a top view of a d-IGT in accordance with some embodiments of the disclosed subject matter.

**[0015]** FIG. 7 shows a microfabricated array of internal-ion gated electrochemical transistors (IGTs) for characterizing effects of channel dimensions in accordance with some embodiments of the disclosed subject matter.

**[0016]** FIGS. 8A, 8B, and 8C show graphs that illustrate effects of dimensions of a d-IGT in accordance with some embodiments of the disclosed subject matter.

**[0017]** FIGS. 9A and 9B show examples of logic gates created using d-IGTs and temporal responses of the logic gates, respectively, in accordance with some embodiments of the disclosed subject matter.

**[0018]** FIGS. 10A and 10B show an example of a cascaded amplifier and output responses of the cascaded amplifier, respectively, in accordance with some embodiments of the disclosed subject matter.

**[0019]** FIG. 11A shows a circuit diagram for using an IGT for recording electroencephalogram (EEG) signals in accordance with some embodiments of the disclosed subject matter.

**[0020]** FIG. 11B shows a diagram of a device for measuring cortical activity using IGTs in accordance with some embodiments of the disclosed subject matter.

**[0021]** FIG. 12 shows schematic diagrams for an enhancement mode internal-ion gated electrochemical transistor (e-IGT) in accordance with some embodiments of the disclosed subject matter.

**[0022]** FIG. 13 shows a top view of an e-IGT in accordance with some embodiments of the disclosed subject matter.

**[0023]** FIGS. 14A and 14B show output characteristics of an e-IGT in accordance with some embodiments of the disclosed subject matter.

**[0024]** FIGS. 15A and 15B show processes for fabricating an e-IGT in accordance with some embodiments of the disclosed subject matter.

**[0025]** FIGS. 16A, 16B, 16C, and 16D show graphs that illustrate the effects of varying parameters of an e-IGT in accordance with some embodiments of the disclosed subject matter.

**[0026]** FIG. 17 shows a schematic diagram of logic gates created using e-IGTs and resulting output waveforms of the logic gates in accordance with some embodiments of the disclosed subject matter.

[0027] FIG. 18 shows a schematic diagram for combining a d-IGT and an e-IGT to create a non-linear rectification circuit in accordance with some embodiments of the disclosed subject matter.

[0028] FIG. 19 shows a detailed example of hardware that can be used in a device in accordance with some embodiments of the disclosed subject matter.

### **Detailed Description**

[0029] In accordance with various embodiments, internal-ion gated electrochemical transistors (IGTs) are provided.

[0030] In accordance with some embodiments, IGTs that use contained mobile ions within a conducting polymer channel to permit both volumetric capacitance and shortened ionic transit time are provided. In some embodiments, the mobile ions contained within the conducting polymer channel can create a self-de/doping process that eliminates the need for ion exchange from a shared external electrolyte. In some embodiments, due to the contained mobile ions within the polymer channel, IGTs can have high transconductance and high speed. Additionally, note that, in some embodiments, due to inclusion of an ion membrane between a channel of an IGT and a gate electrode of the IGT, IGTs can be independently gated to create scalable, conformable integrated circuits.

[0031] As shown in and described below in more detail in connection with FIG. 1, depletion mode IGTs (d-IGTs) are provided. Note that a voltage that is applied to generate a voltage between a gate electrode and a source electrode of an IGT is referred to herein as  $V_G$ . In some embodiments, d-IGTs can operate such that the d-IGT is in an ON state when there is no voltage between a gate electrode and a source electrode ( $V_G = 0V$ ) due to ions in a channel of the d-IGT causing a current between the source electrode and a drain electrode in an intrinsic state of the d-IGT. In some embodiments, a d-IGT can be turned OFF by applying a positive voltage between the gate electrode and the source electrode ( $V_G > 0V$ ). Continuing with this example, in some embodiments, the d-IGT can then be turned ON by the voltage between the gate electrode and the source electrode (such that  $V_G = 0V$ )

[0032] Additionally, as shown in and described below in more detail in connection with FIG. 12, enhancement mode IGTs (e-IGTs) are provided. In some embodiments, e-IGTs can operate such that the e-IGT is in an OFF state when there is no voltage between a gate electrode

and a source electrode ( $V_G = 0V$ ). In some embodiments, an e-IGT can be turned ON by applying a negative voltage between the gate electrode and the source electrode ( $V_G < 0V$ ). Continuing with this example, in some embodiments, the e-IGT can then be turned OFF by removing the voltage between the gate electrode and the source electrode (such that  $V_G = 0V$ )

**[0033]** In some embodiments, an IGT (a d-IGT and/or an e-IGT) can be repetitively doped and de-doped based on a voltage between a gate electrode and a source electrode of the IGT. For example, in some embodiments, in a doped state, mobile cations in a channel of an IGT can be unbonded from anions of a polymer in a channel of the IGT, thereby increasing the conductivity in the channel. Continuing with this example, in some embodiments, in a de-doped state, the mobile cations can be ionically bonded to the anions of the polymer in the channel of the IGT, thereby decreasing the conductivity in the channel. In some embodiments, the IGT can switch between the doped and de-doped state based on the voltage between the gate electrode and the source electrode. That is, in some embodiments, a “doped” state of an IGT can correspond to an ON state of the IGT, and a “de-doped” state of an IGT can correspond to an OFF state of the IGT.

**[0034]** In some embodiments, IGTs can be used for any suitable applications, such as recording biomedical and/or neurophysiological data. For example, in some embodiments, IGTs can be fabricated to create a comfortable interface with human skin and using local amplification to record high quality electrophysiological activity (e.g., electrocardiogram (ECG) activity, electromyography (EMG) activity, electroencephalogram (EEG) activity, and/or any other suitable electrophysiological activity). As another example, in some embodiments, IGTs can be miniaturized and fabricated for insertion (e.g., in a cortical layer of a brain, and/or in any other suitable location) for recording any suitable neurophysiological activity (e.g., local field potentials (LFPs), action potentials, and/or any other suitable neurophysiological activity).

**[0035]** Turning to FIG. 1, an example 100 of a schematic diagram of a d-IGT is shown in accordance with some embodiments of the disclosed subject matter. As illustrated, d-IGT 100 can include a gate electrode 102, a source electrode 104, and a drain electrode 106. In some embodiments, each of gate electrode 102, source electrode 104, and drain electrode 106 can be made of any suitable material, such as gold (Au on the periodic table), and/or any other suitable material(s).

**[0036]** As illustrated in FIG. 1, in some embodiments, d-IGT 100 can include a channel 110 between source electrode 104 and drain electrode 106. In some embodiments, channel 110 can be made of any suitable material or combination of materials that can provide a supply of ions and that can facilitate movement of ions, such as ion 112, within channel 110. For example, in some embodiments, channel 110 can be made of a conducting polymer, such as poly(3, 4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS). As another example, in some embodiments, channel 110 can include a conducting polymer that is combined with any suitable material that can provide an ion reservoir. As a more particular example, in some embodiments, the ion reservoir can include mobile ions of any suitable type, such as ions from a salt (e.g., KCl, NaCl, MgCl<sub>2</sub>, CaCl<sub>2</sub>, and/or any other suitable salt). In some embodiments, channel 110 can be made of a combination of PEDOT:PSS with any suitable biocompatible hydrophilic sugar alcohol that uptakes water molecules, such as D-sorbitol, which can keep channel 110 hydrated. Note that, in some embodiments, any other suitable materials can be included in channel 110. For example, in some embodiments, any suitable solvent, such as ethylene glycol, can be added to increase the conductivity of PEDOT:PSS within channel 110. Additionally, note that, in some embodiments, channel 110 can have any suitable length and width, as described below in more detail in connection with FIGS. 8A, 8B, and 8C.

**[0037]** As illustrated in FIG. 1, in some embodiments, d-IGT 100 can include an ion membrane 108 that can be between gate electrode 102 and channel 110. In some embodiments, ion membrane 108 can allow gate electrode 102 to have efficient ionic, but not electronic, conduction with the bulk of channel 110. In some embodiments, ion membrane 108 can be made of any suitable material. For example, in some embodiments, ion membrane 108 can be made of any suitable biocompatible and stable material, such as chitosan. In some embodiments, any other suitable biocompatible and stable material can be used in ion membrane 108, such as gelatin, polyvinyl alcohol (PVA), PVA:PSS, and/or any other suitable biopolymer. Note that, in some embodiments, to reduce an electrochemical impedance between gate electrode 102 and ion membrane 108, a layer of the conducting polymer (e.g., PEDOT:PSS) can be deposited onto gate electrode 102, as shown by layer 109 of FIG. 1.

**[0038]** Schematic 150 shows an example of a cross-sectional view of channel 110 of d-IGT 100. As illustrated, channel 110 can include PEDOT-rich regions 152 and PSS lamellas 154.

**[0039]** In some embodiments, d-IGT 100 can operate in depletion mode. That is, in some embodiments, d-IGT can be in an ON state when a gate voltage of  $V_G = 0V$  is applied, and conversely, can be in an OFF state when a positive gate voltage is applied. In particular, when a positive gate voltage is applied, mobile ions within the ion reservoir that are in the vicinity of PEDOT-rich regions (e.g., of region 152, such as shown in FIG. 1) of the polymer of the channel of the d-IGT can compensate or ionically bond to the sulphonate anions on the PSS (e.g., of PSS lamella 154, such as shown in FIG. 1). In some embodiments, this process can lead to a decrease of the hole density in the PEDOT, and consequently a decrease in the channel current, corresponding to the OFF state of the d-IGT. In some embodiments, the reaction can be reversed when a negative gate voltage is applied. More particularly, in some embodiments, in response to a negative gate voltage being applied (or a gate voltage of  $V_G = 0V$ ), the ions can unbond from PEDOT of the channel to lead to an increase in channel current, corresponding to the ON state of the d-IGT.

**[0040]** Turning to FIG. 2, a top view 200 of an IGT taken with an optical micrograph is shown in accordance with some embodiments of the disclosed subject matter. As illustrated, top view 200 shows gate electrode 102, source electrode 104, drain electrode 106, ion membrane 108, and channel 110.

**[0041]** Turning to FIG. 3A, output characteristics ( $I_D$ - $V_D$ ) of a d-IGT are shown in accordance with some embodiments of the disclosed subject matter. FIG. 3A includes multiple  $I_D$ - $V_D$  curves, each corresponding to a different gate voltage,  $V_G$ . For example, FIG. 3A includes a curve 302 corresponding to a gate voltage of  $V_G = +0.6V$ , and a curve 304 corresponding to a gate voltage of  $V_G = 0V$ .

**[0042]** Turning to FIG. 3B, a transfer curve 306 of a d-IGT with a drain voltage of  $V_D = -0.6V$  that shows drain current  $I_D$  as a function of an applied gate voltage is shown in accordance with some embodiments of the disclosed subject matter. FIG. 3B also shows a corresponding transconductance curve 308 in accordance with some embodiments of the disclosed subject matter.

**[0043]** Note that the  $I_D$ - $V_D$  curves shown in FIG. 3A, the transfer curve shown in FIG. 3B, and the transconductance curve shown in FIG. 3B were measured using a d-IGT with a channel length of 5  $\mu m$  and a width of 500  $\mu m$ . In some embodiments, a d-IGT with different

channel dimensions can have different characteristics, such as shown in and described below in connection with FIGS. 8A, 8B, and 8C.

**[0044]** Additionally, note that, in some embodiments, characteristics of a d-IGT can be based on the mixture of ions in the PEDOT:PSS dispersion that is included in a channel of the d-IGT. For example, in some embodiments, ions with large hydrated radii, such as  $Mg^{2+}$  and  $Ca^{2+}$ , can exhibit relatively slower modulation. As another example, in some embodiments, monovalent ions with smaller hydrated radii, such as  $Na^{+}$  and  $K^{+}$ , can have relatively faster time constants. Note that, in some embodiments, a d-IGT with particular time constant characteristics can be fabricated by including a particular salt species in the channel.

**[0045]** In some embodiments, a conducting polymer of a channel of an IGT can be doped and de-doped repetitively without a decrement in speed or drift in drain current. Turning to FIGS. 4A and 4B, example schematic diagrams and temporal responses of a d-IGT operating under different gate voltage conditions are shown in accordance with some embodiments of the disclosed subject matter.

**[0046]** Referring to FIG. 4A, an example 402 of a schematic diagram of a d-IGT operating under normal device conditions is shown in accordance with some embodiments of the disclosed subject matter. As illustrated in schematic 402, a pulsed gate voltage with an amplitude of  $V_G=0.4V$  is applied. Note that the amplitude of  $V_G$  is below a threshold voltage 403. As shown in schematic 402, mobile ions are maintained in an ion reservoir of a channel of the d-IGT. A temporal response curve 404 shows the drain current  $I_D$  in response to the pulsed gate voltage. As illustrated in temporal response curve 404, the drain current has a rise 406 (corresponding to a de-doping of the polymer of the channel of the d-IGT) that is symmetric to a fall 408 of the drain current (corresponding to a doping of the polymer of the channel of the d-IGT).

**[0047]** Turning to FIG. 4B, an example 410 of a schematic diagram of a d-IGT operating with a pulsed gate voltage that exceeds a threshold is shown in accordance with some embodiments of the disclosed subject matter. As illustrated in schematic 410, a pulsed gate voltage with an amplitude of  $V_G=0.9V$  is applied that exceeds threshold 403, and mobile ions are forced to exit the channel of the d-IGT and enter the ion membrane. A temporal response curve 412 shows the drain current  $I_D$  in response to the pulsed gate voltage. As illustrated in temporal response curve 412, the drain current has a rise 414 (corresponding to a de-doping of the

polymer of the channel of the d-IGT) with a duration that is shorter than a fall 416 of the drain current (corresponding to a doping of the polymer of the channel of the d-IGT).

**[0048]** Note that, for the temporal response curves shown in FIGS. 4A and 4B, a fixed drain voltage of  $V_D = -0.4V$  is used.

**[0049]** Turning to FIGS. 5A, 5B, 5C, 5D, 5E, and 5F, an example of a fabrication process for a d-IGT is shown in accordance with some embodiments of the disclosed subject matter.

**[0050]** Referring to FIG. 5A, Au electrodes 502, 504, and 506 (e.g., corresponding to a gate electrode, a drain electrode, and a source electrode) and interconnects can be patterned on a substrate 508. In some embodiments, any suitable photolithography and lift-off processes can be used, as described below in more detail.

**[0051]** In some embodiments, the substrate can be made of any suitable material or combination of materials, such as quartz wafers of any suitable thickness (e.g., 1 mm, 1.5 mm, and/or any other suitable thickness) that are coated with a parylene layer of any suitable thickness (e.g., 2  $\mu m$ , 2.5  $\mu m$ , and/or any other suitable thickness).

**[0052]** In some embodiments, photoresist 510 can be used for photolithography. In some embodiments, photoresist 510 can be any suitable photoresist, such as a negative photoresist (e.g., AZnLOF2020, and/or any other suitable photoresist). In some embodiments, photoresist 510 can be spin coated (e.g., at 3000 rpm, and/or at any other suitable revolutions per minute), baked on a proximity hot plate at any suitable temperature (e.g., 110°C, 115°C, and/or any other suitable temperature) and for any suitable duration of time (e.g., 90 seconds, 95 seconds, and/or any other suitable duration of time), exposed using any suitable technique(s) (e.g., using a Suss MA6 Mask Aligner, and/or in any other suitable manner), and developed with any suitable developer (e.g., AZ 726 MIF developer, and/or any other suitable developer).

**[0053]** In some embodiments, a Titanium (Ti in the periodic table) adhesion layer of any suitable thickness (e.g., 10 nm, 12 nm, and/or any other suitable thickness) can be deposited, followed by an Au layer of any suitable thickness (e.g., 100 nm, 110 nm, and/or any other suitable thickness). In some embodiments, Ti and Au layers can be deposited with any suitable e-beam metal evaporator.

**[0054]** In some embodiments, the lift-off process can be performed using any suitable technique or combination of techniques, for example, by immersing the substrate in a bath with any suitable stripper (e.g., 1165 stripper, and/or any other suitable stripper).

**[0055]** Referring to FIG. 5B, an additional parylene layer 512 can be coated to electrically isolate the Au electrodes. In some embodiments, additional parylene layer 512 can have any suitable thickness (e.g., 2  $\mu\text{m}$ , 2.5  $\mu\text{m}$ , and/or any other suitable thickness). In some embodiments, adhesion of additional parylene layer 512 can be improved in any suitable manner, for example, by using 3-(trimethoxysilyl)propyl methacrylate (A-174 Silane) during coating.

**[0056]** Referring to FIG. 5C, an anti-adhesive layer 514 can be spin-coated on additional parylene layer 512. In some embodiments, anti-adhesive layer 514 can be a dilution of any suitable cleaning solution (e.g., Micro 90, and/or any other suitable solution) at any suitable concentration (e.g., 8% in DI water, and/or any other suitable concentration). In some embodiments, a third sacrificial parylene layer 516 can be deposited on top of anti-adhesive layer 514.

**[0057]** Referring to FIG. 5D, in some embodiments, areas corresponding to a transistor channel and contact pads can be etched via successive photolithography and plasma etching steps. In some embodiments, photolithography can be performed using photoresist 518, such as shown in FIG. 5D. In some embodiments, photoresist 518 can be any suitable positive photoresist (e.g., AZ9260, and/or any other suitable photoresist). In some embodiments, photoresist 518 can be spin-coated (e.g., at 5000 rpm, and/or any other suitable revolutions per minute), baked at any suitable temperature (e.g., 115  $^{\circ}\text{C}$ , and/or any other suitable temperature) for any suitable duration of time (e.g., 90 seconds, and/or any other suitable duration), exposed in any suitable manner (e.g., using a Suss MA6 Mask Aligner, and/or in any other suitable manner), and developed using any suitable developer (e.g., AZ400K developer, and/or any other suitable developer) at any suitable concentration (e.g., 1:4 with deionized (DI) water, and/or at any other suitable concentration). In some embodiments, the patterned areas can be etched with any suitable plasma reactive ion etching process.

**[0058]** Referring to FIG. 5E, in some embodiments, an ion membrane 520 can be formed. In some embodiments, an ion membrane layer that includes any suitable thickness (e.g., 200 nm, 250 nm, and/or any other suitable thickness) of PEDOT:PSS at any suitable concentration (e.g., with 1% (3-glycideloxypropyl)trimethoxysilane (GOPS) as a cross-linker) and chitosan of any suitable thickness (e.g., 700 nm, 750 nm, and/or any other suitable thickness) can be spin coated successively to form the ion membrane that covers gate electrode 504. In some embodiments, the ion membrane can be patterned in any suitable manner. For example,

similar to what is described above in connection with FIGS. 5A and 5D, any suitable photolithography (e.g., using photoresist 524) and plasma etching steps can be performed after depositing a protective layer of polymethyl methacrylate (PMMA) 522 of any suitable thickness (e.g., 200 nm, 220 nm, and/or any other suitable thickness).

**[0059]** Referring to FIG. 5F, in some embodiments, a channel of the d-IGT can be formed in any suitable manner. For example, in some embodiments, residues of photoresist 524 and PMMA 522 can be rinsed off in any suitable manner (e.g., using acetone, and/or in any other suitable manner), leaving the ion membrane layers intact. Continuing with this example, in some embodiments, a channel 526 can be formed by spin coating any suitable material. For example, as described above in connection with FIG. 1, channel 526 can be formed by spin coating a mixture of PEDOT:PSS with D-sorbitol in any concentration (e.g., 40% D-sorbitol, 1% GOPS as crosslinker, and 0.1% dedecylbenzene sulfonic acid (DBSA) to improve film processing and wettability). In some embodiments, third parylene layer 516 can then be peeled off.

**[0060]** Referring to FIGS. 5G and 5H, example schematic diagrams of a d-IGT fabricated using the steps shown in and described above in connection with FIGS. 5A, 5B, 5C, 5D, 5E, and 5F are shown in accordance with some embodiments of the disclosed subject matter. Note that, unlike d-IGT 100 shown in FIG. 1, the d-IGT shown in FIGS. 5G and 5H, as fabricated using the steps described above in connection with FIGS. 5A, 5B, 5C, 5D, 5E, and 5F has a gate electrode in a bottom position. Note that, in some embodiments, a d-IGT with a gate electrode in a top position (such as shown in and described above in connection with FIG. 1) can have identical electrical characteristics to a d-IGT with a gate electrode in a bottom position (such as shown in FIGS. 5G and 5H).

**[0061]** Turning to FIG. 6, a top view of a d-IGT fabricated using the steps shown in and described above in connection with FIGS. 5A, 5B, 5C, 5D, 5E, and 5F is shown in accordance with some embodiments of the disclosed subject matter. As illustrated in FIG. 6, the d-IGT can include an ion membrane 602 and a channel 604.

**[0062]** Turning to FIG. 7, an example 700 of an array of IGTs that can be used to characterize effects of different channel dimensions is shown in accordance with some embodiments of the disclosed subject matter. In some embodiments, array 700 can include any suitable number of IGTs. For example, as shown in FIG. 7, array 700 can include any suitable rows (e.g., rows 702, 704, 706, 708, 710, and 712) and any suitable columns (e.g., columns 714,

716, 718, 720, 722, and 724), where each row includes IGTs with channels of different widths and where each column includes IGTs with channels of different lengths. Note that, although six rows and six columns are shown in FIG. 7, in some embodiments, any suitable number of IGTs can be included in an array. In some embodiments, an array of IGTs can be created in any suitable manner, for example, by using any suitable microfabrication technique(s).

**[0063]** Turning to FIGS. 8A, 8B, and 8C, graphs that show effects of different channel dimensions are shown in accordance with some embodiments of the disclosed subject matter. Note that, in some embodiments, properties of a d-IGTs with different channel dimensions, such as shown in the graphs shown in FIGS. 8A, 8B, and 8C, can be measured using an array of IGTs, such as shown in and described above in connection with FIG. 7.

**[0064]** Referring to FIG. 8A, a curve 802 that shows transconductance of a d-IGT as a function of channel thickness is shown in accordance with some embodiments of the disclosed subject matter. As shown in FIG. 8A, in some embodiments, a d-IGT with a larger channel thickness can have a relatively larger transconductance. Additionally, FIG. 8A includes a curve 804 that shows transconductance as a function of gate electrode area.

**[0065]** Referring to FIG. 8B, a graph that shows transconductance of a d-IGT as a function of channel volume is shown in accordance with some embodiments of the disclosed subject matter. As shown in FIG. 8B, a d-IGT with a larger channel volume can have a relatively larger transconductance.

**[0066]** Referring to FIG. 8C, a graph that shows an On/Off current ratio as a function of channel volume is shown in accordance with some embodiments of the disclosed subject matter. As illustrated, in some embodiments, a d-IGT with a larger channel volume can have a relatively larger  $I_{on}/I_{off}$  ratio.

**[0067]** As shown in FIGS. 9A, 9B, 10A, and 10B, in some embodiments, d-IGTs can be combined, for example, to form a logic gate (e.g., as shown in and described below in connection with FIGS. 9A and 9B), to form an amplifier (e.g., as shown in and described below in connection with FIGS. 10A and 10B), and/or for any other suitable purpose.

**[0068]** Turning to FIG. 9A, examples of d-IGT-based logic gates are shown in accordance with some embodiments of the disclosed subject matter. As illustrated, FIG. 9A shows a NOR gate 902 and a NAND gate 904. As shown in FIG. 9A, NOR gate 902 can include a first d-IGT that has a gate electrode 906, a source electrode 908, and a drain electrode 910, and

a second d-IGT that has a gate electrode 912, a source electrode 914, and a drain electrode 916. As shown in FIG. 9A, NAND gate 904 can include a first d-IGT that has a gate electrode 918, a source electrode 920, and a drain electrode 922, and a second d-IGT that has a gate electrode 924, a source electrode 926, and a drain electrode 928. In some embodiments, logic gates can be fabricated in any suitable manner, for example, by fabricating d-IGTs on any suitable supports (e.g., parylene-C supports, and/or any other suitable supports) of any suitable thickness (e.g., 2  $\mu\text{m}$ , and/or any other suitable thickness). Note that, in some embodiments, input signals can be applied to the gate electrodes of each d-IGT, as shown in FIG. 9A.

**[0069]** Turning to FIG. 9B, output drain currents of the logic gates shown in FIG. 9A are shown in accordance with some embodiments of the disclosed subject matter. As shown in FIG. 9B, output current 952, present at terminal O of NOR gate 902 of FIG. 9A, is the result of inputs 954 and 956 at terminals I2 and I1, respectively, of NOR gate 902 of FIG. 9A. Output current 958, present at terminal O of NAND gate 904 of FIG. 9A, is the result of inputs 960 and 962 at terminals I2 and I1, respectively, of NAND gate 904 of FIG. 9A. Note that dashed lines 964 and 966 illustrate thresholds for high and low logics, respectively.

**[0070]** Turning to FIG. 10A, an example a d-IGT-based cascaded amplifier is shown in accordance with some embodiments of the disclosed subject matter. As shown, the cascaded amplifier can include a first d-IGT that has a gate electrode 1002, a source electrode 1004, and a drain electrode 1006, and can include a second d-IGT that has a gate electrode 1008, a source electrode 1010, and a drain electrode 1012.

**[0071]** Turning to FIG. 10B, an example circuit diagram 1050 of a d-IGT-based cascaded amplifier is shown in accordance with some embodiments of the disclosed subject matter. As shown in FIG. 10B, in some embodiments, a first d-IGT T<sub>1</sub> 1052 (which can have a gate electrode 1058, a source electrode 1060, and a drain electrode 1062) can register the input (shown as V<sub>G</sub> in circuit diagram 1050) from gate electrode 1058 of d-IGT T<sub>1</sub> 1052 and can amplify the input. In some embodiments, the output current from d-IGT T<sub>1</sub> 1052 can then be converted to a voltage using a resistor 1070, and can then be connected to the gate of a second d-IGT T<sub>2</sub> 1054 (which can include a gate electrode 1064, a source electrode 1066, and a drain electrode 1068). Continuing further, d-IGT T<sub>2</sub> 1054 can produce an amplified output current (shown as I<sub>D</sub> in circuit diagram 1050). Note that, in some embodiments, a value of resistor 1070 can control an amplification of the circuit such that a higher resistor value results in a higher

gain. In some such embodiments, a higher resistor value can result in an increased output impedance. In some embodiments, any suitable resistor value can be used (e.g., 100  $\Omega$ , 200  $\Omega$ , and/or any other suitable value) to optimize a tradeoff between a desired amplification and a desired output impedance. Note that, in some embodiments, any suitable load (not shown) can be connected to d-IGT T<sub>2</sub> 1054. In some embodiments, as shown in FIG. 10B, circuit diagram 1050 can additionally include a voltage source 1056 (e.g., a battery, and/or any other suitable voltage source).

**[0072]** FIG. 10B also shows corresponding input and output signals, with an input voltage  $V_{in}$  1072 (corresponding to a gate voltage  $V_G$  at d-IGT T<sub>1</sub> 1052 as shown in circuit diagram 1050), a current 1074 through d-IGT T<sub>1</sub> 1052, and a final amplified current 1076 through d-IGT T<sub>2</sub> 1054 (corresponding to current  $I_D$  shown in circuit diagram 1050). Note that, the final amplified output from the d-IGT T<sub>2</sub> 1054 is shown as a current, which, in some embodiments can be converted to a voltage by connecting a resistor to drain electrode 1068 of d-IGT T<sub>2</sub> 1054.

**[0073]** Turning to FIG. 11A, an example diagram for using a d-IGT for recording EEG signals is shown in accordance with some embodiments of the disclosed subject matter. In some embodiments, any suitable locations can be used for device placement. For example, as shown in FIG. 11A, an IGT 1102 can be placed over an occipital location (O1) and neurophysiological signals can be recorded relative to a reference electrode placed over a left frontopolar location (FP1), as shown in FIG. 11A. In some embodiments, IGT 1102 can include a gate electrode 1106, a source electrode 1110, and a drain electrode 1108 such that gate electrode 1106 or an ion membrane corresponding to gate electrode 1106 is placed on the scalp of the subject. In some embodiments, a resistor (not shown) of any suitable resistance (e.g., 500  $\Omega$ , 1 k $\Omega$ , and/or any other suitable value) can be placed in series with the IGT channel (e.g., by placing the resistor in series with a drain terminal of the IGT) to convert a current of IGT 1102 (labeled  $I_D$  in FIG. 11A) to a voltage, and the output voltage can be measured with any suitable acquisition system (e.g., an Intan acquisition system, and/or any other suitable system). In some embodiments,  $V_D$  and  $V_G$  can have any suitable values. For example, in some embodiments,  $V_D = -0.6$  V and  $V_G = 0.4$  V. Note that the locations shown in FIG. 11A are merely examples, and, in some embodiments, EEG electrodes can be affixed to any suitable scalp locations. Additionally, note that although the diagram shown in FIG. 11A depicts a configuration for recording EEG signals

using only one d-IGT, in some embodiments, any suitable number of IGTs (e.g., two, ten, twenty, one hundred, and/or any other suitable number) can be used. Additionally, note that, in some embodiments, e-IGTs, as shown in and described below in connection with FIG. 12 can be used to record EEG signals.

**[0074]** Note that, in some embodiments, an EEG electrode that uses IGTs can be fabricated in any suitable manner. For example, in some embodiments, any suitable number (e.g., two, three, five, ten, one hundred, two hundred, and/or any other suitable number) of IGTs can be fabricated into any suitable number of conformable ribbon structures that can be placed on the scalp of a subject. Note that, in some embodiments, an IGT used for EEG electrode can adhere to the scalp of the subject in any suitable manner. For example, in some embodiments, an IGT can adhere to a scalp without use of any additional chemicals due to the light weight of the IGT and the flexibility of the conformable ribbon structure. As another example, in some embodiments, sorbitol and/or any other suitable coating can be applied to a gate electrode of each IGT to serve as an intrinsic adhesive. Note that, in some embodiments, a conformable ribbon structure can be constructed with dimensions (e.g., 1.5 mm wide, 1.7 mm wide, and/or any other suitable width) such that the ribbon conforms to the scalp of a subject between hair follicles.

**[0075]** Additionally, note that, in some embodiments, EEG recordings can be obtained using the IGTs in any suitable manner. For example, in some embodiments, any suitable resistor (e.g., a 500  $\Omega$  resistor, and/or any other suitable resistor) can be placed in series with a channel of the IGT to convert current to voltage. Continuing with this example, in some embodiments, the output voltage can be recorded using any suitable acquisition system. In some embodiments, any suitable frequencies or rhythms can be captured (e.g., alpha bands or oscillations of 8-12 Hz, beta bands or oscillations of 13-25 Hz, and/or any other suitable frequencies or bands). In some embodiments, any suitable processing can be performed on recorded signals, for example, to isolate particular frequencies, remove particular frequencies, and/or any other suitable processing. For example, in some embodiments, an acquired EEG signal can be notch filtered to remove any suitable frequencies. As a more particular example, in some embodiments, an EEG signal can be filtered to remove any frequencies that may be caused by an environmental system (e.g., 55-65 Hz caused by a power system in the United States and other parts of the world that produce noise at 60 Hz, and/or any other suitable frequencies). As another example, in some

embodiments, epochs that include blinking or other eye movements can be identified and removed.

**[0076]** In accordance with some embodiments of the disclosed subject matter, an IGT can be fabricated that operates in enhancement mode, such that the IGT is in an OFF state when a positive gate voltage or a gate voltage of  $V_G = 0V$  is applied, and such that the IGT is in an ON state when a negative gate voltage is applied. Note that an IGT that operates in enhancement mode is referred to herein as an e-IGT. In some embodiments, an e-IGT can have a channel that includes a mixture of PEDOT:PSS, D-sorbitol, polyethylenimine (PEI), and any suitable cross-linking additives, such as described below in connection with FIGS. 12, 15A, and 15B. Similar to d-IGTs as described above, in some embodiments, an e-IGT can have high transconductance, exhibit volumetric capacitance, and can be stably operated over extended periods of time. In some embodiments, the temporal response of an e-IGT can be best described by hole mobility.

**[0077]** Turning to FIG. 12, an example 1200 of a schematic of an e-IGT with an applied gate voltage of  $V_G = 0V$  and an example 1250 of a schematic of an e-IGT with an applied gate voltage of  $V_G < 0V$  is shown in accordance with some embodiments of the disclosed subject matter. As illustrated in FIG. 12, an e-IGT can include a gate electrode 1202, a source electrode 1204, and a drain electrode 1206. Additionally, as shown in FIG. 12, an e-IGT can include an ion membrane 1208 and a channel 1210.

**[0078]** Similar to what was described above in connection with a d-IGT, gate electrode 1202, source electrode 1204, and drain electrode 1206 can each be made of any suitable material, such as Au, and/or any other suitable material.

**[0079]** Similar to what was described above in connection with FIG. 1, an e-IGT can include an ion membrane 1208 that can be between gate electrode 1202 and channel 1210. In some embodiments, ion membrane 1208 can allow gate electrode 1202 to have efficient ionic, but not electronic, conduction with the bulk of channel 1210. In some embodiments, ion membrane 1208 can be made of any suitable material. For example, in some embodiments, ion membrane 1208 can be made of any suitable biocompatible and stable material, such as chitosan. In some embodiments, any other suitable biopolymer can be used for ion membrane 1208, such as gelatin, PVA, PVA:PSS, and/or any other suitable biopolymer. Note that, in some embodiments, to reduce an electrochemical impedance between gate electrode 1202 and ion

membrane 1208, a layer of a conducting polymer (e.g., PEDOT:PSS) can be deposited onto gate electrode 1202, as shown by layer 1209 of FIG. 12.

**[0080]** In some embodiments, channel 1210 can include any suitable material or combination of materials. For example, as shown in FIG. 12, channel 1210 can include a combination of PEDOT:PSS, PEI, D-sorbitol, and/or any other suitable combination of materials. In some embodiments, D-sorbitol in channel 1210 can enhance electronic conductivity of the PEDOT:PSS film. Additionally, in some embodiments, D-sorbitol can facilitate maintenance and movement of mobile ions within channel 1210 by forming a hydrated ion reservoir. In some embodiments, amine groups of PEI can serve as reducing agent through electron transfer to PEDOT:PSS and can decrease the intrinsic conductivity of channel 1210 by several orders of magnitude.

**[0081]** Referring to schematic 1200 of FIG. 12, during an OFF state of the e-IGT (i.e., when  $V_G = 0$  V, as shown in FIG. 12, or when a positive gate voltage is applied), protonated  $\text{PEI}^+$  1212 can bond ionically with  $\text{PSS}^-$  1214 to maintain charge balance. Note that, in the OFF state of the e-IGT, PEDOT 1213 can be in its reduced state ( $\text{PEDOT}^0$ ). In some embodiments, the bonding of  $\text{PEI}^+$  1212 to  $\text{PSS}^-$  1214 can be facilitated by the presence of sulfonic acid groups in PSS and the basic nature of PEI.

**[0082]** Referring to schematic 1250 of FIG. 12, in some embodiments, during an ON state of the e-IGT, a negative applied gate voltage (i.e.,  $V_G < 0$  V) can compensate  $\text{PEI}^+$  1212 in channel 1210, causing the bonded  $\text{PSS}^-$  1214 to be released. In some embodiments,  $\text{PSS}^-$  1214 can then recombine with PEDOT 1213, as shown in schematic 1250 of FIG. 12. In some embodiments, the formation of  $\text{PEDOT}^+:\text{PSS}^-$  can increase the conductivity of channel 1210, thereby allowing the gate voltage to modulate the channel current. In some embodiments, the hydrated reservoirs established by D-sorbitol within the channel facilitate these ion exchanges by maintaining channel hydration within the e-IGT and facilitating ion mobility within channel 1210.

**[0083]** Turning to FIG. 13, a top view 1300 of an e-IGT is shown in accordance with some embodiments of the disclosed subject matter. As illustrated in FIG. 13, the e-IGT includes an ion membrane 1302 and a channel 1304. Note that the channel of the e-IGT shown in FIG. 13 has a length of 12  $\mu\text{m}$ , a width of 12  $\mu\text{m}$ , and a channel thickness of 1.9  $\mu\text{m}$ .

**[0084]** Turning to FIG. 14A, output characteristics ( $I_D$ - $V_D$ ) of an e-IGT are shown in accordance with some embodiments of the disclosed subject matter. FIG. 14A includes multiple  $I_D$ - $V_D$  curves, each corresponding to a different gate voltage,  $V_G$ . For example, FIG. 14A includes a curve 1402 corresponding to a gate voltage of  $V_G = 0V$ , and a curve 1404 corresponding to a gate voltage of  $V_G = -0.6V$ .

**[0085]** Turning to FIG. 14B, a transfer curve 1406 of an e-IGT and a corresponding transconductance curve 1408 for a drain voltage of  $V_D = -0.6V$  is shown in accordance with some embodiments of the disclosed subject matter.

**[0086]** Note that the  $I_D$ - $V_D$  curves shown in FIG. 14A, the transfer curve shown in FIG. 14B, and the transconductance curve shown in FIG. 14B were measured using an e-IGT with a channel length of  $5\text{ }\mu\text{m}$ , a width of  $500\text{ }\mu\text{m}$ , and a PEDOT:PSS thickness of  $300\text{ nm}$ . In some embodiments, an e-IGT with different channel dimensions can have different characteristics, such as shown in and described below in connection with FIGS. 16A, 16B, 16C, and 16D.

**[0087]** Turning to FIGS. 15A and 15B, schematic diagrams that show steps for fabrication of an e-IGT are shown in accordance with some embodiments of the disclosed subject matter. Note that FIG. 15A illustrates a process in which an e-IGT is fabricated using layer-by-layer deposition of PEDOT:PSS and PEI, and that FIG. 15B illustrates an alternative process in which an e-IGT is fabricated using a solution-based PEDOT:PSS-PEI.

**[0088]** At 1501, Au electrodes 1502, 1504, and 1506 (e.g., corresponding to a gate electrode, a drain electrode, and a source electrode) and interconnects can be patterned on a substrate 1508. In some embodiments, any suitable photolithography and lift-off processes can be used.

**[0089]** In some embodiments, substrate 1508 can be made of any suitable material or combination of materials, such as quartz wafers of any suitable thickness (e.g.,  $1\text{ mm}$ ,  $1.5\text{ mm}$ , and/or any other suitable thickness) that are coated with a parylene layer 1509 of any suitable thickness (e.g.,  $1\text{ }\mu\text{m}$ ,  $1.2\text{ }\mu\text{m}$ ,  $2\text{ }\mu\text{m}$ ,  $2.5\text{ }\mu\text{m}$ , and/or any other suitable thickness).

**[0090]** In some embodiments, a photoresist 1510 can be used for photolithography. In some embodiments, photoresist 1510 can be any suitable photoresist, such as a negative photoresist (e.g., AZnLOF2020, and/or any other suitable photoresist). In some embodiments, photoresist 1510 can be spin coated (e.g., at  $3000\text{ rpm}$ , and/or at any other suitable revolutions per minute), baked on a proximity hot plate at any suitable temperature (e.g.,  $105^\circ\text{C}$ ,  $110^\circ\text{C}$ ,

and/or any other suitable temperature) and for any suitable duration of time (e.g., 90 seconds, 95 seconds, and/or any other suitable duration of time), exposed using any suitable technique(s) (e.g., using a Suss MA6 Mask Aligner, and/or in any other suitable manner), and developed with any suitable developer (e.g., AZ 300 MIF developer, and/or any other suitable developer).

**[0091]** In some embodiments, a Ti adhesion layer of any suitable thickness (e.g., 10 nm, 12 nm, and/or any other suitable thickness) can be deposited, followed by an Au layer of any suitable thickness (e.g., 150 nm, 160 nm, and/or any other suitable thickness). In some embodiments, the Ti layer and the Au layer can be deposited in any suitable manner (e.g., an Angstrom EvoVac Multi-Process, and/or any other suitable process) and can be patterned in any suitable manner (e.g., by soaking the substrate in a bath of resist remover, and/or in any other suitable manner).

**[0092]** Referring to 1503, an additional parylene layer 1512 can be coated to electrically isolate the Au electrodes. In some embodiments, additional parylene layer 1512 can have any suitable thickness (e.g., 2  $\mu\text{m}$ , 2.5  $\mu\text{m}$ , and/or any other suitable thickness). In some embodiments, adhesion of additional parylene layer 512 can be improved in any suitable manner, for example, by using 3-(trimethoxysilyl)propyl methacrylate (A-174 Silane) during chemical vapor deposition.

**[0093]** Referring to 1505, an anti-adhesive layer 1514 can be spin-coated on additional parylene layer 1512. In some embodiments, anti-adhesive layer 1514 can be a dilution of any suitable cleaning solution (e.g., Micro 90, and/or any other suitable solution) at any suitable concentration (e.g., 8% in DI water, and/or any other suitable concentration). In some embodiments, a third sacrificial parylene layer 1516 can be deposited on top of anti-adhesive layer 1514.

**[0094]** Referring to 1507, in some embodiments, areas corresponding to a transistor channel and contact pads can be etched via successive photolithography and plasma etching steps. In some embodiments, photolithography can be performed using photoresist 1518, as shown in FIGS. 15A and 15B. In some embodiments, photolithography can be performed in any suitable manner and using any suitable technique(s). For example, in some embodiments, any suitable positive photoresist (e.g., AZ9260, and/or any other suitable photoresist) can be spin-coated (e.g., at 5000 rpm, and/or any other suitable revolutions per minute), baked at any suitable temperature (e.g., 115 °C, 120 °C, and/or any other suitable temperature) for any suitable

duration of time (e.g., 90 seconds, 95 seconds, and/or any other suitable duration of time), exposed in any suitable manner (e.g., using a Suss MA6 Mask Aligner, and/or in any other suitable manner), and developed using any suitable developer (e.g., AZ400K developer, and/or any other suitable developer) at any suitable concentration (e.g., 1:4 with DI water, and/or at any other suitable concentration). In some embodiments, the patterned areas can be etched with any suitable plasma reactive ion etching process. In some embodiments, to prevent the first layer of parylene from being over-etched, an extra layer of a photoresist (e.g., AZnLOF202, and/or any other suitable photoresist) can be spin-coated between the metal layer and the silane-treated parylene.

**[0095]** Referring to 1509, in some embodiments, an ion membrane 1520 can be formed. In some embodiments, an ion membrane layer that includes any suitable thickness (e.g., 200 nm, 250 nm, and/or any other suitable thickness) of PEDOT:PSS at any suitable concentration (e.g., 1% GOPS) and chitosan of any suitable thickness (e.g., 700 nm, 750 nm, and/or any other suitable thickness) can be spin coated successively to form the ion membrane that covers gate electrode 1504. In some embodiments, the ion membrane can be patterned in any suitable manner. For example, in some embodiments, any suitable photolithography (e.g., using photoresist 1524) and plasma etching steps can be performed after depositing a protective layer of PMMA 1522 of any suitable thickness.

**[0096]** As described above, in some embodiments, a channel of the e-IGT can be formed using layer-by-layer deposition of PEDOT:PSS, as shown in FIG. 15A. At 1511, in some such embodiments, residues of photoresist 1524 and PMMA 1522 can be rinsed off in any suitable manner (e.g., using acetone, and/or in any other suitable manner), leaving the ion membrane layers intact. Continuing with this example, in some embodiments, a channel 1526 can be formed by spin coating any suitable material. For example, as described above in connection with FIG. 1, channel 1526 can be formed by spin coating a mixture of PEDOT:PSS with D-sorbitol at any suitable concentration (e.g., 40% D-sorbitol, 1% GOPS as a crosslinker, 0.1% DBSA, to improve film processing and wettability). In some embodiments, third parylene layer 1516 can then be peeled off. Continuing to 1513, in some embodiments, the PEDOT:PSS can then be coated with a PEI layer 1528, yielding the e-IGT shown at 1513 of FIG. 15A.

**[0097]** Alternatively, in some embodiments, a channel of the e-IGT can be formed using a solution-based PEDOT:PSS-PEI. Referring to FIG. 15B, at 1515, residues of photoresist 1524

and PMMA 1522 can be rinsed off in any suitable manner (e.g., using acetone, and/or in any other suitable manner), leaving the ion membrane layers intact. Continuing with this example, in some embodiments, a channel 1530 can be formed by coating a PEDOT:PSS-PEI solution. In some embodiments, third parylene layer 1516 can then be peeled off, yielding the e-IGT shown at 1517 of FIG. 15B.

**[0098]** In some embodiments, modifying characteristics of an e-IGT (e.g., characteristics of a channel of an e-IGT, characteristics of a gate electrode of an e-IGT, and/or any other suitable characteristics) can change performance characteristics of the e-IGT, such as a transconductance of the e-IGT. FIGS. 16A, 16B, 16C, and 16D show example graphs that illustrate effects of different e-IGT parameters on e-IGT transconductance in accordance with some embodiments of the disclosed subject matter. In some embodiments, the relationships between e-IGT characteristics and e-IGT transconductance shown in FIGS. 16A, 16B, 16C, and 16D can be used to fabricate an e-IGT with a particular transconductance, for example, to generate an e-IGT capable of a particular level of amplification. Note that, for all graphs shown in FIGS. 16A, 16B, 16C, and 16D, transconductance was calculated from a transfer curve for a drain voltage  $V_D = -0.6V$  and with a gate voltage  $V_G$  varying from 0V to -0.6V.

**[0099]** Turning to FIG. 16A, a graph 1602 illustrates a relationship between a ratio of PEDOT:PSS to PEI in a channel of an e-IGT on transconductance of the e-IGT. Additionally, FIG. 16A shows a graph 1604 that illustrates a relationship between a concentration of PEI used in a channel of an e-IGT on transconductance of the e-IGT.

**[0100]** Turning to FIG. 16B, a graph that illustrates a relationship between a thickness of a channel of an e-IGT on transconductance is shown in accordance with some embodiments of the disclosed subject matter.

**[0101]** Turning to FIG. 16C, a graph that illustrates a relationship between an area of a gate electrode of an e-IGT on transconductance is shown in accordance with some embodiments of the disclosed subject matter.

**[0102]** Turning to FIG. 16D, a graph that illustrates a relationship between a volume of a channel of an e-IGT on transconductance is shown in accordance with some embodiments of the disclosed subject matter. Note that, in some embodiments, operating characteristics of e-IGTs with different channel dimensions can be measured in any suitable manner. For example, similar

to what is shown in and described above in connection with FIG. 7, an array of any suitable number of e-IGTs can be microfabricated, each having different channel dimensions.

**[0103]** In some embodiments, e-IGTs can be used to fabricate digital logic gates, for example, for use in integrated circuits. Note that, due to the low current and high resistance of an e-IGT in an unbiased, OFF state, there can be high resistance paths between adjacent e-IGTs without any channel patterning. Conversely, depletion mode transistors, such as the d-IGTs shown in and described above in connection with FIG. 1, may have high conductivity in a channel in an unbiased OFF state, which may necessitate complex patterning processes to prevent cross-talk and current leakage between adjacent depletion mode transistors on an integrated circuit.

**[0104]** Turning to FIG. 17, examples of an OR gate 1702 and an AND gate 1704 fabricated using e-IGTs are shown in accordance with some embodiments of the disclosed subject matter. As shown in FIG. 17, OR gate 1702 can include a first e-IGT that has a gate terminal 1714, a source terminal 1716, and a drain terminal 1718, and a second e-IGT that has a gate terminal 1720, a source terminal 1722, and a drain terminal 1724. In some embodiments, input signals (shown as IN 1 and IN 2 in the micrographs shown in FIG. 17) can be applied to gate terminal 1714 of the first e-IGT and to gate terminal 1720 of the second e-IGT, respectively. FIG. 17 shows input voltage signals 1706 and 1708 that can be used as inputs to OR gate 1702 at gate terminal 1714 of the first e-IGT and gate terminal 1720 of the second e-IGT, respectively. FIG. 17 also shows an OR output signal 1710, which can be a drain current (shown as  $I_{Dout}$  in the micrograph shown in FIG. 17).

**[0105]** As shown in FIG. 17, AND gate 1704 can include a first e-IGT that has a gate terminal 1726, a source terminal 1728, and a drain terminal 1730, and a second e-IGT that has a gate terminal 1732, a source terminal 1734, and a drain terminal 1736. In some embodiments, input signals (shown as IN1 and IN2 in the micrographs shown in FIG. 17) can be applied to gate terminal 1726 of the first e-IGT and gate terminal 1732 of the second e-IGT respectively. FIG. 17 shows an AND output signal 1712 that can be a drain current (shown as  $I_{Dout}$  in the micrograph shown in FIG. 17) that is produced when input voltage signals 1706 and 1708 are applied to gate terminal 1726 of the first e-IGT and to gate terminal 1732 of the second e-IGT, respectively.

**[0106]** In some embodiments, a d-IGT and an e-IGT can be combined in the same circuit. For example, as shown in FIG. 18, in some embodiments, a d-IGT and an e-IGT can be combined to create a non-linear rectification circuit, which can be used for any suitable purpose, such as for inclusion in a neurostimulation device to improve a Signal-to-Noise Ratio (SNR) of detected signals. In some embodiments, an input to the circuit,  $V_{in}$ , can be connected to a gate electrode of a d-IGT 1802 and to a gate electrode of an e-IGT 1804. Therefore, as shown in FIG. 18,  $V_{in}$  can correspond to a gate voltage  $V_g$  applied to each of d-IGT 1802 and e-IGT 1804.

**[0107]** In some embodiments, when  $V_{in} < 0V$ , d-IGT 1802 can be doped at its full capacity, and changes in  $V_{in}$  at negative voltages do not change a conductance of d-IGT 1802. Therefore, in some embodiments, when  $V_{in} < 0V$ , d-IGT 1802 can act as a low value resistor with a resistance dependent on a geometry of d-IGT 1802. In some embodiments, when  $V_{in} < 0V$ , e-IGT 1804 can be in its linear region of operation. Therefore, in some embodiments, when  $V_{in} < 0V$ , the combination of d-IGT 1802 acting as a resistor and e-IGT operating in its linear region can form a non-inverting amplifier circuit, where the input signal  $V_{in}$  will be amplified using the e-IGT-based non-inverting amplifier.

**[0108]** In some embodiments, when  $V_{in} \approx 0V$ , e-IGT 1804 can be de-doped and can therefore act as a significantly higher-value resistor compared to d-IGT 1802, which can still be in a doped state. Therefore, a voltage drop across d-IGT 1802 (measured across a drain electrode and a source electrode of d-IGT 1802) can be low, and the d-IGT will not be able to function as a transistor. Continuing further, in this state, the circuit shown in FIG. 18 can be approximated as a resistor equal to the resistance of the e-IGT in its de-doped state. Therefore, when  $V_{in} \approx 0V$ , no amplification occurs, and the output current can be proportional to a resistance of the e-IGT.

**[0109]** In some embodiments, when  $V_{in} > 0V$ , e-IGT 1804 can be in a de-doped state, and will maintain a high channel resistance. Additionally, when  $V_{in} > 0V$ , d-IGT 1802 can begin gradually de-doping as  $V_{in}$  increases and can have a resistance comparable to a resistance of e-IGT 1804. Therefore, at positive values of  $V_{in}$ , the sum of resistance of both d-IGT 1802 and e-IGT 1804 in their de-doped state will be the total circuit resistance, and no amplification occurs.

**[0110]** In some embodiments, characteristics of the non-linear rectification circuit shown in FIG. 18 can be changed by varying a geometry of the d-IGT relative to the e-IGT. For example, when an input voltage  $V_{in}$  1806 (e.g., a 1 Hz sine wave, as shown in FIG. 18) is applied to the gate electrodes of d-IGT 1802 and e-IGT 1804, in an instance in which d-IGT 1802 and e-

IGT 1804 have equivalent geometry (e.g., the same dimensions, and/or equivalent geometry in any other suitable manner), can result in thresholding at 0V, as shown by output voltage signal 1808 (e.g., measured at  $V_{out}$ , as shown in the circuit diagram of FIG. 18). As another example, in an instance in which d-IGT 1802 is smaller than e-IGT 1804 (e.g., a smaller channel width, a smaller channel length, and/or smaller in any other suitable manner), applying input voltage  $V_{in}$  1806 to the gate electrodes of d-IGT 1802 and e-IGT 1804 can result in thresholding at negative voltages, as shown by output voltage signal 1810 (e.g., measured at  $V_{out}$ , as shown in the circuit diagram of FIG. 18).

**[0111]** In some embodiments, IGTs can be used for any suitable applications. For example, in some embodiments, IGTs can be used for recording electrical signals from a skin surface of a subject. As a more particular example, as described above in connection with FIG. 11A, in some embodiments, IGTs can be used to record EEG signals from a scalp of a subject. As another more particular example, in some embodiments, electrocardiography (ECG) recordings can be performed using IGTs by placing a probe that includes an IGT on the skin over the left anterior chest of a subject. As yet another more particular example, in some embodiments, electromyography (EMG) recordings can be performed using IGTs placed on the skin over any suitable muscle (e.g., a biceps muscle, a triceps muscle, a quadriceps muscle, and/or any other suitable muscle(s)). In some embodiments, a gate electrode of an IGT can be used as a reference electrode, and can be placed on a reference position of the subject (e.g., on a wrist of the subject, and/or any other suitable reference position).

**[0112]** As another example, in some embodiments, IGTs can be used for invasively recording neurophysiological signals, such as action potentials, local field potentials (LFPs), and/or any other suitable neurophysiological signals. As a more particular example, in some embodiments, IGTs can be placed on a cortical surface to record any suitable cortical surface neurophysiological activity. In some such embodiments, any suitable number of IGTs (e.g., one, two, five, ten, and/or any other suitable number) can be fabricated on a conformable substrate of any suitable material that can be placed on the cortical surface. In some embodiments, recordings can be made with IGTs in any suitable configuration. For example, in some embodiments, a resistor can be placed in series with a drain electrode of each IGT to convert a drain current to a voltage, which can be acquired by any suitable acquisition system as a measure of neural activity. As another example, in some embodiments, in an instance in which multiple

IGTs are fabricated in an array, each IGT can have a common source. As yet another example, in some embodiments, a gate electrode of each IGT in a fabricated array can be connected to a screw (e.g., a surgical-grade stainless steel screw) inserted in any suitable brain area (e.g., the cerebellum, and/or any other suitable brain area). Note that, in some embodiments, voltages from each e-IGT can be measured with respect to any suitable ground or reference electrode placed at any suitable location (e.g., another brain area, such as the cerebellum, and/or any other suitable area). In some such embodiments, surgical-grade stainless steel screws can be used as ground or reference electrodes.

**[0113]** As another more particular example, neural signals from deep cortical layers can be recorded by inserting one or more IGTs at any suitable cortical location and to any suitable depth (e.g., 1.5 mm, and/or any other suitable depth). Turning to FIG. 11B, an example of a device 1150 that includes e-IGTs to record neurophysiological signals by inserting a probe in a cortical area is shown in accordance with some embodiments of the disclosed subject matter. As illustrated, in some embodiments, any suitable number of e-IGTs (e.g., e-IGTs 1152, 1154, 1156, and 1158, as shown in FIG. 11B) can be fabricated on any suitable conformable substrate (e.g., a conformable parylene-C substrate, and/or any other suitable substrate). In some embodiments, the device can then be inserted in a cortical area in any suitable manner. For example, in some embodiments, the device can be inserted by wrapping the device around any suitable guide wire (e.g., a tungsten microwire, and/or any other suitable guide wire), which can then be used to guide the device during insertion. In some embodiments, a guidewire can be connected to the fabricated e-IGT device via an anchor hole 1160, and when device 1150 reaches a desired cortical depth, the guidewire can be removed from anchor hole 1160, leaving device 1150 at the desired cortical depth and location.

**[0114]** Note that, in some embodiments, the e-IGTs can share a common source. In some embodiments, a gate electrode of the e-IGT can be connected to a screw (e.g., a surgical-grade stainless steel screw, and/or any other suitable screw) implanted in any suitable brain area (e.g., the cerebellum, and/or any other suitable area). In some embodiments, a resistor of any suitable value can be placed in series with each drain electrode to convert a corresponding drain current to a voltage, which can then be measured using any suitable acquisition system as a measure of neural activity. Note that, in some embodiments, voltages from each e-IGT can be measured with respect to any suitable ground or reference electrode placed at any suitable

location (e.g., another brain area, such as the cerebellum, and/or any other suitable area). In some such embodiments, surgical-grade stainless steel screws can be used as ground or reference electrodes. Note that placement of IGT probes for invasive neurophysiological recording can be performed in connection with any suitable surgical procedure(s).

**[0115]** In some embodiments, IGTs, whether operating in depletion mode or enhancement mode, can be used to form biomedical sensors or stimulus sources and can be connected to any suitable additional circuits, devices, systems, etc. More particularly, for example, IGTs as described herein can be used to act as sensors for detecting biomedical data that can be captured by a biomedical device, a fitness device, a portable computer, an Internet-of-Things (IoT) device, a smart watch, a smart ring, and/or any other suitable device.

**[0116]** Such a biomedical device, a fitness device, a portable computer, an Internet-of-Things (IoT) device, a smart watch, a smart ring, and/or any other suitable device can include and/or be any of a general-purpose device or a special-purpose device. Any such general-purpose device or special-purpose device can include any suitable hardware. For example, as illustrated in example hardware 1900 of FIG. 19, such hardware can include a hardware processor 1902, memory and/or storage 1904, an input device controller 1906, an input device 1908, display/audio drivers 1910, display and/or audio output circuitry 1912, communication interface(s) 1914, an antenna 1916, and a bus 1918.

**[0117]** Hardware processor 1902 can include any suitable hardware processor, such as a microprocessor, a micro-controller, digital signal processor, dedicated logic, and/or any other suitable circuitry for controlling the functioning of a general-purpose computer or special purpose computer in some embodiments.

**[0118]** Memory and/or storage 1904 can be any suitable memory and/or storage for storing programs, data, metrics, and/or any other suitable information in some embodiments. For example, memory and/or storage 1904 can include random access memory, read only memory, flash memory, hard disk storage, optical media, and/or any other suitable storage device.

**[0119]** Input device controller 1906 can be any suitable circuitry for controlling and receiving input from one or more input devices 1908 in some embodiments. For example, input device controller 1906 can be circuitry for receiving input from a touch screen, from one or more buttons, from a voice recognition circuit, from a microphone, from a camera, from an optical sensor, from an accelerometer, from a temperature sensor, from a near field sensor, and/or any

other suitable circuitry for receiving user input. In some embodiments, an input device can include an IGT for sensing biomedical conditions of a human. In some embodiments, input device controller 1906 or an input device 1908 can include an analog-to-digital converter for converting analog signals from an IGT, or a sensor or circuit including one or more IGTs, into a digital signal suitable for processing by hardware processor 1902.

**[0120]** Display/audio drivers 1910 can be any suitable circuitry for controlling and driving output to one or more display and/or audio output circuitries 1912 in some embodiments. For example, display/audio drivers 1910 can be circuitry for driving an LCD display, a speaker, an LED, and/or any other display/audio device. In some embodiments, an output device can include an IGT for providing stimulus to a user (e.g., neurostimulation, electrical stimulation on a skin surface of a user, and/or any other suitable stimulus).

**[0121]** Communication interface(s) 1914 can be any suitable circuitry for interfacing with one or more communication networks, such as the Internet or any other suitable network or combination of networks, in some embodiments. For example, interface(s) 1914 can include network interface card circuitry, wireless communication circuitry, and/or any other suitable circuitry for interfacing with one or more communication networks.

**[0122]** Antenna 1916 can be any suitable one or more antennas for wirelessly communicating with a communication network in some embodiments. In some embodiments, antenna 1916 can be omitted when not needed.

**[0123]** Bus 1918 can be any suitable mechanism for communicating between two or more of components 1902, 1904, 1906, 1910, and 1914 in some embodiments.

**[0124]** Any other suitable components can be included in hardware 1900 in accordance with some embodiments.

**[0125]** In some embodiments, any suitable computer readable media can be used for storing instructions for performing the functions and/or processes herein. For example, in some embodiments, computer readable media can be transitory or non-transitory. For example, non-transitory computer readable media can include media such as non-transitory forms of magnetic media (such as hard disks, floppy disks, and/or any other suitable magnetic media), non-transitory forms of optical media (such as compact discs, digital video discs, Blu-ray discs, and/or any other suitable optical media), non-transitory forms of semiconductor media (such as flash memory, electrically programmable read-only memory (EPROM), electrically erasable

programmable read-only memory (EEPROM), and/or any other suitable semiconductor media), any suitable media that is not fleeting or devoid of any semblance of permanence during transmission, and/or any suitable tangible media. As another example, transitory computer readable media can include signals on networks, in wires, conductors, optical fibers, circuits, any suitable media that is fleeting and devoid of any semblance of permanence during transmission, and/or any suitable intangible media.

**[0126]** Accordingly, internal-ion gated electrochemical transistors are provided.

**[0127]** Although the invention has been described and illustrated in the foregoing illustrative embodiments, it is understood that the present disclosure has been made only by way of example, and that numerous changes in the details of implementation of the invention can be made without departing from the spirit and scope of the invention, which is limited only by the claims that follow. Features of the disclosed embodiments can be combined and rearranged in various ways.

**What is Claimed Is:**

1. An internal-ion gated electrochemical transistor, comprising:  
a gate electrode, a source electrode, and a drain electrode;  
a channel formed between the source electrode and the drain electrode, wherein the channel comprises a material that includes a conducting polymer and a biocompatible solution, wherein the channel serves as a reservoir of positively charged mobile ions; and  
an ion membrane between the channel and the gate electrode, wherein:  
in an off state of the internal-ion gated electrochemical transistor, at least a subset of the positively charged mobile ions are ionically bonded to negatively charged ions of the conducting polymer, and wherein in an on state of the internal-ion gated electrochemical transistor, at least a subset of the positively charged mobile ions are unbonded from the negatively charged ions of the conducting polymer to induce a current within the channel, and wherein at least one of the off state and the on state of the internal-ion gated electrochemical transistor is actuated by application of a voltage to the gate electrode.
2. The internal-ion gated electrochemical transistor of claim 1, wherein the on state of the internal-ion gated electrochemical transistor is a state of the internal-ion gated electrochemical transistor when no voltage is applied to the gate electrode.
3. The internal-ion gated electrochemical transistor of claim 1, wherein the off state of the internal-ion gated electrochemical transistor is a state of the internal-ion gated electrochemical transistor when no voltage is applied to the gate electrode.
4. The internal-ion gated electrochemical transistor of claim 1, wherein the conducting polymer is comprised of PEDOT:PSS.
5. The internal-ion gated electrochemical transistor of claim 4, wherein the conducting polymer is further comprised of polyethylenimine (PEI).
6. The internal-ion gated electrochemical transistor of claim 1, wherein the biocompatible solution is comprised of D-sorbitol.

7. The internal-ion gated electrochemical transistor of claim 1, wherein the ion membrane is comprised of chitosan.
8. The internal-ion gated electrochemical transistor of claim 1, wherein a transconductance of the internal-ion gated electrochemical transistor is based on a volume of the channel.
9. The internal-ion gated electrochemical transistor of claim 1, wherein the gate electrode, the source electrode, and the drain electrode are patterned on a conformable substrate.
10. The internal-ion gated electrochemical transistor of claim 1, wherein the conformable substrate comprises parylene.

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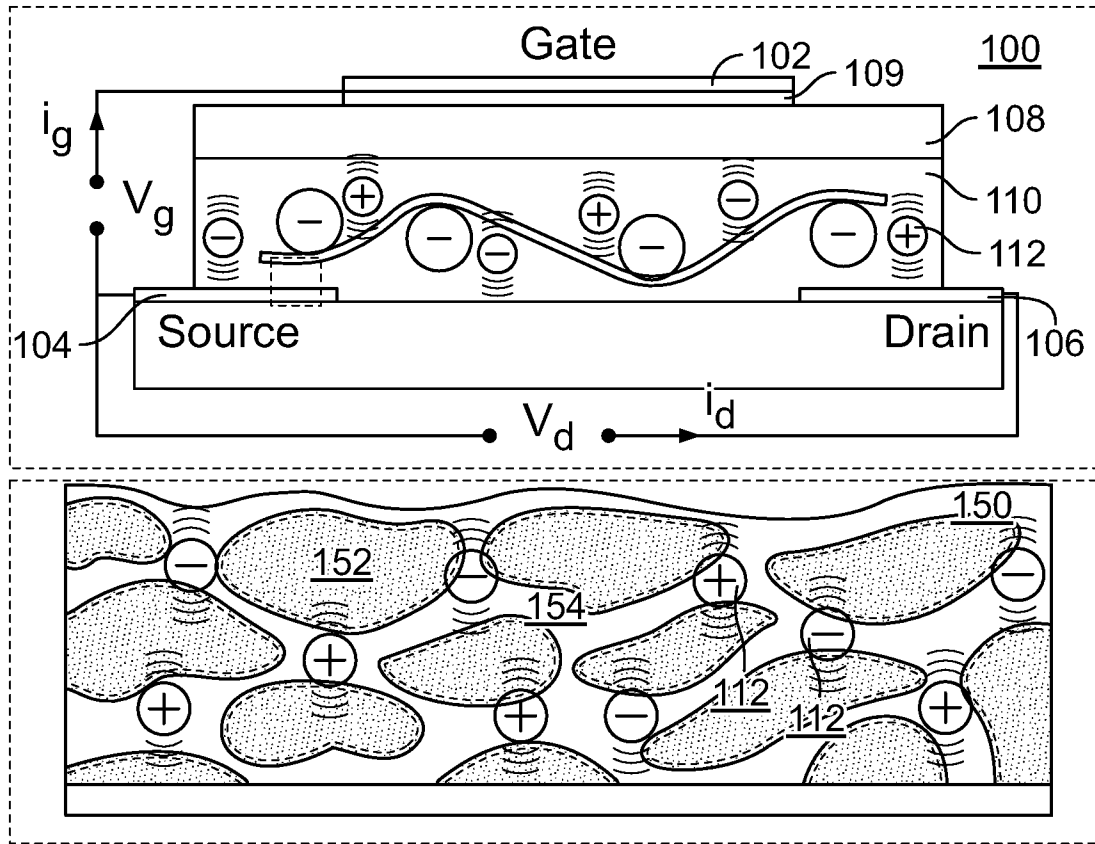


FIG. 1

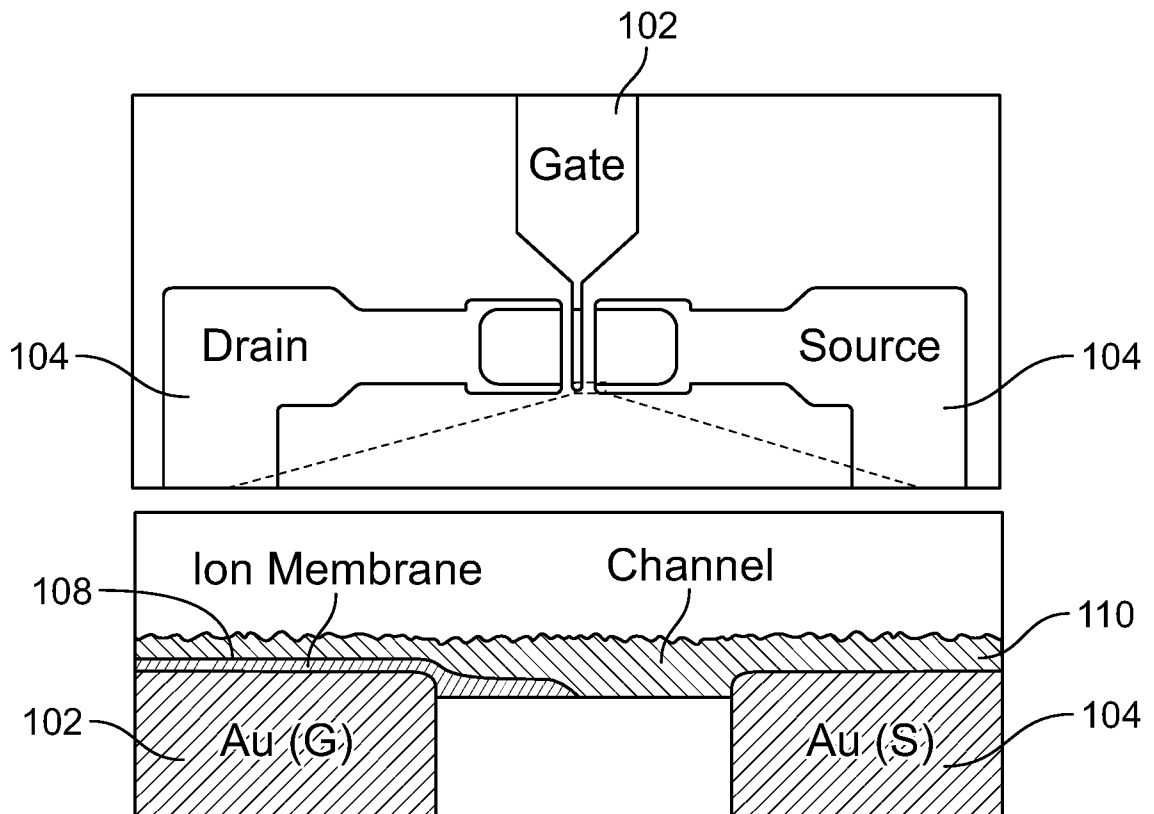


FIG. 2

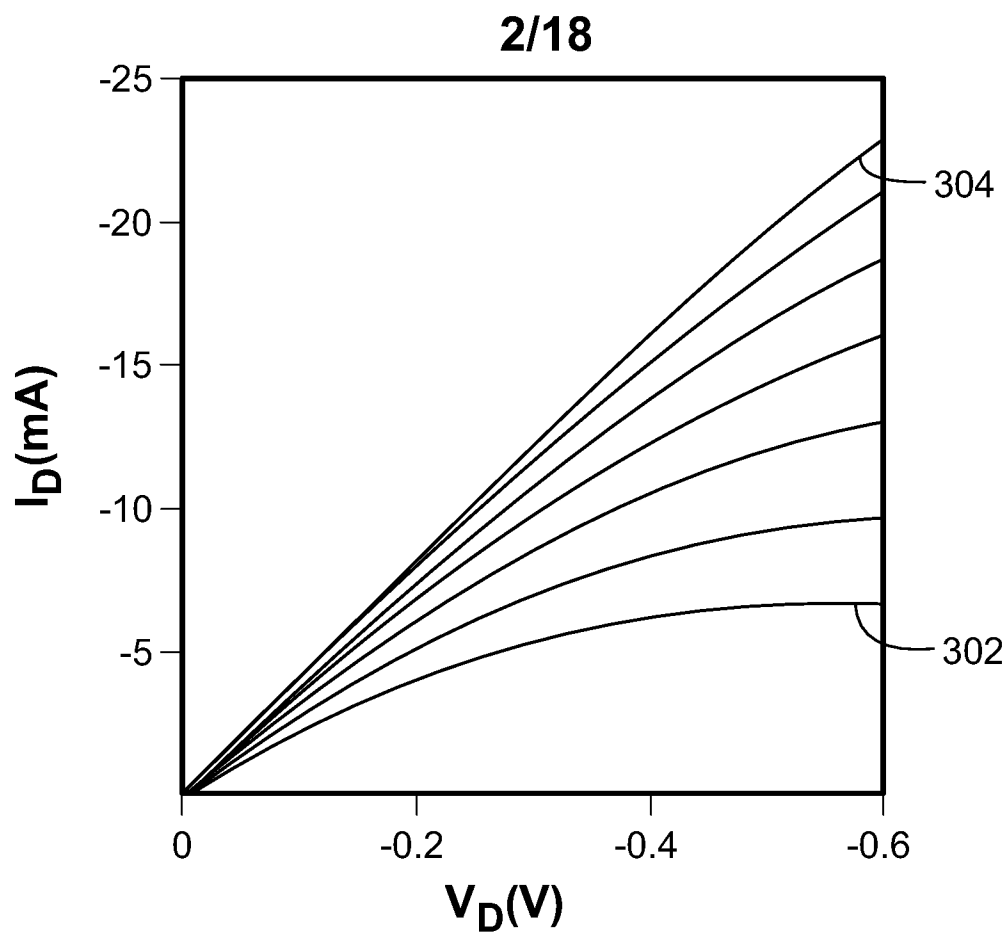


FIG. 3A

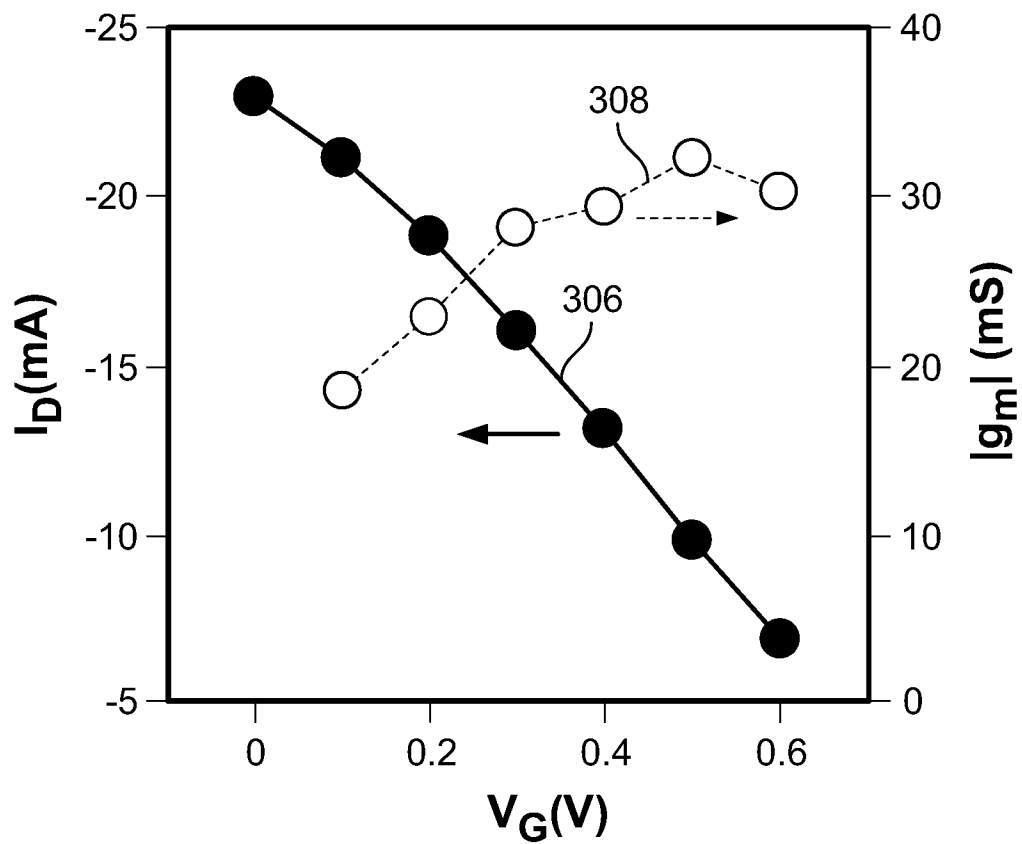


FIG. 3B

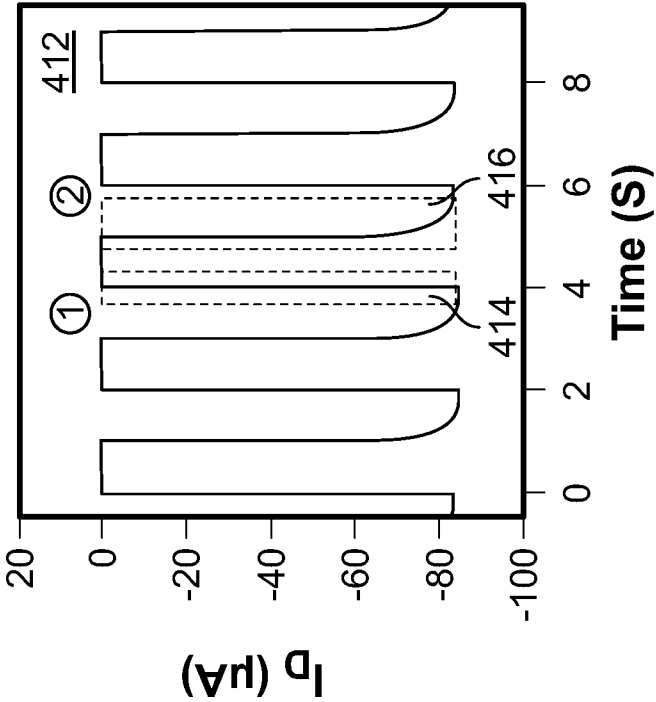
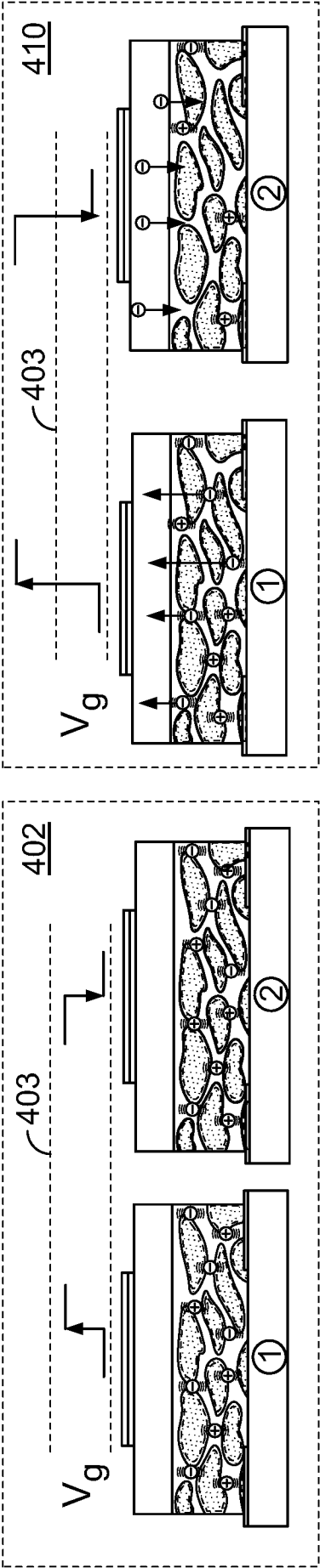


FIG. 4B

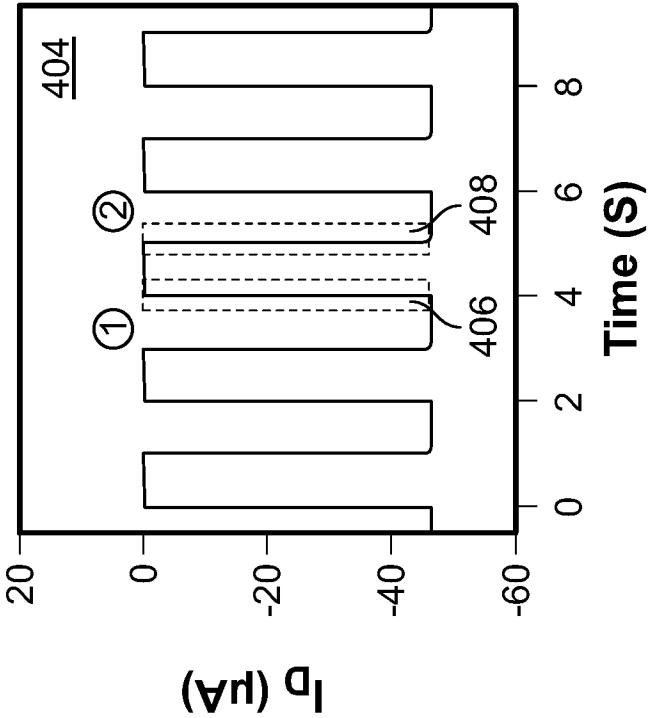


FIG. 4A

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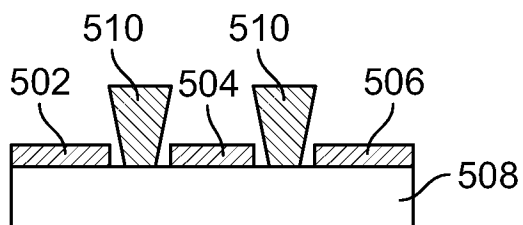


FIG. 5A

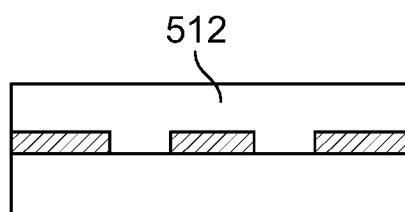


FIG. 5B

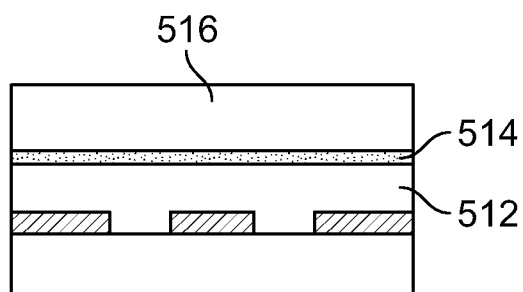


FIG. 5C

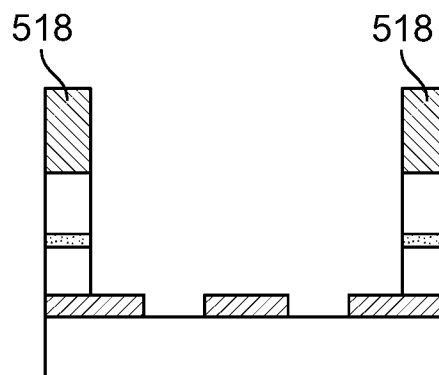


FIG. 5D

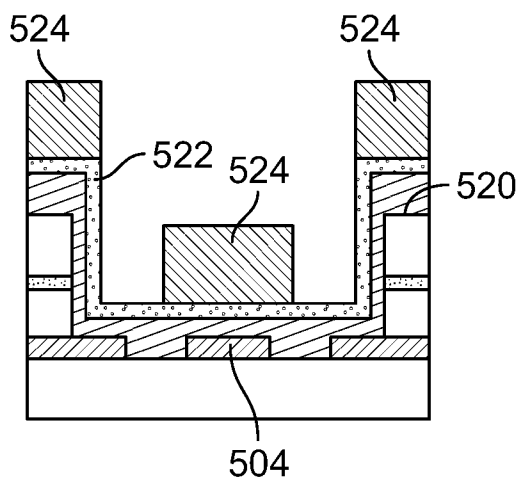


FIG. 5E

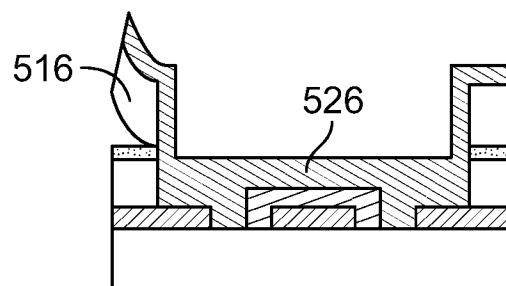


FIG. 5F

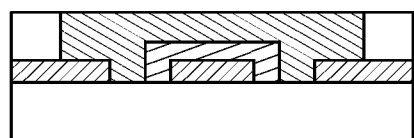


FIG. 5G

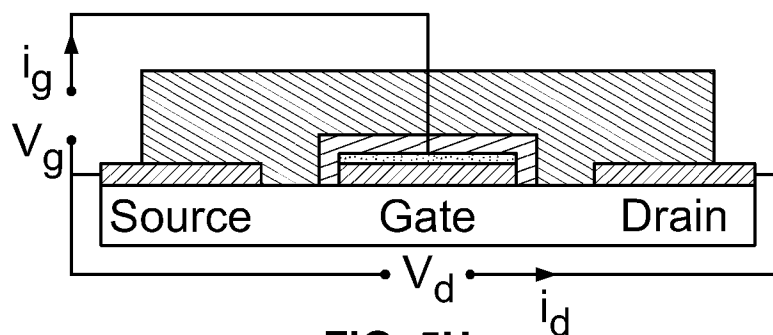


FIG. 5H

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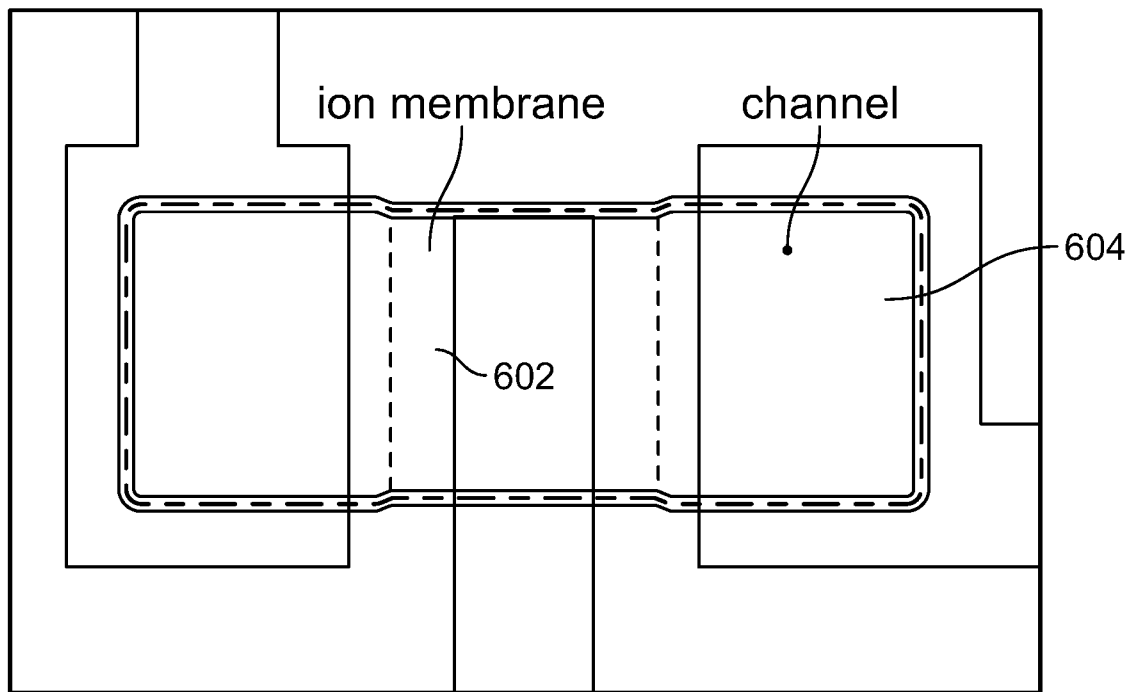


FIG. 6

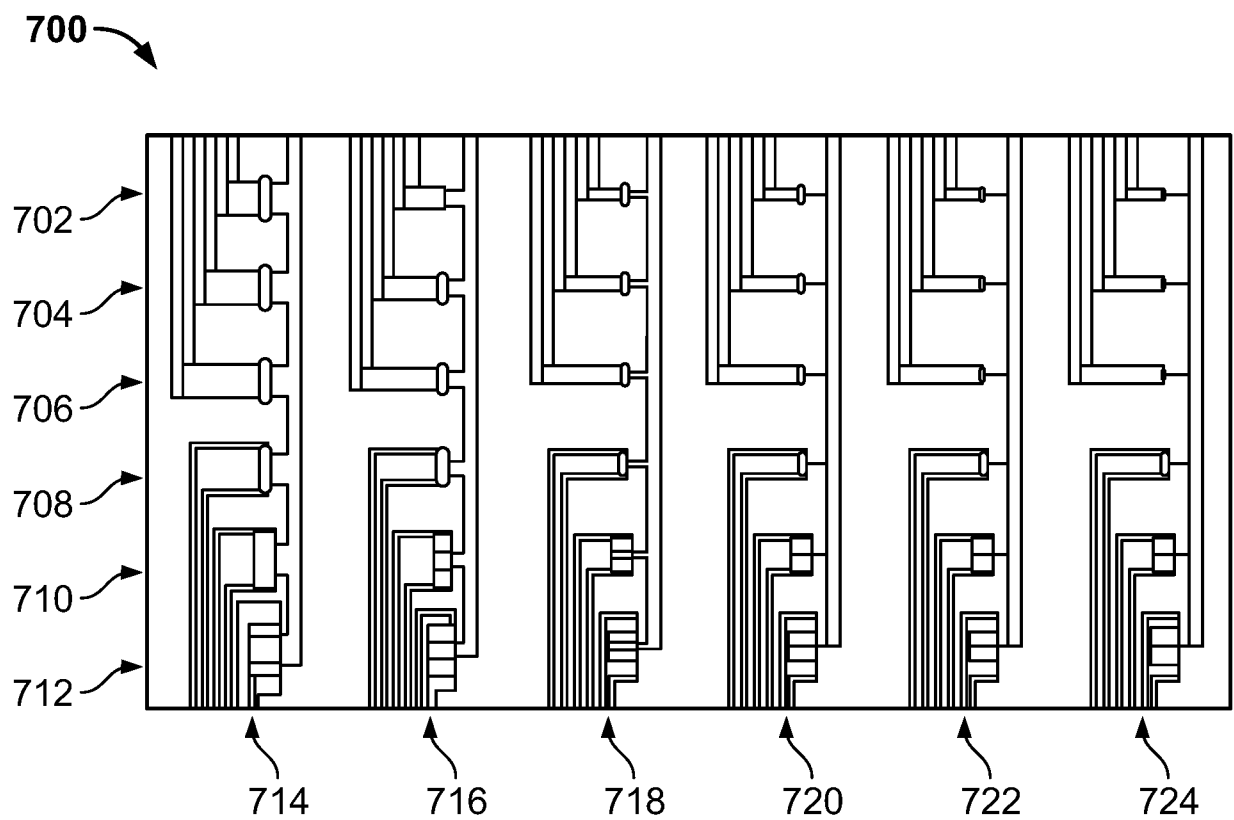
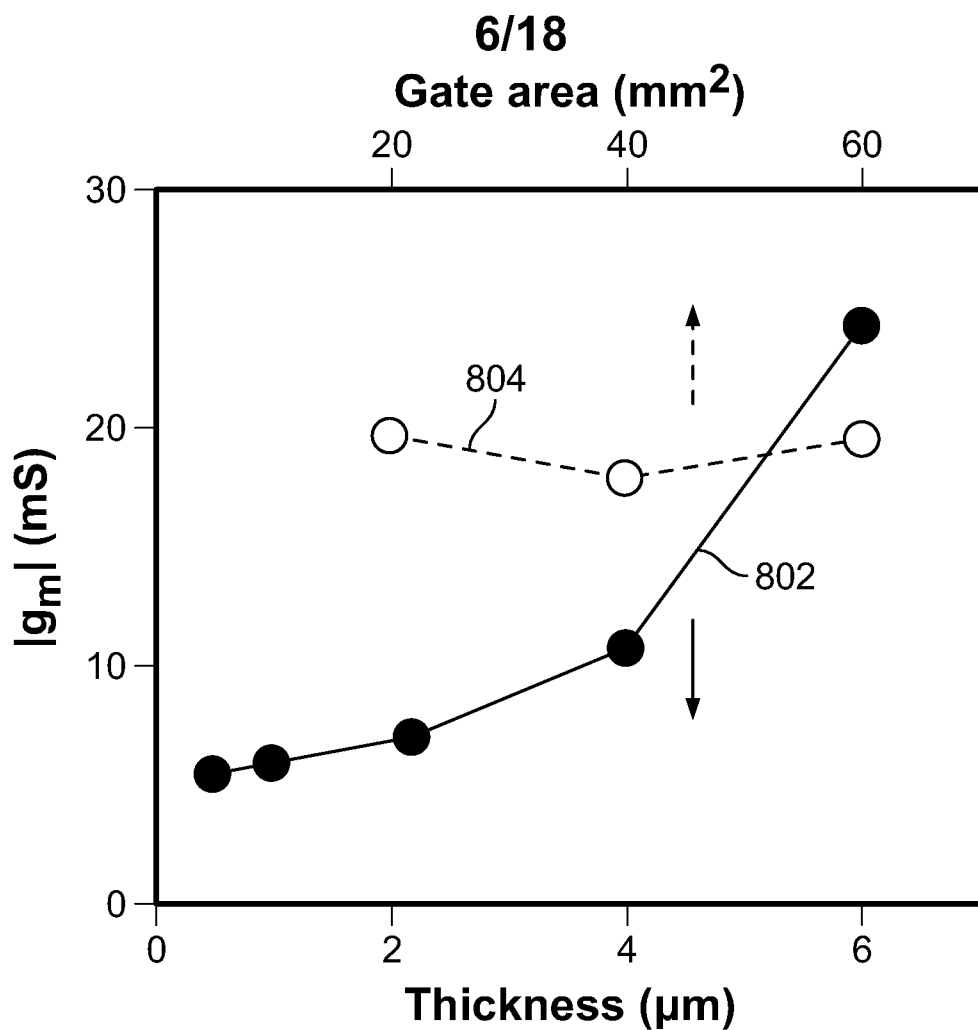
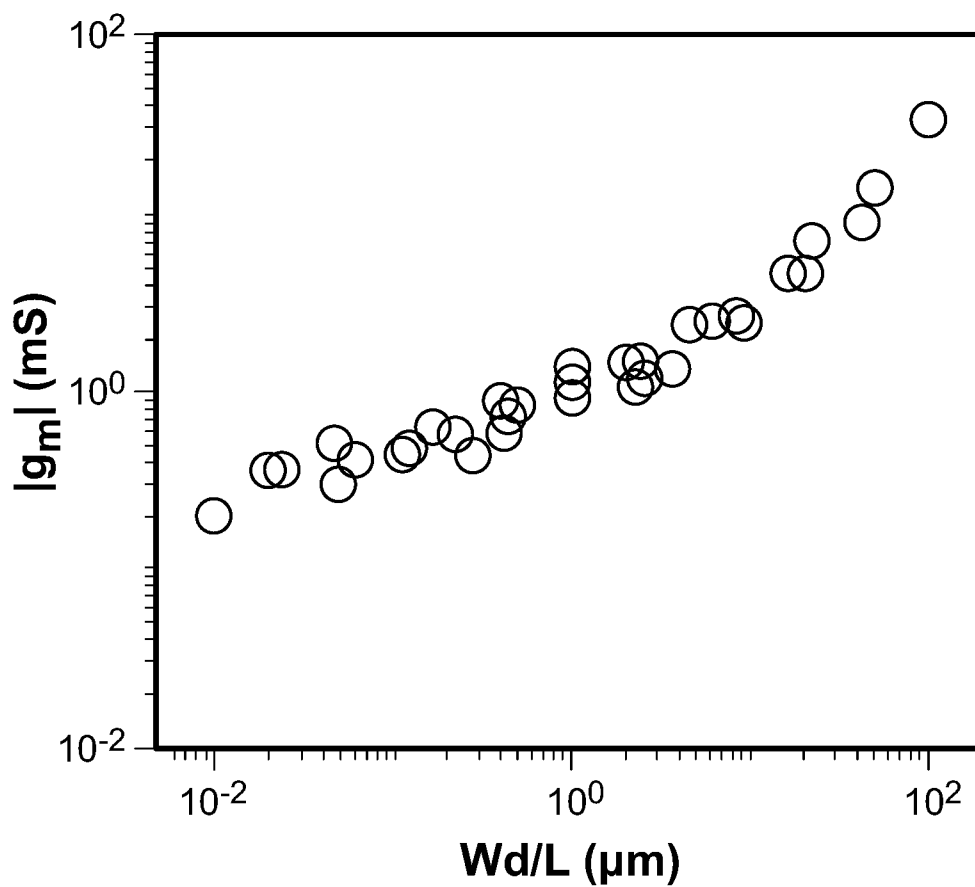


FIG. 7



**FIG. 8A**



**FIG. 8B**

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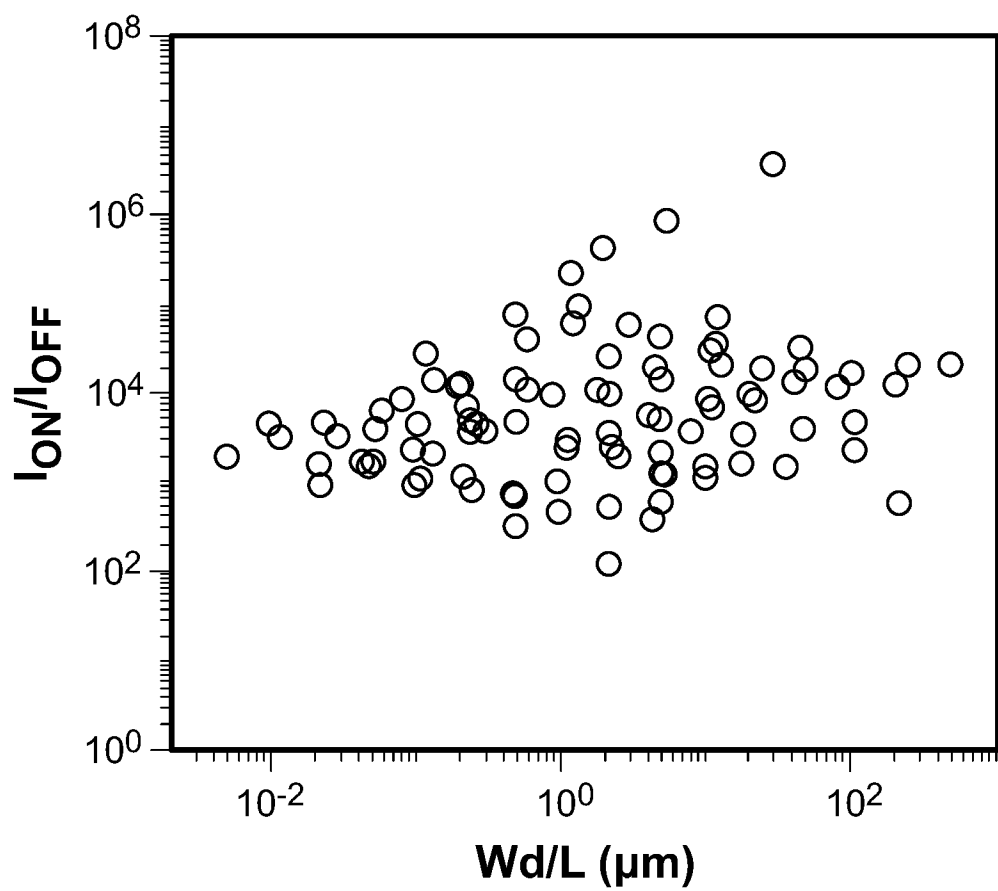


FIG. 8C

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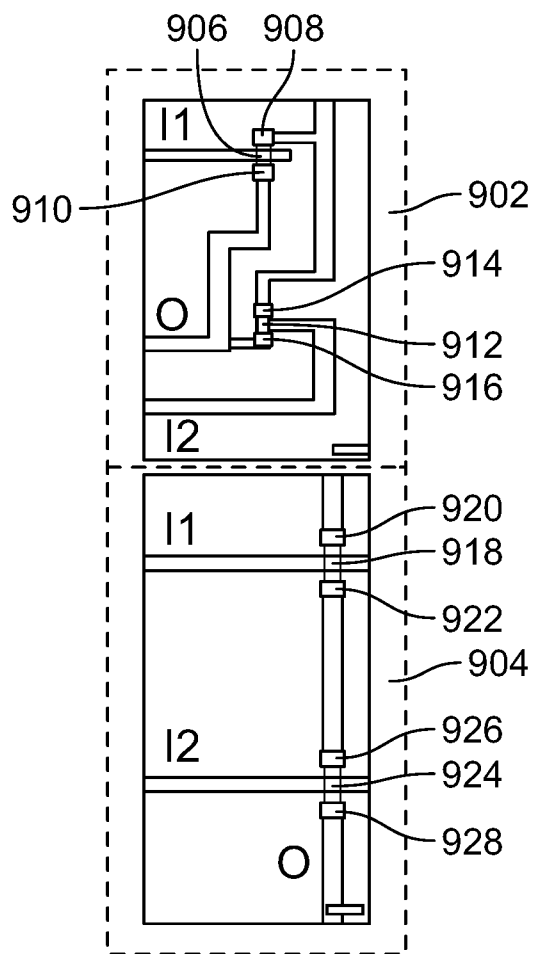


FIG. 9A

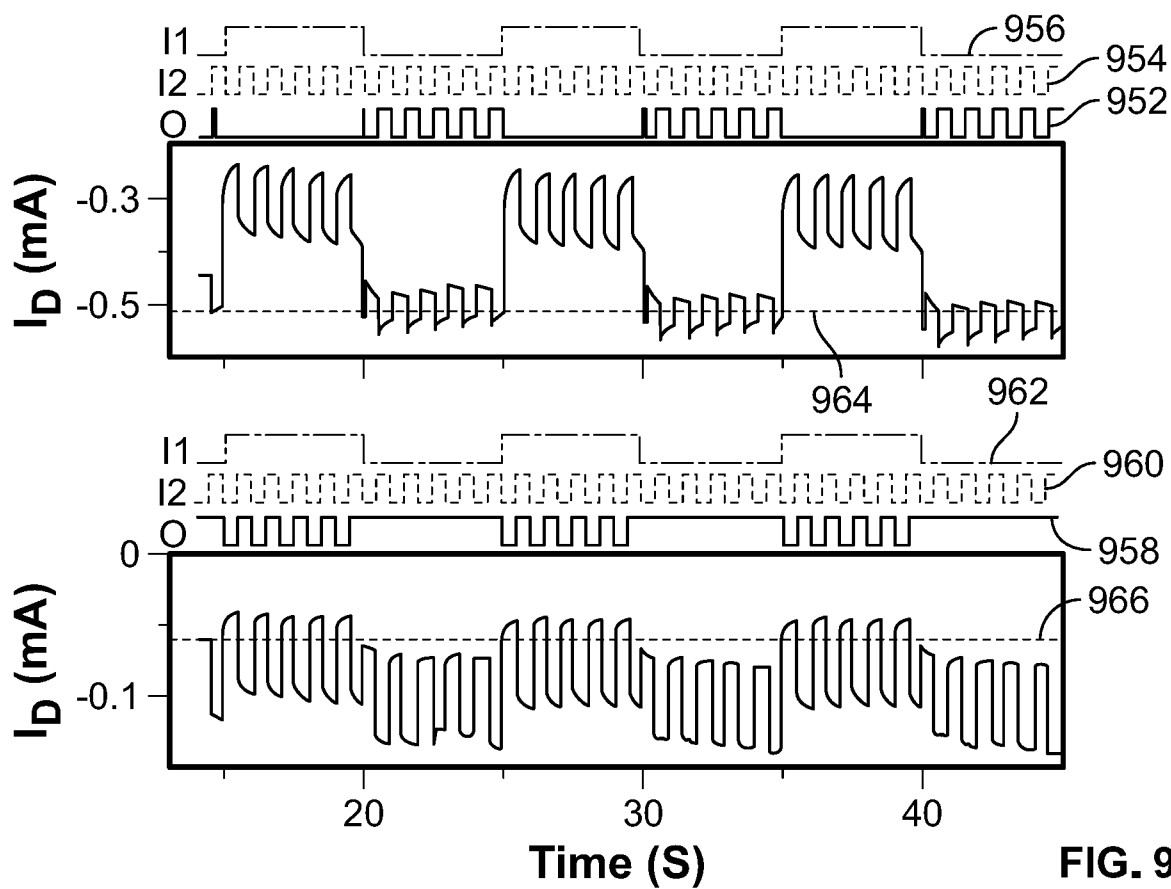


FIG. 9B

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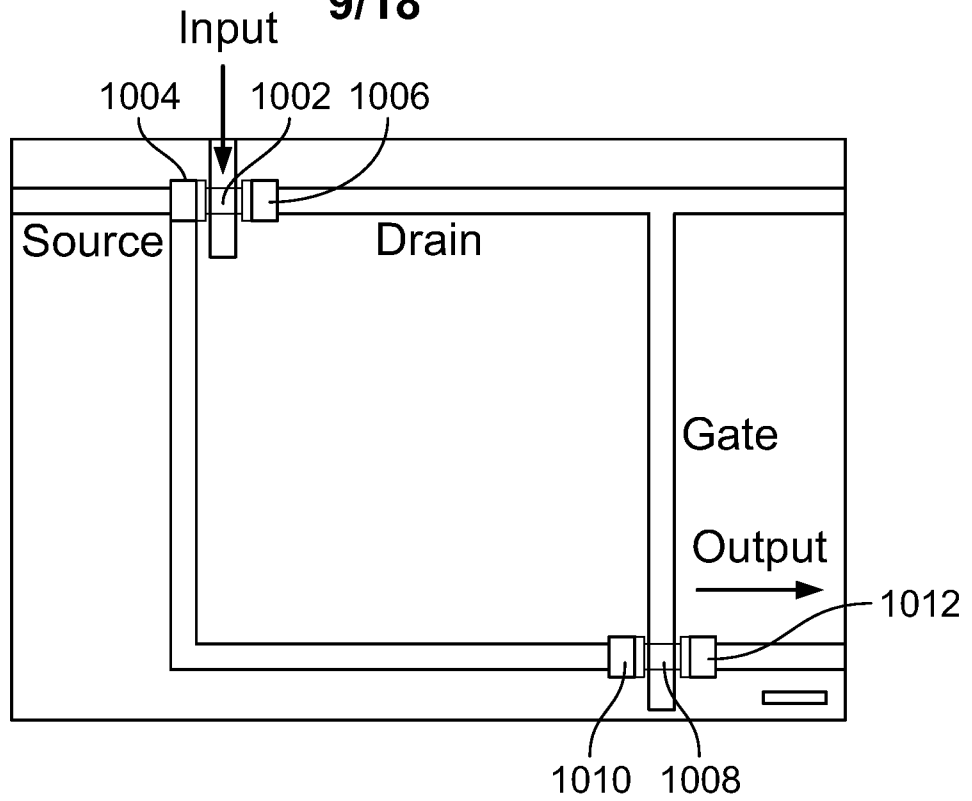


FIG. 10A

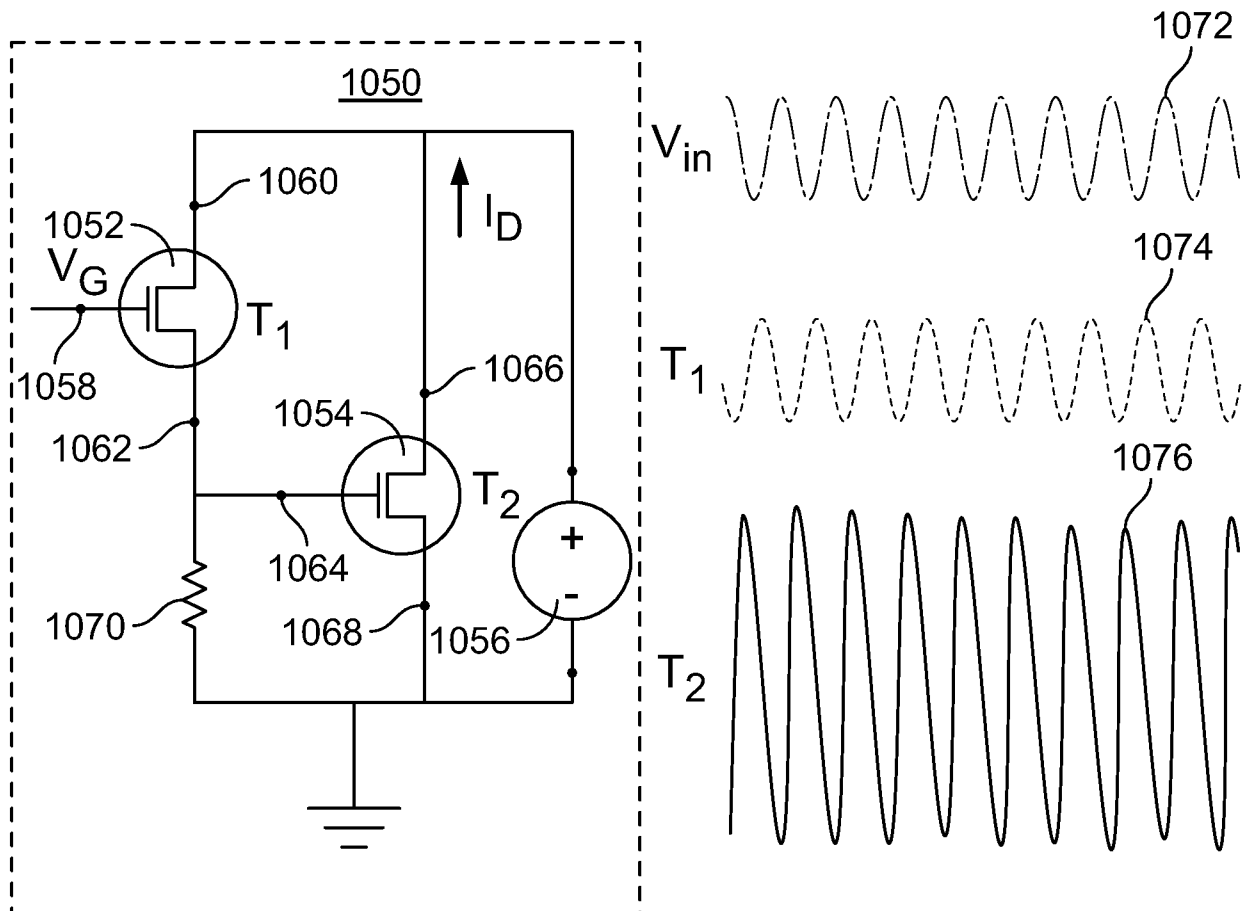


FIG. 10B

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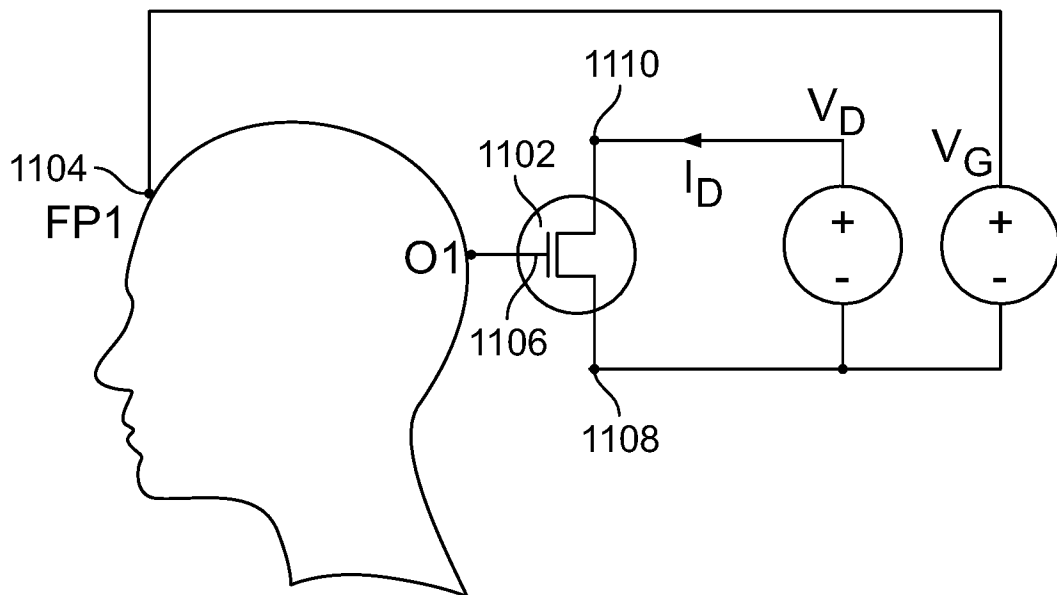


FIG. 11A

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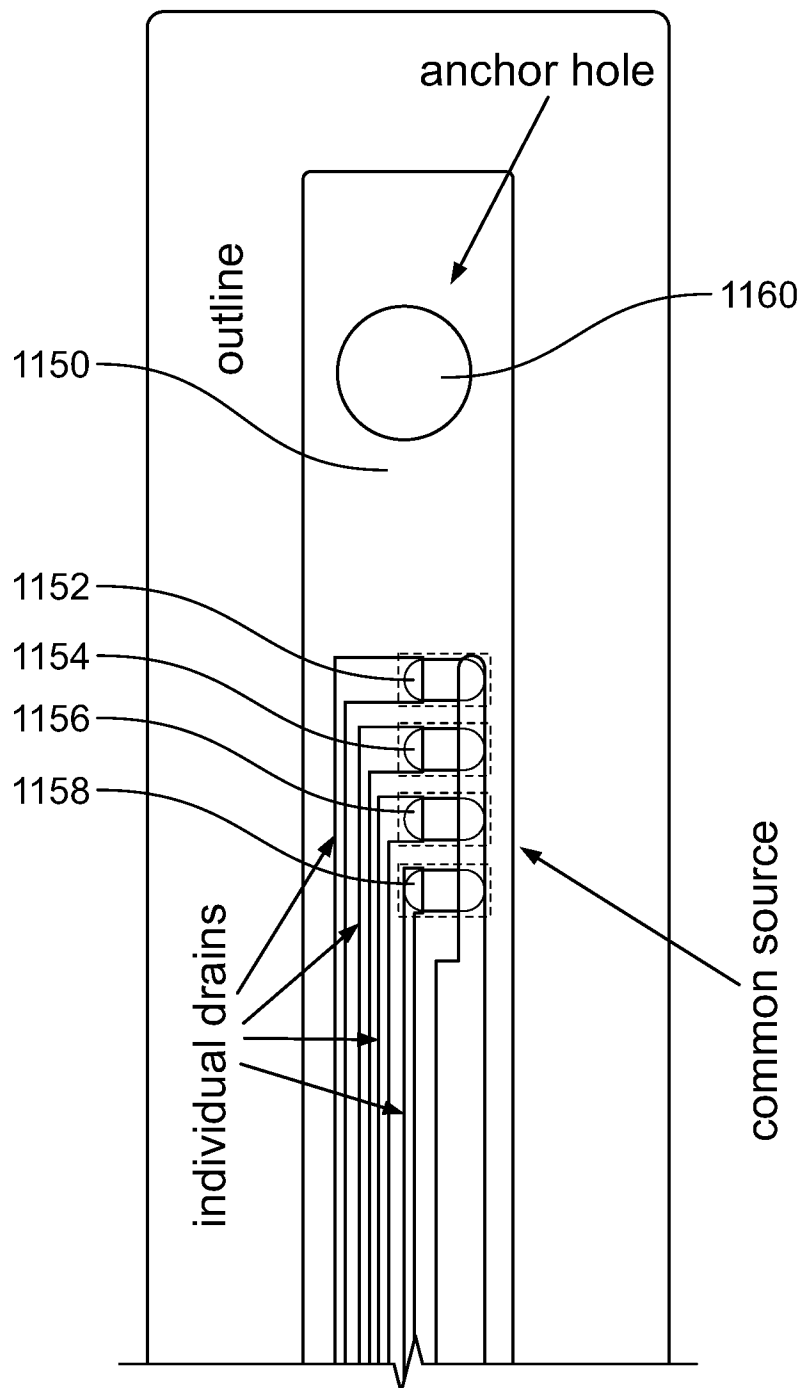


FIG. 11B

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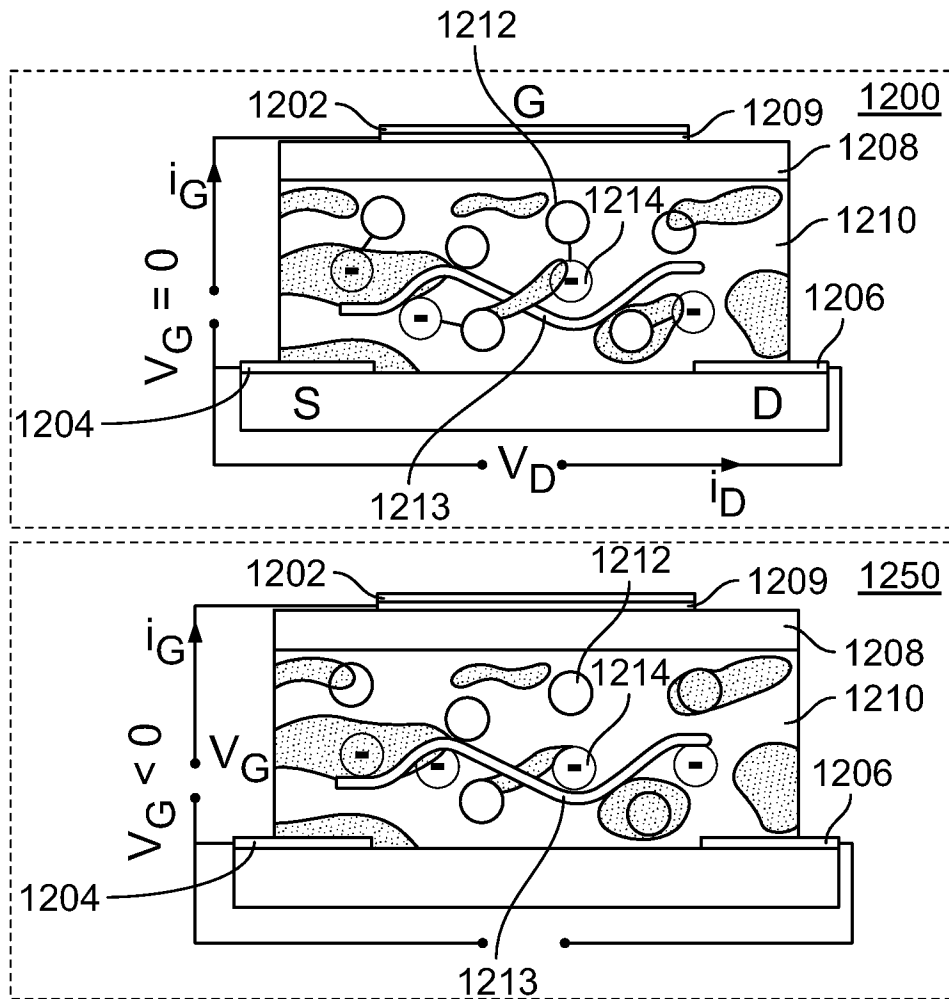


FIG. 12

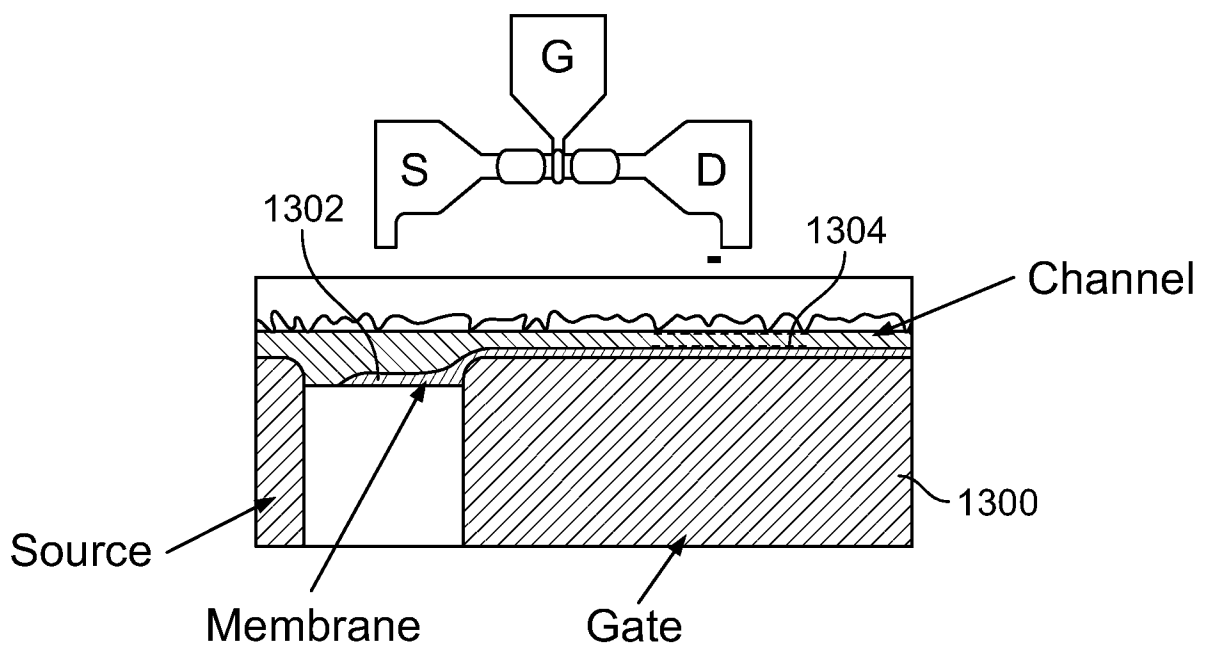


FIG. 13

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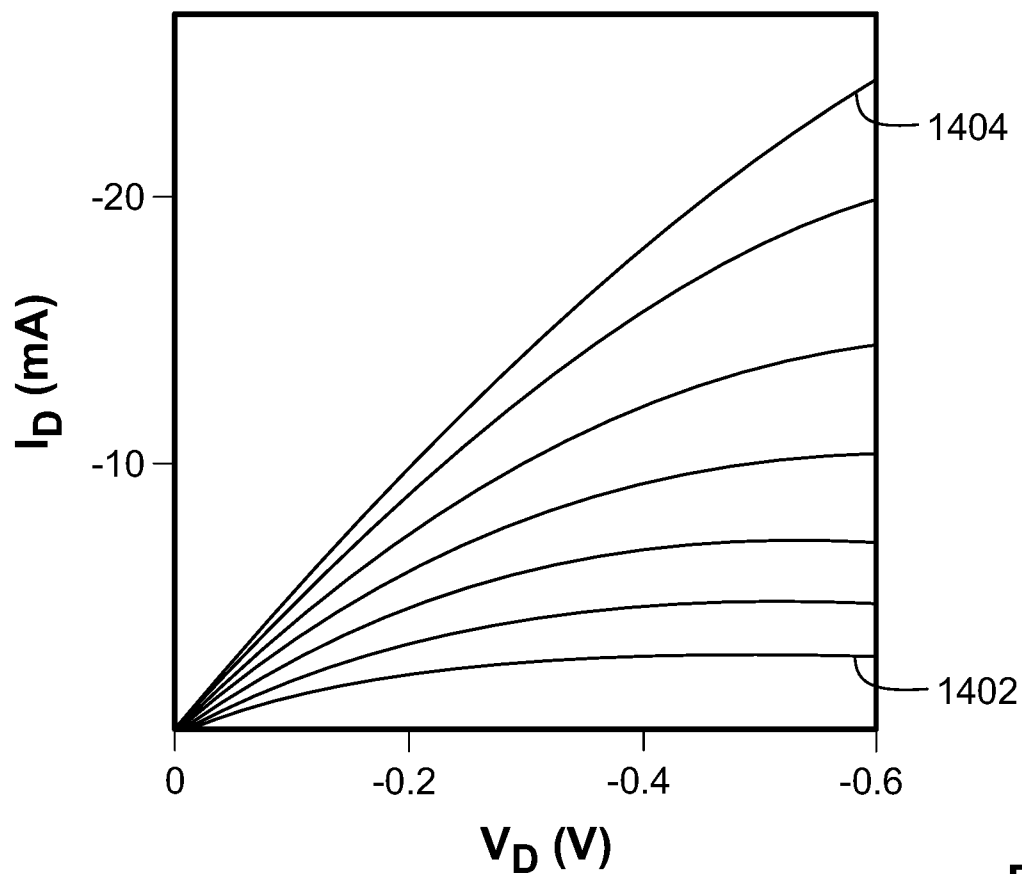


FIG. 14A

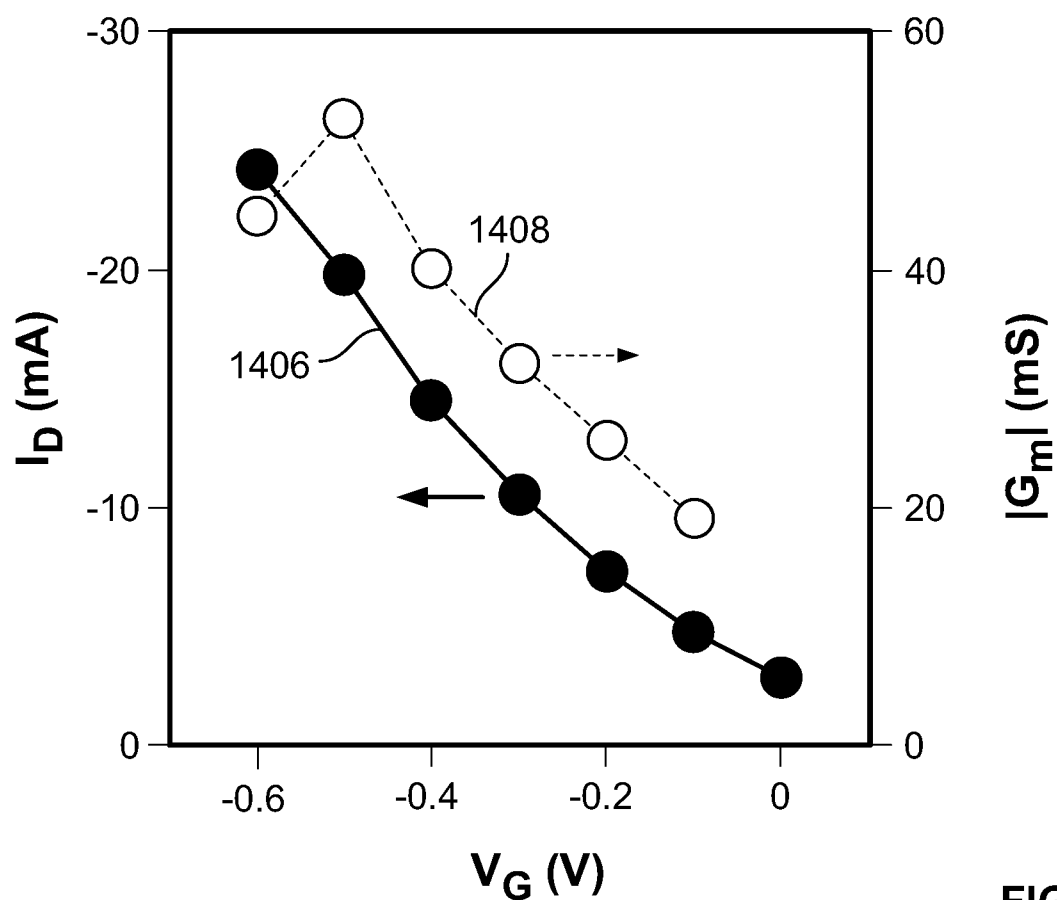


FIG. 14B

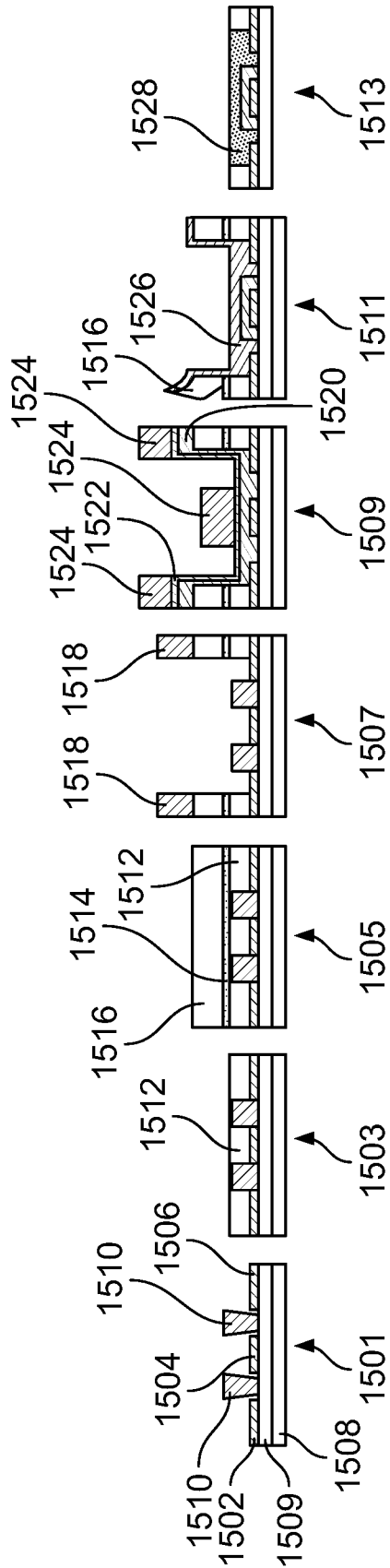


FIG. 15A

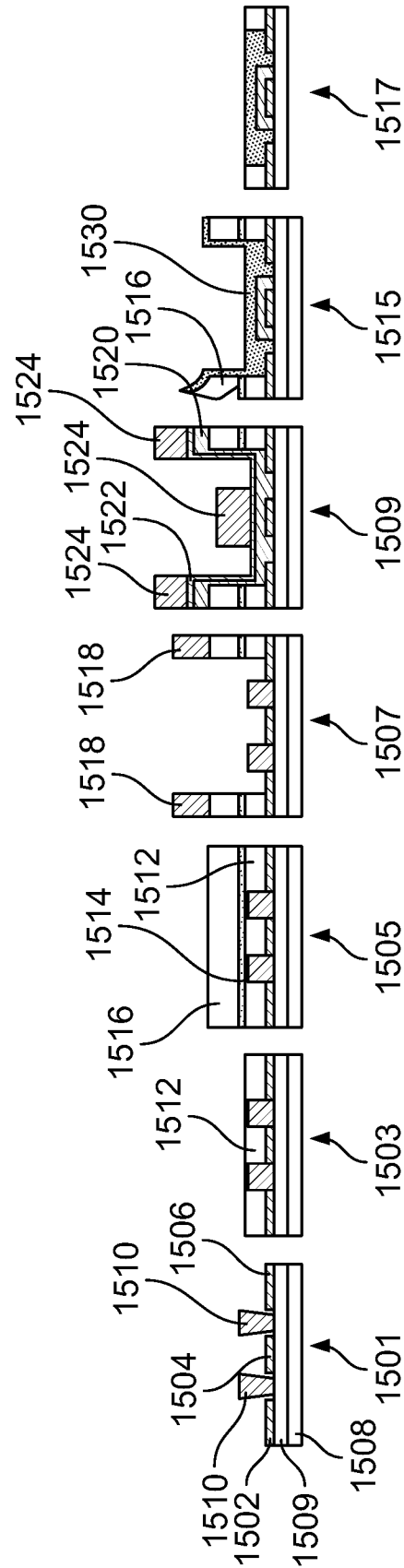


FIG. 15B

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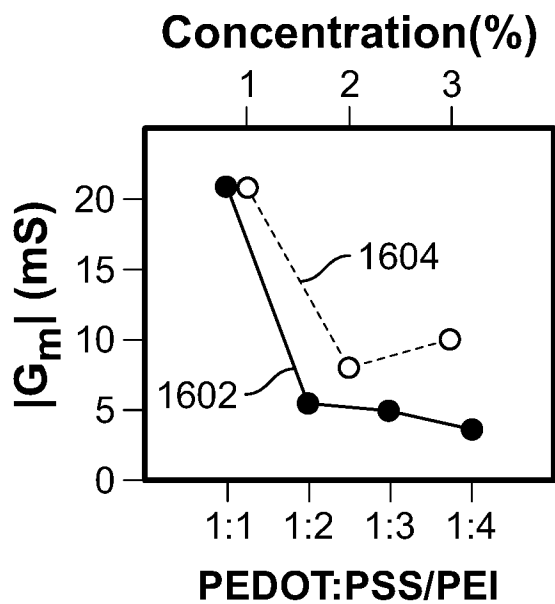


FIG. 16A

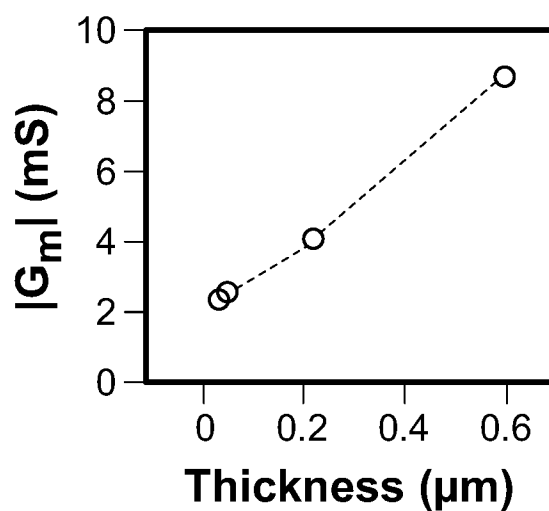


FIG. 16B

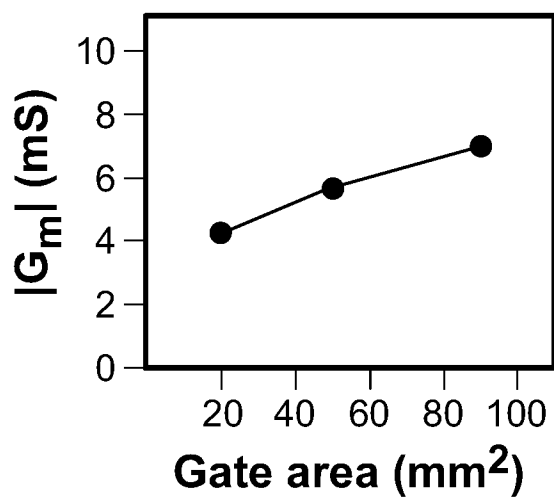


FIG. 16C

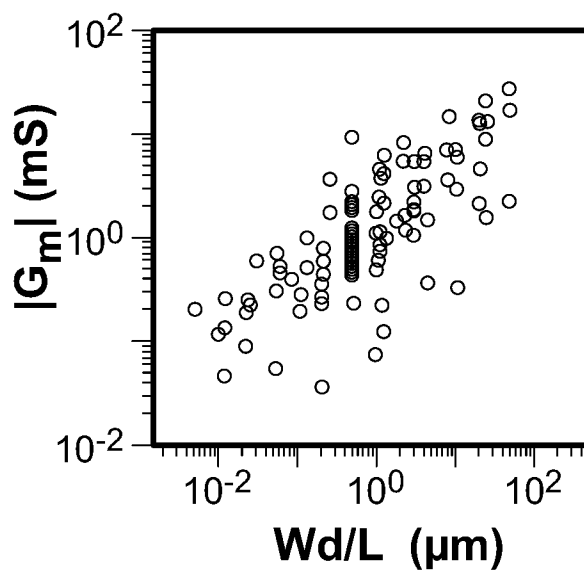


FIG. 16D

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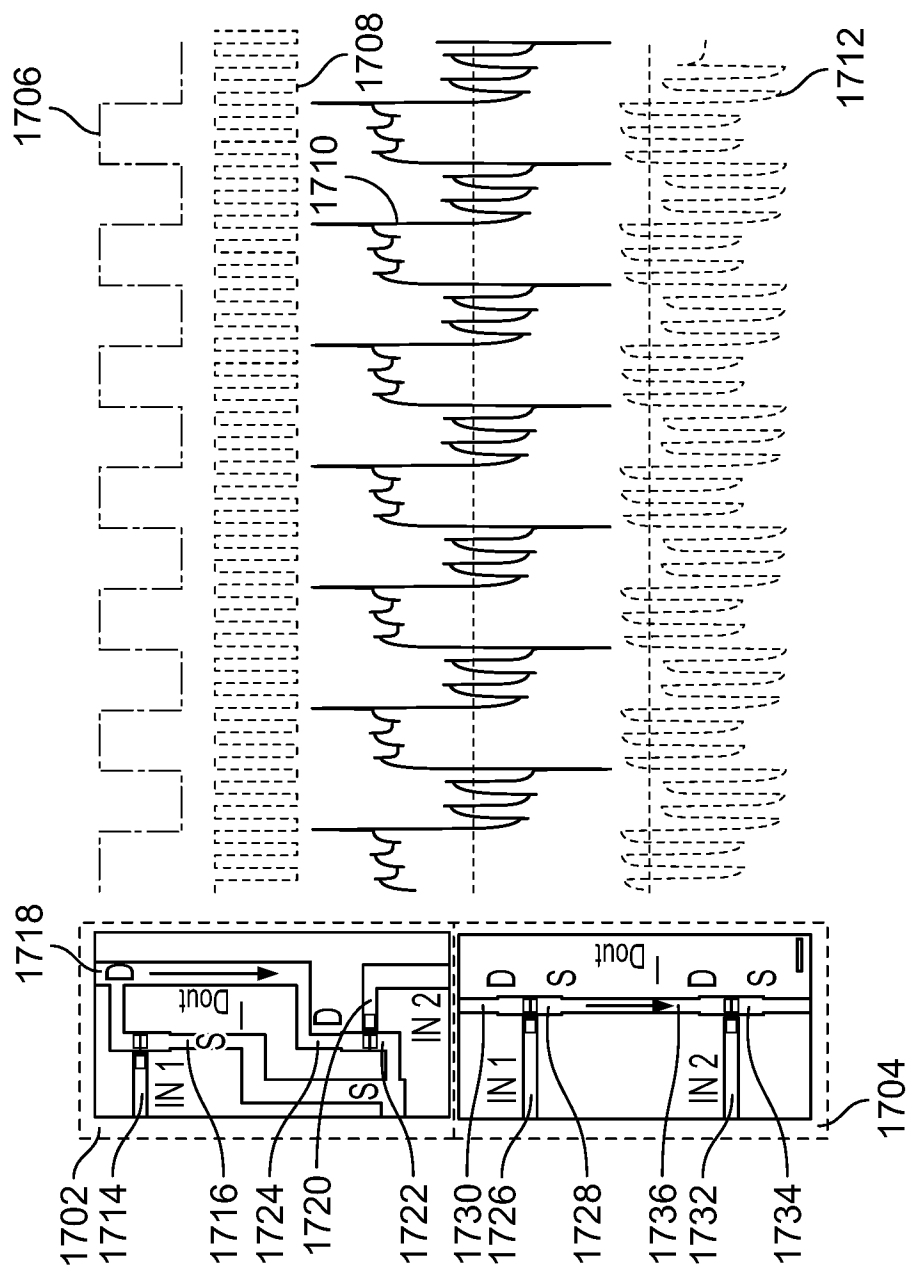


FIG. 17

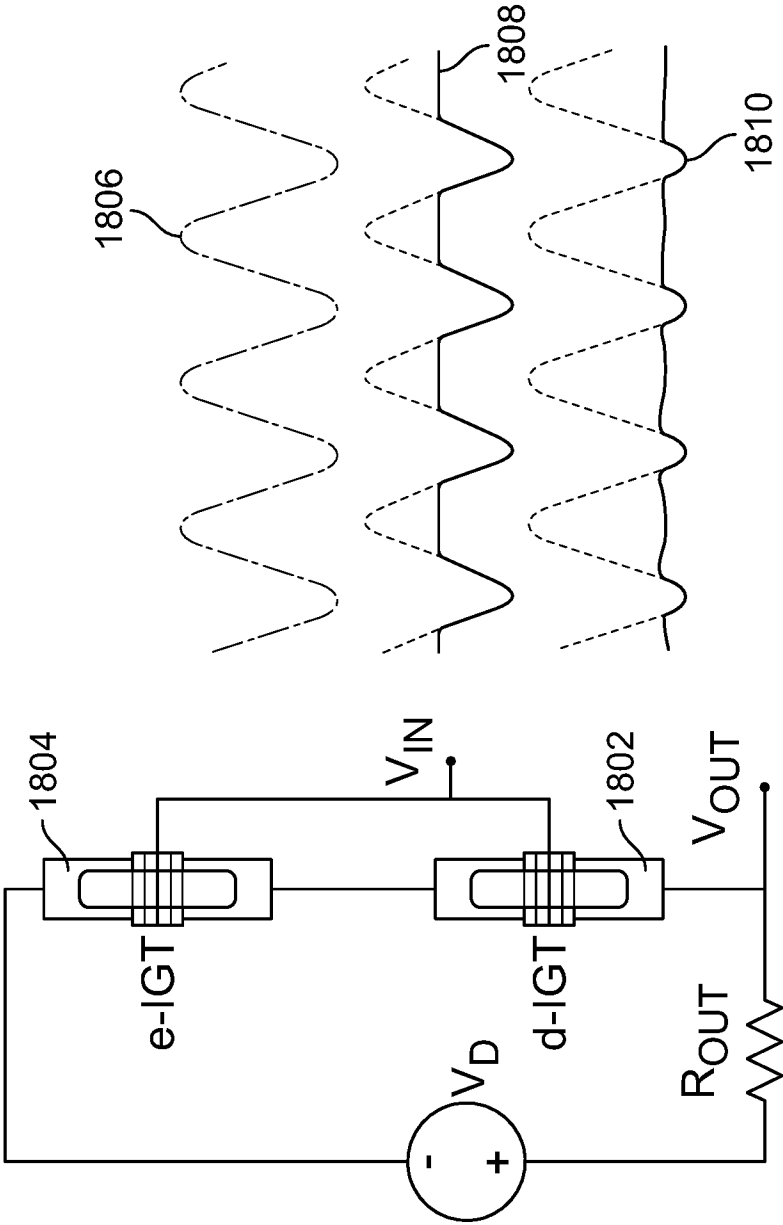


FIG. 18

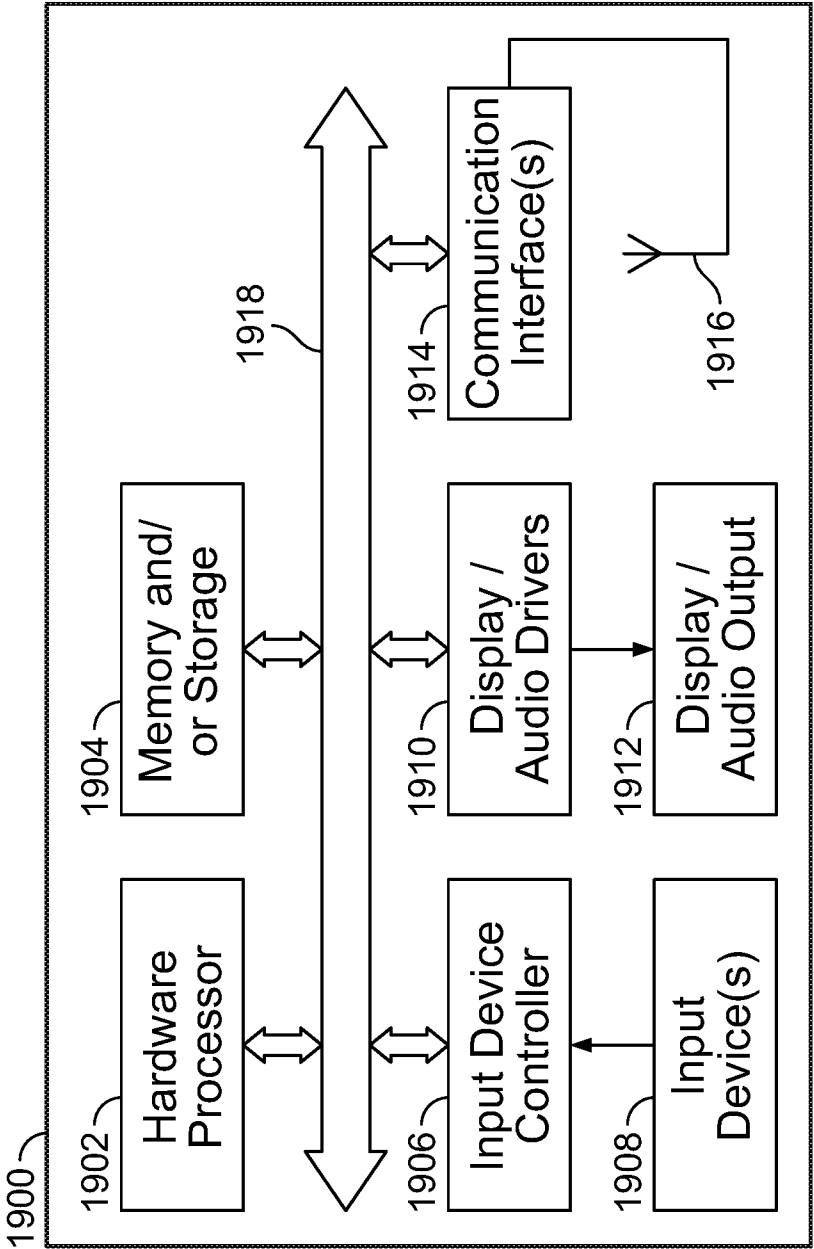


FIG. 19

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US2019/068363

## A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - H01L 51/05; G01N 27/00; H01L 21/00; H01L 51/00; H01L 51/10 (2020.01)

CPC - H01L 51/0037; G01N 27/00; H01L 27/28; H01L 51/00; H01L 51/05; H01L 51/102; H01L 51/105 (2020.02)

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

USPC - 257/40; 327/100; 327/405; 330/311 (keyword delimited)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Relevant to claim No. |
|-----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| Y         | — SHELIAKINA et al., An all-solid-state biocompatible ion-to-electron transducer for bioelectronics, Materials Horizons, Vol. 5, 17 January 2018 [retrieved on 11 February 2020]. Retrieved from the Internet: <URL: <a href="https://www.semanticscholar.org/paper/An-all-solid-state-biocompatible-ion-to-electron-Sheliakin-a-Moster/cde347ff4ab1ece2fa1fc8f7309ff7428558632d">https://www.semanticscholar.org/paper/An-all-solid-state-biocompatible-ion-to-electron-Sheliakin-a-Moster/cde347ff4ab1ece2fa1fc8f7309ff7428558632d</a> >. Pgs. 256-263                                                                              | 1-10                  |
| Y         | — KR 10-1713240 B1 (SEOUL NATIONAL UNIVERSITY R&DB FOUNDATION (SNU)) 07 March 2017 (07.03.2017) see machine translation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1-10                  |
| Y         | — US 8,137,524 B2 (BERGGREN et al) 20 March 2012 (20.03.2012) entire document                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1-10                  |
| Y         | — VENKATRAMAN et al., Subthreshold operation of organic electrochemical transistors for biosignal amplification, Advanced Science, Vol. 5, 04 July 2018 [retrieved on 16 February 2020]. Retrieved from the Internet: <URL: <a href="https://www.ncbi.nlm.nih.gov/pmc/articles/PMC6097142/pdf/ADVS-5-1800453.pdf">https://www.ncbi.nlm.nih.gov/pmc/articles/PMC6097142/pdf/ADVS-5-1800453.pdf</a> >. Pgs. 1-7                                                                                                                                                                                                                         | 3                     |
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☒ Further documents are listed in the continuation of Box C.☐ See patent family annex.

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Date of the actual completion of the international search

17 February 2020

Date of mailing of the international search report

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## C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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