Sept. 29, 1959 M. A. WRIGHT 2,906,999

ELECTRICAL SIGNAL STORAGE SYSTEMS

Filed Feb. 7, 1955

2 Sheets-Sheet 1

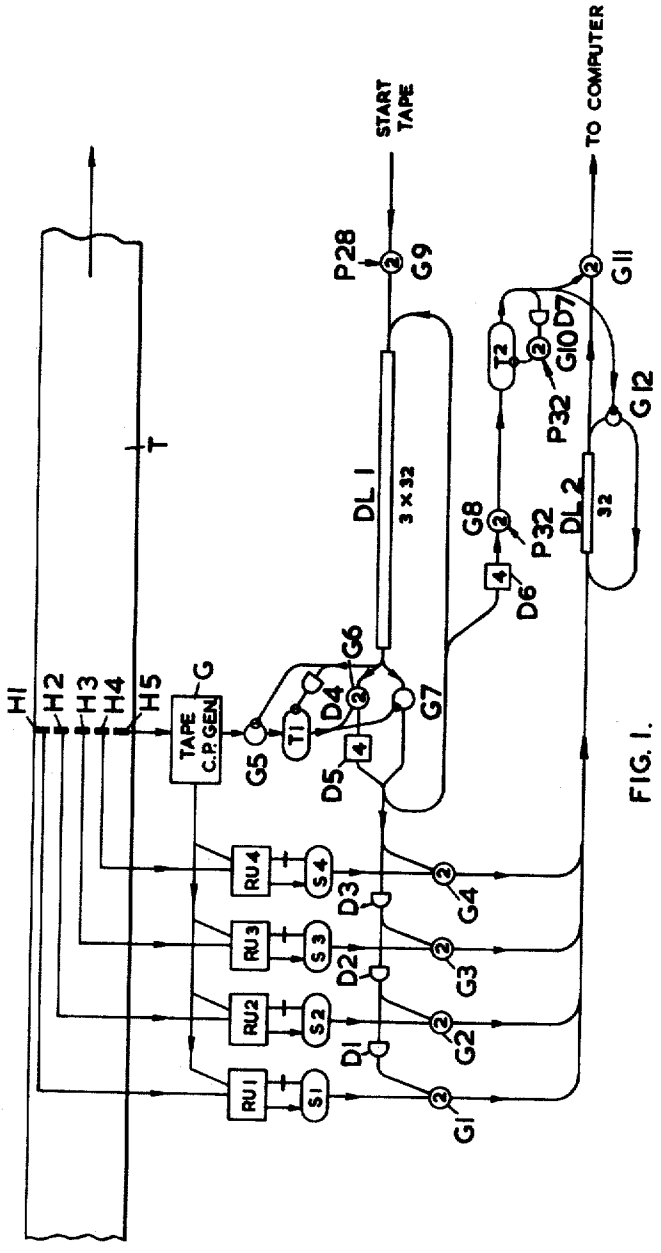


FIG. 1.

MICHAEL A. WRIGHT
Inventor

By
Stevens, Davis, Miller & Mosher
Attorneys

Sept. 29, 1959 M. A. WRIGHT 2,906,999

ELECTRICAL SIGNAL STORAGE SYSTEMS

Filed Feb. 7, 1955

2 Sheets-Sheet 2

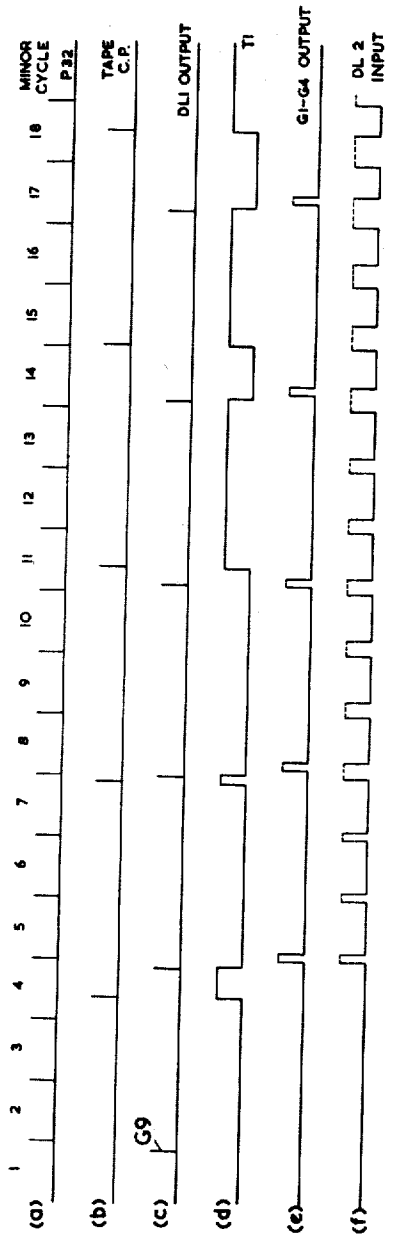


FIG. 2.

MICHAEL A. WRIGHT

Inventor

By

Stevens, Davis, Miller & Mosher

Attorneys

United States Patent Office 2,906,999
Patented Sept. 29, 1959

2,906,999

ELECTRICAL SIGNAL STORAGE SYSTEMS

Michael Arthur Wright, Hampton Hill, England, assignor to National Research Development Corporation, London, England, a corporation of Great Britain

Application February 7, 1955, Serial No. 486,617

Claims priority, application Great Britain February 12, 1954

5 Claims. (Cl. 340—173)

The present invention relates to electrical signal storage systems and is concerned with arrangements for transferring signals from a relatively low-speed store, from which signals are normally made available at a relatively low rate to a high-speed store, from and to which signals are normally fed at a high rate. Such arrangements are required to be provided in the input devices of high-speed digital computers in order to enable them to assimilate signals supplied at a lower speed.

The invention is concerned with arrangements for transferring signals between stores which do not accurately maintain their relative speeds of operation due to fluctuations in the speed of operation of one or both of the stores. These fluctuations will occur, for example, when a magnetic recording tape is one of the stores.

Signals may readily be transferred from a low-speed to a high-speed store if there is no limitation in the temporal positions that the signals are to occupy in the high-speed store, but difficulties arise when the low-speed signals must be absorbed into the high-speed store so that they follow each other in a desired order at the normal rate of the high-speed store.

Previous arrangements for transferring signals to a high-speed store in this manner have transferred the signals to the desired temporal positions in the high-speed train of signals only after each signal has temporarily occupied another position or other positions. As a result a delay is unavoidable before the transferred signals can be utilised in the high-speed store and it is an object of the present invention to provide a transfer arrangement by which slow-speed signals are accepted directly into desired positions in a high-speed signals train.

According to the present invention, an arrangement for transferring signals from a low-speed store to a high-speed store in which the high-speed store stores a serial train of signals in such a manner that each signal is made respectively available at times which are separated by a given repetition period and in which the slow-speed store produces signals at a maximum rate which is less than the repetition rate of the high-speed store comprises a signal transfer path from the low-speed store to the high-speed store, a timing device for controlling the transfer path and which when operating normally produces at basic time intervals timing pulses for opening the transfer path to permit the passage of signal units, said basic time intervals being a whole number including one times said given repetition period of the high-speed store, and means for modifying the normal operation of the timing device whereby the time interval preceding the timing pulse which permits the first passage of a signal unit through the transfer path is changed by the time period allocated in the high-speed store to a signal unit, the greater one of the modified and basic time intervals of the timing device being arranged to be less than the minimum time interval between successive signal units produced by the low-speed store.

As a result, if the basic time interval of the timing

device is increased by the time interval allocated in the high-speed store to a transferred signal unit, successive transferred signal units are stored in the same order in successive temporal positions in the high-speed store whereas if the basic time interval is decreased the transferred signal units are stored in reversed order in progressively earlier temporal positions. Usually the first arrangement is employed so that signals are assembled in the high-speed store in the order that they are delivered from the low-speed store.

An arrangement for transferring digit signals from a magnetic recording tape to a high-speed digital computer employing acoustic delay line stores will now be described by way of example with reference to the drawings filed with this specification in which:

Figure 1 is a diagram of the circuit arrangement; while Figure 2 shows the waveform of voltages occurring at various parts of the circuit shown in Figure 1.

The circuit arrangement shown in Figure 1 is an input device to a serial-mode binary digital computer in which binary digit signals each occupying digit periods of one microsecond are organised into trains of 32 digit signals forming numbers called words which occupy a time period of 32 microseconds called a minor cycle. Digit signals are numbered 1 to 32 in the order that they appear in a minor cycle. P pulses and various circuit elements shown in Figure 1 are in accordance with the Turing notation for electronic digital computers as described in U.S.A. Patent No. 2,686,632.

The low-speed store input is in the form of a magnetic recording tape T on which blocks of signal units in the form of four binary digit signals are recorded in lines of four signals running transversely across the tape. In addition to the four signal tracks there is a track of synchronising signals, each synchronising signal marking a line of signals. Five recording heads H1 to H5 are arranged in line across the path of the tape to read the signals stored on the five tracks. The heads H1 to H4 feed four reading units RU1 to RU4 which identify each signal as a 1 or 0 type binary digit signal and set up the staticisor triggers S1 to S4 in accordance with the nature of these digit signals. When the recording tape T has progressed far enough for the next line of signals to be read by the heads H1 to H4 and identified by the read units RU1 to RU4, the state of the staticisors S1 to S4 is modified so that they are set up in accordance with this line of signals.

The synchronising signals are read by the head H5 and are applied to a tape clock pulse generator G which produces a tape clock pulse when a line of digit signals is ready to be identified by the read units RU1 to RU4. The tape clock pulses are used to regulate the action of the read units RU1 to RU4 and to mark the moments when a new set of digit signals are staticised in the staticisors S1 to S4. The tape clock pulses are applied (through a gate G5 whose function will be described later but which is normally open) to a trigger T1 having two stable states and which is arranged to be set in one stable state by each tape clock pulse and remain so set until the corresponding signal unit of four digit signals staticised in staticisors S1 to S4 are accepted into a high-speed delay line store DL2 of the computer in a manner which will now be described.

The transfer path from the staticisors S1 to S4 to the store DL2 is through four gates G1 to G4 controlled by a timing device which consists of a delay line DL1 and its associated circuits. The timing device functions when, soon after the recording tape T is set in motion, an output derived from the tape driving motor permits a start pulse to pass through a gate G9 when the next P28 pulse occurs into the three minor cycle delay line DL1. It will be assumed that this start pulse which is labelled by G9 in Figure 2(c), occurs as shown just before the end of

minor cycle 1 as shown in Figure 2(*a*) with the result that the delay line DL1 produces the first of a series of output pulses as shown in Figure 2(*c*) just before the end of minor cycle 4.

The circuit arrangement shown in Figure 1 is arranged to deal with a recording tape T which is driven so that of the order of 10,000 lines of digit signals pass the recording heads each second. This is because the speed of the tape must be adjusted, so that when it has fluctuated to its maximum possible value, lines of digit signals pass the recording heads H1 to H5 at intervals which are greater by a reasonable tolerance than the maximum circulation time of a pulse through the delay line DL1 and its associated circuits which is three minor cycles plus four digit periods, that is 100 microseconds. The speed of the recording tape in the arrangement shown in Figure 1 is therefore set to about 9,000 lines per second, so that the time interval between lines is more than 100 microseconds.

As a result, a series of tape clock pulses are produced by the tape clock pulse generator G at intervals of about three-and-a-half minor cycles as shown in Figure 2(*b*), the trigger T1 being set by each tape clock pulse as shown in Figure 2(*d*) through an inhibiting gate G5, whose action will be fully described later, but which meanwhile will be assumed to be in its normal open condition. The trigger T1 is arranged to be reset through the short delay D4 immediately after the delay line DL1 next produces an output. Thus each time that a new signal unit of four digit signals is stored in the staticisors S1 to S4 (as indicated by tape clock pulses) the trigger T1 is set when the delay line DL1 next produces an output pulse, and a gate G6 controlled by the trigger T1 is opened and passes the output pulse, while an inhibiting gate G7 is closed. The output pulse from the delay line DL1 thus circulates back to the beginning of the line through a four digit period delay D5 so that each time a new set of digit signals is stored in the staticisors S1 to S4 the next output pulse from the delay line DL1 is delayed by four digit periods. At the same time the output pulse is delayed by four digit periods before it acts through the digit period delay units, D1, D2 and D3 to open in four successive digit periods the gates G4, G3, G2 and G1 in the transfer path from the recording tape T to the high-speed delay line store DL2. The combined output of the gates G1 to G4 is shown in Figure 2(*e*) and, due to the precessional movement of the output pulse from the delay line DL1, each time a new set of digit signals is ready to be transferred successive sets of digit signals are passed into the delay line DL2 to form a lengthening continuous train of signals. This action is shown in Figure 2(*f*) which shows the combined input to the delay line DL2. It will be seen that whereas the gates G1 to G4 are opened by each output pulse from the delay line DL1 the train of digit signals in the delay line DL2 is lengthened only when the digit signals passed by these gates are different from those passed on the previous occasion. The train is not lengthened on each occasion when there is neither a change in the staticisors S1 to S4 nor a tape clock pulse to set the trigger T1 to delay the timing pulse output from the delay line DL1 prior to its application to the gates G1 to G4. Thus whereas, as shown in Figures 2(*b*) and 2(*c*), in minor cycles 4 and 7 there is a change in the state of the staticisors S1 to S4 (simultaneous with the production of a tape clock pulse) immediately preceding a pulse from the delay line DL1, in minor cycle 11 the pulse from the delay line DL1 emerges before the tape clock pulse so that the output of the delay line passes through the gate G7 during minor cycle 11 with the result that the gates G1 to G4 are opened during the same digit periods in a minor cycle as they were during minor cycle 8. As a result the second set of four digit signals which are still stored in the staticisors S1 to S4 are merely written again into the delay line DL2 in the same digit periods of a minor cycle.

The transfer of sets of digit signals from the magnetic recording tape to the delay line store DL2 builds up the train of digits signals circulating through the store as shown in Figure 2(*f*), each digit signal being placed and retained in its pre-allocated temporal position in the signal train circulating through the delay line DL2 so that it is available for transfer to the computer immediately or at any required time before the delay line DL2 is filled with a train of 32 digit signals; as when this occurs the delay line must be cleared to enable a fresh train of digit signals to be built up. The store is full at the end of the minor cycle in which the output from the delay D5 to the gates G1 to G4 takes place at P28 time. The contents of the delay line DL2 is then transferred to the computer during the following minor cycle, there being three complete minor cycles during which this can take place before the new set of digit signals are fed in from the gates G1 to G4.

This minor cycle transfer to the computer is arranged to take place in the following manner. The output from the delay D5 is applied through a further delay D6 of four digit periods to a gate G8 controlled by P32 pulses. Thus a pulse is produced by the gate G8 at the end of the minor cycle in which the output from the delay D5 occurs at P28 time. The pulse from the gate G8 is used to set a trigger T2 which resets itself at the end of the minor cycle through a short delay D7 and a gate G10 controlled by P32 pulses. The trigger T2 opens a gate G11 and closes an inhibiting gate G12 for the duration of the minor cycle that it is set so that the contents of the delay line store DL2 is passed to the computer and prevented from circulating through the store again.

The action of the inhibiting gate G5 will now be described. The gate G5 is inserted in the path from the tape clock pulse generator G to the trigger T1 in order to prevent the trigger T1 being set by a tape clock pulse during the small but finite time that a pulse is emerging from the delay line DL1. The trigger T1 is arranged to be set either before or after the arrival of a pulse from the line DL1 by arranging for the tape clock pulses to be considerably broader than the output pulses from the delay line DL1 and applying these output pulses to control the inhibiting gate G5. This provision is made as otherwise it may be possible for the trigger T1 to be set by a tape clock pulse and then reset so quickly by the output pulse from the delay line DL1 that the gate G6 would not be opened or the gate G7 closed with the result that the signals stored in the staticisors S1 to S4 would be transferred to the delay line DL2 without being delayed and would be written over the previous set of transferred signals.

It is also necessary in the circuit arrangement shown in Figure 1 to arrange for the staticisors S1 to S4 to be not set up in accordance with the nature of a new set of digit signals read from the magnetic recording tape T until four digit periods or so after the production of the corresponding tape clock pulse and the consequent putting on of the trigger T1. This is to ensure that the staticisors S1 to S4 cannot change during the four digit periods after a timing pulse from the delay line DL1 has been allowed to pass through the inhibiting gate G7 as any such change would cause some or all of the new digit signals to be written into the delay line store DL2 over the previously transferred signals which would then be lost.

The tape reading arrangement shown in Figure 1 employs a delay line DL1 which is three minor cycles long but this delay line may be made one minor cycle long without changing the mode of operation of the arrangement. An output pulse from the delay line DL1 would of course be produced every minor cycle so that each set of signals on the staticisors S1 to S4 would be written in the same position in the delay line DL2 at least three times instead of at least once.

Also the tape reading arrangement employs a delay line DL2 which is one minor cycle long and which transfers

to the computer complete words of 32 digit signals at intervals of about 30 minor cycles. Each word must be transferred as soon as it is assembled in the delay line DL2 as the assembling of the next words begins forthwith. In the arrangement shown in Figure 1 in which the delay line DL1 is three minor cycles long the delay line DL2 also may be made three minor cycles long. Then it is not necessary to tarnsfer any of the contents of the delay line DL2 until this store has been filled with three words. The first word and/or the second word to be assembled in the delay line or any portions thereof may however be transferred at any required time before the three words are assembled. As the interval between the assembling of successive words in the delay line DL2 is about 30 minor cycles a delay line DL2 which is three minor cycles long can act as a convenient buffer store between the magnetic recording tape and those parts of the computer which are required to receive the signals read from the recording tape.

In general the delay lines DL1 and DL2 may be made of any convenient lengths provided that the delay of the delay line DL1 is less than that of the interval between the reading of signals from the low-speed store and is equal to or an integral number of times longer than that of the delay line DL2. In place of the delay line DL1 any suitable pulse delaying or timing circuit may be employed which can produce an output pulse a predetermined time after it is supplied with an input pulse.

The signal transfer arrangement described may be readily adapted to transfer signal units of any type from a magnetic recording tape or other type of slow-speed store.

I claim:

1. An arrangement for transferring signals from a low-speed store to a high-speed store which stores a serial train of signals in such a manner that each signal is made repetitively available at times which are separated by a given repetition period and in which the low-speed store produces signal units at a maximum rate which is less than the repetition rate of the high-speed store, and comprising a signal transfer path from the low-speed store to the high-speed store, a gate in the said transfer path, a timing device which produces timing pulses which open the gate to permit the passage of signal units, the timing device either being in a first condition when it produces timing pulses at basic time intervals which are a whole number including one times the said given repetition period of the high-speed store or being in a second condition when it produces timing pulses at time intervals which are different from the basic time interval by the time period allocated in the high-speed store to a signal unit, a trigger circuit for controlling the timing device and having two stable states, means for producing a clock signal from the low-speed store when a signal unit is available for transfer from the low-speed store, a trigger input circuit for applying the clock signals to the trigger circuit to put it in a second stable state, and means for applying the output from the timing device to restore the trigger circuit to its first stable state if it is not so already, the said trigger circuit controlling the timing device whereby when the trigger circuit is in its first stable state the timing device is put in the said first condition while when the trigger circuit is in its second stable state the timing device is put in the said second condition.

2. An arrangement for transferring signals from a low-speed store to a high-speed store which stores a serial train of signals in such a manner that each signal is made repetitively available at times which are separated by a given repetition period and in which the low-speed store produces signal units at a maximum rate which is less than the repetition rate of the high-speed store, and comprising a signal transfer path from the low-speed store to the high-speed store, a gate in the said transfer path, a timing device which produces timing pulses which open the gate to permit the pasage of signal units, the timing device either being in a first condition when it produces timing pulses at basic time intervals which are a whole number including one times the said given repetition period of the high-speed store or being in a second condition when it produces timing pulses at time intervals which are longer than the basic time interval by the time period allocated in the high-speed store to a signal unit, a trigger circuit for controlling the timing device and having two stable states, means for producing a clock signal from the low-speed store when a signal unit is available for transfer from the low-speed store, a trigger input circuit for applying the clock signals to the trigger circuit to put it in a second stable state, and means for applying the output from the timing device to restore the trigger circuit to its first stable state if it is not so already, the said trigger circuit controlling the timing device whereby when the trigger circuit is in its first stable state the timing device is put in the said first condition while when the trigger circuit is in its second stable state the timing device is put in the said second condition.

3. An arrangement according to claim 2 and in which the said timing device comprises a timing circuit which when supplied with an input pulse produces an output pulse after a delay of the said basic time interval, and means for applying the output from the timing circuit to its input direct when the said timing device is in its said first condition and through a delay circuit when it is in its said second condition, the delay circuit imposing a delay equal to the said time period allocated in the high-speed store to a signal unit.

4. An arrangement according to claim 3 and comprising means for supplying a short pulse to the timing circuit when the low-speed store commences to operate.

5. An arrangement according to claim 2 and comprising an inhibiting gate in the trigger input circuit and which when closed prevents the trigger circuit being put into the second state, and means for closing the inhibiting gate by an output pulse from the timing circuit, each clock signal being arranged to be substantially longer than the output pulse from the timing circuit.

References Cited in the file of this patent

Buffering Between Input-Output and the Computer, by A. L. Leinen in Joint AIEE-ARE-ACM Computer Conference, March 1953 (pages 22–31).