## (19) World Intellectual Property Organization

International Bureau





(43) International Publication Date 9 December 2004 (09.12,2004)

**PCT** 

# (10) International Publication Number $WO\ 2004/107352\ A3$

- (51) International Patent Classification<sup>7</sup>: **H01L 21/764**, 27/115, 21/8247
- (21) International Application Number:

PCT/US2004/013986

- (22) International Filing Date: 3 May 2004 (03.05.2004)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:

10/443,502

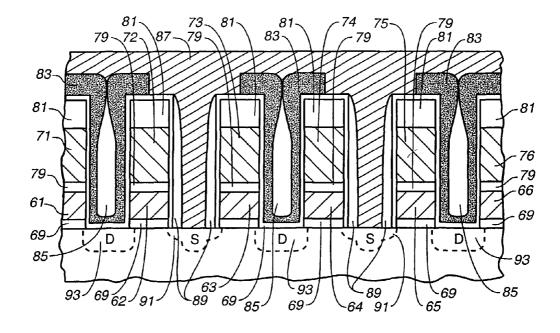
21 May 2003 (21.05.2003) U

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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: USE OF VOIDS BETWEEN ELEMENTS IN SEMICONDUCTOR STRUCTURES FOR ISOLATION



(57) Abstract: A flash EEPROM or other type of memory cell array having adjacent charge storage elements is formed with a gas filled void between them in order to reduce the level of capacitive coupling between storage elements, thus reducing cross-coupling between charge storage elements and resulting errors occurring in the data read from the array.

# WO 2004/107352 A3



#### **Published:**

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

 $\textbf{(88)} \ \ \textbf{Date of publication of the international search report:}$ 

3 February 2005

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

### INTERNATIONAL SEARCH REPORT

International Application No

CT/US2004/013986 A. CLASSIFICATION OF SUBJECT MATTER IPC 7 H01L21/764 H01L27/115 H01L21/8247 According to International Patent Classification (IPC) or to both national classification and IPC B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC 7 H01L Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data, PAJ C. DOCUMENTS CONSIDERED TO BE RELEVANT Category ° Citation of document, with indication, where appropriate, of the relevant passages Relevant to claim No.

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χ Further documents are listed in the continuation of box C.	χ Patent family members are listed in annex.
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Date of the actual completion of the international search  29 November 2004	Date of mailing of the international search report $10/12/2004$
Name and mailing address of the ISA  European Patent Office, P.B. 5818 Patentlaan 2  NL – 2280 HV Rijswijk  Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  Fax: (+31-70) 340-3016	Authorized officer  Albrecht, C

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International Application No

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