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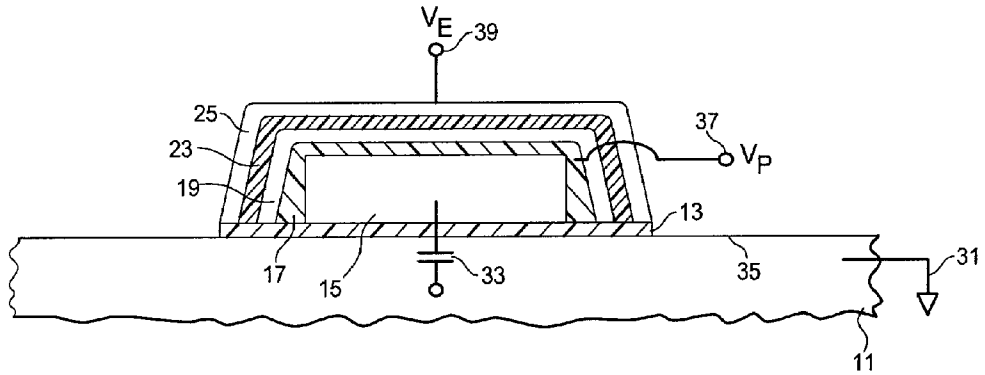
(54) Title: SOLID STATE FIELD EMISSION CHARGE STORAGE



(57) Abstract: Solid state field emission charge storage device is formed by a midgap metal plate (19) and another conductive plate (25) acting as capacitor plates in tunneling relation to a floating charge storage reservoir (15) on a substrate (11). The plates (19, 25) can be reversibly biased for tunneling of holes or electrons. The devices are tiny islands formed using semiconductor chip fabrication techniques. The islands can form a memory array just as similar islands form a field emitter array for a display screen.

WO 2008/051675 A1

Description

SOLID STATE FIELD EMISSION CHARGE STORAGE

TECHNICAL FIELD

The invention relates to solid state memories, and in particular, to field emission charge storage devices.

BACKGROUND ART

Solid state field emitters are used for stimulating phosphors for displays. For example, in U.S. Pat. No. 6,729,928 a polysilicon cone having a metal silicide coating serves as a cathode. An anode that is phosphoric is built opposite the cathode to draw electrons from the cathode with an intermediate gate therebetween. Multiple anodes include multiple phosphors. Individual cones are built in an array of rows and columns and are accessed by a microprocessor addressing row and column decoders.

Field emitters work well for displays because they are fast, responding immediately to changes in electric fields. The switching speed of field emitters is faster than the program or erase speed of most semiconductor non-volatile memory transistors which are more complex structures having greater RC delay. Yet field emitters are not used as solid state charge storage in nonvolatile devices because field emission works well in only a single direction, allowing charge transfer, possibly for storage, but not charge removal, i.e. writing but not erasing, due to an asymmetry in barrier voltages.

An object of the invention was to devise a fast charge storage device, similar to a semiconductor non-volatile memory transistor but with faster program and erase capability.

SUMMARY OF INVENTION

The above object has been achieved with a new solid state field emission charge storage device having bidirectional program and erase capability achieved with a capacitive structure having thin midgap metal films called Aelectrodes@, in tunneling relation to an insulated floating conductive charge storage reservoir. Thus, the device has characteristics of both a capacitor and a floating gate transistor, except without source and drain electrodes and without a channel. One of the electrodes, called an Aemitter@, is connected to an emitter supply, while the other electrode, called a Acollector@, is connected to a plate supply. The words Aemitter@ and Acollector@ are words specifically defining electrodes of the solid state device herein and not the electrodes of a BJT device. The electrodes are spaced closely enough for electron tunneling to occur between electrodes when the emitter supply is negative relative to the plate supply.

Some of the electrons emitted from the emitter will overcome the oxide barrier beyond the collector plate and be trapped on the storage reservoir. When polarities on the supplies are reversed, holes migrate from emitter to collector and some are injected into the reservoir where they neutralize electrons.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-4 are side sectional views of manufacturing steps for making a device of the present invention.

Fig. 5 is an alternate embodiment of the device shown in Fig. 4.

DESCRIPTION OF PREFERRED EMBODIMENT

The basic principle employed herein is that the electric field between emitter and collector electrodes of a capacitor-like thin film structure is made sufficiently high that carriers are drawn from the emitter and gain enough energy from the electric field to tunnel through the collector and into an electrically insulated charge storage reservoir below the collector. With reference to Fig. 1, a flat substrate 11 is shown for use as a base to support field emitter charge storage devices of the present invention. Substrate 11 may be a silicon wafer or a glass disk. Silicon is an exemplary material because of its well-known chemical mechanical and electrical properties, its flatness, its availability and because mass production handling tools and facilities presently exist. Although the present invention is illustrated as a single charge storage unit, it is contemplated that arrays of similar devices would be built, similar to memory arrays.

An insulative oxide layer 13 is deposited over substrate 11. The oxide layer would typically have a thickness of approximately 100 Angstroms or less. Some silicon wafers can be obtained commercially with an insulative oxide layer prefabricated. Over the oxide layer 13 a polysilicon layer 15 is deposited by chemical vapor deposition. This layer would have a thickness in the range of 500-1000 Angstroms.

With reference to Fig. 2, the polysilicon layer 15 is patterned to form an island which will ultimately become a charge storage reservoir, similar to a polysilicon floating gate in an EEPROM transistor. An oxide or nitride layer 17 is deposited over the patterned polysilicon charge storage reservoir 15. Whether oxide or nitride is selected depends on subsequent processing to form a thin midgap metal film over layer 17. An oxide

layer would have a preferred thickness in the range of 10-50 Angstroms, an electron or hole tunnel distance.

With reference to Fig. 3, other layers are subsequently deposited over the insulative oxide or nitride layer 17. A midgap metal layer 19 is vapor deposited over oxide or nitride layer 17 to a thickness of several nanometers. This metal layer has the thickness and consistency of metal layers that can be made in semiconductor chip manufacturing. Deposition of midgap films is described, for example, in the article AFabrication of Midgap Metal Gates Compatible with Ultrathin Dielectrics@ in Applied Physics Letters, Vol. 73, No. 12, p. 1676-1678 (21 Sept. 1998), by D.A. Buchanan et al. The article describes formation of tungsten film capacitors. Similar film plates are used in the present invention. The term Amidgap@ as used in this application has the same meaning as used in this article, namely that the Fermi level of the collector material lies in the midband between the valence and conduction band edges of the charge storage material, i.e. silicon n the preferred embodiment. A second oxide or nitride layer 23 similar to the insulative layer 17 is deposited over the metal layer. A conductive layer 25, metal or polysilicon, is deposited over the second oxide or nitride layer 23. The thickness and consistency of the conductive layer 25 is the same as the metal layer 19. The entire structure is then covered with a suitable mask layer and etched to form the field emitter island structure illustrated in Fig. 4.

With reference to Fig. 4, the insulative oxide layer 13, as well as the first oxide or nitride layer 17, the midgap metal layer 19, the second oxide or nitride layer 23, and the conductive layer 25 are all trimmed down to the surface 35 of substrate 11, leaving a mesa or island structure. A first electrical connection 37, a plate voltage, V_p, is associated with the midgap metal layer 19. A second emitter voltage on terminal 39 is

associated with the conductive layer 25. The two voltages on the two metal layers resemble a capacitor with insulative material in layer 23 between the two metal plates.

When the emitter voltage V_e is negative with respect to the collector voltage V_p, electrons tunnel from the emitter plate of the conductive layer 25 to the midgap metal layer 19. When the emitter voltage is approximately -4 volts, electrons will reach the first insulative oxide or nitride layer 17 and some of them will overcome the insulative barrier and move to charge storage reservoir 15 where they are trapped.

The charge storage reservoir 15 is seen to have a capacitive relationship with substrate 11, indicated by the virtual capacitor 33. The substrate 11 is grounded, as indicated by grounding connection 31. When the terminal 39 applying emitter voltage is positive with respect to terminal 37 having collector voltage, emitted holes overcome the second oxide or nitride insulative layer 23 as well as the first oxide or nitride layer 17 and are injected into the charge storage reservoir 15. With a collector voltage of approximately 5 volts, the magnitude between the charge storage reservoir 15 and the midgap metal layer 19 required to collect holes injected over the potential barrier is approximately 0.6 volts. The tunneling of electrons and holes may be referred to as Abidirectional@. Therefore the total voltage is approximately 5.6 volts, or roughly 6 volts to inject holes into the reservoir, i.e. removing electrons.

In EEPROMs, injection is usually from the substrate, rather than from above as in the present charge storage device. When injecting from the substrate, there is greater inter-electrode capacitance that slows the device in comparison to a field emitter structure of the type described herein. Greater field emission and charge storage efficiency can be achieved by shaping the charge storage reservoir in a manner that

increases electric field strength between the charge storage reservoir and overlying electrodes.

With reference to Fig. 5, charge storage reservoir 115 is seen to be in insulative relationship to substrate 111 by means of the insulative oxide layer 113 and the surrounding insulative layer 117. The polysilicon charge storage reservoir 115 is shaped to have a frustro-conical shape. Such shapes have been built for optical devices, as described in U.S. Pat. No. 6,729,928 mentioned above. Over the first insulative layer 117 is a midgap metal film layer 119 and a second conductive layer 125 separated by the insulative layer 123. Electrical connections are the same as previously described, with the upper or conductive layer 125 connected to terminal 139 and the midgap metal plate connected to terminal 137. Connection to the midgap metal plate 119 may be by means of a via extending through the layers, but not shorting them together. Reversible bias leads to bidirectional tunneling for charge storage and erasing.

The deposition of midgap tungsten films as described by Buchanan et al., supra, involves cold wall reactor cracking of $W(CO)_6$ onto a substrate held in a heated graphite pedestal with a chamber pressure of 5×10^{-4} Torr flow conditions and 10^{-9} Torr base conditions. The films had a thickness of 2.8 to 7.5 nm, about 20-80 D, and areas in the range of 1.3×10^{-3} to 5.2×10^{-3} cm^2. A reactor internal temperature of 450-600 EC was found to be effective. Addressing and final metallization is the same as field emitters for video displays. Spacing of field emitters is at least the same as for video displays but closer spacing is desired as limited by metal wiring.

Claims

1. A solid state field emission charge storage device comprising:

a substrate,

an electrically floating, conductive charge storage reservoir on the substrate,

a first insulative layer over the storage reservoir that is sufficiently thin as to permit electron and hole tunneling,

a midgap metal collector electrode over the first insulative layer,

a second insulative layer over the collector plate that is sufficiently thin as to permit electron and hole tunneling, and

a conductive emitter electrode over the second insulative layer.

2. The device of claim 1 wherein the charge storage reservoir is silicon.

3. The device of claim 1 wherein the midgap collector electrode is tungsten.

4. The device of claim 1 wherein the emitter electrode is metal.

5. The device of claim 1 wherein the emitter electrode is polysilicon.

6. The device of claim 1 wherein the substrate is a semiconductor wafer.

7. The device of claim 1 wherein the substrate is glass.

8. A solid state field emission charge storage device comprising:

a midgap metal collector electrode separated by an insulative material from a conductive emitter electrode and in field emission relation therewith,

a conductive, floating, charge storage reservoir separated from the midgap metal collector electrode by an insulative material by a charged particle tunnel distance,

reversible bias means connected to the electrodes for stimulating field emission from the emitter electrode with charged particle tunneling from the collector electrode and into the charge storage reservoir in a bidirectional manner when bias is reversed.

9. The device of claim 8 wherein the emitter plate is polysilicon.

10. The device of claim 8 wherein the midgap collector electrode is tungsten.

11. The device of claim 8 wherein the collector electrode is a midgap metal film.

12. A method of making a field emission charge storage device comprising:

depositing a polysilicon layer on a substrate,

etching the polysilicon layer to form at least one charge storage region,

depositing a first insulative layer over the field emitter region,

depositing a midgap metal layer over the first insulative layer, thereby forming a collector electrode,

depositing a second insulative layer over the first midgap metal layer,

depositing a conductive layer over the second insulative layer as an emitter electrode, the collector electrode in field emission relation to the emitter electrode and the collector electrode in tunnelling relation to the charge storage region.

13. The method of claim 12 wherein the first and second insulative layers are deposited to a thickness in the range of 10-50 Angstroms.

14. The method of claim 12 wherein the midgap metal layer has a thickness in the range of 20-80 Angstroms.

15. The method of claim 12 further defined by shaped etching of the polysilicon layer in a truncated conical shape.

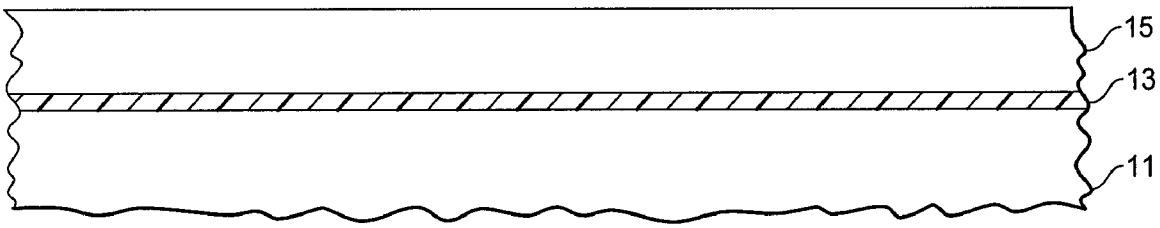


Fig._ 1

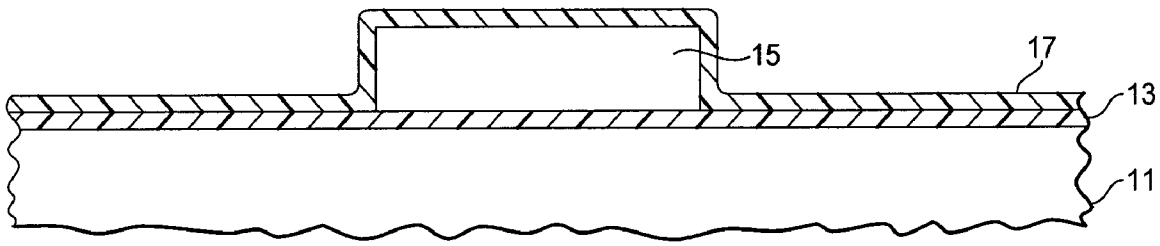


Fig._ 2

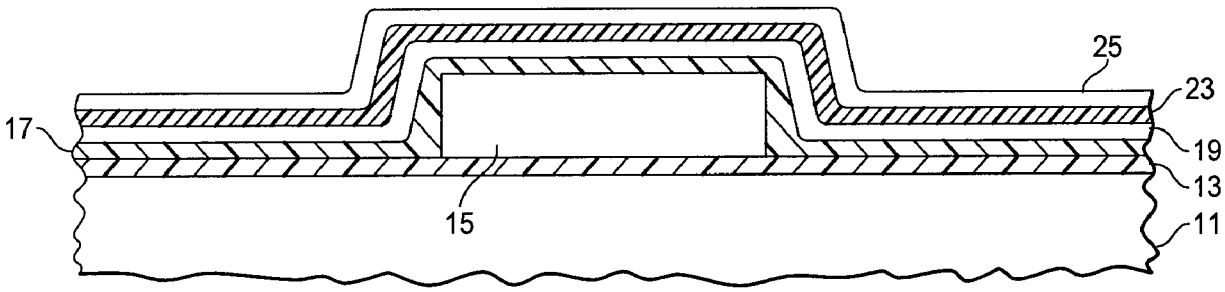


Fig._ 3

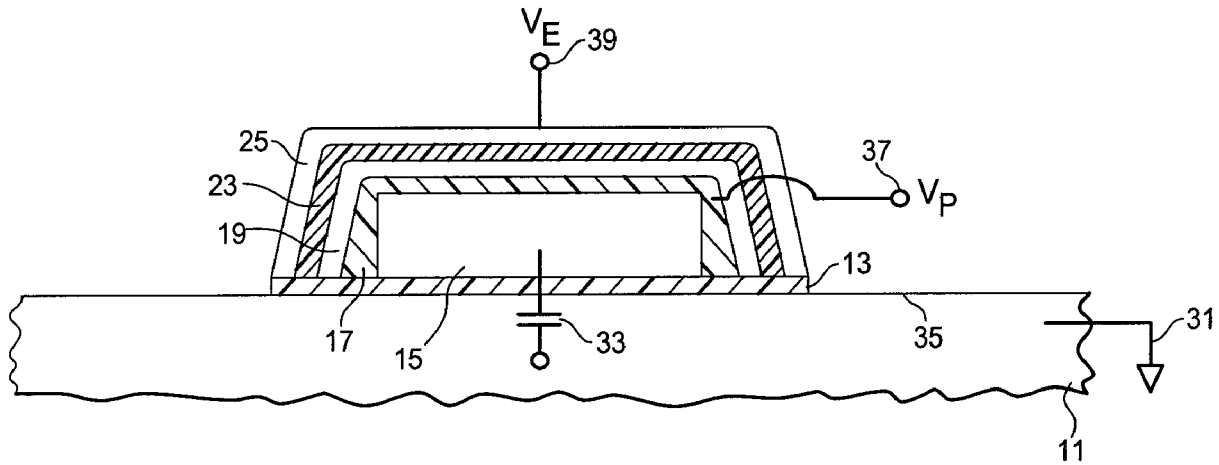

V_E
39
25
23
19
37
V_P
13
17
15
33
35
31
11

Fig._ 4

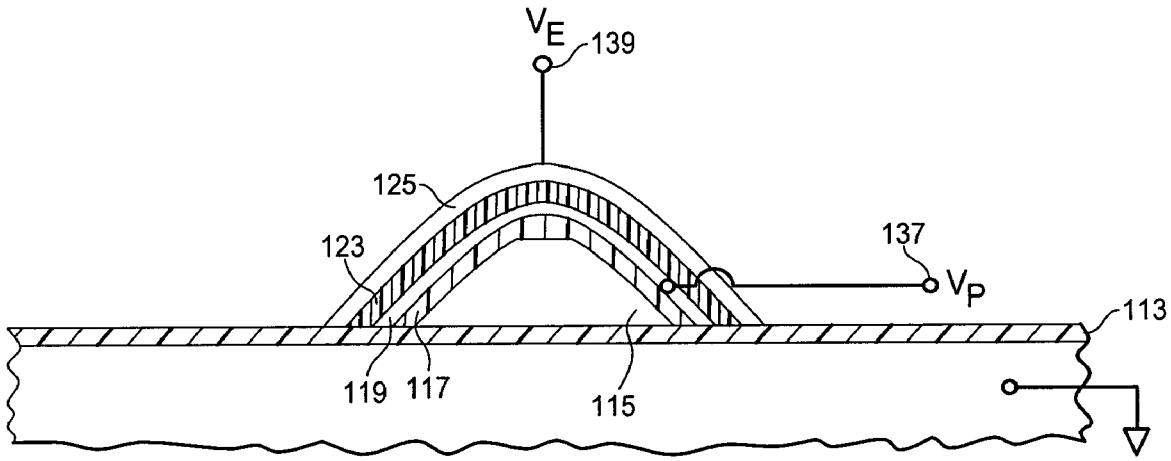

V_E
139
125
123
137
V_P
113
119
117
115

Fig._ 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/79418

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 21/336 (2008.01)
USPC - 438/257
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
ICP(8): H01L 21/336 (2008.01)
USPC: 438/257

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
IPC(8): H01L 21/336 (2008.01) (text search)
USPC: 438/257, 261, 263, 264 (text search)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST(USPT,PGPB,EPAB,JPAB); Internet search via Google Web and Google Scholar search engines. Search Terms Used: bidirectional electrode memory refractory tungsten wolfram charge biased chemical vapor CVD LCVD etching metal tunnel tunneling collect collector emitter floating gate thickness angstrom nanometer silicon

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 6,348,380 B1 (WEIMER et al.) 19 February 2002 (19.02.2002) col. 1 ln. 5 to col. 16 ln. 9, Fig. 1-12	1-4, 6-8 and 10-13 --- 5, 9, 14 and 15
Y	US 6,069,380 A (CHOU et al.) 30 May 2000 (20.05.2000) col. 1 ln. 5 to col. 14 ln. 9, Fig. 1-15	5, 9 and 14
Y	US 6,465,837 B1 (WU) 15 October 2002 (15.10.2002) col. 1 ln. 5 to col. 10 ln. 8, Fig. 1-6E(c)	15
A	US 2006/0199395 A1 (POWELL) 07 September 2006 (07.09.2006) para. [0006] through [0030], Fig. 1-2	1-15
A	US 5,619,051 A (ENDO) 08 April 1997 (08.04.1997) col. 1 ln. 7 to col. 10 ln. 54, Fig. 1-8(c)	1-15
A	US 6,380,029 B1 (CHANG et al.) 30 April 2002 (30.04.2002) col. 1 ln. 6 to col. 12 ln. 21, Fig. 1-2H	1-15
A	US 6,867,097 B1 (RAMSBEY et al.) 15 March 2005 (15.03.2005) col. 1 ln. 6 to col. 6 ln. 11, Fig. 1-7	1-15
A	US 7,115,469 B1 (HALLIYAL et al.) 03 October 2006 (03.10.2006) col. 1 ln. 15 to col. 14 ln. 16, Fig. 1-7	1-15

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 January 2008 (15.01.2008)	26 MAR 2008
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

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