March 12, 1974 V. R. PORTER ET AL 3,796,597

METHOD OF PRODUCING SEMICONDUCTING MONOCRYSTALLINE SILICON ON SPINEL SUBSTRATES

Filed Nov. 2, 1970 2 Sheets-Sheet 1

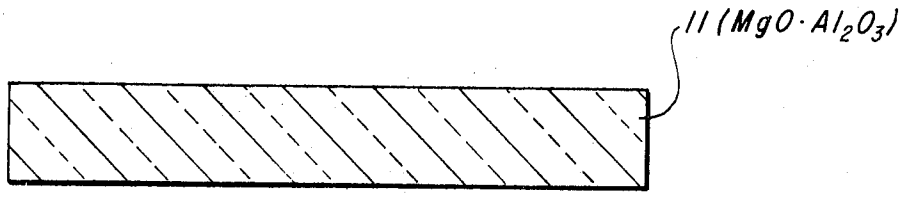

Fig. 1

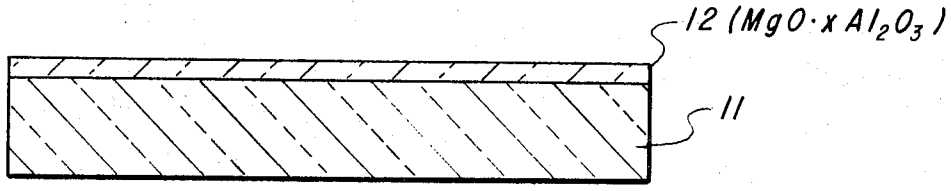

Fig. 2

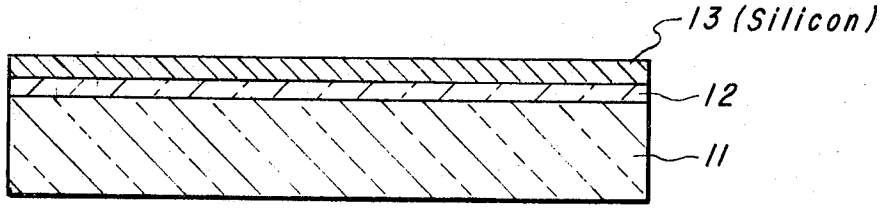

Fig. 3

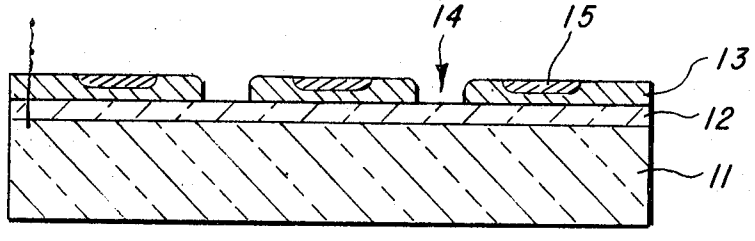

Fig. 4

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Fig. 5

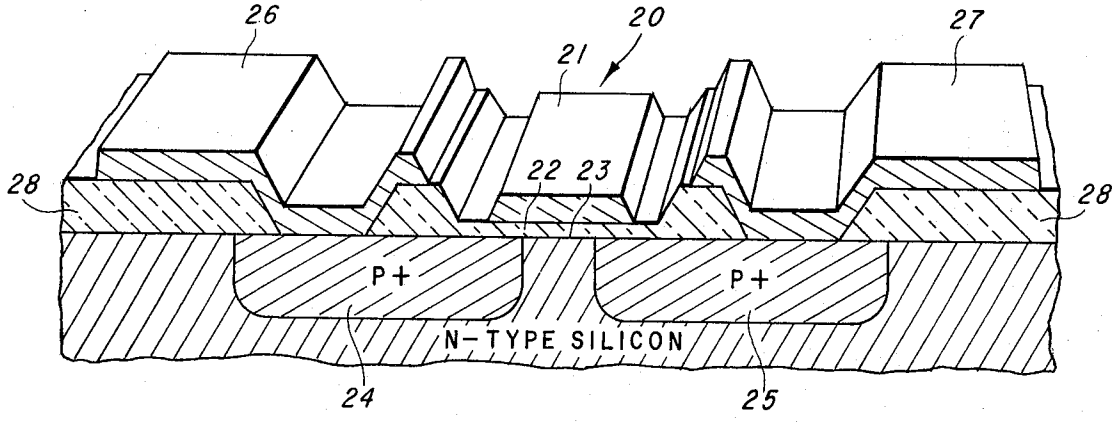
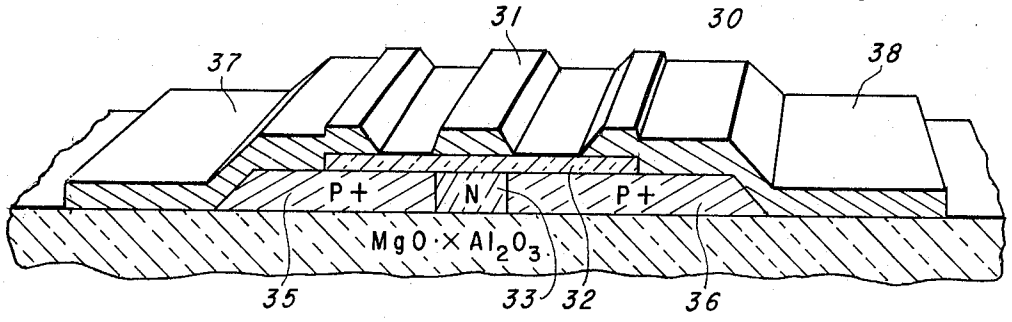


Fig. 6



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3,796,597

METHOD OF PRODUCING SEMICONDUCTING MONOCRYSTALLINE SILICON ON SPINEL SUBSTRATES

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Int. Cl. B44d 1/18
U.S. Cl. 117—213 3 Claims

ABSTRACT OF THE DISCLOSURE

There is disclosed an improved method of producing monocrystalline semiconductor material on a substrate of dielectric material. The method comprises heat treating of the substrate, specifically $MgO \cdot Al_2O_3$ spinel to modify the composition of its surface and then growing a monocrystalline semiconductor material, silicon, thereon. Resultant semiconductor devices have demonstrated improved switching speed.

This invention relates to semiconductor-on-insulator (SOI) electronic device manufacture and, more specifically, to an improved method of producing monocrystalline silicon on spinel.

The invention is directed to a method of producing single crystal semiconducting layers epitaxially on insulating substrate crystals and particularly to improvement in the art as taught in U.S. Pats. 3,414,434, H. M. Manasevit and 3,424,955, H. Seiter and C. Zaminer.

One of the problems that arises with the growth of monocrystalline semiconductor layers on variable composition insulating spinel crystals such as $MgO \cdot xAl_2O_3$ is that the chemical composition for optimum growth of the spinel is very closely $MgO \cdot 1Al_2O_3$, whereas the optimum chemical composition for growth of monocrystalline silicon thereon is $MgO \cdot xAl_2O_3$ where x is between 1.05 and 1.1. $MgO \cdot Al_2O_3$ spinel is readily grown by the Czochralski technique, is crystallographically quite perfect, and has no inherent limitations upon diameter. $MgO \cdot xAl_2O_3$ spinel, wherein x is greater than 1, may be grown by the Verneuil or flame fusion technique, but the diameter is essentially limited to less than 1 inch by problems with cracking of the boule, and the crystalline quality is low because of grain boundaries. It is an object of this invention to provide a method utilizing the Czochralski-grown material of composition very nearly $MgO \cdot Al_2O_3$ and of high perfection by shifting the composition of the surface layer toward a more desirable composition with regard to deposition of the semiconductor material. It is a further object of the invention to provide a method wherein a high degree of crystallographic perfection of the insulating surface is achieved while accomplishing the shift of composition. A further object of the invention is to provide a method achieving a greater degree of crystal quality than gained by flame fusion techniques.

The present invention may be generally described as a heat treatment of the insulating substrate in a stream of reducing gas such as hydrogen while maintaining the substrate within a relatively narrow temperature range so that MgO will be preferentially removed from the surface layer until the layer reduces an optimum composition with regard to deposition and, at the same time, any amorphous spinel material left from the polishing procedure is converted to well-oriented spinel of high perfection. The time and temperature are controlled so that deleterious defects such as grain boundaries, twins, and high concentrations of dislocations are not permitted to arise in the spinel. Thus, when the epitaxial layer of silicon is deposited thereon, said layer similarly exhibits a high degree of perfection.

Further objects and advantages of the invention will be apparent from the following complete specification and the drawings wherein:

FIG. 1 is a cross-section of a starting substrate in accordance with the invention;

FIG. 2 is a cross-section of the substrate after heat treating;

FIG. 3 is a cross-section of the substrate with the semiconductor layer thereon;

FIG. 4 is a cross-section of the substrate with semiconductor devices diffused and isolated in the semiconductor layer;

FIG. 5 is a standard insulated gate field effect transistor; and

FIG. 6 is an insulated gate field effect transistor from a silicon-on-insulator substrate.

Referring now to FIG. 1, there is depicted generally schematically a spinel substrate **10**. This substrate **10** is a (111) slice from a boule of monocrystalline $MgO \cdot Al_2O_3$ grown by the Czochralski technique. This technique has been found to produce crystals which are essentially perfect. The substrate **10** may be obtained from the boule by any appropriate technique as, for example, sawing. The slice is then polished to remove any marks resulting from the slicing operation. The substrate **10** therefore has surfaces which, when tested by electron diffraction techniques, are found to be essentially amorphous. The surface upon which the monocrystalline semiconductor is to be deposited must be converted to a proper crystal structure before such deposition and surface annealing or chemical etch have been previously suggested as suitable for this purpose.

However, in accordance with the invention, the substrate **10** may be placed in a suitable reactor, heat treated at a temperature between 1040° C. and 1145° C. and in a reducing hydrogen atmosphere to recrystallize the amorphous surface region and preferentially remove MgO in the surface layer **12** (FIG. 2) to produce monocrystalline $MgO \cdot xAl_2O_3$ wherein x is between 1.05 and 1.1. The temperature of the heat treatment must be controlled to assure conversion of the entire surface of the substrate **10** to the desired composition without producing deleterious defects such as cracks, twins and dislocations. These defects are found to be created to an unacceptable level when the substrate is heated over 1145° C. At a preferred temperature of approximately 1116° C., total conversion of the surface has been found to take place when the substrate has been heated for a period of two hours. The heat treatment has been found to yield good results at even lower temperatures, but at approximately 1040° C., the time of treatment exceeds four hours and at 900° C., the time of treatment becomes impractical.

The substrate **10** with layer **11** thereon is a monocrystalline semiconductor layer **13** preferably of silicon (FIG. 3). The layer **13** can be conveniently epitaxially produced as a further step in the same reactor as the heat treatment by changing the hydrogen atmosphere to a mixture of 0.3% silane in hydrogen with a phosphine dopant. The layer **13** could be produced by any appropriate epitaxial technique with or without dopant material added. From the foregoing, there is thus provided a semiconductor-on-insulator structure suitable for the manufacture of semiconductor devices and integrated circuits.

As depicted in FIG. 4, an array of semiconductor dioxides **15** may be produced in the epitaxial layer **13** by suitable masking and diffusion techniques as are well-known. Etching of openings **14** through the epitaxial layer provides electric isolation between diodes.

Results of the process in accordance with the invention are given in the following examples:

Example I—A slice .020 inch thick was cut from a 1⅜ inch diameter boule of Czochralski-grown spinel crystal

and polished. The crystal orientation of the slice was approximately (111) and its composition very nearly

$$MgO \cdot Al_2O_3$$

Electron diffraction by reflected high energy electrons revealed that the surface layers were essentially amorphous, due to the slicing and polishing processes. The slice was heated in hydrogen gas along with a high resistivity bulk silicon control slice on a silicon carbide coated susceptor for two hours at a temperature of 1116° C., after which a two micron silicon layer was epitaxially deposited on both samples from a .3% silane-in-hydrogen mixture at a deposition temperature of approximately 1080° C. A phosphine dopant was added to the deposition gas stream so that the silicon layer on silicon was n-doped to .15 ohm-cm. After deposition, the silicon-on-spinel was again subjected to reflected high energy electron diffraction and to X-ray measurements. The results of electron diffraction showed excellent single crystal silicon films, with no twins and a good Kikuchi diagram pattern. The resistivity across the slice was .40±.05 ohm-cm. The silicon on spinel can be said to have a merit factor of

$$100 \times \frac{.15}{.40} = 37.5\%$$

as defined by Mercier in the Journal of the Electrochemical Society 117, No. 5, p. 666 (1970). The surface composition lay in the range where x was between 1.05 and 1.1.

Example II—Another $MgO \cdot Al_2O_3$ spinel slice was treated as in Example I, except that the time of heat treatment was only ½ hour. The electron diffraction results were the same, i.e., high quality silicon. However, only the edges showed substantial MgO removal to produce x between 1.05 and 1.1. The average resistivity was now 1.30 ohm-cm., or a merit factor of 11.7%. Thus, although the crystalline quality was acceptable at ½ hour treatment, the composition was not.

Example III—Another slice was treated as in Example I, except that the time of treatment at 1116° C. was only 10 minutes. This time the resistivity was uniform within ±15% over the entire slice, but its magnitude was 1.03 ohm-cm., which corresponds to a 16% merit figure. Thus, 10 minutes is too short a time for the heat treatment to achieve the crystallographic perfection of the slice in Example I.

Example IV—Another slice was treated as in Example I, except that the temperature and time of heat treatment were 1200° C. and one hour respectively. The deposited silicon had a merit factor of 28% but now showed a series of steps that would make the slice unacceptable for defect content. The defect stemmed from cracks in the silicon. Thus, a temperature of heat treatment of 1200° C. is too hot for maintaining surface quality at an acceptable level.

Example V—Another slice was treated as in Example I, except that the temperature and time of heat treatment were 1145° C. and two hours, respectively. The deposited silicon had a merit factor of 37.6% but also showed a series of steps that would generally make the slice unacceptable for defect content. Thus, a temperature of 1145° C. is too high for maintaining surface quality with great consistency.

Example VI—Another slice was treated as in Example I, except that the temperature and time of heat treatment were 1100° C. and two hours, respectively. The deposited silicon had a merit factor of 38.1% and was free of the steps resulting in Examples IV and V. Thus, heat treatment at 1100° C. for two hours gives acceptable results.

FIGS. 5 and 6 illustrate insulated gate field effect transistors on a standard silicon substrate and on a spinel substrate made in accordance with the invention. The standard device **20** includes a gate electrode **21** on dielectric **22** overlying a channel **23** defined between source and drain diffusion **24**, **25**. Electrodes **26** and **27** make ohmic contact with the diffusions and overlie the insulating layer **28**. The inherent capacitances in the device of this type are the lead capacitance (C_l) between electrodes and substrate, junction capacitance (C_j) between diffusions and substrate, and the Miller capacitance (C_m) between gate electrode **21** and the channel **23**. The insulated gate field effect transistor **30** includes a gate electrode **31** on dielectric layer **32** overlying a channel **33** defined by a diffusion **34**. The source **35** and drain **36** are of the epitaxial silicon from the foregoing process. Electrodes **37** and **38** make electrical contact with regions **35** and **36** and lie directly on the spinel substrate. With the latter construction, the lead capacitance (C_l) becomes approximately 0 and the junction capacitance (C_j) and Miller capacitance (C_m) greatly reduced. A comparison of electrical characteristics is as follows:

Characteristics	Bulk silicon device	SOI device
Silicon type	N-type	N-type.
Resistivity	0.15 ohm-cm	0.5 to 5 ohm-cm.
Carrier concentration	5×10^{16} e.'s/cm.^{3}	5×10^{15}/cm.^{3}.
Mobility	280 cm.^{2}/v. sec	
Field effect mobility	140 cm.^{2}/v. sec	50–90 cm.^{2}/v. sec. (35–70% of bulk).
Threshold voltage	12–14 v	10–12 v.
Leakage	$<10^{-10}$ A. at 10 v.	$\approx 10^{-8}$ A. at 10 v.
Capacitance	5 pf	.3 pf.

Although the invention has been described and illustrated in accordance with the preferred embodiment thereof, it will be apparent to one skilled in the art that certain modifications can be made therein without departing from the spirit and scope of the invention.

What is claimed is new and desired to be secured by Letters Patent of the United States:

1. A method of producing monocrystalline semiconductor-on-insulator comprising:
   (a) heat treating a substrate of $MgO \cdot Al_2O_3$ at 1045–1145° C. for a time sufficient to modify the surface composition of the substrate to $MgO \cdot xAl_2O_3$ where x is between 1.05 and 1.1; and
   (b) epitaxially depositing a thin monocrystalline layer of silicon on the modified surface.
2. A method as recited in claim **1** wherein said heating is at a temperature of 1116° C. for approximately two hours.
3. A method as recited in claim **1** wherein said heating is in a hydrogen atmosphere.

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U.S. Cl. X.R.

117—201; 148—175; 317—234 R