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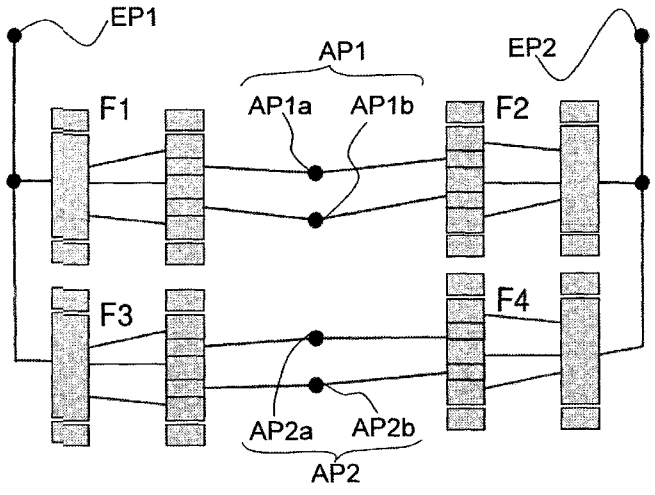
(54) **Title**: CHIP HAVING FOUR FILTERS OPERATING WITH SURFACE ACOUSTIC WAVES

Fig. 3



(57) **Abstract**: The invention relates to a chip (CH) which has four filters (Fl, F2, F3, F4) operating with surface acoustic waves, and input ports and output (EP1, EP2, API, AP2). Each filter (Fl, F2, F3, F4) covers a different frequency band. Each of the input and output ports (EP1, EP2, API, AP2) is connected to one or two filters (Fl, F2, F3, F4).

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Description

Chip having four filters operating with surface acoustic waves

The invention relates to a chip which has four filters operating with surface acoustic waves.

Modules are known which have four SAW (Surface Acoustic Wave) filters and also have diplexers at their input and output ports so that four filters can be driven via two input ports and two output ports in each case.

It is the object of the present invention to simplify the known modules and optimise them with regard to costs and space requirement.

The object is achieved by a chip according to the present Claim 1 and by a package according to the present Claim 21. Advantageous embodiments of the invention are found in further claims.

According to the invention, a chip is proposed which has four filters, operating with surface acoustic waves, and input and output ports. Each filter covers a different frequency band. Each of the input and output ports is connected to one or two filters each.

Furthermore, a particularly advantageous arrangement of the filters on the chip can be selected. For this purpose, the four filters are arranged on the chip in such a manner that two filters form a left-hand column and the remaining two

filters form a right-hand column and two filters each from different columns are arranged opposite one another.

An input and/or an output port can be connected to two filters. In this case, they form a diplexer.

If the chip has two input ports which are in each case connected to two filters which form one diplexer each, the two filters of the left-hand column can be connected to the first input port and the two filters of the right-hand column can be connected to the second input port.

If the chip has two output ports which are in each case connected to two filters which form one diplexer each, two oppositely located filters each can be connected to an output port arranged between the two mutually opposite filters.

If the diplex functionality for four filters operating with surface acoustic waves is integrated in one chip, it is possible to achieve distinct advantages with regard to the space requirement in this manner.

Such a chip can be used in a transmitting and receiving circuit of a mobile telephone. If the input and/or output ports of the chip are then arranged as a diplexer, the remaining components of the transmitting and receiving circuit can be simplified. If, for example, the input ports for the four filters are arranged as a diplexer, the component has only two input ports instead of four input ports. The input ports are usually optionally connected individually to an antenna via a switch. Arranging the chip with only two input ports makes it possible to use a less complex and correspondingly more advantageous switch for

distinguishing between the received frequency bands. On the output side, the number of signal lines between the chip and a receiving circuit can be reduced by a factor of two due to the diplex output ports.

Each of the two input ports is advantageously connected to a filter which is connected to the first output port and to a filter which is connected to the second output port.

In a first embodiment of the present invention, the four SAW filters are arranged in a row on a common chip substrate.

In a second embodiment, the four filters are arranged in the form of a 2 x 2 matrix on the chip. In this arrangement, two filters form a left-hand column and the remaining two filters form a right-hand column, the two filters of the left-hand column being connected to the first input port and the two filters of the right-hand column being connected to the second input port. Two filters each from different columns are arranged opposite one another in this case, the two mutually opposite filters each being connected to an output port arranged between the two mutually opposite filters.

Compared with the first embodiment, this second embodiment has some advantages. On the one hand, crossing-over of the signal lines on the chip can be avoided. Furthermore, an arrangement of the filters according to the second embodiment makes it possible to construct a chip, the ratio of length and width of which has more advantageous characteristics. A chip according to the first embodiment only has a very great length but on the other hand a small width. In the case of a chip according to the second embodiment, the ratio of length to width is closer to one.

The length-to-width ratio of the second embodiment corresponds to the standard forms which are used, for instance, in the case of 2 in 1 filter chips. On the market, numerous dual-band mobile telephones are known in which a 2 in 1 filter chip is used which has two SAW filters for two different frequency bands. The chip of the second embodiment according to the invention has the same dimensions and thus the same length-to-width ratio as the known 2 in 1 filter chips. It is therefore possible to replace a 2 in 1 filter chip by the 4 in 1 filter chip according to the invention, without much expenditure, and thus to upgrade the dual-band mobile telephone to form a quad-band mobile telephone. If, in contrast, a 4 in 1 filter chip according to the first illustrative embodiment, having a great length and small width is used, greater changes are required in the circuit board design.

Since the dimensions of the second illustrative embodiment correspond to the standard forms, existing tools can be used for the production and for testing the chip.

In addition, the second embodiment, due to the changed ratio of length to width, has a better mechanical stability. Since a chip according to the second embodiment has a ratio of length to width which is closer to one, it is, in particular, more insensitive to deformations due to temperature fluctuations. In a chip according to the first illustrative elastic embodiment, mechanical stresses can arise. Since in a chip according to the second embodiment, the absolute dimension has been reduced in length, the mechanical stresses which can arise due to thermal deformations are reduced. The improved mechanical stability results in better reliability and reduced probability of failure.

The advantages of a chip according to the second embodiment are thus a more compact layout, improved reliability and the possibility of using existing tools.

The frequency space can be divided into a high band and a low band. The definition of high and low band depends on the standard used in each case and is initially purely arbitrary. One possible definition allocates frequencies below 1 GHz to the low band and frequencies which are higher than 1 GHz are allocated to the high band. In the text which follows, this definition is used as a basis without the invention being restricted to this definition.

Two of the four SAW filters can each cover a frequency band from a high band and the remaining two SAW filters then each cover a frequency band from a low band. In this case, the first input port can be connected to a filter which covers a first frequency band from the high band and to a filter which covers a first frequency band from the low band. Correspondingly, the second input port can be connected to a filter which covers a second frequency band from the high band and to a filter which covers a second frequency band from the low band.

On the output side, the first output port can be connected to the two filters which cover the two frequency bands from the high band, and the second output port can be connected to the two filters which cover the two frequency bands from the low band.

The filters can cover, for example, four GSM bands. These can be the GSM 850 and GSM 900 frequency bands from the low band and the GSM 1800 and GSM 1900 frequency bands from the high

band. However, the invention is not restricted to filters for GSM bands. The invention can also comprise, for example, filters for frequency bands which are defined according to the UMTS standard.

The output ports can be balanced or single-ended. The filters can be ladder-type or DMS filters or hybrids of the two.

The chip can also have matching elements which make it possible to match the frequency characteristics of the filters to one another. This is decisive, in particular, when two filters form a diplexer. In this case, each filter should reflect the signals located within the passband range of the other filter in each case.

For the purpose of matching, an inductance and a capacitance can be arranged between two filters on the chip. It is possible to implement this inductance and the capacitance by means of a resonator. Furthermore, an input port can be connected to an external coil. In addition, further matching elements can be implemented on the chip, for instance by means of an inductance of copper.

The chip substrate can be quartz, lithium niobate or lithium tantalate.

The invention also relates to a package which has a chip according to the invention. Such a package preferably also exhibits one or more inductances, particularly a copper coil, for improved diplexer separation. The inductances can be arranged on the surface of the package or integrated into the substrate of the package.

The invention also relates to a package in which four filters operating with surface acoustic waves are arranged in the second embodiment described above, each filter covering a different frequency band. In this arrangement, the four filters are arranged in such a manner that two filters form a left-hand column and the remaining two filters form a right-hand column. Two filters each from one column each are arranged opposite one another.

The filters can be arranged on two or more chips. The chips can comprise different substrate materials. The filters are preferably distributed on two chips. The filters which form the left-hand column are arranged on a first chip and the filters which form the right-hand column are arranged on a second chip. The two chips are positioned opposite one another.

Furthermore, each of the two chips can have one input port, the input port being connected to the two filters of the chip. The two chips form a diplexer. This arrangement corresponds to the illustrative embodiment discussed above, in which two filters each form one input diplexer. However, in distinction from the illustrative embodiment discussed above, the four filters are now distributed over two separate chip substrates.

The package can have two output ports and each of the output ports can be connected to one filter each on each of the two chips. In this case, two filters each form one diplexer, a first filter being arranged on the one chip and a second filter being arranged on the other chip.

A package according to present Claim 18 thus essentially corresponds to a chip according to the present Claim 2, only the filters being distributed over two or more chips.

In the text which follows, the invention will be explained in greater detail with reference to illustrative embodiments and the associated figures. The figures show different illustrative embodiments of the invention by means of diagrammatic representations which are not true to scale.

Figure 1 shows a diagrammatic representation of a transmitting and receiving circuit.

Figure 2 shows a diagrammatic representation of a first illustrative embodiment of the chip.

Figure 3 shows a diagrammatic representation of a second illustrative embodiment of the chip.

Figure 4 shows the insertion loss and the standing wave ratio for the first filter F1.

Figure 5 shows the insertion loss and the standing wave ratio for a second filter F2.

Figure 6 shows the insertion loss and the standing wave ratio for a third filter F3.

Figure 7 shows the insertion loss and the standing wave ratio for a fourth filter F4.

Figure 8 shows a package.

Figure 9 shows an advantageous package.

Figure 10 shows a further variant of the second illustrative embodiment of the chip in diagrammatic representation.

Figure 1 shows a diagrammatic representation of a transmitting and receiving circuit which, in a mobile telephone, connects an antenna 1 to an RF circuit 2. The transmitting and receiving circuit has four signal paths SP1, SP2, SP3, SP4, the upper two signal paths SP1, SP2 forming the receiving circuit and the lower two signal paths SP3, SP4 forming the transmitting circuit. The two signal paths SP1, SP2 of the receiving circuit are each connected to one input port EP1, EP2 of a chip CH.

The chip CH has four SAW filters F1, F2, F3, F4 and two input ports EP1, EP2 and two output ports AP1, AP2. At the input ports EP1, EP2, two filters are in each case interconnected to form a diplexer. Each of the two input ports EP1, EP2 is therefore connected to in each case two SAW filters F1, F3 and F2, F4, respectively. The output ports AP1, AP2 are also embodied as diplexers and connected crossed-over to in each case two SAW filters F1, F2 and F3, F4, respectively. In addition, the output ports AP1, AP2 are balanced here so that the chip has a total of four output terminals AP1a, AP1b, AP2a, AP2b, two output terminals AP1a, AP1b and AP2a, AP2b in each case forming one output port AP1 and AP2, respectively.

The antenna 1 can be optionally connected via a switch S to one of the two signal paths SP1, SP2 of the receiving circuit, each of the two signal paths SP1, SP2 leading to one of the input ports EP1, EP2 of the chip. On the output side,

the output ports AP1, AP2 of the chip are connected to two low-noise amplifiers LNA1, LNA2.

In addition, the antenna 1 can be connected to one of two transmitting paths SP3, SP4 of the transmitting circuit via the switch S. Each transmitting path SP3, SP4 has a pre-amplifier VV1, VV2, a main amplifier HV1, HV2 and a low-pass filter LPF1, LPF1.

Figure 2 shows the arrangement of the SAW filters F1, F2, F3, F4 in a chip CH according to the invention in accordance with a first illustrative embodiment. On the input side, the two input ports EP1 and EP2 are located. The first input port EP1 is connected to filters F1 and F3. The second input port EP2 is connected to filters F2 and F4. Filters F1 and F2 are filters for a frequency band from the high band, filters F3 and F4 are filters for a frequency band from the low band. These can be, for example, frequency bands which are defined in accordance with the GSM standard. Filter F1 is designed for the GSM frequency band at 1960 MHz, filter F2 for the GSM frequency band at 1842.5 MHz. Correspondingly, both frequency bands are in the high band. Filters F3 (942.5 MHz) and F4 (881.5 MHz) cover frequency bands according to the GSM standard and are located in the low band.

However, the invention is in no way restricted to frequency bands according to the GSM standard. The four filters F1, F2, F3, F4 can also be designed, for example, for four frequency bands according to the UMTS standard.

According to the first illustrative embodiment shown in Figure 2, the four filters F1-F4 are DMS structures. In this context, each of the four filters F1-F4 consists of a

combination of two filter structures FS1a, DMS1b, FS2a, DS2b, FS3a, DMS3b, FS4a, DMS4b, one of which can be a DMS structure.

The configuration of such a filter of two filter structures is discussed by means of the first filter F1. The further filters F2, F3, F4 can have an analogous filter structure.

The first filter structure FS1a of the first filter F1 is a series resonator. The output of the first filter structure FS1a is here simultaneously connected to the structural units of the second filter structure DMS1b via three parallel signal lines SL1, SL2, SL3.

The second filter structure DMS1b is a DMS structure and has three coupling converters and two output converters. The signal lines SL1, SL2, SL3, which are connected to the output of the first filter structure FS1, are in each case connected to the coupling converters. The outputs AO1, AO2 of the two output converters of the DMS structure DMS1b are in each case connected to one output port AP1, AP2 of the chip CH. In this arrangement, a first output port AP1 is connected to one of the filters F1 and F2 each. The first output port AP1 has two output terminals AP1a, AP1b and is arranged to be balanced. A second output port AP2 which also has two output terminals AP2a, AP2b and is arranged to be balanced is connected to filters F3 and F4.

The arrangement shown here represents a simplification of the actual filter structure. A filter for the GSM 1900 MHz frequency band can be formed by a series circuit of a resonator and a DMS filter structure having six IDTs. Resonator and DMS filter correspondingly represent the first

and the second filter structure. A filter for the GSM 1800 MHz frequency band can have serial and parallel resonators as the first filter structure and a DMS filter structure with six IDTs as the second filter structure. The filters for the GSM 850 and 950 MHz frequency bands can have DMS structures with three IDTs on the output side as second filter structures and serial and parallel resonators as first filter structures. Furthermore, further resonators can be used at the input between the diplexed filters to provide improved matching.

If two filters form one diplexer, the frequency characteristic of the two filters must be matched to one another by means of matching elements. Signals located in the passband of one filter should be reflected by the other filter. On the input side of the chip, other elements can therefore be arranged which provide for a corresponding matching of the filters.

For example, an external coil could be used which is connected to one of the input ports EP1, EP2. Furthermore, an inductance and a capacitance can be arranged between two filters which form a diplexer. This combination of inductance and capacitance can also be implemented by a resonator. A copper coil which is mounted on the chip CH can be used as further matching element.

The present invention is in no way restricted to the arrangement of the SAW filters F1-F4 shown here. Apart from DMS structures, the filters F1-F4 can also be arranged as ladder-type filters, or hybrids of ladder type and DMS filters are conceivable. In these contexts, ladder-type structures are cascaded with DMS structures.

The input ports EP1 and EP2, respectively, are connected to in each case one filter F1 and F2, respectively, for a frequency band from a high band, and a filter F1 and F4, respectively, for a frequency band from a low band, whilst one output port AP1 is connected to filters F1, F2 for one frequency band each from a high band and the other output port AP2 is connected to filters F3, F4 for one frequency band each from a low band. Correspondingly, cross-overs of the signal lines on the input side or on the output side cannot be avoided in a chip CH according to this first embodiment.

Figure 3 shows a second illustrative embodiment of the chip CH according to the invention. The second illustrative embodiment differs from the illustrative embodiment shown in Figure 2, in particular, by the arrangement of the SAW filters F1-F4 on the chip substrate. The four filters F1-F4 are now arranged in the form of a 2 x 2 matrix with two rows and two columns. Filters F1 and F2 form a first row, filters F3 and F4 form a second row, filters F1 and F3 and filters F2 and F4, respectively, in each case forming a column. Filters F1 and F3 are arranged on the left-hand side of the chip CH and connected to a first input port EP1. Filters F2 and F4 are arranged on the right-hand side and connected to a second input port EP2.

Terminals AP1a, AP1b, AP2a, AP2b for output ports AP1, AP2 are each arranged between filters F1-F4. Terminal AP1a, AP1b for the first output port AP1 is arranged between filter F1 and filter F2. Terminal AP2a, AP2b for the second output port AP2 is arranged between filters F3 and F4 and connected to these two filters F3, F4. The output ports AP1, AP2 are here in each case arranged to be balanced.

Compared with the arrangement shown in Figure 2, the arrangement of filters F1-F4 according to the second illustrative embodiment exhibits some advantages. The chip CH is more compact overall resulting in a more advantageous ratio of length and width. This allows standard tools to be used for installing and testing the chip CH. Furthermore, no cross-over of signal lines is necessary on the input side. There are no signal cross-overs on the output side, either.

Thus, signal cross-overs are avoided at chip level. It is only when the chip is connected to solder pads of a package that line cross-overs can occur on the output side.

The invention is not restricted to the embodiment of the chip shown here. Thus, for example, the acoustic tracks of each individual SAW filter F1-F4 can be rotated by 90° around their respective centre point in an arrangement according to Figure 3. Correspondingly, the outputs of the SAW filters F1-F4 would also be rotated to a different position. In this case, shorter signal paths can be produced for connecting the output terminals AP1a/b and AP2a/b to the terminals of a package.

Figure 10 shows a diagrammatic representation of a possible embodiment of the second illustrative embodiment. This representation is more detailed, thus, in particular, the filter structures are broken down more accurately.

The four SAW filters F1, F2, F3 and F4 are again arranged in a square on the chip. Filters F1-F4 form a 2x2 matrix, two filters F1 and F3 and, respectively, F2 and F4 each being arranged in one column. Furthermore, filters F1 and F2 and

filters F3 and F4, respectively, from different columns are arranged opposite one another.

On the input side, the two input ports EP1 and EP2 are located. The first input port EP1 is connected to filters F1 and F3, which form a diplexer. The second input port EP2 is connected to filters F2 and F4. Filters F1 and F2 are filters for a frequency band from the high band, filters F3 and F4 are filters for a frequency band from the low band. These can be, for example, frequency bands which are defined in accordance with the GSM standard. Filter F1 is designed, e.g. for the GSM frequency band at 1960 MHz, filter F2 is designed for the GSM frequency band at 1842.5 MHz. Correspondingly, both frequency bands are located in the high band. Filters F3 (942.5 MHz) and F4 (881.5 MHz) cover frequency bands according to the GSM standard and are located in the low band.

Each one of filters F1-F4 consists of a number of filter structures. Filter F1 for the GSM frequency band at 1900 MHz has a DMS structure DMS1a which is connected in series with a second filter structure FS1b. The first DMS structure DMS1a has two input converters and four coupling converters. The second filter structure FS1b has two resonators which are implemented in a four-port resonator in this case. The outputs of the second filter structure FS1b of the first filter F1 are connected to the output terminals AP1a, AP1b of the first output port AP1. The first output port AP1 is balanced. The two signal paths for balanced operation are conducted via the two-port resonator FS1b.

The second filter F2 for the GSM frequency band at 1800 MHz is arranged opposite the first filter F1. The second filter

has three filter structure DMS2a, FS2b and FS2c. The first filter structure of the second filter F2 is a DMS structure DMS2a and has a total of six IDTs, two input converters and four coupling converters. The DMS structure DMS2a is connected in series with the second filter structure FS2b. The second filter structure FS2b has two resonators which are again implemented here in a four-port resonator. A third filter structure FS2c, which also has two resonators of a four-port resonator, is connected in parallel with the second filter structure FS2b. The parallel two-port resonator FS2c is virtually connected to ground and on the input side, two balanced signals are connected to it. The output terminals AP1a, AP1b of the first output port AP1 are connected in series with the second filter structure FS2b and in parallel with the third filter structure FS2c of the second filter F2.

The third filter F3 for the GSM frequency band at 942.5 MHZ, together with the first filter F1, forms a diplexer. The third filter F3 has three resonators FS3a, FS3b, FS3c and a DMS structure DMS3d. The first resonator FS3a is connected directly to the first input port EP1. A third resonator FS3c is connected in series with the first resonator FS3a. Furthermore, a second resonator FS3b is connected in parallel to ground between the first and the third resonator. The third resonator FS3c is connected via three parallel signal lines to the DMS structure DMS3d which has three coupling converters and two output converters. The two outputs of the DMS structure DMS3d are in each case connected to one of the output terminals AP2a, AP2b of the second output port AP2, the second output port AP2 being balanced.

The fourth filter F4 for the GSM frequency band at 850 MHz is structured analogously to the third filter F3. The fourth

filter F4 also has three resonators FS4a, FS4b, FS4c and a DMS structure DMS4d, the first resonator FS4a being connected directly to the second input port EP2. The output of the first resonator FS4a is also connected to the third resonator FS4c. A second resonator FS4b is connected in parallel to ground between the first and the third resonator. The third resonator FS4c is connected via three parallel signal lines to the DMS structure DMS3d which has three coupling converters and two output converters. The two outputs of the DMS structure DMS4d are in each case connected to one of the output terminals AP2a, AP2b of the second output port AP2.

The invention is by no means restricted to the arrangement of filters F1-F4 shown in Figure 10 and to the precise configuration of filters F1-F4 shown here. Thus, it is also possible within the scope of the invention that the chip has four input ports and four output ports, each filter F1-F4 being connected to precisely one input port and precisely one output port. Furthermore, two filters each could be interconnected to form one diplexer only on the input side or only on the output side.

Figure 4 shows the insertion loss and the standing wave ratio for a first filter F1. The first filter F1 is designed for the GSM band at 1960 MHz. The upper diagram shows the insertion loss. It can be seen here that there is a very slight insertion loss in the passband between 1930 and 1990 MHz. In the stop band, in contrast, the insertion loss is more than 35 dB.

In the two lower diagrams, the standing wave ratio is shown. The left-hand diagram shows the standing wave ratio on the input side of the filter. This diagram shows that the

reflected signal becomes very low in the passband. The right-hand diagram shows the standing wave ratio on the output side. Here, too, only a very slight signal component is reflected in the passband.

Figures 5 to 7 show correspondingly the insertion loss and the standing wave ratio on the input side and on the output side for filters F2, F3 and F4. Filter F2 is designed for the GSM band at 1842.5 MHz. Filter F3 is designed for the GSM low band at 942.5 MHz. Filter F4 is designed for the GSM low band at 881.5 MHz.

Figure 8 shows a diagrammatic representation of a package PA which has a chip CH according to the invention. The package PA has a rectangular basic shape with two long sides and two short sides, the short sides in each case forming an angle of 90° with the long sides.

The package PA also has eight pins Pin1 – Pin8 via which it can be connected to a circuit board and to other components. Four pins Pin1-Pin4 are arranged on a first long side and four other pins Pin5-Pin8 are arranged on the opposite second long side.

Pin1 could be typically used for the first input port EP1 and Pin4 for the second input port EP2. Furthermore, Pin5 and Pin8 are used for connecting the two output ports AP1, AP2 if the output ports AP1, AP2 are single-ended. In the case of balanced output ports AP1, AP2, Pin5 and Pin6 are used for the first output port AP1 and Pin7 and Pin8 for the second output port AP2.

Pin2 and Pin3 can be used as ground supplies.

Figure 9 shows an improved arrangement of the package PA. This package PA additionally has two further pins Pin9 and Pin10 which are arranged on a short side of the package, and also two further pins Pin11 and Pin12 which are arranged on the opposite second short side.

Pin9-Pin12 are now used for connecting the output ports AP1, AP2. This configuration offers the advantage that the output ports AP1, AP2 of the chip CH can be connected to terminals Pin9-Pin12 of the package PA via short and symmetrical signal lines.

Reference symbols

1	-	Antenna
2	-	RF circuit
SP1	-	First signal path
SP2	-	Second signal path
SP3	-	Third signal path
SP4	-	Fourth signal path
CH	-	Chip
EP1	-	First input port
EP2	-	Second input port
F1	-	First filter
F2	-	Second filter
F3	-	Third filter
F4	-	Fourth filter
AP1	-	First output port
AP2	-	Second output port
AP1a	-	First terminal of AP1
AP1b	-	Second terminal of AP1
AP2a	-	First terminal of AP2
AP2b	-	Second terminal of AP2
S	-	Switch
LNA1	-	First low-noise amplifier
LNA2	-	Second low-noise amplifier
VV1	-	First preamplifier
VV2	-	Second preamplifier
HV1	-	First main amplifier
HV2	-	Second main amplifier
LPF1	-	First low-pass filter
LPF2	-	Second low-pass filter
FS1a	-	First filter structure of F1
DMS1b	-	Second DMS structure of F1
FS2a	-	First filter structure of F2

DMS2b- Second DMS structure of F2
FS3a - First filter structure of F3
DMS3b- Second DMS structure of F3
FS4a - First filter structure of F4
DMS4b- Second DMS structure of F4
SL1 - First signal line
SL2 - Second signal line
SL3 - Third signal line
AO1 - First output of DMS1b
AO2 - Second output of DMS1b
PA - Package
Pin1 - First pin

Patent Claims

1. Chip (CH) having
four filters (F1, F2, F3, F4) operating with surface acoustic waves, each filter (F1, F2, F3, F4) covering a different frequency band, and input and output ports (EP1, EP2, AP1, AP2), each of the input and output ports (EP1, EP2, AP1, AP2) being connected to one or two filters (F1, F2, F3, F4).

2. Chip (CH) according to claim 1,
in which the four filters (F1, F2, F3, F4) are arranged on the chip (CH) in such a manner that two filters (F1, F3) form a left-hand column and the remaining two filters (F2, F4) form a right-hand column and
in which two filters (F1, F2, F3, F4) each from one column each are arranged opposite one another.

3. Chip (CH) according to Claim 1 or 2,
in which the chip has two input ports (EP1, EP2) and each of the input ports (EP1, EP2) is connected to two filters (F1, F2, F3, F4) which form a diplexer.

4. Chip (CH) according to Claims 2 and 3,
in which the two filters (F1, F3) of the left-hand column are connected to the first input port (EP1) and the two filters (F2, F4) of the right-hand column are connected to the second input port (EP2).

5. Chip (CH) according to one of Claims 1-4,
in which the chip has two output ports (AP1, AP2) and each of the output ports (AP1, AP2) is connected to two filters (F1, F2, F3, F4) each which form one diplexer.

6. Chip (CH) according to Claims 2 and 5, in which two oppositely located filters (F1, F2, F3, F4) each are connected to an output port (AP1, AP2) arranged between the two mutually opposite filters (F1, F2, F3, F4).

7. Chip (CH) according to Claim 3 and Claim 5 or 6, in which each of the two input ports is connected to a filter which is connected to the first output port and to a filter which is connected to the second output port.

8. Chip (CH) according to one of Claims 1-7, in which two of the filters (F1, F2) each cover a frequency band from a high band and two of the filters (F3, F4) each cover a frequency band from a low band.

9. Chip (CH) according to Claims 3 and 8, in which the first input port (EP1) is connected to a filter (F1) which covers a first frequency band from the high band and to a filter (F3) which covers a first frequency band from the low band, and in which the second input port (EP2) is connected to a filter (F2) which covers a second frequency band from the high band and to a filter (F4) which covers a second frequency band from the low band.

10. Chip (CH) according to Claim 5 and Claim 8 or 9, in which the first output port (AP1) is connected to the two filters (F1, F2) which cover the two frequency bands from the high band and the second output port (AP2) is connected to the two filters (F3, F4) which cover the two frequency bands from the low band.

11. Chip (CH) according to one of Claims 1-10, which has further elements for matching the frequency characteristics of the filters (F1, F2, F3, F4).

12. Chip (CH) according to one of Claims 1-11, in which the output ports (AP1, AP2) are balanced.

13. Chip (CH) according to one of Claims 1-11, in which the output ports (AP1, AP2) are single-ended.

14. Chip (CH) according to one of Claims 1-13, in which the filters (F1, F2, F3, F4) are in each case constructed as ladder-type or DMS filters or as hybrids of the two filter types.

15. Chip (CH) according to one of Claims 1-14, in which a filter (F1) has a DMS structure (DMS1a) which is connected to an input port (EP1) and connected in series with a resonator (FS1b) and in which the resonator (FS1b) is connected to an output port (AP1).

16. Chip (CH) according to one of Claims 1-15, in which a filter (F2) has a DMS structure (DMS2a) and two resonators (FS2b, FS2c), the DMS structure (DMS2a) being connected to an input port (EP2) and connected in series with the first resonator (FS2b),
a second resonator (FS2c) is connected in parallel with the first resonator (FS2b)
the second resonator (FS2c) is virtually connected to ground and
the first resonator (FS2b) is connected to an output port (AP2).

17. Chip (CH) according to one of Claims 1-16, in which a filter (F3, F4) has three resonators (FS3a, FS3b, FS3c, FS4a, FS4b, FS4c) and a DMS structure (DMS3d, DMS4d), a first resonator (FS3a, FS4a) being connected to an input port (EP1, EP2), a third resonator (FS3c, FS4c) being connected in series with the first resonator (FS3a, FS4a), a second resonator (FS3b, FS4b) being connected in parallel to ground between the first and the third resonator (FS3a, FS4a, FS3c, FS4c), the third resonator (FS3c, FS4c) being interconnected in series with the DMS structure (DMS3d, DMS4d), and the DMS structure (DMS3d, DMS4d) being connected to an output port (AP3, AP4).

18. Package (PA) which has a chip (CH) according to one of Claims 1-17.

19. Package (PA) according to Claim 18, which also has an inductance for improved diplexer separation.

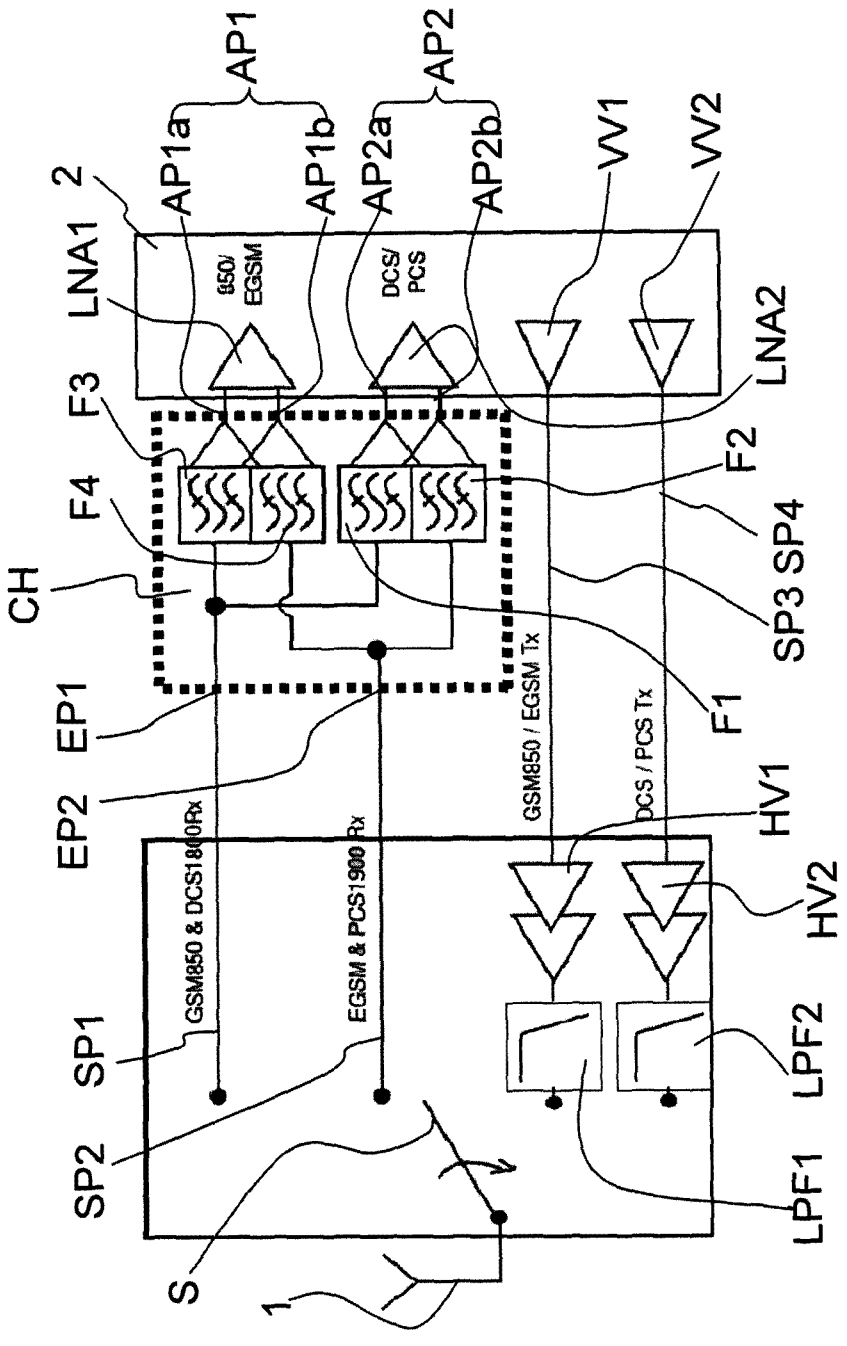
20. Package (PA) according to Claim 18 or 19, the underside of which has a rectangular shape with two long sides and two short sides perpendicular thereto, pins (Pin1, Pin4) for connecting the input ports (EP1, EP2) being arranged on a long side and the pins (Pin5-Pin8, Pin9-Pin12) for connecting the output ports (AP1, AP2) being arranged on the other long side or on the two short sides.

21. Package (PA),
which has four filters (F1, F2, F3, F4) operating with surface acoustic waves, which are arranged in such a manner that two filters (F1, F3) form a left-hand column and the remaining two filters (F2, F4) form a right-hand column, and
in which two filters (F1, F2, F3, F4) each from one column each are arranged opposite one another, the filters (F1, F2, F3, F4) being arranged on two or more chips (CH), and
each filter (F1, F2, F3, F4) covering a different frequency band.

22. Package (PA) according to Claim 21,
in which the filters (F1, F3) which form the left-hand column are arranged on a first chip (CH) and in which the filters (F2, F4) which form the right-hand column are arranged on a second chip which is opposite the first chip in such a manner that two filters (F1, F2, F3, F4) each from one column each are arranged opposite one another.

23. Package (PA) according to Claim 22,
in which each of the two chips has one input port (EP1, EP2) and each of the input ports (EP1, EP2) is connected to two filters (F1, F2, F3, F4) which form a diplexer.

24. Package (PA) according to Claim 22 or 23,
in which the package (PA) has two output ports (AP1, AP2) and each of the output ports is connected to one filter (F1, F2, F3, F4) each on each of the two chips (CH) in such a manner that two filters (F1, F2, F3, F4) form one diplexer.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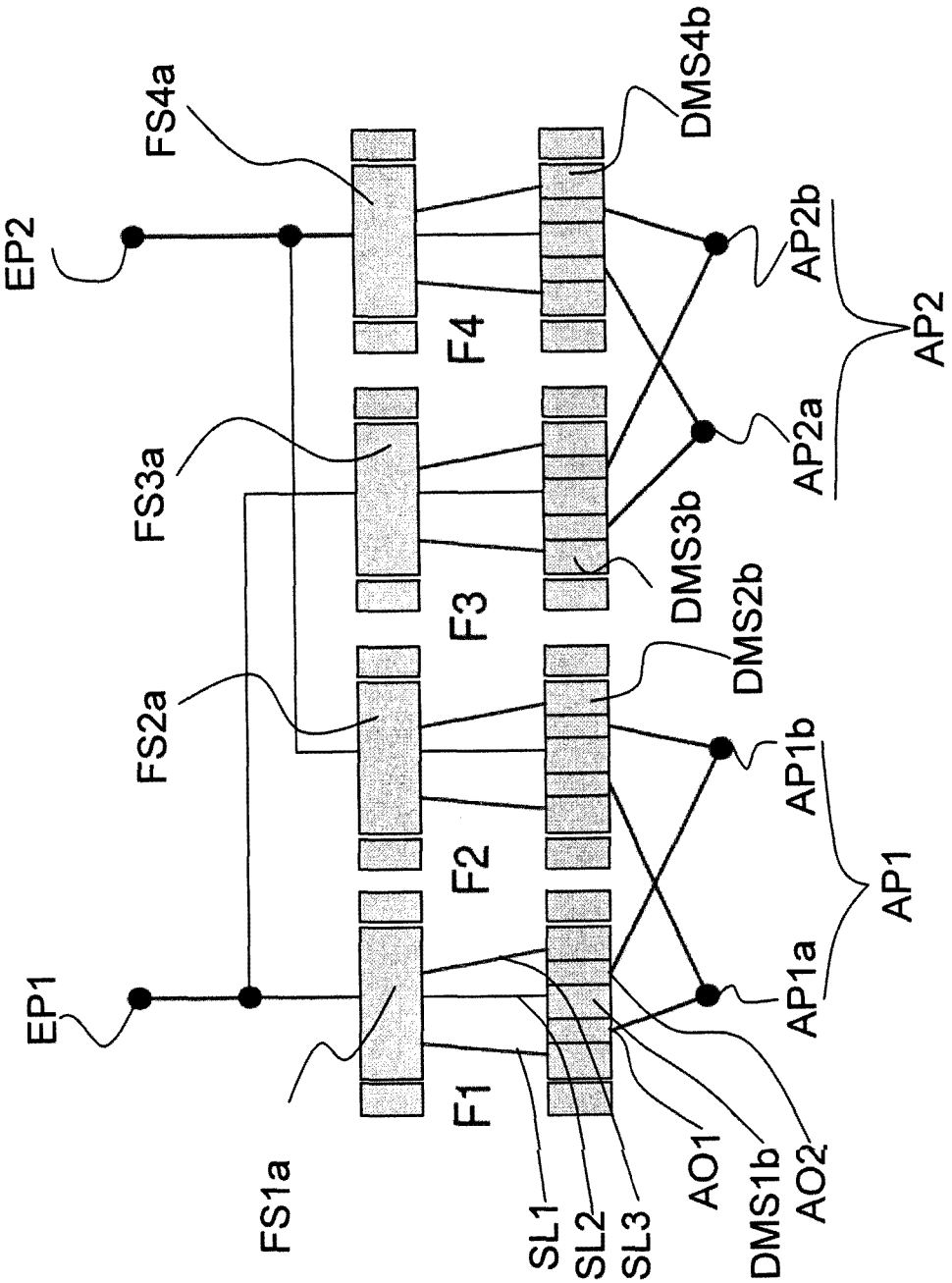
AP2
AP1a
AP1b
AP2a
AP2b
VV1
VV2
2
LNA1
LNA2
850/ EGSM
DCS/ PCS
F3
F4
F2
CH
SP3 SP4
EP1
EP2
F1
GSM850 / EGSM Tx
DCS / PCS Tx
HV1
HV2
GSM850 & DCS1800Rx
EGSM & PCS1900 Rx
SP1
SP2
LPF2
LPF1
S
1

Fig. 1


EP2
EP1
FS4a
FS3a
FS2a
FS1a
F4
F3
F2
F1
DMS4b
DMS3b
DMS2b
AP2b
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SL2
SL3
AO1
AO2
DMS1b

Fig. 2

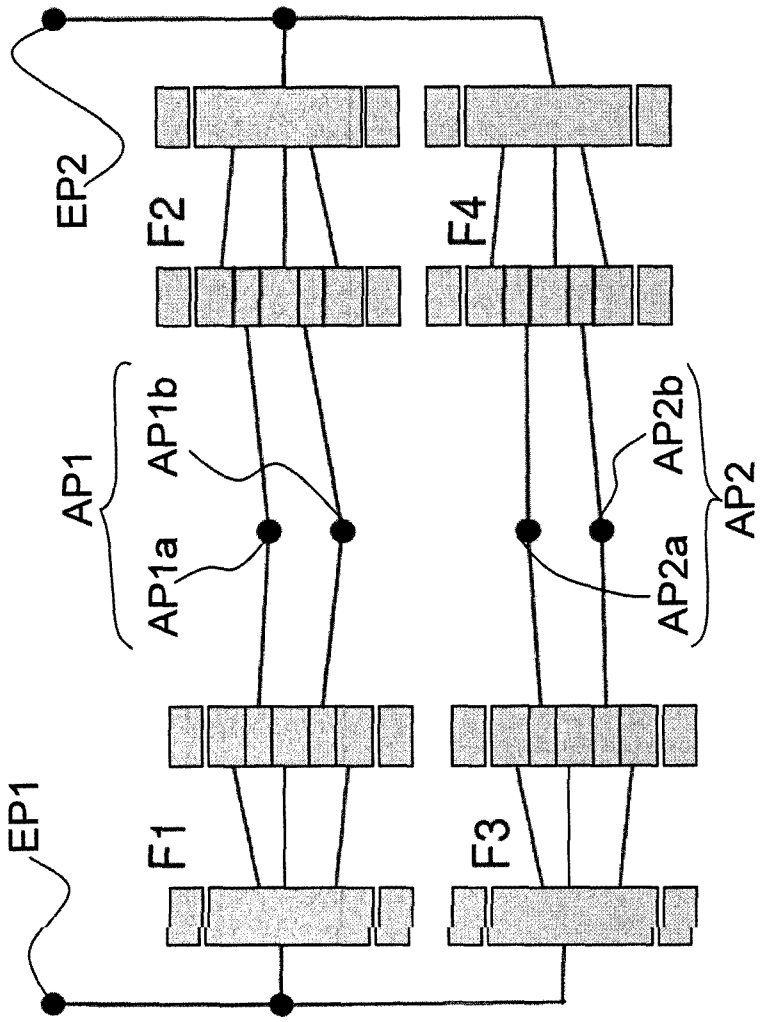
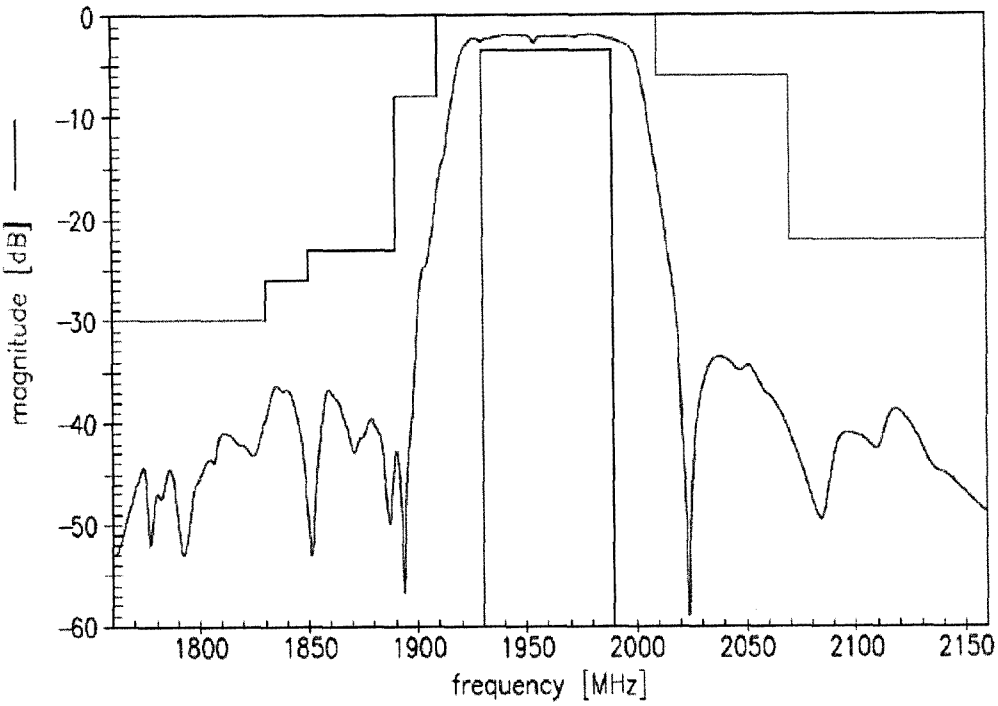
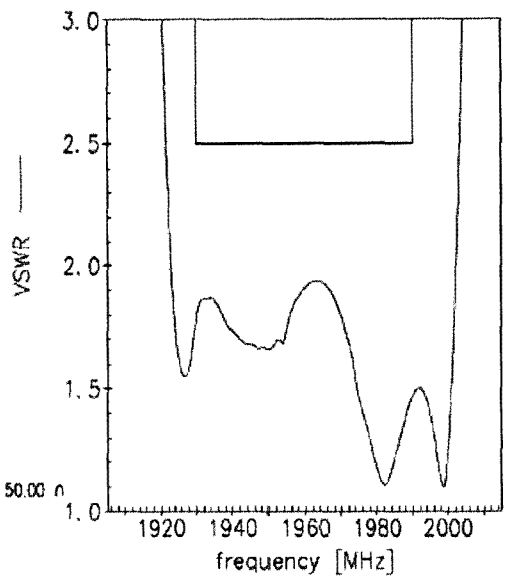


Fig. 3

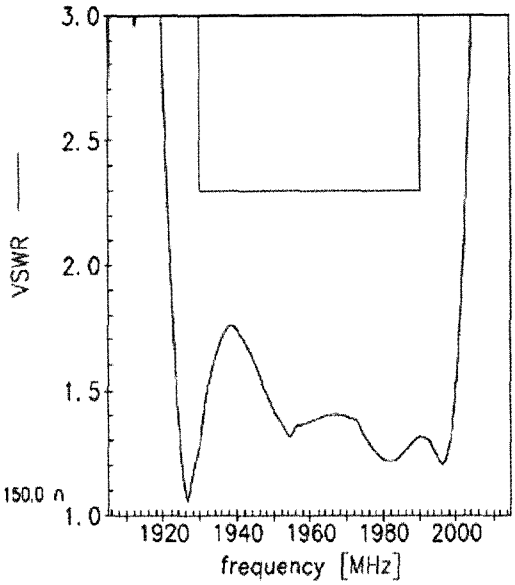
Fig. 4



(1) Transfer function

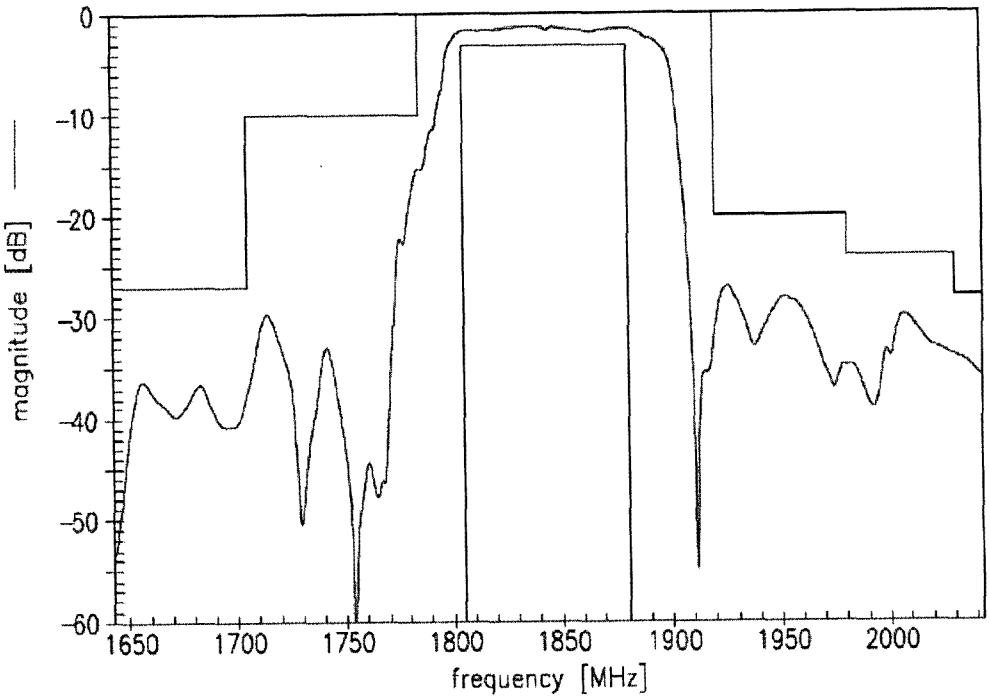


(2) Input VSWR

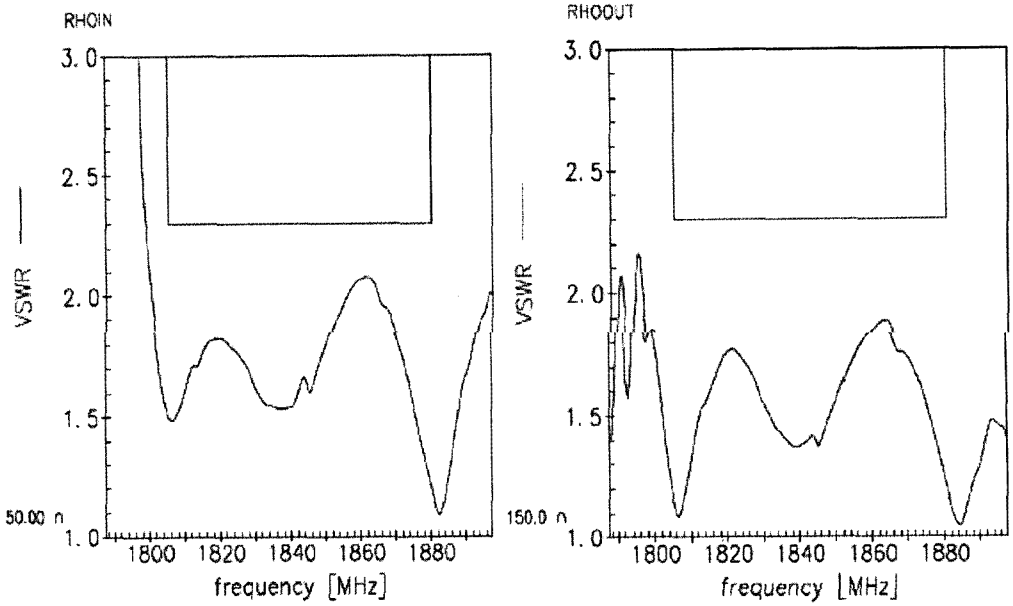


(3) Output VSWR

Fig. 5



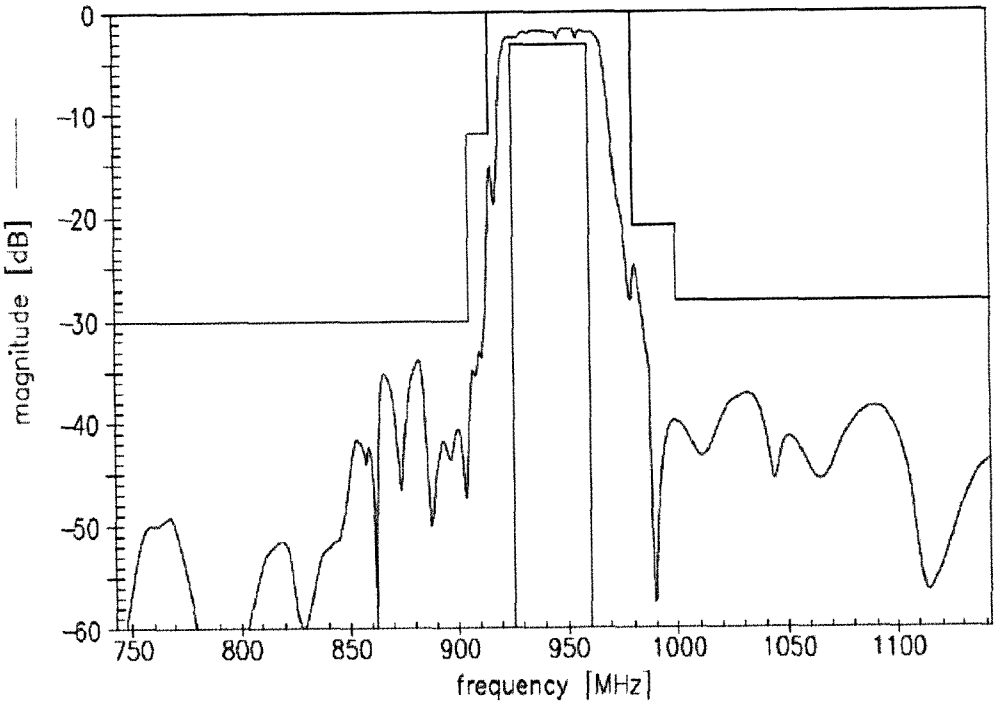
(1) Transfer function



(2) Input VSWR

(3) Output VSWR

Fig. 6



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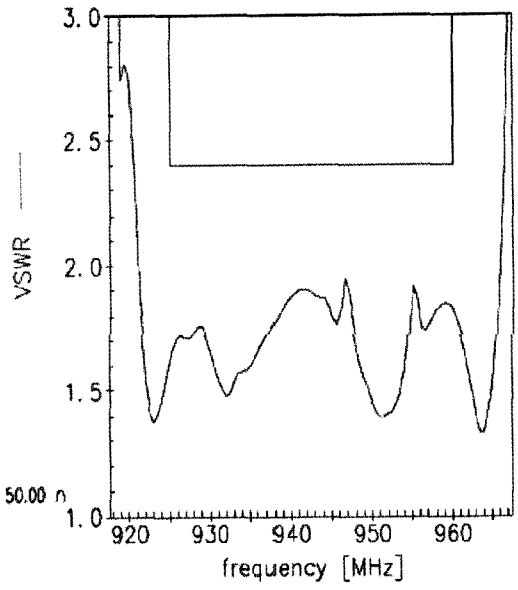
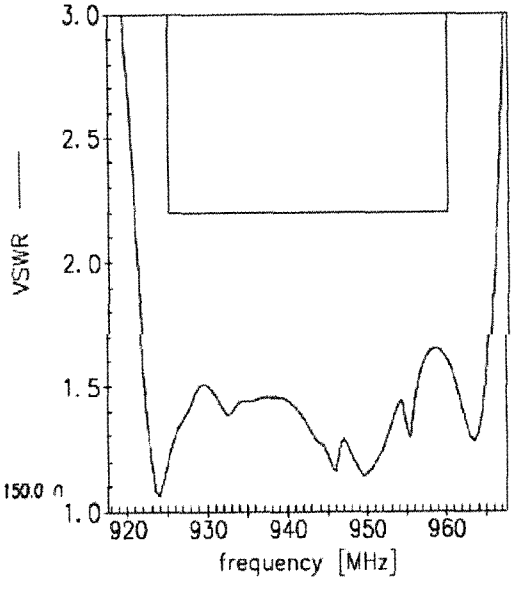
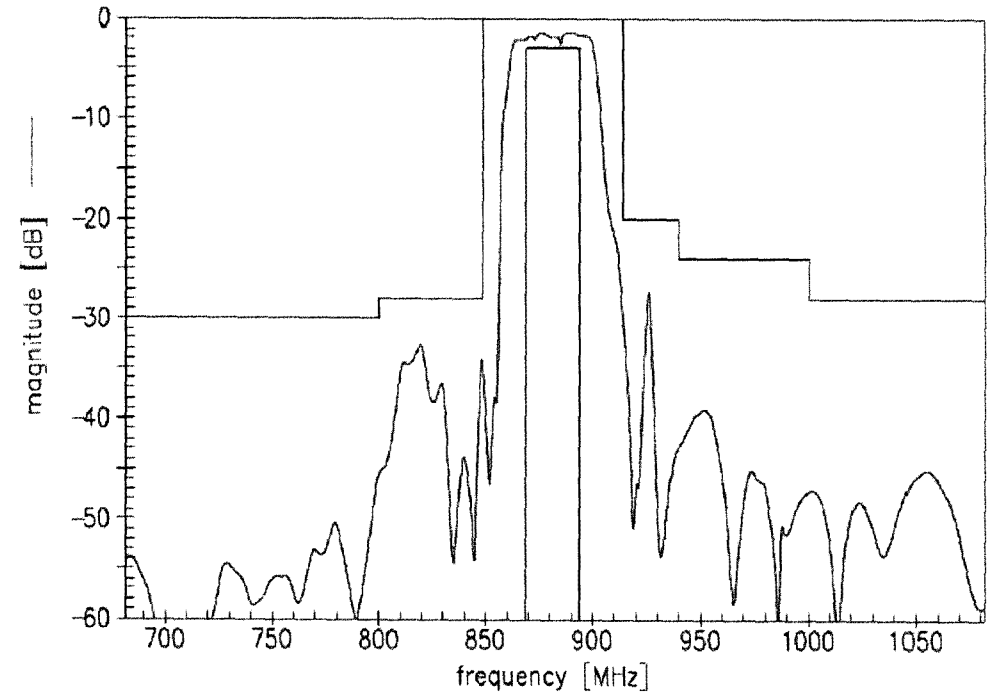


(2) Input VSWR

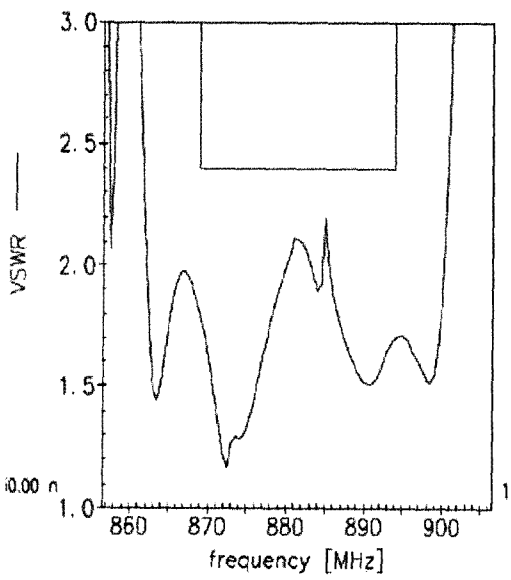


(3) Output VSWR

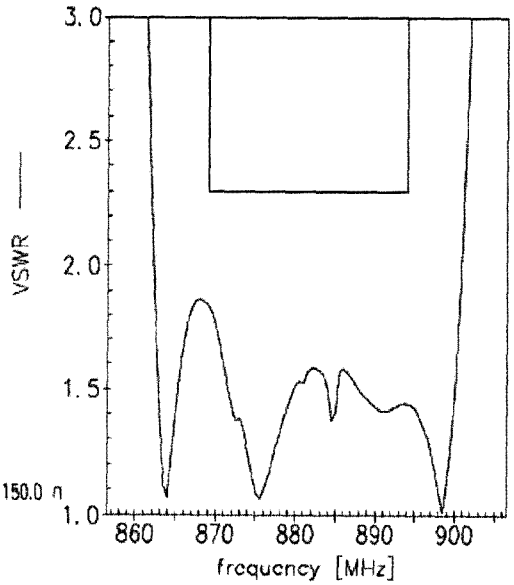
Fig. 7



(1) Transfer function



(2) Input VSWR



(3) Output VSWR

Fig. 8

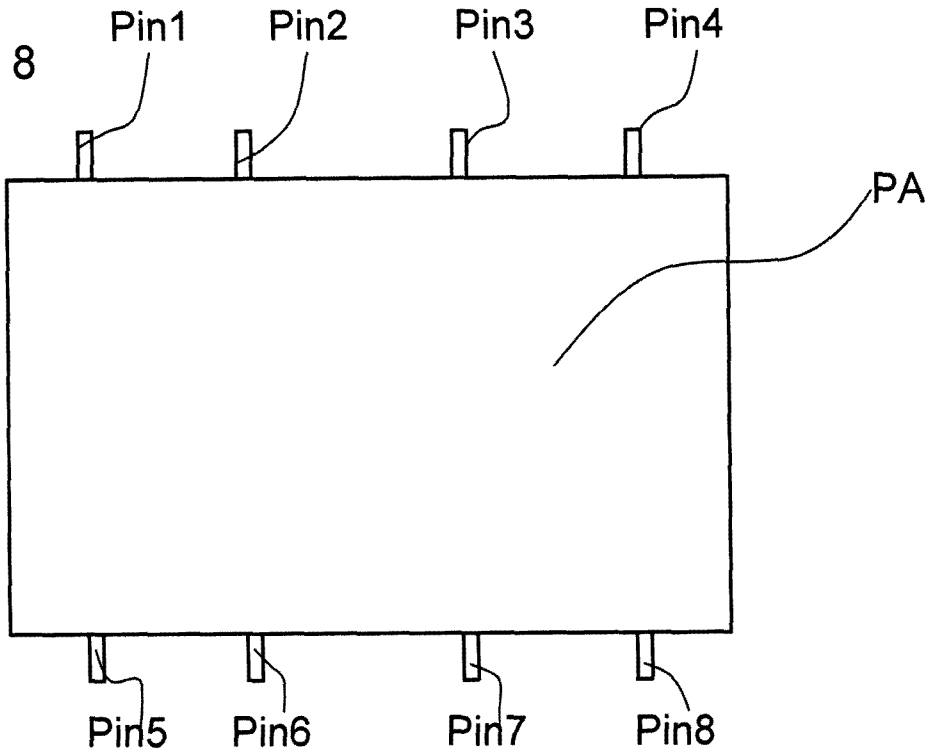
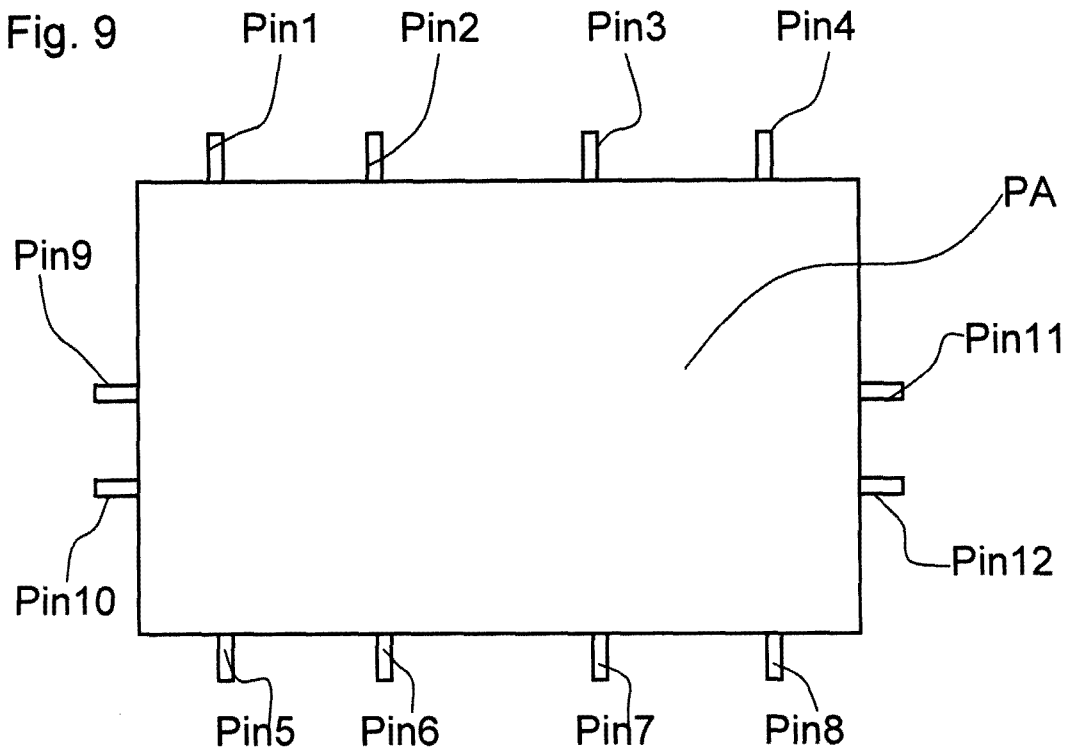

Pin1
Pin2
Pin3
Pin4
PA
Pin5
Pin6
Pin7
Pin8

Fig. 9


Pin1
Pin2
Pin3
Pin4
PA
Pin9
Pin11
Pin10
Pin12
Pin5
Pin6
Pin7
Pin8

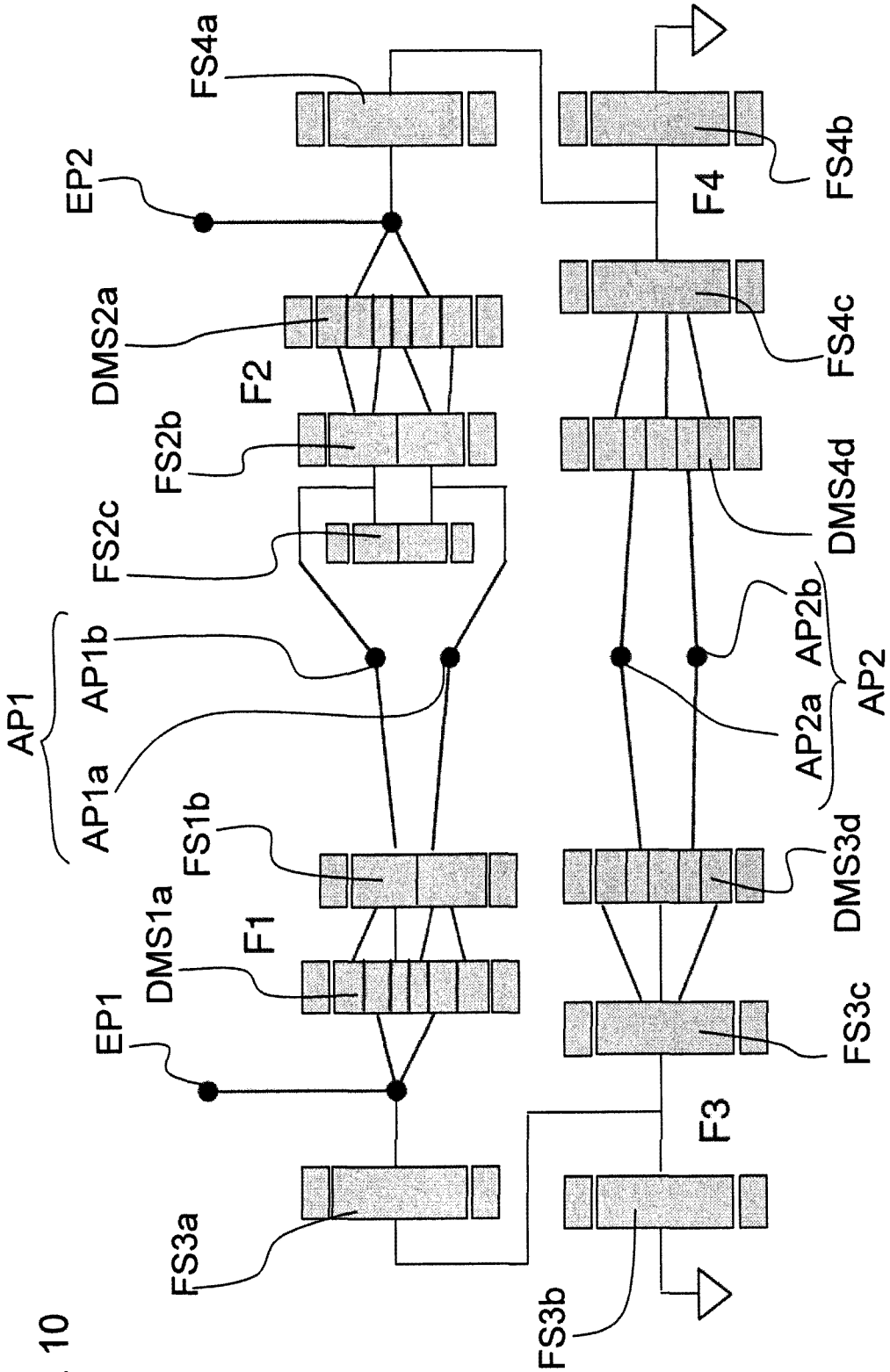

FS4a
EP2
DMS2a
F2
FS2b
FS2c
AP1
AP1b
AP1a
FS1b
DMS1a
F1
EP1
FS3a
FS3b
F3
FS3c
DMS3d
AP2a
AP2b
AP2
DMS4d
F4
FS4c
FS4b

Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/EP2011/069353

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-13, 18-24

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/069353

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03H9/72 H03H9/05 H03H9/00 H03H9/64 H04B1/00
H04B1/18
ADD.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03H H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 733 122 A (SHINONAGA HIDEYUKI [JP] ET AL) 22 March 1988 (1988-03-22) figures 2,7,8(A)	1
X	US 2003/076194 A1 (MACHUI JURGEN [DE] MACHUI JUERGEN [DE]) 24 April 2003 (2003-04-24) paragraphs [0008], [0009], [0012], [0013], [0017]; figures 3,4	1-13, 18-24
X	US 2004/048634 A1 (SATOH YUKI [JP] ET AL) 11 March 2004 (2004-03-11) paragraphs [0034], [0035], [0041], [0043], [0049]; figures 3,4,7	1-13, 18-24

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 January 2012	28/03/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Maget, Judith

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2011/069353

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2002/186097 A1 (SAKURAGAWA TORU [JP] ET AL) 12 December 2002 (2002-12-12) paragraphs [0028] - [0035]; figures 1,3,4	21-24 1-13, 18-20
X	US 6 380 823 B1 (IKATA OSAMU [JP] ET AL) 30 April 2002 (2002-04-30) figures 2,6,9	1-13, 18-24
X	US 2003/148750 A1 (YAN KELVIN KAI TUAN [US] ET AL) 7 August 2003 (2003-08-07) paragraph [0017]; figure 1	1-13, 18-24
X	US 4 647 881 A (MITSUTSUKA SYUICHI [JP]) 3 March 1987 (1987-03-03) figure 1	1,2
X	US 4 737 742 A (TAKOSHIMA TAKEHIRO [JP] ET AL) 12 April 1988 (1988-04-12) figure 1	21
A	US 2010/056204 A1 (TANG WEIMIN [SG] ET AL) 4 March 2010 (2010-03-04) paragraphs [0018], [0020]; figure 1	1-13, 18-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2011/069353

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4733122 A	22-03-1988	JP 62105514 A	16-05-1987
		US 4733122 A	22-03-1988
US 2003076194 A1	24-04-2003	CA 2392833 A1	21-06-2001
		CN 1411632 A	16-04-2003
		DE 19960299 A1	21-06-2001
		EP 1238464 A2	11-09-2002
		JP 2003517239 A	20-05-2003
		US 2003076194 A1	24-04-2003
		WO 0145273 A2	21-06-2001
US 2004048634 A1	11-03-2004	EP 1427114 A1	09-06-2004
		JP 2003087150 A	20-03-2003
		US 2004048634 A1	11-03-2004
		WO 03026154 A1	27-03-2003
US 2002186097 A1	12-12-2002	CN 1383608 A	04-12-2002
		EP 1292025 A1	12-03-2003
		JP 4524864 B2	18-08-2010
		JP 2001352227 A	21-12-2001
		US 2002186097 A1	12-12-2002
		WO 0195487 A1	13-12-2001
US 6380823 B1	30-04-2002	DE 10024956 A1	21-12-2000
		JP 3403669 B2	06-05-2003
		JP 2000349586 A	15-12-2000
		US 6380823 B1	30-04-2002
US 2003148750 A1	07-08-2003	NONE	
US 4647881 A	03-03-1987	DE 3539697 A1	14-05-1987
		FR 2590078 A1	15-05-1987
		GB 2182514 A	13-05-1987
		JP 1642724 C	28-02-1992
		JP 3003411 B	18-01-1991
		JP 61094409 A	13-05-1986
		NL 8503103 A	01-06-1987
		US 4647881 A	03-03-1987
US 4737742 A	12-04-1988	JP 62173814 A	30-07-1987
		US 4737742 A	12-04-1988
US 2010056204 A1	04-03-2010	CN 101662295 A	03-03-2010
		DE 102009039134 A1	11-03-2010
		US 2010056204 A1	04-03-2010

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-13, 18-24

   Physical arrangement and interconnection of four SAW filters on chip(s)/in a package

   ---

2. claims: 1, 14-17

   Realization of SAW filters in a group of four filters on a chip

   ---