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(54) Title: FLEXIBLE DISPLAY

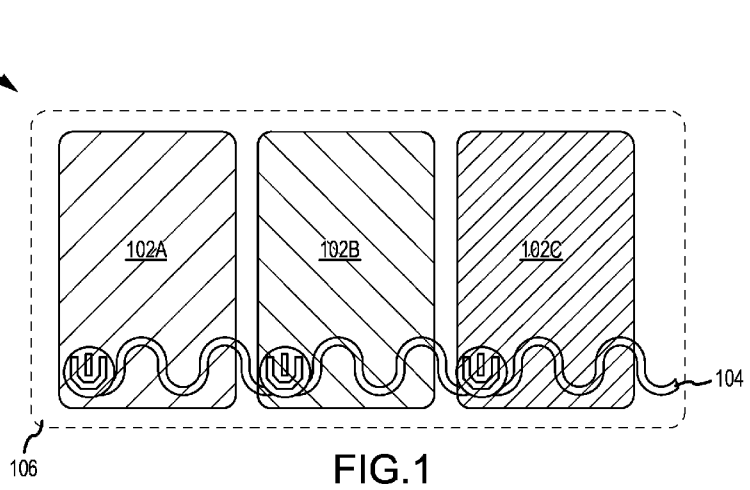

FIG.1

(57) Abstract: A flexible display having an array of pixels or sub-pixels is provided. The display includes a flexible substrate and an array of thin film transistors (TFTs) corresponding to the array of pixels or sub-pixels on the substrate. The display also includes a first plurality of metal lines coupled to gate electrodes of the TFTs and a second plurality of metal lines coupled to source electrodes and drain electrodes of the TFTs. At least one of the first plurality of metal lines and the second plurality of metal lines comprises a non-stretchable portion in the TFT areas and a stretchable portion outside the TFT areas.

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FLEXIBLE DISPLAY

Cross-Reference to Related Applications

This Patent Cooperation Treaty patent application claims priority to U.S. Non-Provisional Application No. 13/837,311, filed March 15, 2013, entitled "Flexible Display", which claims priority to U.S. Provisional Patent Application No. 61/727,473, entitled "Flexible Display", filed on November 16, 2012, the contents of each of which are incorporated herein by reference in their entirety.

Technical Field

Embodiments described herein generally relate to flexible displays for computing devices, and more particularly to implementing a flexible display with metal traces that may bend as the display flexes, without breaking or cracking.

Background

To fabricate a flexible display, many display components have been developed to use organic materials, such as organic light emitting layer, organic passivation layer and polymer substrate as a flexible substrate. However, it is difficult to replace metal traces of the display with an organic material, because electrical conductivity of the organic material is not as high as the metal traces. The metal traces may be broken or disconnected when a display panel is bent, because the metal traces have a fracture strain limit of about 1%. Some other components still use silicon nitride, which may also be cracking. Therefore, it is desirable to have display components to be bendable or flexible.

Brief Summary

Generally, embodiments described herein relate to a display for an electronic device. The display may be an organic light emitting diode (OLED) display. The display includes a flexible substrate that supports an array of pixels or sub-pixels and thin film transistors that drive each pixel or sub-pixel. The display may be flexible about one or more axes. For example, the display may be rolled to form a cylinder or bent into a non-planar shape. By providing such flexibility, portability and certain operations of the display may be enhanced.

In one embodiment, a flexible display having an array of pixels or sub-pixels is provided. The display includes a flexible substrate and an array of thin film transistors (TFTs) corresponding to the array of pixels or sub-pixels on the substrate. The display also includes a first plurality of metal lines coupled to gate electrodes of the TFTs and a second plurality of metal lines coupled to source electrodes and drain electrodes of the TFTs. At least one of the first plurality of metal lines and the second plurality of metal lines comprises a non-stretchable portion in the TFT areas and a stretchable portion outside the TFT areas.

In another embodiment, a flexible display having an array of pixels or sub-pixels is provided. The display includes a flexible substrate and a buffer layer over the flexible substrate. The display also includes an array of thin film transistors (TFTs) corresponding to the array of pixels or sub-pixels on the substrate. The display further includes a first plurality of metal lines coupled to gate electrodes of the TFTs, and a second plurality of metal lines coupled to source electrodes and drain electrodes of the TFTs. The display also includes an integration circuit (IC) board outside the TFT and pixels, and a plurality of metal traces coupled between the TFTs and the IC board. The plurality of metal traces is formed of at least one of the first metal for gate electrode of the TFT and the second metal for source electrode and drain electrode of the TFT. The plurality of metal traces being disposed over the buffer layer. The buffer layer outside the TFT area is configured to have a striation pattern.

Additional embodiments and features are set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the specification or may be learned by the practice of the embodiments discussed herein. A further understanding of the nature and advantages of certain embodiments may be realized by reference to the remaining portions of the specification and the drawings, which forms a part of this disclosure.

Brief Description of the Drawings

Fig. 1 depicts a single pixel of a sample display.

Fig. 2 shows one example of a flexible display exerting a stretching stress on a metal line.

Fig. 3 generally depicts a data line overlapping a series of gate lines.

Fig. 4 shows a series of thin-film transistors (TFTs) for the display device.

Fig. 5 illustrates a flexible display having a serpentine data line capable of accepting strain due to flexing of the display.

Fig. 6 depicts a metal trace resembling a sine wave along its length.

Fig. 7 illustrates two possible redundancy designs for metal traces in accordance with embodiments described herein.

Fig. 8 depicts the gate/control lines and data lines of a sample display, along with a number of TFTs.

Fig. 9 generally depicts a cross-section of a portion of a display pixel's TFT and metal traces associated with the TFT.

Fig. 10 shows a simplified view of the buffer layer of Fig. 9.

Fig. 11 shows a simplified view of an alternative embodiment of the buffer layer of Fig. 9.

Figs. 12 and 13 depict one sample masking and ashing operation that may generate the buffer layer shown in Fig. 10.

Fig. 14 shows an alternative embodiment of a buffer layer with striations formed in the silicon nitride of the buffer layer at the expected crack intervals.

Fig. 15 depicts an alternative embodiment of a buffer layer in which the silicon nitride has been thinned to form an area that may bend or flex without cracking.

Fig. 16 depicts an ILD suitable for use in a flexible display, in which striations are formed in the silicon nitride portion of the ILD.

Fig. 17 is an alternative of an ILD, in which the silicon nitride is removed from above the gate metal fanout but preserved in the intra-gate metal regions.

Fig. 18 is yet another embodiment of an ILD suitable for use in a flexible display.

Fig. 19A illustrates a sample serpentine pattern for a stretchable metal trace in a first embodiment.

Fig. 19B illustrates a sample sine wave pattern for a stretchable metal trace in a second embodiment.

Fig. 19C illustrates a sample sine wave shaped pattern for a stretchable metal trace in a third embodiment.

Fig. 19D illustrates a pair of serpentine patterns for a stretchable metal trace in a fourth embodiment.

Fig. 19E illustrates a pair of sine wave shaped patterns for a stretchable metal trace in a fifth embodiment.

Fig. 19F illustrates a pair of square wave shaped patterns for a stretchable metal trace in a sixth embodiment.

Fig. 19G illustrates the cross-sectional view of the first overlapping region between two metal traces of Fig. 19D in accordance with embodiment of the present disclosure.

Fig. 19H illustrates the cross-sectional view of the second overlapping region between two metal traces of FIG. 19D in accordance with embodiment of the present disclosure.

Fig. 20A illustrates a top view of a flexible display in accordance with embodiments of the present disclosure.

Fig. 20B illustrates a top view of the area including uniform buffer or interlayer dielectric (ILD) overlapping metal traces coupled between integrated circuit (IC) board and TFTs in accordance with first embodiment of the present disclosure.

Fig. 20C illustrates a top view of the area including striated buffer or ILD pattern overlapping metal traces coupled between integrated circuit (IC) board and TFTs in accordance with second embodiment of the present disclosure.

Fig. 20D illustrates a top view of the area including striated buffer or ILD pattern offsetting from metal traces coupled between integrated circuit (IC) board and TFTs in accordance with third embodiment of the present disclosure.

Fig. 21A illustrates a cross-sectional view of Fig. 20A in accordance with embodiments of the present disclosure.

Fig. 21B illustrates a cross-sectional view of Fig. 20B in accordance with embodiments of the present disclosure.

Fig. 21C illustrates a cross-sectional view of Fig. 20C in accordance with embodiments of the present disclosure.

Fig. 21D illustrates a cross-sectional view of Fig. 20D in accordance with embodiments of the present disclosure.

Detailed Description

Generally, embodiments described herein relate to a display for an electronic device. The display may be an organic light emitting diode (OLED) display. The display includes a flexible substrate that supports an array of pixels or sub-pixels and thin film transistors (TFTs) that drive each pixel or sub-pixel. The display may be flexible about one or more axes. For example, the display may be rolled to form a cylinder or bent into a non-planar shape. By providing such flexibility, portability and certain operations of the display may be enhanced.

The display may be flexible outside the TFTs. For example, the display may include stretchable gate lines and/or stretchable data lines in areas outside the TFTs. The display may also include a buffer layer between the flexible substrate and the TFTs and pixels or sub-pixels. The buffer layer may be configured to be resistant to cracking. The display may also include an interlayer dielectric (ILD) is between a first metal layer for gate electrodes and a second metal layer for source/drain electrodes of the TFTs. The ILD may also be configured to be resistant to cracking. Both the buffer and the ILD layers may include a sublayer of silicon oxide and a sublayer of silicon nitride. As the silicon nitride may be more susceptible to cracking when bent, one embodiment may include striations in silicon nitride.

The display may also include a flexible area near its border. Generally, the display includes an integrated circuit (IC) area outside the pixel regions or active area. There may be many metal traces coupled between the IC and the TFTs. These metal traces may be formed of either the gate metal layer or the source/drain metal layer, i.e. a first metal layer or a second metal layer. These metal traces may be configured to be stretchable. The metal traces are formed supported by a flexible substrate with a buffer layer between the metal traces and the flexible substrate. The buffer layer may be striated patterned to be resistant to cracking.

The display may include a number of individual pixels, each of which may be formed from a set of subpixels. For example, Fig. 1 displays a single pixel of a display. The pixel includes three subpixels, namely a red, green and blue subpixel.

The pixels and their subpixels may be formed from an organic light-emitting diode (OLED) material, in some embodiments. In others, different flexible materials may be used to form the pixels and subpixels.

Broadly, a sample flexible display may be constructed from a polymer substrate, an organic light-emitting layer (e.g., an OLED layer) upon the substrate, and an organic passivation layer encapsulating or overlying the light-emitting layer. The substrate may be formed from any suitable material; a polymer is but one example. As a more specific example, the substrate may be formed from polyimide. It should be appreciated that additional layers may be present in a sample flexible display. Likewise, the layers discussed herein may themselves be made up of multiple layers. A sample partial cross-section of an example flexible display is discussed in more detail below, with respect to Fig. 9.

Generally, and as shown in Fig. 1, a flexible display 100 includes flexible substrate that supports subpixels 102A-C. A metal line 104 may connect the various subpixels 102A-C and also the pixels. Such lines may be, for example, gate and/or data lines as known to those skilled in the art. These are but two examples; the metal signal lines may carry other information and/or signals.

Conventional metal signal lines or traces are straight, and may be subject to cracking or breaking when the flexible display is bent. That is, the bending motion may strain the metal lines, which may result in cracking or breaking. Accordingly, certain

embodiments disclosed herein employ serpentine metal traces, as shown in Fig. 1. These serpentine traces may have several properties making them suitable for use with flexible displays. For example, when the flexible display is bent, rolled or otherwise deformed, the serpentine metal lines may stretch along their circular portions, rather than break. An example of a flexible display exerting a stretching stress on a metal line is shown in Fig. 2. As shown in the figure, the metal line 104 may stretch in the direction as pointed by arrows 202 and/or distort in response to the stress exerted by bending the display. Again, it should be appreciated that what is shown in Fig. 2 is a single pixel of a larger display.

Generally, the serpentine metal line shown in Figs. 1 and 2 is formed from a repeating pattern of joined semicircles. The upper and lower edges of the serpentine metal trace generally are the portions that stretch or deform in response to a bending motion of the display. That is, the serpentine metal line, when stretched, bent or the like, extends such that the semicircular portions become longer and somewhat partially ellipse-shaped. This can be seen by comparing the metal line of Fig. 2 to that of Fig. 1.

The metal trace shown in Figs. 1 and 2 typically experiences a greater strain on the interior portion of each semicircular segment that on the outer portions of such segments and/or the connecting portions between semicircular segments.

It should be appreciated that different designs and/or shapes for the metal lines may be used in alternative embodiments. Likewise, the metal lines may be formed from a variety of materials. As one example, the lines may be formed from gold. Still other sample materials include copper, silver, and other conductive metals. The metal line may or may not be formed from a relatively ductile metal. In embodiments having serpentine metal traces formed from gold, the maximum strain exerted on the trace may be approximately 0.5%, which is lower than the strain fracture limit of gold (e.g., 1%).

The subpixels 102A-102C may be formed as OLEDs subpixels. An OLED subpixel generally includes an anode, one or more organic layers, and a cathode. The corresponding OLED can either be a bottom emission type or a top emission type. In a bottom emission OLED, light is extracted from an anode side. In contrast, in a top emission OLED, light is extracted from a cathode side. The cathode is optically

transparent, while the anode is reflective. This top emission OLED normally enables a larger OLED aperture than a bottom emission OLED.

It should be mentioned here that the serpentine metal lines 104 overlap with the pixel area of a top emission OLED as shown in Figs. 1 and 2. The serpentine metal lines generally do not affect the aperture ratio for the top emission OLED device, because the metal lines are under the OLED emitting layers and thus do not block light emission. However, for a bottom emission OLED, the serpentine metal lines do not overlap with the pixel area (not shown).

It will be appreciated by those skilled in that art that a flexible display may include mesh type serpentine metal traces or other mesh type metal traces. Active components may overlap with the mesh of the serpentine metal traces, for a top emission OLED display.

Fig. 3 generally depicts a gate line overlapping a series of data lines 302. As shown, the gate line 304 may be straight for a first portion 304A of its length and then serpentine for a second portion 304B of its length. In such an arrangement, it is contemplated that the section of the panel having the straight data line would not bend, while the section having the serpentine line would be capable of bending. It should be appreciated that some embodiments may permit bending of the display even if the gate (or other) lines are all straight. The line labeled “bending edge” illustrates one possible line along which the flexible display may bend. It should be appreciated that the location of the bending edge is arbitrary and used for illustrative purposes; the display may bend at many other points or along many other lines that are not labeled. Likewise, the display may bend along a complex curve or in multiple dimensions. Some embodiments may even permit the folding of a display.

The data line 302 may also overlap other control signal lines for the flexible display, such as an emission control line. Generally, it may be useful to have the capacitive load in overlapping area 306 of the data and gate lines to be equal in flat and bendable portions of the display. Accordingly, the gate metal space, which is indicated by dimension 308 in Fig. 3, should be wider than the minimum width of the data metal 302, indicated by dimension 306 on Fig. 3. That is, dimension 308 should be greater than dimension 306. If the two are equal, then the side wall capacitance may provide additional loading on the data and/or gate lines in the bent/flexed portion of the

display. In some embodiments, the data metal lines may be thinned by approximately 0.5 micrometers on each side to create the minimum data metal width a. Such a margin may ensure that the overlap capacitance remains the same regardless of whether or not the display is bent or otherwise flexed.

Fig. 4 shows a series of thin-film transistors (TFTs) for the display device. Each TFT 402 is generally located at the intersection of a gate/control line 304 and a data line 302. Drain and source 404 is in the same metal layer as the data line 302. Generally, each TFT operates a single pixel (not shown). Generally, in the case of displays having a bendable and non-bendable area, each TFT 402 should overlap the gate/control line(s) 304 to the same extent as the other TFTs. That is, the overlap between the gate/control line(s) and a TFT in a non-bendable area (as shown on the left hand side of Fig. 4) should be the same as the overlap between the two in a bendable portion of the display (as illustrated on the right-hand side of Fig. 4). The overlap may generally be equal for all TFTs and gate/control lines regardless of whether the lines are straight, serpentine or otherwise vary. In this manner, capacitive line loading due to the TFTs may be constant, regardless of the portion of the display in question.

Fig. 5 illustrates a flexible display 500 having a serpentine data line 502 capable of accepting strain due to flexing of the display. In this flexible display, gate lines 504 may be substantially straight. The bending edge is substantially parallel to the gate lines 504. As with the embodiment of Fig. 4, capacitive line loading between the TFT and the various metal lines should be equal for TFTs located in both the flexible and non-flexible portions of the display. This may be accomplished by overlapping the TFT with a relatively straight portion of the serpentine metal line, as shown in Fig. 5. In this example, the serpentine metal data line has relatively straight edges and connectors, with rounded transitions between edge portions and connector portions. Each TFT overlies an edge portion. Because the edge portion is essentially straight, line loading for the serpentine data line of Fig. 5 is identical or near-identical to the line loading between a TFT and a straight data line. It should be appreciated that the serpentine line configuration shown in Fig. 5 (e.g., with flattened or straight edge portions, instead of semicircular edge portions) may be used with other embodiments discussed herein, such as the embodiment of Fig. 4.

As previously mentioned, some embodiments may employ metal signal lines having a non-linear shape, but that are not serpentine. For example, Fig. 6 depicts a metal trace 600 resembling a sine wave along its length. Such a configuration may reduce the area of the display that is designated for, or dedicated to, the metal line, for example. Such configurations may be used in high density OLEDs, among other applications that either have high pixel densities and/or multiple control, data, or gate lines. The exact height and amplitude of a sine-wave shaped metal trace may vary depending on the electrical characteristics of the panel, its intended use and operating parameters, and so on. Accordingly, exact dimensions are not discussed herein as such dimensions may depend on application and could be empirically determined.

As still another option, multiple metal traces may be employed instead of a single metal trace, as shown in the foregoing figures. It should be appreciated that any metal line in the flexible display may be made redundant. Further, as such a display generally has multiple layers on which metal lines may be routed, the first and second (e.g., normal and redundant) metal traces may be located in different metal layers. Fig. 7 illustrates two possible redundancy designs.

The first design 700A shown in Fig. 7, employs a pair of sine wave-shaped metal traces 702 and 704. The two metal traces overlap only at certain points 706. Essentially, the first and second metal traces are approximately 180 degrees out of phase with one another, such that the upper part of the second metal trace is linearly aligned with the lower part of the first metal trace. This can be seen along the line marked “bending edge” in first redundancy design 700A of Fig. 7. It should be appreciated that the offset between the two traces may be as large or as small as desired.

As another example, the first and second metal traces may overlap one another along all or part of their lengths, as shown in Fig. 7, and specifically in the redundancy design 700B. By overlapping the two traces 702 and 704, one may continue to operate even if the other breaks, cracks or otherwise is interrupted.

Fig. 8 depicts the gate/control lines and data lines of a sample display, along with a number of TFTs. Again, each TFT 402 including drain/source 404 generally corresponds to a single pixel. The gate/control lines 804 connect all TFTs in a row,

while the data lines 802 connect all TFTs in a column. As with prior embodiments, the schematic view of Fig. 8 is intended to illustrate a display having both a non-bendable portion (e.g., the portion where the gate/control lines are linear) and a bendable portion (e.g., the portion where the gate/control lines are serpentine). It should be appreciated that displays may be fully bendable and have no no-bendable portions, depending on the embodiment, and still incorporate the illustrated qualities of Fig. 8 (for example, a serpentine multi-trace pattern may be used across an entirety of a display). Likewise, both data and gate/control lines may be serpentine, sine-shaped or otherwise patterned to be flexible under stress.

As illustrated in Fig. 8, both overlapping and offset redundant metal traces may be employed in the same display. Fig. 8 shows an offset pair of serpentine metal traces along the top set of gate/control lines and an overlapping pair of metal traces along the bottom gate/control lines. It should also be appreciated that this redundancy may be used only in certain portions of a display, such as those in an area or section that may be more susceptible to breaking or fracturing under stress, or in areas having sufficient space to support such redundancy.

Sample stack-ups of a flexible display will now be discussed. Fig. 9 generally depicts a cross-section of a portion of a display pixel's TFT and metal traces associated with the TFT. The cross-section is taken as shown by arrows A-A in Fig. 4. Generally, the TFT itself does not bend (although in alternative embodiments, it may). Rather, the display bends along and to the right of the line labeled "bending area" (with respect to Fig. 9). The TFT itself is generally to the left of the bending area line in Fig. 9, while the inter-TFT area, including the metal traces previously discussed, is to the right.

By way of explanation, the labels for various layers will now be discussed. Substrate 902 may be formed of polyimide (PI), which is one example of a suitable substrate on which a flexible display may be formed. Other embodiments may use different substrates. The buffer layer 904 is a base layer between the substrate (e.g., PI) and gate metal 910/gate insulators 908. The buffer layer may be formed from one or both of silicon nitride and silicon oxide. The layer 906 is the active semiconductor layer of the TFT. The semiconductor may be formed of amorphous silicon, low temperature polysilicon or metal oxide. The gate insulator (GI) layer 908 may be formed of a

silicon oxide. Atop the GI layer is the gate layer, which is again a metal. An inter-layer dielectric (ILD) partially surrounds the gate 910 and is partially atop the GI layer 908. This inter-layer dielectric may be formed from one or both of silicon nitride and silicon oxide. (It should be appreciated that any silicon oxide and/.or silicon nitride may be suitable in any of the layers.) Source/drain metal 918 connect to active layer 906. A passivation layer 914, denoted by "PAS," is formed above the source/drain metal 918 and may be made from a silicon nitride. The "PAD" shown on Fig. 9 is the contact pad, e.g., the bonding site between the panel and/or driver integrated circuit and a flex circuit.

In some embodiments, an encapsulation layer overlies the TFT structure.

A sample simplified view of the buffer layer 904 of Fig. 9 is shown in Fig. 10. Buffer layer 904 may include a first layer 904B, which may be formed of silicon oxide and the like. Buffer layer 904 may also include a second layer 904A, which may be formed of silicon nitride and the like. In particular, the dashed line in Figs. 10-13 is the same as the dashed line in Fig. 9, labeled "bending area." Generally, silicon oxides may bend more reliably without failing than silicon nitrides when used in the structure shown in Fig. 9, or similar structures. The second layer 904 may have some striations 906. Generally, the interval between cracks in the silicon nitride of a given layer is a function of the layer thickness. Thus, it may be useful to form a specialized pattern in the silicon nitride portion of the buffer layer to prevent cracking when the display flexes.

Different embodiments may change the deposition order of silicon nitride (e.g., SiNx) and silicon oxide (e.g., SiO) in the buffer layer 904. Accordingly, Figs. 10-13 presume that silicon oxide is deposited first and then silicon nitride is deposited. By contrast, Figs. 14-15 presume that silicon nitride is first deposited, followed by silicon nitride.

Continuing with Fig. 10, it may be useful to create striations in the silicon nitride of the buffer layer (or other layer) at fairly regular intervals to prevent the formation of cracks in the buffer layer. Since the crack interval may be determined as a function of the layer thickness, the layer can be striated at the same intervals at which expected crack or breaks may form. Fig. 10 depicts the buffer layer 904 with these striations formed at such intervals.

As another option, the silicon nitride may be thinned instead of striated. A thinned layer may be more likely to flex or bend than crack. Accordingly, thinning the SiNx layer 904C in the bending region to the right of the dash line, as shown in Fig. 11, may enhance performance of the display. In particular, one or more thinned areas may be formed such that a step pattern is created. The thinned areas may be larger or smaller than shown in Fig. 11. In some embodiments, the SiNx may define a thinned area, then may increase to a thicker area and then define another thinned area. Such thinned areas may be formed at expected cracking intervals.

Figs. 12 and 13 depict one sample masking and ashing operation that may generate the buffer layer shown in Fig. 10. Initially, a half tone photoresist (labeled "PR") mask 1202 may be deposited across the entirety of the SiNx layer of the buffer layer 904. Exposure to ultraviolet light may ash the photoresist and the SiNx layer. Here, three different exposures may be used. 100% exposure to ultraviolet light may be used to ash entirely through the photoresist and silicon nitride layer to form the striations. 30% exposure to ultraviolet light may be used to remove the photoresist, but not remove any of the silicon nitride layer. Additionally, 0% exposure to ultraviolet light may keep the photoresist, which protects the active layer 906. What is left after such ashing is shown in Fig. 13. This photoresist may be deposited through an additional masking operation when forming the TFT and metal line structure.

Figs. 14 and 15 generally depict sample buffer layers for use with a flexible display. Unlike the buffer layers shown in Figs. 10 and 11, in these layers silicon oxide overlays silicon nitride. Again, the silicon oxide and silicon nitride of the buffer may be formed on a polyimide substrate.

Fig. 14 is similar to Fig. 10, in that striations may be formed in the silicon nitride 1402B of the buffer layer 904 at the expected crack intervals. Here, however, the silicon oxide 1402A may partially or completely fill in such striations. An extra mask may be needed to form the silicon nitride layer when compared to masking operations that lack the aforementioned striations or trenches.

Fig. 15, by contrast, is similar to Fig. 11. Again, the silicon nitride 1502B has been thinned to form an area that may bend or flex without cracking. Again, the silicon oxide may overlay this thinned area. Although Fig. 15 shows the silicon oxide layer 1502A as having an approximately even thickness along the entire layer, in some

embodiments the silicon oxide may be thicker where it overlies the thinned silicon nitride. In this manner, the buffer layer may have a uniform, smooth upper surface. Since the silicon oxide is less prone to cracking during a bending or flexing operation, it may be thickened as necessary in certain embodiments.

Figs. 16-18 will now be discussed. These figures show various embodiments of the inter-layer dielectric (ILD) layer shown generally in Fig. 9. The cross section is taken as shown by arrows B-B in Fig. 4. As can be seen from the figures, the ILD 912 generally lies between the buffer 904 and/or gate insulator layers 908 and the passivation layer 914. The active element 906 shown in the figures is a portion of the source/drain metal shown in Fig. 9. Note that the gate metal is between gate insulator 908 and the ILD 912, which is not shown above the active layer 906 in Figs. 16-18. Also, the source/drain metal is between the ILD 912 and passivation layer 914, which is not shown above the active layer 906 in Figs. 16-18.

The ILD layer 1602 is generally formed from a sublayer of silicon oxide 1602A and a sublayer of silicon nitride 1602B. Thus, the silicon nitride portion of the ILD may also be susceptible to cracking during flexing of the display. Accordingly, and as shown in Fig. 16, striations may be formed in the silicon nitride portion of the ILD. Silicon nitride nonetheless generally overlays the fanout portions of the gate metal, as also shown in Fig. 16. Further, the silicon oxide may at least partially fill in the striations in the silicon nitride, as may the passivation layer above the ILD 1602.

Fig. 17 is an alternative embodiment to the embodiment of Fig. 16. Here, the silicon nitride 1602B of the ILD 1602 is removed from above the gate metal fanout but preserved in the intra-gate metal regions.

Fig. 18 is yet another embodiment of an ILD suitable for use in a flexible display. In this embodiment, the ILD 1702 is completely removed from the bending area of the display. That is, the silicon oxide 1702A and silicon nitride 1702B layers of the ILD do not cover the gate metal fanout area at all.

Figs.19A-C show sample patterns of the serpentine portion 104 of FIG. 1 as alternative embodiments. As shown in Fig. 19A, the stretchable metal trace may have a serpentine pattern. In a particular embodiment, the trace width “w” as shown in Fig. 19A may be about 4 μm while the radius “r” as shown in Fig. 19A may be

about 5 µm. The trace width may also increase to about 8 µm while the radius "r" may increase to about 6 µm. It should be appreciated that there are sample dimensions for one embodiment; the dimensions may vary from embodiment to embodiment and so should be considered examples and not limitations or requirements.

As shown in Fig. 19B, the stretchable metal trace may have a sine wave pattern. In a particular embodiment, the trace width "w" as shown in Fig. 19B may be about 4 µm while the radius "r" shown in Fig. 19B may be about 8 µm. The trace width may also increase to about 8 µm while the radius may increase to about 20 µm.

As shown in Fig. 19C, the stretchable metal trace may have a square pattern. The trace width "w" and the radius "r" are defined as shown in Fig. 19C. The trace width and the radius may be similar to the sine wave pattern. It will be appreciated by those skilled in the art that the pattern may vary, as long as the pattern allows the metal trace to be stretchable.

Figs. 19D-F show sample patterns of the redundancy design 700A of Fig. 7 as alternative embodiments. As shown, two metal traces are interleaved with a first overlapping region and a second overlapping region 1904 between a first metal trace 1906 and a second metal trace 1908. The first and second overlapping regions 1902 and 1904 are shown within dashed lines. First metal trace 1902 is formed from a first metal layer which is the same as the gate line or gate electrode. Second metal trace 1904 is formed from a second metal layer which is the same as the data line and source/drain electrodes. The trace width and the radius may be larger than the single metal trace patterns without redundancy as shown in Figs. 19A-C.

Example dimensions are provided below. The definitions of the trace width and the trace radius remain the same as the corresponding single metal trace. In case of the redundancy serpentine pattern as shown in Fig. 19D, the trace width may be 4 µm and the radius may be 10 µm. If the trace width is 8 µm and the radius may be 15 µm. Again, these are sample dimension that may vary in different embodiments, as is true for all dimensions, tolerances, measurements and the like throughout this document.

In the case of the redundancy sine wave pattern as shown in Fig. 19E, the trace width may be 4 µm and the radius may be 15 µm. If the trace width is 8 µm and the radius may be 30 µm. Again, the redundancy square pattern may have similar trace width and radius to the redundancy sine wave pattern.

Figs. 19G-H show the cross-sectional view of the first and second overlapping regions between two metal traces in accordance with embodiment of the present disclosure. The first overlapping region 1902 may connect to straight line portion of either a data line or a gate line (such as overlapping region 706 as shown in Fig. 7). As shown in Fig. 19G, the first metal or gate is connected to the second metal or source/drain electrodes through a conductive layer 1910 by a through hole (VIA) 1912 defined in the passivation layer and gate insulator. The conductive layer 1910 may be formed of a transparent conductor, such as indium-tin-oxide. The conductive layer is also disposed over a passivation layer 914 which is on top of the second metal trace 1908. The first metal is coupled to gate line 304, while the second metal is coupled to data line 302.

Alternatively, the conductive layer 1910 (not shown) may be eliminated. The second metal trace may be on top of the first metal trace in a through hole such that the two metal traces are connected to have redundant metal traces. In case one metal trace is broken, the other metal trace is still connected.

Referring to Fig. 19H now, the first metal trace 1906 and the second metal trace 1908 does not connect to each other in the second overlapping region 1904. They are separated by an ILD 912.

Fig. 20A shows a top view of a flexible display in accordance with embodiments of the present disclosure. As shown, a flexible display 2000 includes a display region 2020 that includes pixel regions 102 and TFTs, gate lines 304 and data lines 302. Additionally, the flexible display includes integrated gate drivers 2008 on the left and right sides of the display region and an integrated circuit (IC) 2006 on the top of the display region. The integrated gate drivers may be fabricated at the same time as the active layer 906. The integrated drivers 2008 and the IC 2006 are outside the display region 2020. The flexible display further includes metal traces 2002 coupled between IC 2006 and display region 2020.

Figs. 20B-20D show top views of a silicon nitride sublayer overlapping with metal traces in according to embodiments of the present disclosure. The silicon nitride sublayer may be included in either the buffer layer or the ILD. The metal traces 2002 are coupled between IC 2006 and display region 2020 as shown in Fig. 20A. Fig. 20B shows that the silicon nitride sublayer 2004A is uniformly cross the metal traces 2002. Fig. 20C shows that the silicon nitride has a striated pattern 2004B, and the striated pattern 2004B overlaps with the metal traces 2002. Fig. 20D shows that the silicon nitride sublayer may also have a striated pattern 2004C, which may shift from overlapping the metal traces 2002 to filling the space between the metal traces 2002.

Figs. 21A-D illustrate sample cross-sectional views of the display in accordance with embodiments of the present disclosure. Fig. 21A shows a cross-sectional view with the silicon nitride sublayer 904A and 912A in a uniform pattern for the buffer layer 904 and the ILD layer 912 as shown in Fig. 20B. As shown, the silicon nitride sublayers in both the buffer layer and the ILD do not have any striated pattern, as the top view Fig. 20B shows. It will be appreciated by those skilled in the art that the silicon nitride sublayer 904A in the buffer layer 904 may be exchanged position with silicon oxide sublayer 904B. Namely, the silicon oxide sublayer 904B may be on top of the silicon nitride sublayer 904A. Likewise, the silicon nitride sublayer 912A in the ILD layer 912 may be exchanged position with silicon oxide sublayer 912B.

Fig. 21B shows a cross-sectional view of the display in accordance with embodiments of the present disclosure. As shown, the silicon nitride sublayer 2014B of the buffer layer 904 has a striated pattern as shown in Fig. 20C. The silicon oxide sublayer 2014B is uniform in some embodiments. The striated pattern 2014B overlaps with the metal trace 2002 of the first metal (e.g. gate metal). In this embodiment, the ILD 912 as shown in Fig. 21A is eliminated in this region beyond the TFTs 402 or display region 2020. Again, it will be appreciated that the silicon nitride sublayer 2014B may be exchanged position with the silicon oxide sublayer 2014A. It will also be appreciated that the display may include an ILD layer that includes a uniform silicon nitride sublayer like in Fig. 21B in an alternative embodiment. The ILD may also include a striated pattern like the silicon nitride sublayer 2014B in the buffer layer in another embodiment.

Fig. 21C a cross-sectional view of the display in accordance with embodiments of the present disclosure. As shown, the silicon nitride sublayer of the ILD layer 912 has a striated pattern as shown in Fig. 20D. The striated silicon nitride pattern 2012B of the ILD layer fills the space between the metal traces 2002. However, the silicon nitride sublayer 2014B with a striated pattern, as shown in Fig. 20C, typically still overlaps with the metal trace 2002 of the first metal (e.g. gate metal).

Fig. 21D a cross-sectional view of the display in accordance with embodiments of the present disclosure. As shown, the ILD layer includes a striated silicon nitride sublayer 2012C with a striated pattern 2004B as shown in Fig. 20C. The striated silicon nitride sublayer 2012C overlaps with metal trace 2002, while the striated silicon nitride sublayer 2014B is offset from the metal trace 2002 and between two metal traces 2002. The silicon oxide sublayer 2014A in the buffer layer 904 and the silicon oxide sublayer 2012A in the ILD layer 912 are uniform with a uniform pattern 2004A as shown in Fig. 20A.

It will be appreciated by those skilled in the art that the metal traces 2002 may be formed of redundant metal traces, such as two metal traces overlapping or interleaved shown in Fig.7 and Figs. 19A-F with different shapes, such as serpentine, sine wave, square wave and the like. The metal traces 2002 may be formed of at least one of the gate metal or drain/source metal or both the gate metal and the drain/source metal. It will be appreciated by those skilled in the art that a combination of the silicon nitride sublayers in the buffer layer and the ILD layer and the metal traces may vary to be resistant to cracking or disconnections subjected to stretching or bending resulted stress or strain.

Although embodiments have been discussed with respect to particular structures and manufacturing processes, it will be apparent to those of skill in the art that variations may be made to such embodiments upon reading the disclosure. Such variations and changes are fully embraced by this document.

Claims

What is claimed is:

1. A flexible display having an array of pixels or sub-pixels, the display comprising:

a flexible substrate;

an array of thin film transistors (TFTs) corresponding to the array of pixels or sub-pixels on the substrate;

a first plurality of metal lines coupled to gate electrodes of the TFTs; and

a second plurality of metal lines coupled to source electrodes and drain electrodes of the TFTs, wherein at least one of the first plurality of metal lines and the second plurality of metal lines comprises a non-stretchable portion in the TFT areas and a stretchable portion outside the TFT areas

2. The flexible display of claim 1, wherein the stretchable portion comprises a metal trace shaped in a pattern configured to be bendable.

3 The flexible display of claim 2, wherein the pattern comprises at least one of serpentine, sine wave, and square wave.

4. The flexible display of claim 1, wherein the pixels or sub-pixels comprise organic light emitting diode.

5. The flexible display of claim 1, further comprising a buffer layer between the substrate and the TFT.

6. The flexible display of claim 5, further comprising an active semiconductor layer over the buffer layer and a gate insulator over the active layer, wherein the gate electrode is disposed over the gate insulator.

7. The flexible display of claim 6, wherein the active semiconductor layer comprises a material selected from a group consisting of amorphous silicon, low temperature polysilicon, and metal oxide.

8. The flexible display of claim 5, wherein the buffer layer comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises striation in the bendable area.

9. The flexible display of claim 5, wherein the buffer layer comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises a thicker portion in the TFT area than the bendable area outside the TFT area.

10. The flexible display of claim 1, further comprising an interlayer dielectric (ILD) between the gate electrode of the TFT and the source/drain of the TFT.

11. The flexible display of claim 10, wherein the ILD comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises a striation pattern in the bendable area outside the TFT area.

12. The flexible display of claim 10, wherein the ILD layer is present in the TFT area and absent outside the TFT area.

13. The flexible display of claim 1, further comprising a passivation disposed over the source electrodes and drain electrodes of the TFTs.

14. The flexible display of claim 13, wherein the passivation layer comprises a flexible organic material.

15. The flexible display of claim 1, wherein the flexible substrate comprises polyimide.

16. The flexible display of claim 1, wherein the stretchable portion of the at least one of the first plurality of metal lines and the second plurality of metal lines further comprises a first stretchable portion interleaved or overlapped with a second stretchable portion as a redundant.

17. The flexible display of claim 16, wherein the first stretchable portion is formed from the first metal for the gate electrode and gate line, and the second stretchable portion is formed from the second metal for the drain and source and data line.

18. The flexible display of claim 17, wherein the first stretchable portion and the second stretchable portion are connected at least one location outside the TFT area.

19. A flexible display having an array of pixels or sub-pixels, the display comprising:

a flexible substrate;

a buffer layer over the flexible substrate;

an array of thin film transistors (TFTs) corresponding to the array of pixels or sub-pixels on the substrate;

a first plurality of metal lines coupled to gate electrodes of the TFTs; and

a second plurality of metal lines coupled to source electrodes and drain electrodes of the TFTs;

an integration circuit (IC) board outside the TFT and pixels; and

a plurality of metal traces coupled between the TFTs and the IC board, the plurality of metal traces being formed of at least one of the first metal for gate electrode of the TFT and the second metal for source electrode and drain electrode of the TFT, wherein the plurality of metal traces being disposed over the buffer layer, wherein the buffer layer outside the TFT area is configured to have a striation pattern.

20. The flexible display of claim 19, wherein the plurality of metal traces are being configured to be stretchable.

21. The flexible display of claim 19, wherein at least one of the first plurality of metal lines and the second plurality of metal lines comprises a non-stretchable portion in the TFT areas and a stretchable portion outside the TFT areas.

22. The flexible display of claim 19, wherein the stretchable portion comprises a metal trace shaped in a pattern configured to be bendable.

23. The flexible display of claim 22, wherein the pattern comprises at least one of serpentine, sine wave, and square wave.

24. The flexible display of claim 19, wherein the pixels or sub-pixels comprise organic light emitting diode.

25. The flexible display of claim 19, further comprising a buffer layer between the substrate and the TFT.

26. The flexible display of claim 25, wherein the buffer layer comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises striation in the bendable area.

27. The flexible display of claim 25, wherein the buffer layer comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises a thicker portion in the TFT area than the bendable area outside the TFT area.

28. The flexible display of claim 19, further comprising an interlayer dielectric (ILD) between the gate electrode of the TFT and the source/drain of the TFT.

29. The flexible display of claim 28, wherein the ILD comprises a sublayer of silicon oxide and a sublayer of silicon nitride, wherein the silicon nitride comprises a striation pattern in the bendable area outside the TFT area.

30. The flexible display of claim 28, wherein the ILD layer is present in the TFT area and absent outside the TFT area.

31. The flexible display of claim 19, further comprising a passivation disposed over the source electrodes and drain electrodes of the TFTs.

32. The flexible display of claim 31, wherein the passivation layer comprises a flexible organic material.

33. The flexible display of claim 19, wherein the flexible substrate comprises polyimide.

34. The flexible display of claim 19, wherein the stretchable portion of the at least one of the first plurality of metal lines and the second plurality of metal lines further comprises a first stretchable portion interleaved or overlapped with a second stretchable portion as a redundant.

35. The flexible display of claim 34, wherein the first stretchable portion is formed from the first metal for the gate electrode and gate line, and the second stretchable portion is formed from the second metal for the drain and source and data line.

36. The flexible display of claim 34, wherein the first stretchable portion and the second stretchable portion are connected at least one location outside the TFT area.

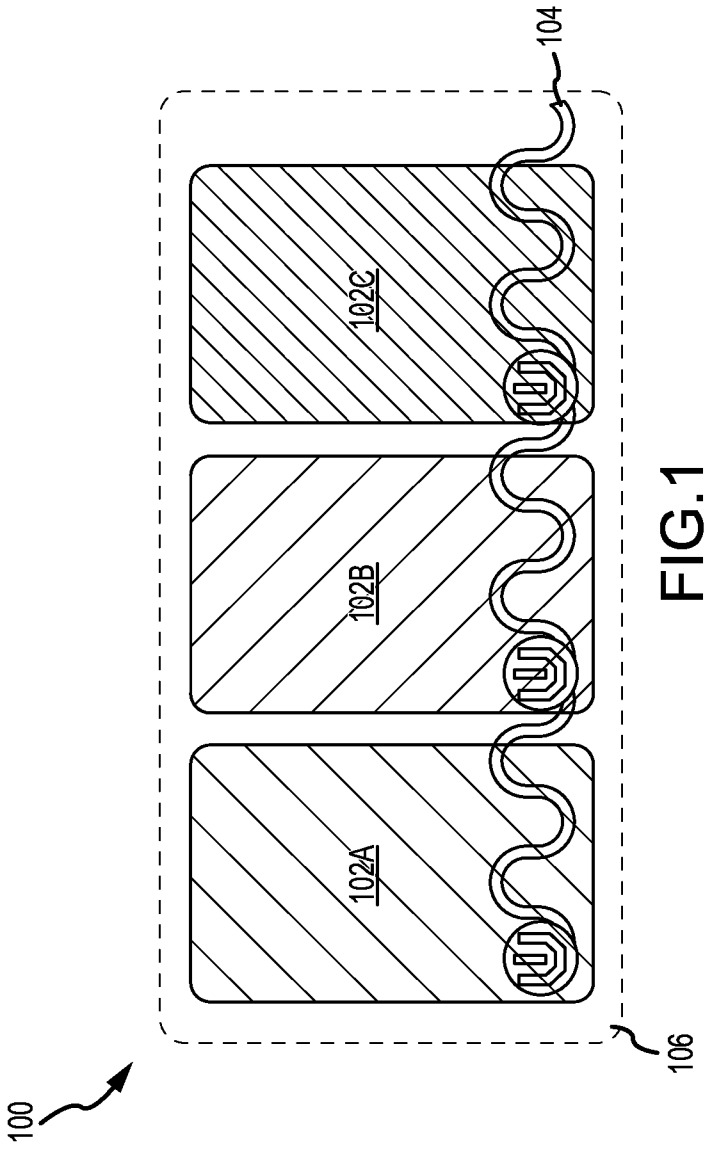

FIG.1

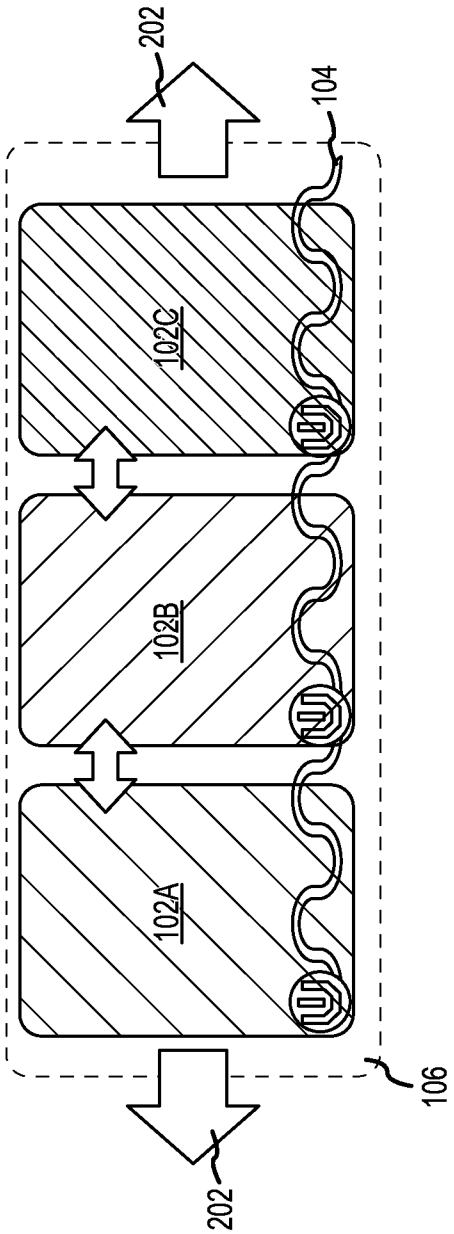

FIG.2

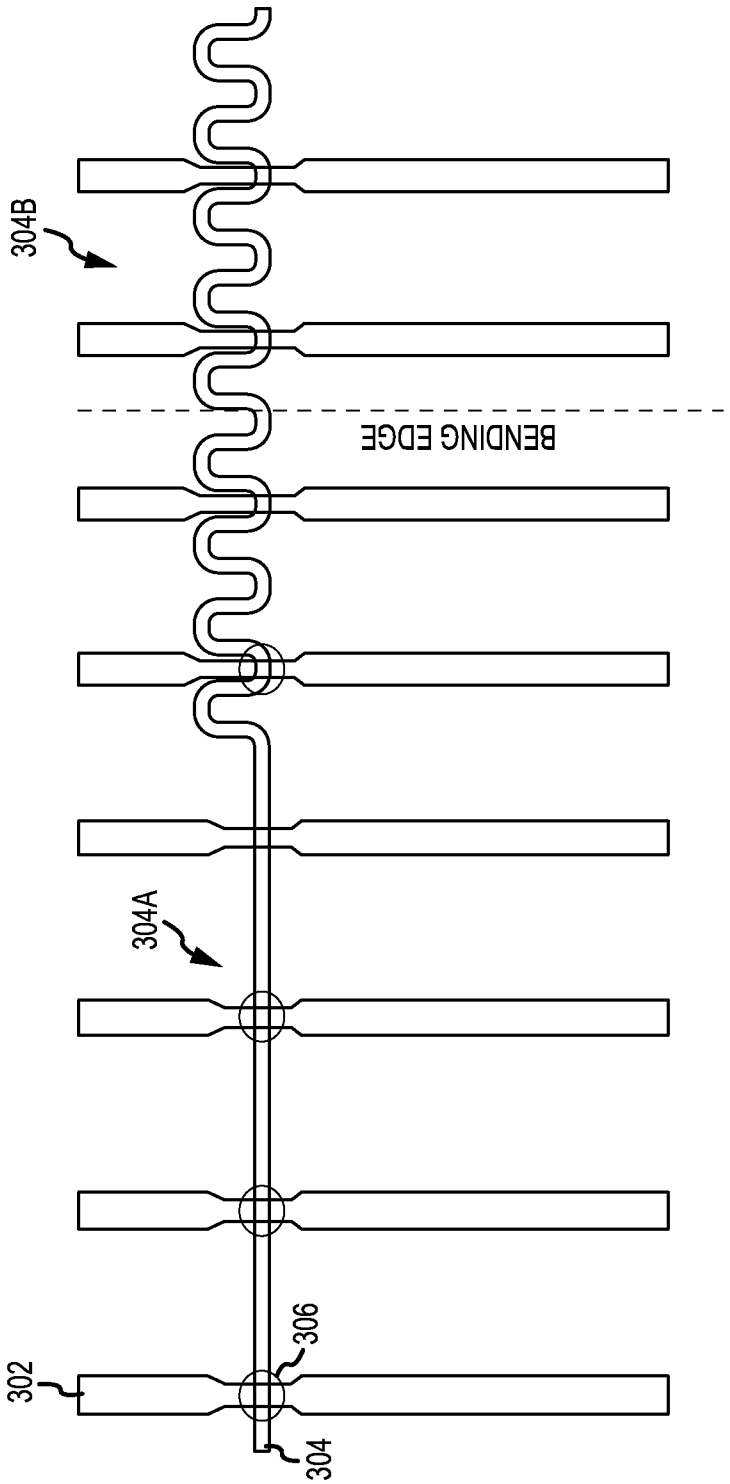

FIG.3

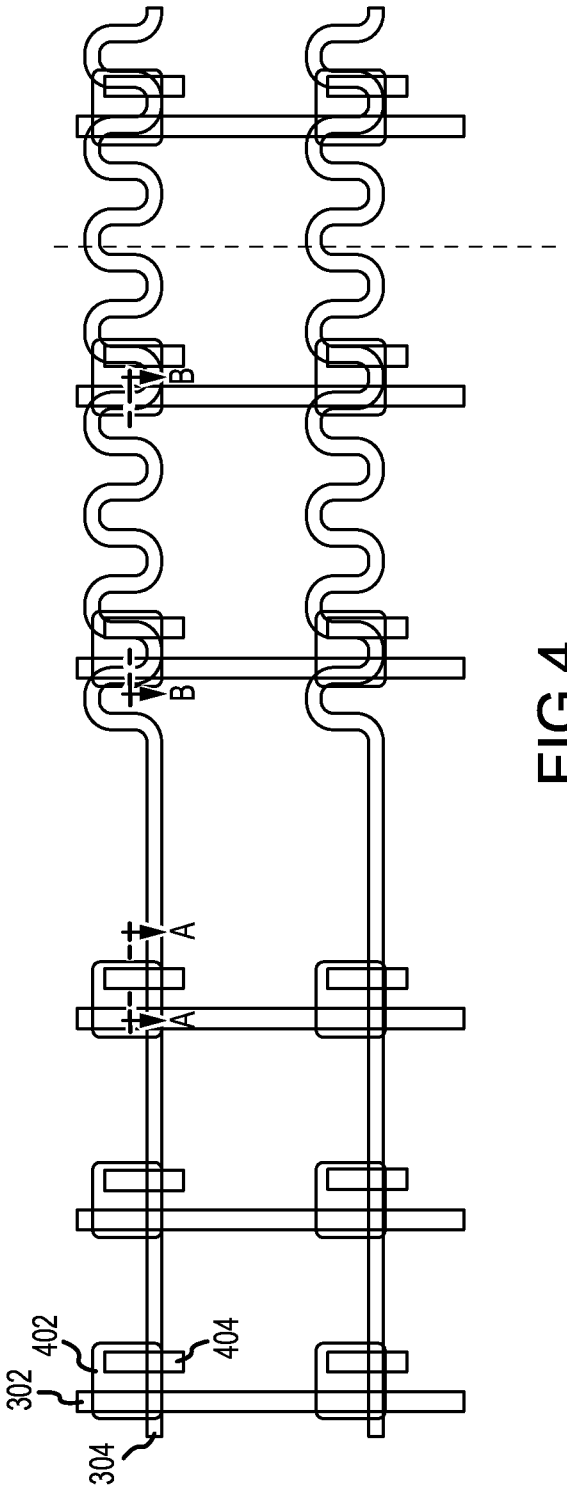

FIG.4

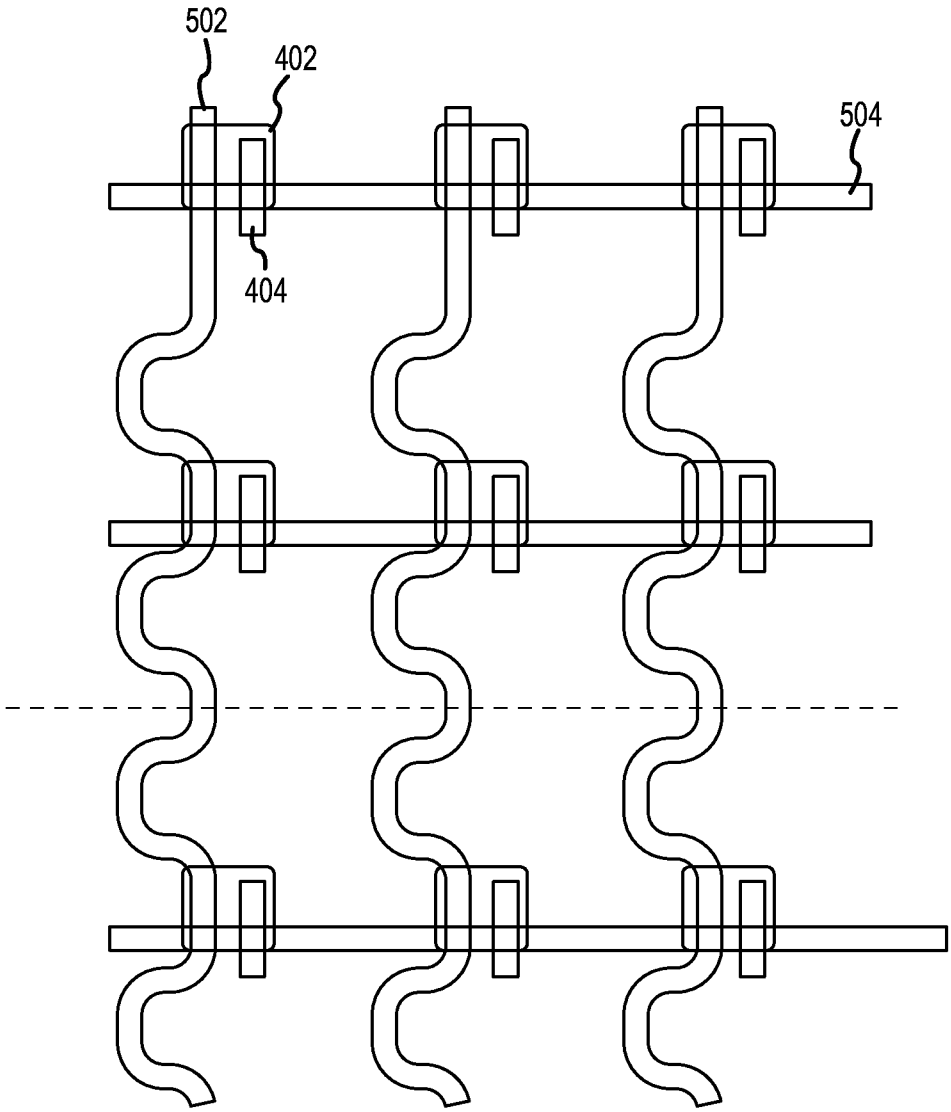

FIG.5

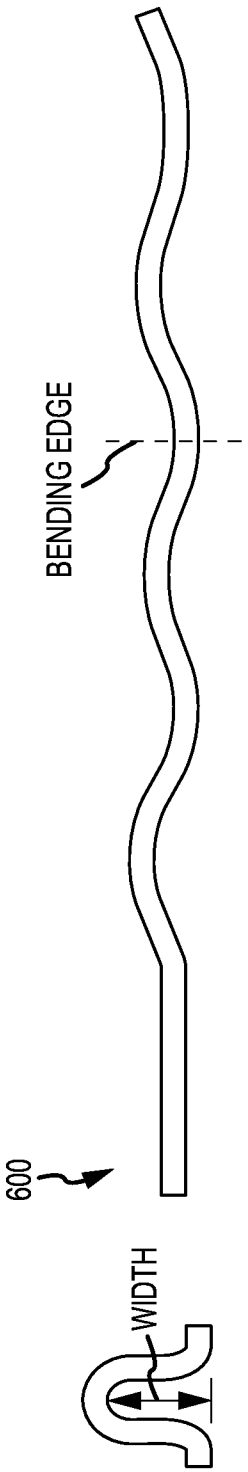

FIG.6

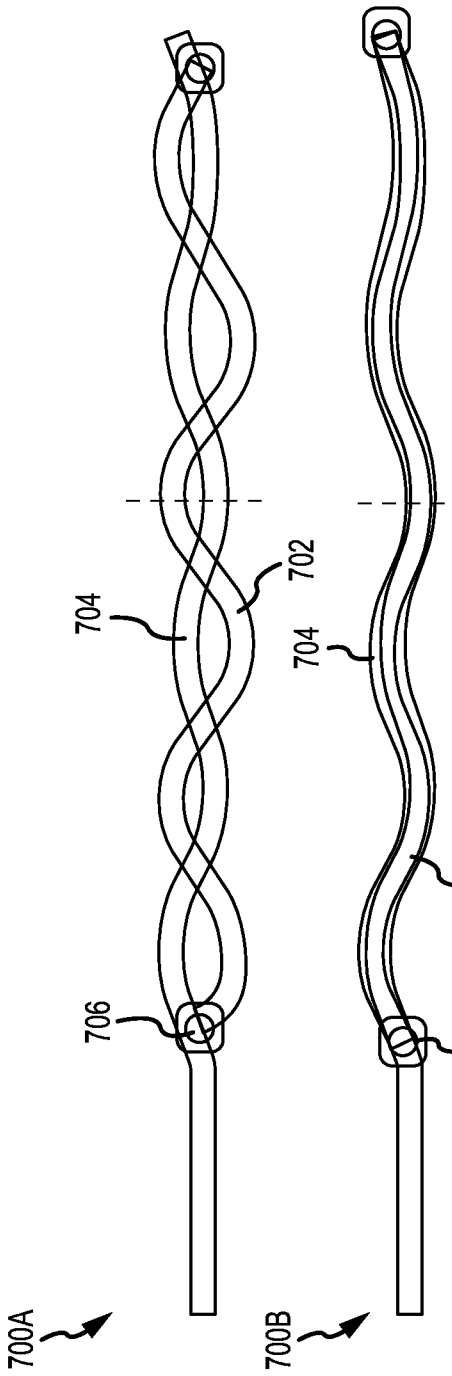

FIG.7

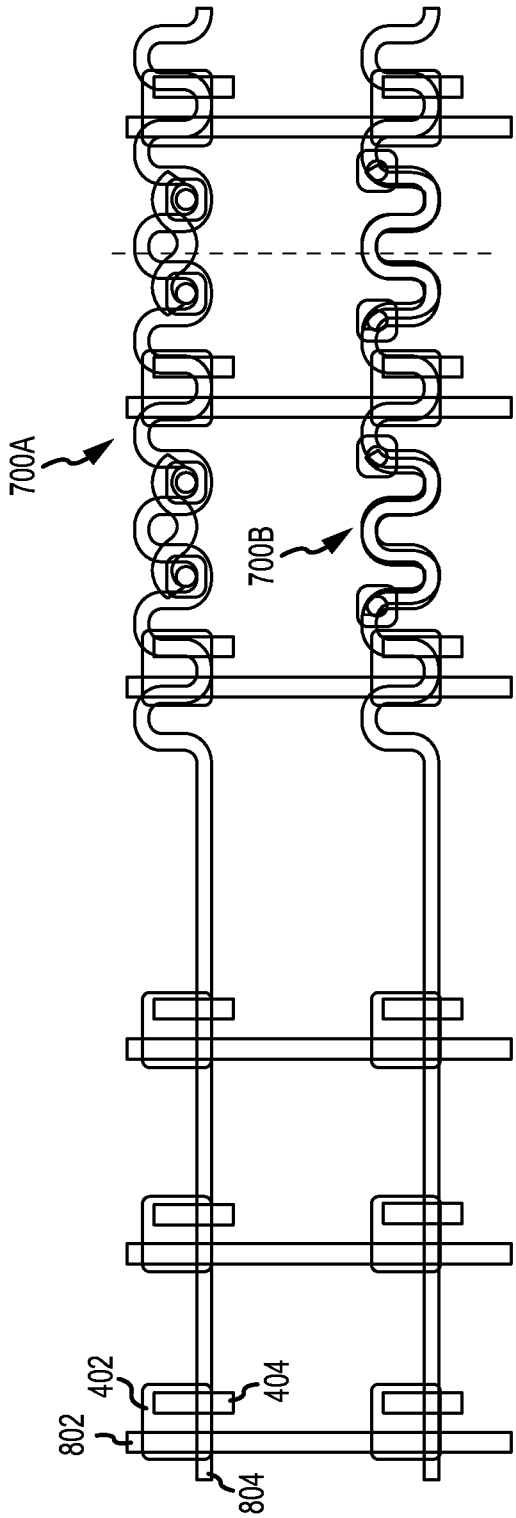

FIG.8

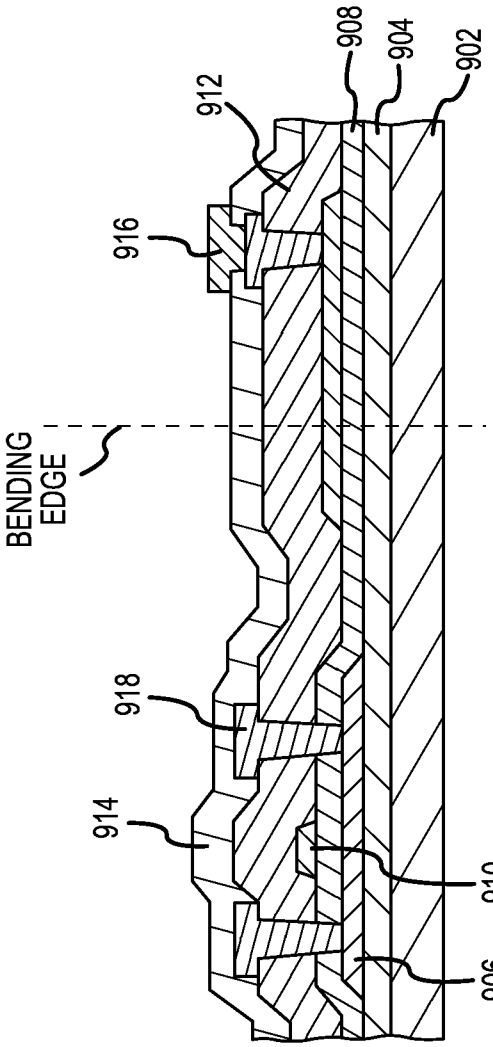

FIG.9

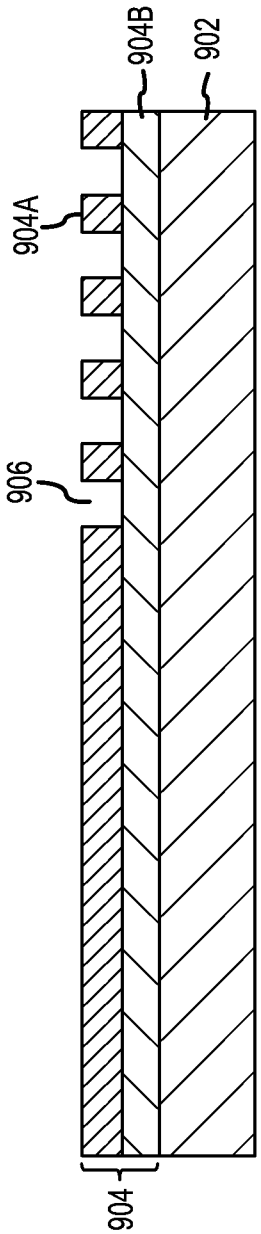

FIG.10

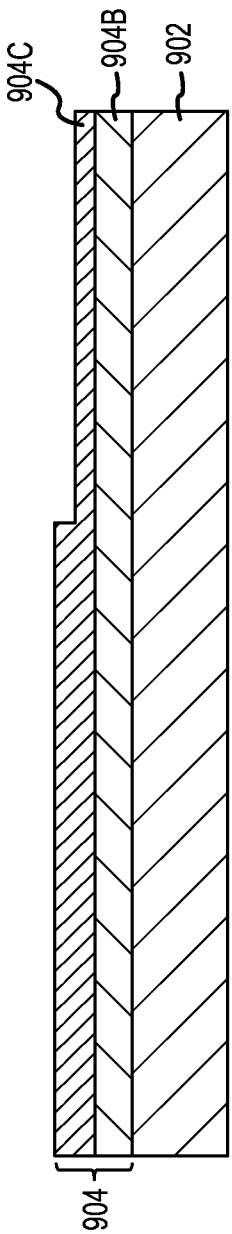

FIG.11

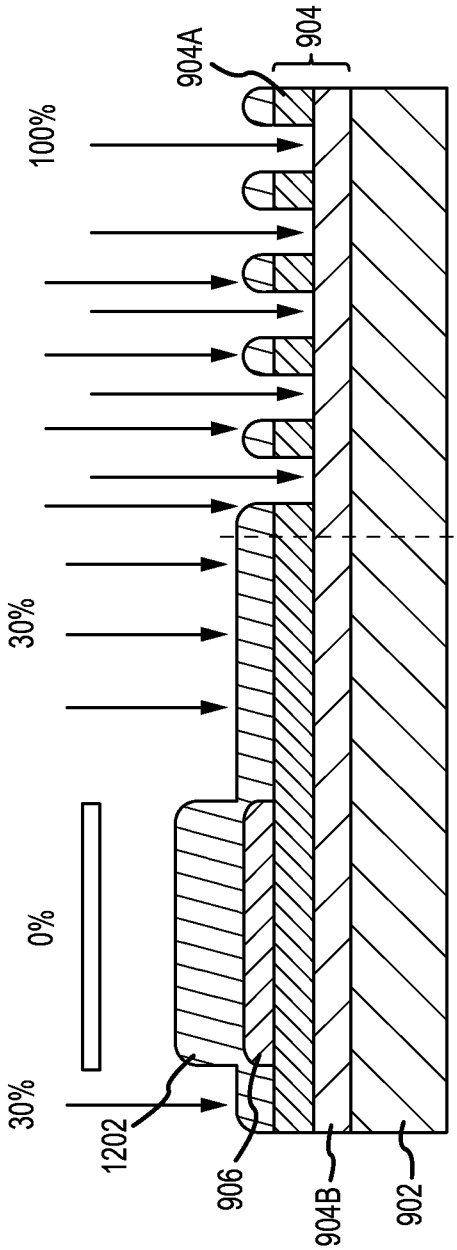
904A
904
100%
30%
0%
30%
1202
906
904B
902

FIG.12

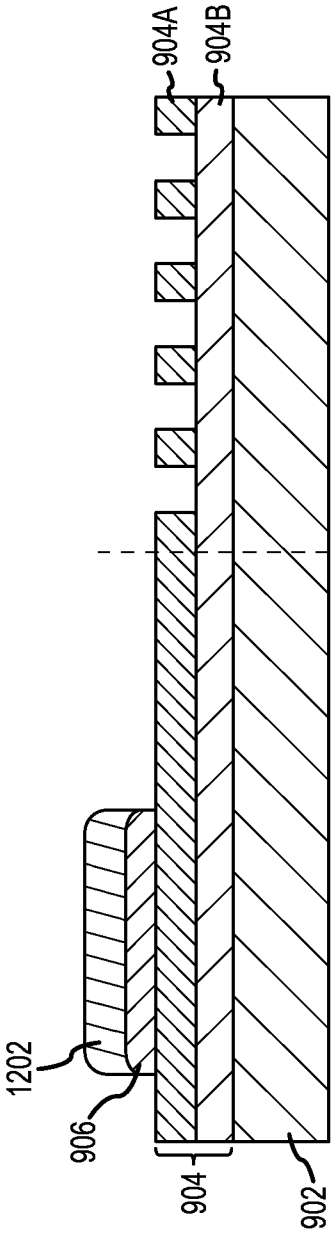
904A
904B
1202
906
904
902

FIG.13

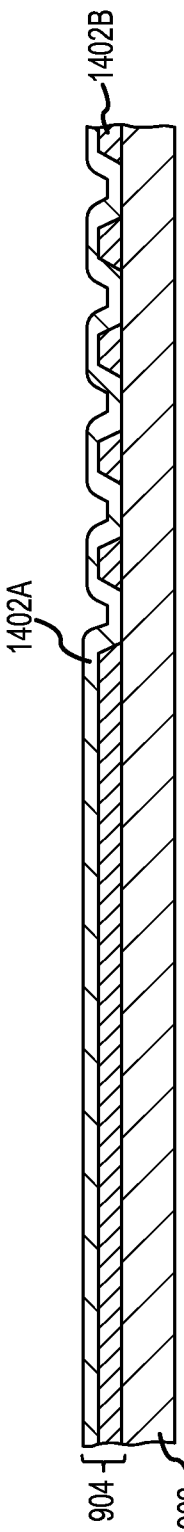

FIG.14

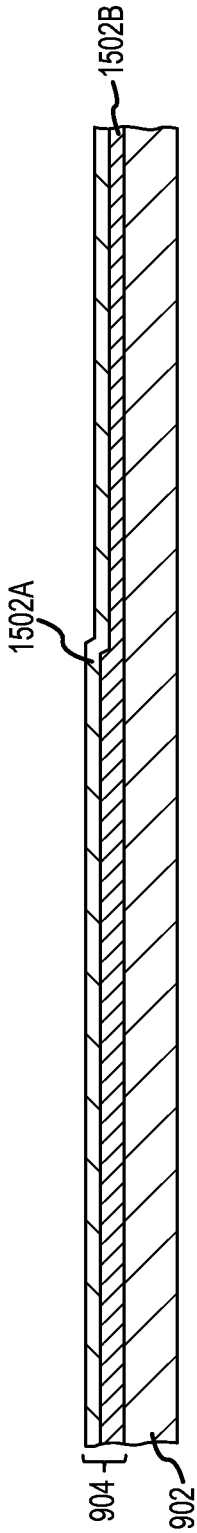

FIG.15

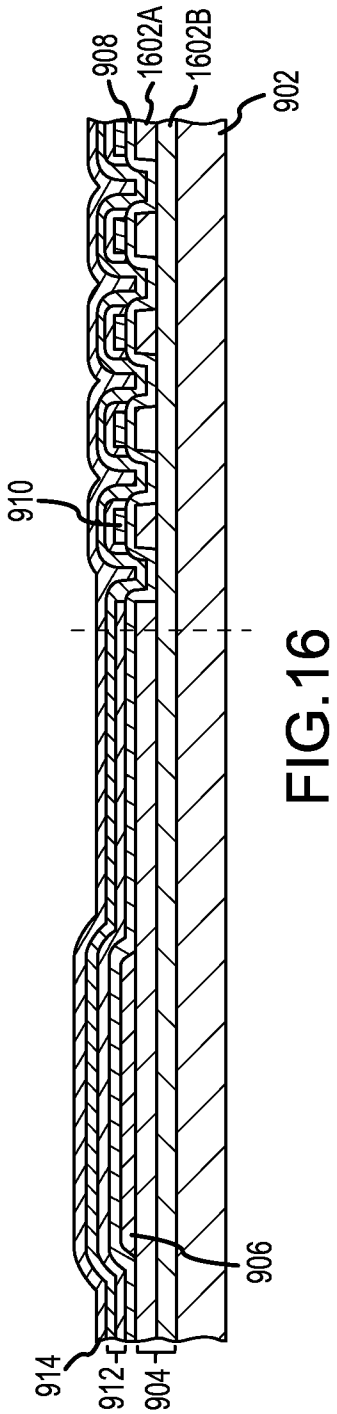
908
1602A
1602B
902
910
906
914
912
904

FIG.16

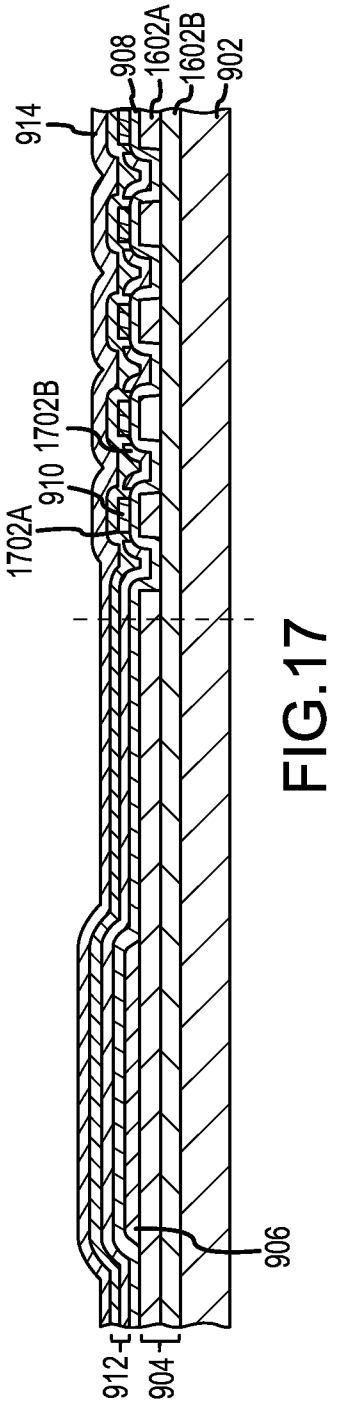
914
908
1602A
1602B
902
1702B
910
1702A
906
912
904

FIG.17

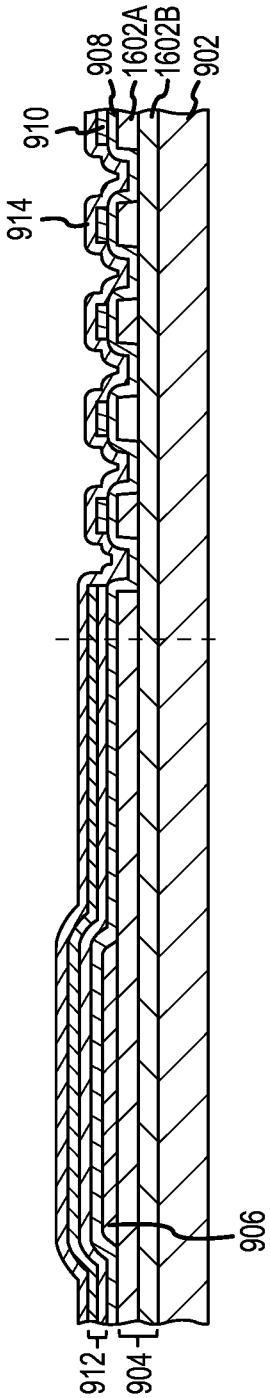

FIG.18

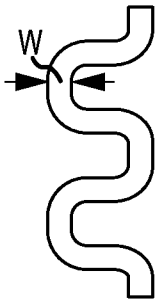

FIG.19A

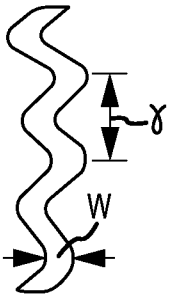

FIG.19B

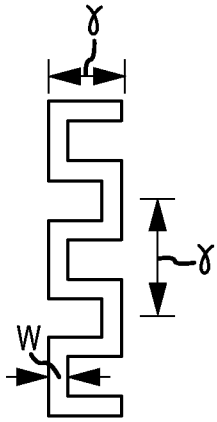

FIG.19C

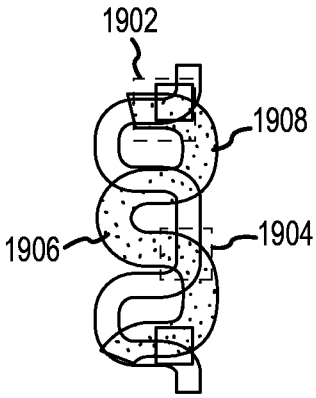

FIG.19D

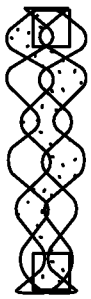

FIG.19E

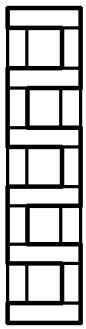

FIG.19F

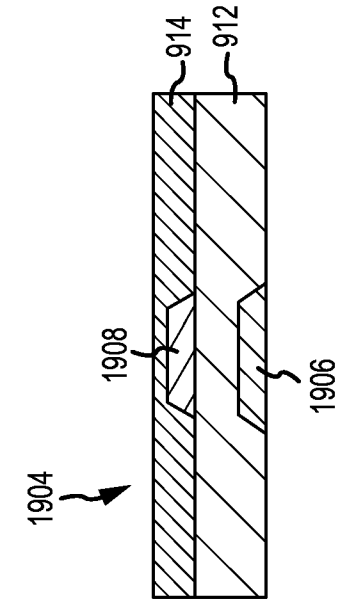

FIG.19H

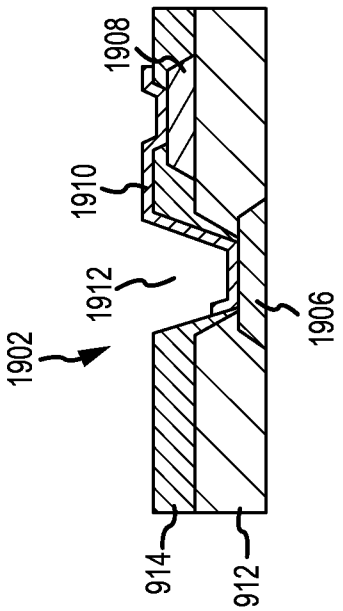

FIG.19G

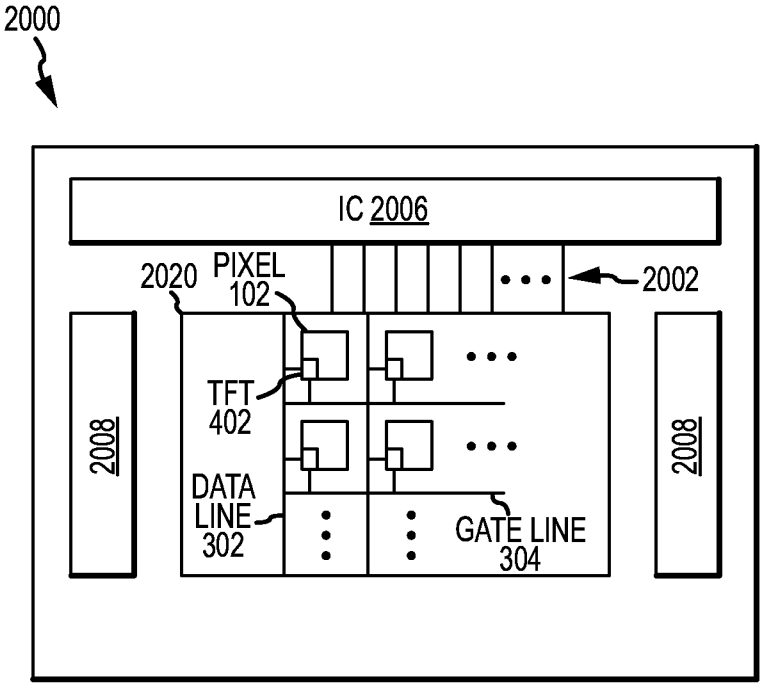

FIG.20A

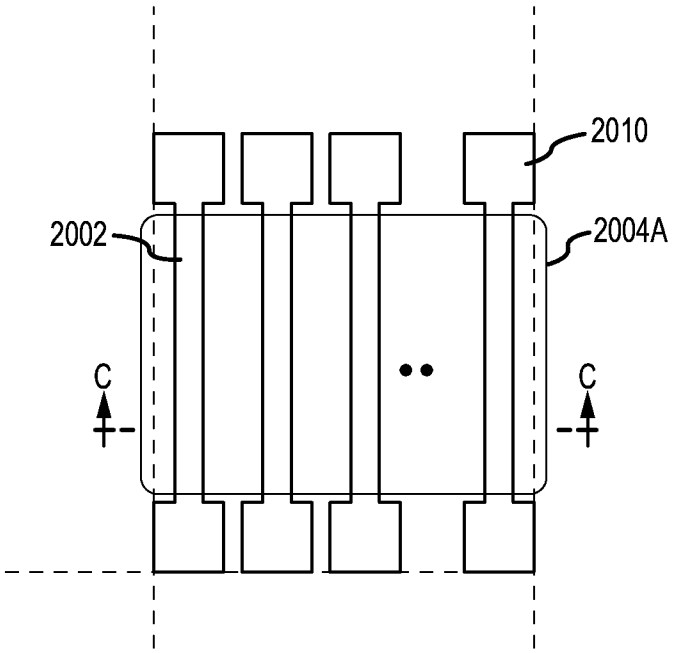

FIG.20B

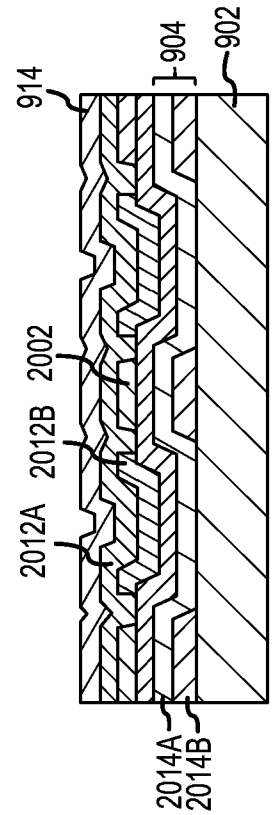

FIG.21C

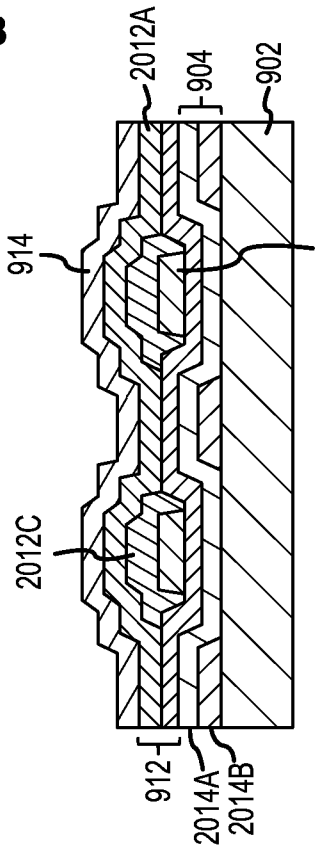

FIG.21D

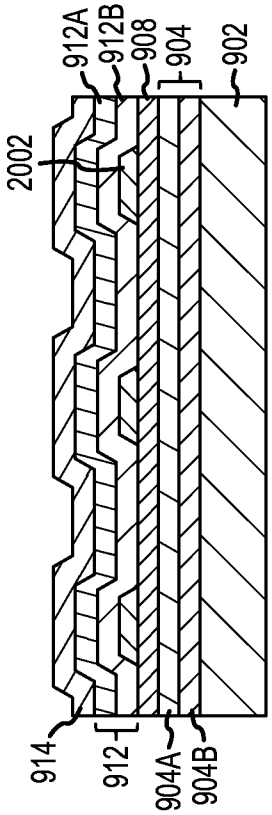

FIG.21A

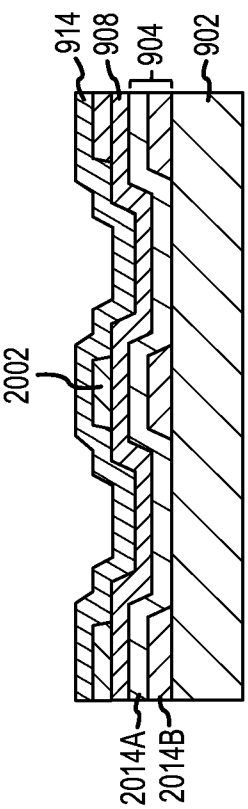

FIG.21B

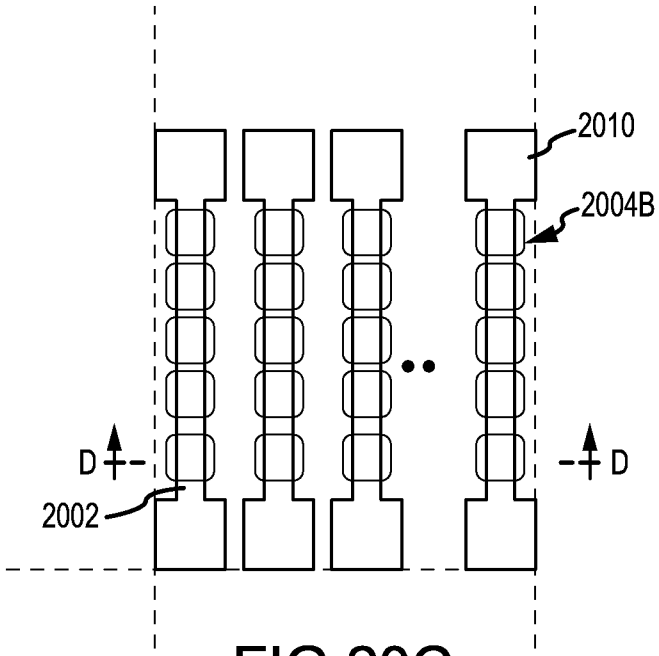

FIG.20C

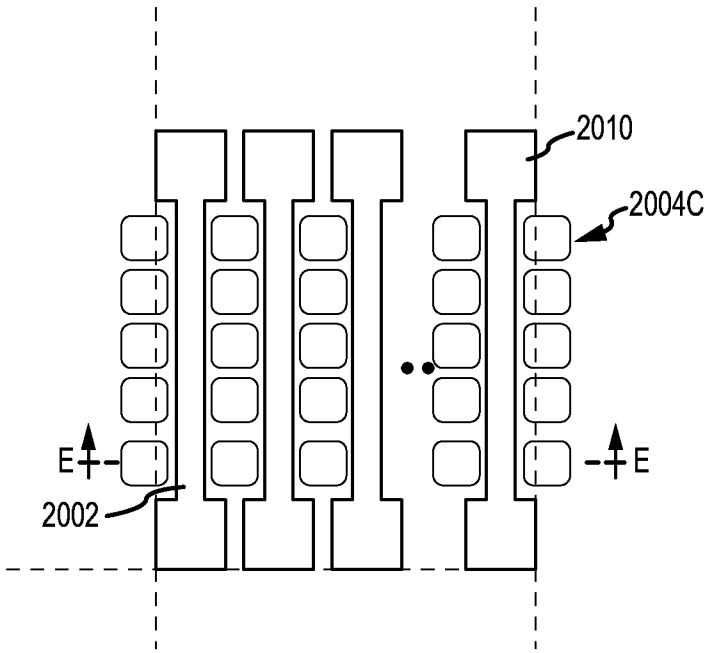

FIG.20D

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/066156

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L27/12
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G02F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2009/051640 A1 (TANAKA MASAHIRO [JP] ET AL) 26 February 2009 (2009-02-26) paragraph [0011] paragraph [0013] paragraph [0057] - paragraph [0064]; figure 3 paragraph [0088] - paragraph [0090]; figure 9 paragraph [0102] - paragraph [0106]; figures 14,15	1-7,10, 13-15 8,9,11, 12

Y	EP 2 341 759 A2 (SAMSUNG MOBILE DISPLAY CO LTD [KR] SAMSUNG DISPLAY CO LTD [KR]) 6 July 2011 (2011-07-06) paragraph [0073]	8,9

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 January 2014	06/05/2014

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Hoffmann, Niels

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009/189204 A1 (HEITZINGER JOHN M [US] ET AL) 30 July 2009 (2009-07-30) paragraph [0012] paragraph [0139] - paragraph [0141]	8,9
Y	US 2007/173031 A1 (KODAIRA TAIMEI [JP] ET AL) 26 July 2007 (2007-07-26) paragraph [0050] paragraph [0093] - paragraph [0101] figures 5,7-14	11,12
X	US 2007/019143 A1 (CHEN BO-CHU [TW] ET AL) 25 January 2007 (2007-01-25) the whole document	1-7,10, 12-15
X	US 2007/090420 A1 (CHU FANG-TSUN [TW] ET AL) 26 April 2007 (2007-04-26) the whole document	1,2,4-7, 10-15
A	WO 2011/071198 A1 (KYONGGI UNIVERSITIY INDUSTRY AND ACADEMIA COOPERATION FOUNDATION [KR];) 16 June 2011 (2011-06-16) abstract; figures	1-15
A	US 2006/169989 A1 (BHATTACHARYA RABIN [NL] ET AL) 3 August 2006 (2006-08-03) paragraph [0012] paragraph [0018] - paragraph [0024] paragraph [0081]	1-15
A	KR 100 961 268 B1 (LG PHILIPS LCD CO LTD [KR]) 3 June 2010 (2010-06-03) the whole document	1-15

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2013/066156

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

2-15(completely); 1(partially)

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 2-15(completely); 1(partially)

   Flexible display having non-stretchable metal lines in the TFT areas and stretchable metal lines outside the TFT areas and a silicon nitride sublayer with a striation at the bendable region.

   ---

2. claims: 16-18(completely); 1(partially)

   Flexible display having metal lines redundant stretchable metal lines

   ---

3. claims: 19-36

   Flexible display having buffer layer with a striation pattern outside the TFT area

   ---

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2013/066156

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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KR 100961268 B1	03-06-2010	NONE	