PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3:	A1	(11) International Publication Number: WO 81/00487
H01L 21/324, 21/477		(43) International Publication Date: 19 February 1981 (19.02.81)

(21) International Application Number: PCT/US80/01020

(22) International Filing Date: 7 August 1980 (07.08.80)

(31) Priority Application Number: 065,806

(32) Priority Date: 13 August 1979 (13.08.79)

(33) Priority Country: US

(71) Applicant: NCR CORPORATION [US/US]; World Headquarters, Dayton, OH 45479 (US).

(72) Inventors: TRUDEL, Murray, Lawrence; 2024 Meadow Side Lane, Centerville, OH 45459 (US). DHAM, Vinod, Kumar; Central Park Apartments, Apt. 92, 1055 Manet Drive, Sunnyvale, CA 94087 (US).

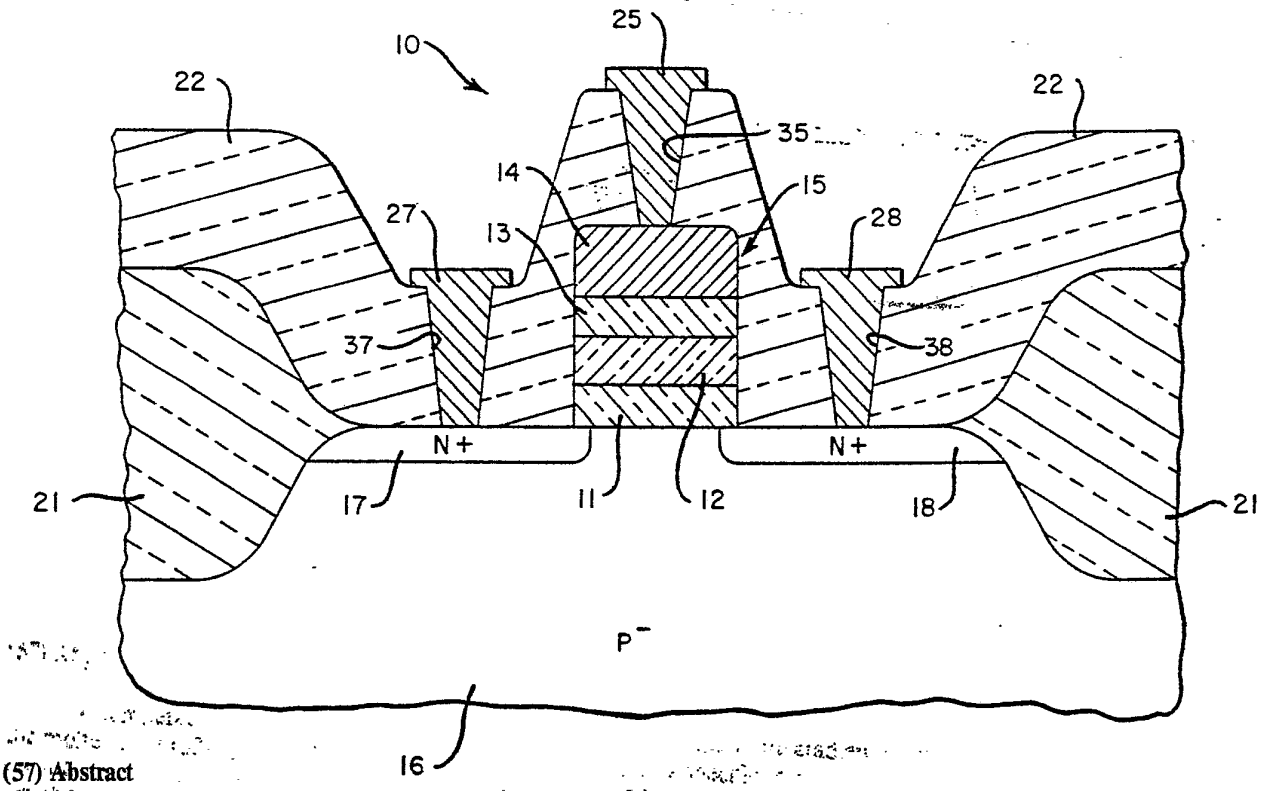
(74) Agents: DALTON, Philip, A., Jr., et al.; Patent Division, NCR Corporation, World Headquarters, Dayton, OH 45479 (US).

(81) Designated States: DE (European patent), GB (European patent), JP, NL (European patent).

Published

With international search report
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments

(54) Title: HYDROGEN ANNEALING PROCESS FOR SILICON GATE MEMORY DEVICE



(57) Abstract

In a method for manufacturing a semiconductor non-volatile SNOS or SONOS memory device having a gate structure which includes a gate oxide layer (11) provided on a semiconductor substrate (16), a nitride layer (12) provided on the gate oxide layer (11) and a polysilicon gate electrode (14) overlying the nitride layer (12), the device is annealed in hydrogen, in an annealing vessel (40), typically for 15-60 minutes at 600-1100°C.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**KP**	Democratic People's Republic of Korea
AU	Australia	**LI**	Liechtenstein
BR	Brazil	**LU**	Luxembourg
CF	Central African Republic	**MC**	Monaco
CG	Congo	**MG**	Madagascar
CH	Switzerland	**MW**	Malawi
CM	Cameroon	**NL**	Netherlands
DE	Germany, Federal Republic of	**NO**	Norway
DK	Denmark	**RO**	Romania
FI	Finland	**SE**	Sweden
FR	France	**SN**	Senegal
GA	Gabon	**SU**	Soviet Union
GB	United Kingdom	**TD**	Chad
HU	Hungary	**TG**	Togo
JP	Japan	**US**	United States of America

HYDROGEN ANNEALING PROCESS FOR SILICON GATE MEMORY DEVICE

Technical Field

This invention relates to processes for manufacturing semiconductor non-volatile memory devices of the kind having a gate structure which includes a gate oxide layer provided on a semiconductor substrate, a nitride layer provided on said gate oxide layer and a polysilicon gate electrode overlying said nitride layer.

Background Art

Before discussing the background art, it is convenient to note the following four definitions of terms used in the present specification:

"SNOS" is silicon (polysilicon)-nitride-oxide-semiconductor.

"SONOS" is silicon (polysilicon)-oxide-nitride-oxide-semiconductor.

"Gate oxide" refers to the silicon oxide dielectric formed between the semiconductor and the silicon nitride (SNOS, SONOS) in the active area of a device such as a capacitor or field-effect transistor.

"Interfacial oxide" refers to the silicon oxide layer formed between the polysilicon and the silicon nitride dielectric in SONOS structures.

Retention and endurance are two very important characteristics of thin gate oxide, nitride non-volatile memory devices. Retention is a measure of the ability of the memory device to retain its stored charge subsequent to a write or erase operation. Endurance is a measure of the retention of the memory device as a function of the number of write-erase cycles to which the device has been subjected.

In the fabrication of thin-oxide nitride non-volatile memory structures, it is important to keep the temperature of post-nitride deposition processing to a

minimum, since high temperature processing of the memory oxide-nitride structure degrades the retention and endurance characteristics. High temperature processing is considered to be that at a temperature substantially higher than the nitride deposition temperature.

With respect to the fabrication of (n-channel) SNOS/SONOS silicon gate non-volatile memory devices, the memory nitride, which can be deposited at a temperature of about 700°C.-750°C., is subjected to subsequent high temperature processing at, for example, 900°C. to 1000°C., which degrades memory characteristics such as retention and endurance. This high temperature processing includes for example, the high temperature (900°C.) phosphorus diffusion step used in doping source, drain and polysilicon gates and oxidation of the polysilicon at 900°C.-1000°C. for generating masking oxide.

Because of this susceptibility to high temperature post-nitride deposition processing, silicon gate memory structures frequently have relatively low retention and endurance as compared to metal gate structures (such as aluminum or aluminum alloy metal gate structures). This characteristic is discussed in an article by Peter C. Y. Chen entitled "Threshold-Alterable Silicon Gate MOS Devices", IEEE Transactions on Electron Devices Vol. ED-24, No. 5, May, 1977, Page 584-86. The article relates to improved SONOS structures and discusses the relatively poor retention of silicon gate structures: for example, Chen indicated that 15 Angstrom thick gate oxide provides retention measured in years in typical MNOS structures, but only in hours in SONOS structures. Chen increased the retention of his SONOS devices by increasing the thickness of the gate oxide to 30 Angstroms. However increasing the gate oxide thickness has the disadvantage of slowing write and erase speeds.

Disclosure of the Invention

It is an object of the present invention to

provide a process for manufacturing a semiconductor non-volatile memory device of the kind specified having improved retention and endurance (or, equivalently, a reduced rate of closure of the memory window) without unduly sacrificing other performance characteristics.

Therefore, according to the present invention, there is provided a process for manufacturing a semiconductor non-volatile memory device of the kind specified, characterized by the steps of loading the device into an annealing vessel, raising the temperature of the vessel to within the range 600-1100°C. in hydrogen ambient, maintaining the temperature and hydrogen ambient for a sufficient time to anneal the device, and reducing the temperature of the vessel to about 100°C. or less while maintaining the hydrogen ambient.

Brief Description of the Drawings

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a cross-sectional representation of a silicon gate memory device which can be fabricated using the hydrogen anneal of the present invention.

Fig. 2 is a schematic representation of apparatus for hydrogen annealing devices using the method of the present invention.

Fig. 3 is a graphical represention of the retention and endurance characteristics of unannealed SONOS devices.

Fig. 4 is a graphical representation of the retention and endurance characteristics of SONOS devices which have been hydrogen annealed using the method of the present invention.

Best Mode for Carrying Out the Invention

Hydrogen annealing has been found to be effective in improving the memory characteristics of

both SNOS and SONOS memory device structures. A cross section of a fabricated n-channel SONOS memory transistor 10 is shown in Fig. 1. The difference between an SNOS device (not shown) and the illustrated SONOS device 10 is the absence in the SNOS device of the interfacial oxide layer 13. The invention will be described with reference to the SONOS device 10, keeping in mind that it is applicable to SNOS devices as well. Also, the illustrated transistor 10 is formed by the well-known LOCOS (localized oxidation of silicon) process, although certainly the invention is not limited to this process.

Typically, in forming the SONOS transistor 10, source 17 and drain 18 are formed in p^- silicon substrate 16 by n-type impurities such as phosphorus (or p-type impurities such as boron for p-channel) using diffusion or ion implantation techniques. Field oxide 21 can be formed by wet thermal oxidation of the substrate 16, to a typical thickness of 14kA to 16kA (14,000 to 16,000 Angstroms). Memory gate oxide 11 of thickness 10-30 Angstroms is preferably formed by dry thermal oxidation, typically within the approximate range 600-750°C. in an oxygen-nitrogen ambient. The memory memory nitride 12 can be deposited by the chemical vapor deposition technique in a vertical reactor at a temperature of about 700-750°C. using an ammonia-silane-nitrogen ambient, to a thickness of about 350-550 Angstroms.

Interfacial oxide 13 may be formed by several methods, for example by high temperature (975°C.) wet oxygen thermal conversion of a portion of the top layer of the memory silicon nitride 12 to oxide 13. Interfacial oxides 13 of 70-150 Angstroms thickness have been used.

Polysilicon gate 14 can be deposited by either the atmospheric CVD (Chemical Vapor Deposition) or low pressure CVD technique over the temperature range

600-700°C. in SiH_4-N_2 and SiH_4 ambients, respectively, to a thickness of 3kA-5kA. Oxide isolation layer 22 is a low temperature (425°C), deposited oxide 6kA° to 12kA° in thickness.

Subsequent to the polysilicon deposition, the memory silicon nitride 12 is subjected to the high temperature (900°C.) phosphorus diffusion step used in doping source, drain and polysilicon gates. Optionally, the nitride may also be subjected to a 1000°C. doped oxide reflow step in a nitrogen ambient.

Subsequent to this high temperature processing, the SONOS transistor 10 is subjected to the hydrogen anneal of this invention, as described below, to enhance retention and endurance. The hydrogen anneal is performed after opening contact windows such as 35, 37 and 38, etc. in the oxide isolation layer 22 using standard photolithographic masking and etching techniques. After the anneal, contacts 25, 27 and 28 of material such as aluminum are formed using standard metallization techniques.

Referring to Fig. 2 there is shown a vertical reactor system 40 for practicing the hydrogen anneal of of the present invention. The system comprises a vessel such as a glass bell jar 41, a graphite susceptor 42 for holding the devices 10, cooling (water and rf heating coil) 43, and gas inlet tube 44. Gas, here N_2 and H_2, is supplied via tube 44 to the vessel from pressurized sources such as tanks 46 and 47. The gas mixture and flow rate are controlled by valves 48, 49 and 51. Valves 48 and 49 can be used to control the relative proportions of hydrogen and nitrogen in the mixture, and valve 51 to control the gas flow rate. Gas flow rate is indicated by meter 52.

A suitable hydrogen anneal process comprises:

1. loading the silicon gate transistor 10 onto the susceptor 42 of the reactor 40;
2. purging the reactor with nitrogen,

e.g., for five minutes, typically at or near room temperature (valves 48 and 51 open; valve 49 closed);

3. purging the reactor with hydrogen, e.g., for, five minutes, typically at room temperature (valves 49 and 51 open; valve 48 closed);

4. activating the rf coil 43 to raise the temperature of the reactor to the desired annealing temperature (within the approximate range 600-1100°C.) within a time span of about five minutes in the presence of hydrogen (valves 49 and 51 open; valve 48 closed);

5. maintaining the hydrogen flow and the temperature for a predetermined time (typically within the range 15-60 minutes) to anneal the silicon gate transistor 10;

6. shutting off the rf coil 43 to allow the silicon gate transistor 10 to cool to the approximate range 24°C. (room temperature)-100°C. in the hydrogen flow; and

7. terminating the hydrogen flow and removing the silicon gate transistor 10 from the reactor 40.

Although not critical, prior to step 1 (the loading step) it may be advantageous to pre-condition (clean) the bell jar 41 by heating to about 900°C. and maintaining the temperature for about 15 minutes in the presence of nitrogen (flow rates of about 48 liters/min. have been used), then shutting off the temperature and gas flow.

It is important that the silicon wafer 16 from which the device is fabricated be in a 100% hydrogen ambient when the temperature is raised from room temperature to the annealing temperature during step 4, and when the temperature is lowered from 800°C. during step 6 to avoid negating the beneficial effects of the hydrogen anneal. Finally, it is noted that the an-

nealing vessel and system are not restricted to the particular vertical reactor 40 or to a vertical reactor at all: for example, a furnace tube (not shown) with suitable safety precautions should constitute a suitable annealing chamber.

Examples

The retention and endurance characteristics of unannealed SONOS devices and hydrogen-annealed SONOS devices 10 are shown in Figs. 3 and 4, respectively. Referring again to Fig. 1, the devices comprised the n-channel silicon gate field-effect transistors 10 described previously. The transistors were formed in accordance with the exemplary procedures described above. The substrate 16 was <100> p-type, 15-20 ohm-cm silicon. The field oxide 21 was about 15kA thick as grown; oxide 22 was about 6kA thick. The approximate dimensions of the gate structure 15 are 10-15 Angstroms for the gate memory oxide 11; 500 Angstroms for the gate memory nitride 12; 70 Angstroms for the interfacial oxide 13; and 3.5kA for the polysilicon gate 14. After forming contact windows as needed in oxide 22, selected devices were annealed as described above in accordance with the principles of this invention. The anneal temperature was 800°C.; the hydrogen flow rate was 48 liters/min. (steps 4, 5 and 6). Then, all samples, both annealed and unannealed, received metal contacts 25, 27, and 28. The metallization was 14kA° thick aluminum. The parts were packaged in metal cans to facilitate handling and testing and avoid interaction with the ambient.

The retention-endurance data of Figs. 3 (unannealed) and 4 (annealed) were obtained by: (1) initializing the FETs by determining the initial written (or "1") and erased (or "0") threshold voltages V_T; (2) generating uncycled retention-curves by storing the devices at an elevated temperature (125°C) for the times

shown in Figs. 3 and 4 and determining the threshold voltages at intervals during this time; (3) write-erase cycling the FETs 10^5 times; (4) reinitializing the FETs per step 1; (5) and generating retention curves for the 10^5 cycles by again storing at elevated temperature per step 2.

The initialization procedure (steps 1 and 4), i.e. obtaining the initial written and erased state threshold voltages, involved applying +25 volts for three seconds and -25 volts for three seconds, respectively, at room temperature to the gates of the memory FETs. Source, drain and substrate were all tied to ground during this initialization.

Write-erase cycling (step 3) was done at room temperature using an applied gate voltage of $\pm$ 25 volts and a 10 millisecond pulse width for both polarities. The source, drain and substrate were all tied to ground during the write-erase cycling.

The storage-at-temperature data for the uncycled and cycled parts (steps 2 and 5) were obtained by first placing the packaged parts in an oven at 125°C. in an air ambient to accelerate charge decay. The parts were removed from the oven at various time intervals and the gate voltage (V_T) required for a 20 microamp drain-source current (I_{DS}) was measured and recorded at room temperature. The decay of the stored charge, or equivalently, the rate of threshold voltage window closure as a function of log time for the unannealed and annealed SONOS transistors 10 is shown in Figs. 3 and 4.

The main features of Figs. 3 and 4 are presented in Table I.

TABLE I

SONOS

Retention, Endurance Characteristics

Hydrogen Anneal (Fig.)	Write-Erase Cycles	Window @1 hr, W_1 (Volts)	Window @100 hr, W_2 (Volts)	Window Decay Rate $\Delta W=(W_1-W_2)$/Decade (Volts per Decade)	Normalized Window Closure $\Delta W/W_1$
No (Fig. 3)	Uncycled	6.4	4.0	1.2	0.19
	10^5	4.9	2.3	1.3	0.26
Yes(Fig. 4)	Uncycled	5.7	4.5	0.6	0.11
	10^5	6.4	5.1	0.65	0.10

The absolute threshold voltage decay rates are significantly improved for the hydrogen annealed devices as compared to the non-annealed parts. More importantly, the normalized threshold voltage window closure is lower for the hydrogen annealed parts than for the non-annealed parts.

It has thus been shown that hydrogen annealing of SNOS/SONOS process devices significantly improves retention and endurance. It is likely that the high temperature processing which the memory gate silicon nitride 12 is subjected to during the fabrication of the memory structure 15 alters the physical and/or chemical characteristics of the silicon nitride in such a way as to degrade the memory characteristics. Annealing in a hydrogen ambient at least partially restores the memory device to its original memory characteristics.

Although the memory gate nitride layer 12 was deposited in a vertical reactor at atmospheric pressure, it is expected that the beneficial effects of hydrogen annealing should also be manifested by memory nitride layers deposited by other techniques, for example, low pressure CVD nitride layers.

Finally, it should be noted that the improved memory characteristics obtained with the pure memory SONOS transistors 10 should be equally valid for the split gate and trigate memory structures taught in U.S. Letters Patent No. 3,719,866 issued March 6, 1973 to Naber and Lockwood and assigned to NCR. Also, the improved memory characteristics are applicable to all silicon gate structures to which gate structure 15 is applicable, and includes capacitor structures as well as transistor structures.

CLAIMS:

1. A process for manufacturing a semiconductor non-volatile memory device having a gate structure which includes a gate oxide layer (11) provided on a semiconductor substrate (16), a nitride layer (12) provided on said gate oxide layer (11), and a polysilicon gate electrode (14) overlying said nitride layer (12), characterized by the steps of loading the device into an annealing vessel (40), raising the temperature of the vessel to within the range 600-1100°C. in hydrogen ambient, maintaining the temperature and hydrogen ambient for a sufficient time to anneal the device, and reducing the temperature of the vessel to about 100°C. or less while maintaining the hydrogen ambient.

2. A process according to claim 1, characterized in that said step of raising the temperature is effected within a time span of about five minutes.

3. A process according to claim 1, characterized in that the maintained temperature of the vessel (40) is about 800°C.

4. A process according to claim 3, characterized in that the temperature and hydrogen ambient are maintained for about 30 minutes.

5. A process according to claim 4, characterized in that said hydrogen ambient is provided at a flow rate of about 48 litres/minute.

6. A process according to claim 1, characterized in that prior to said step of loading the device into the annealing vessel (40), said vessel (40) is temporarily heated to about 900°C. in a nitrogen ambient for about 15 minutes.

7. A process according to claim 1, characterized in that subsequent to said step of loading the device into the annealing vessel (40) the vessel (40) is purged with nitrogen for about five minutes and then purged with hydrogen for about five minutes.

8. A process according to claim 1, characterized in that prior to said step of loading the device into the annealing vessel (40), there are effected the steps of forming a thick isolation oxide layer (22) over the device and forming contact windows (35, 37, 38) in said thick isolation oxide layer.

9. A process according to claim 8, characterized in that after said step of reducing the temperature there is effected the step of forming a patterned conductor array (25, 27, 28) on the device.

10. A process according to claim 1, characterized in that said device is a SONOS device or a SNOS device.

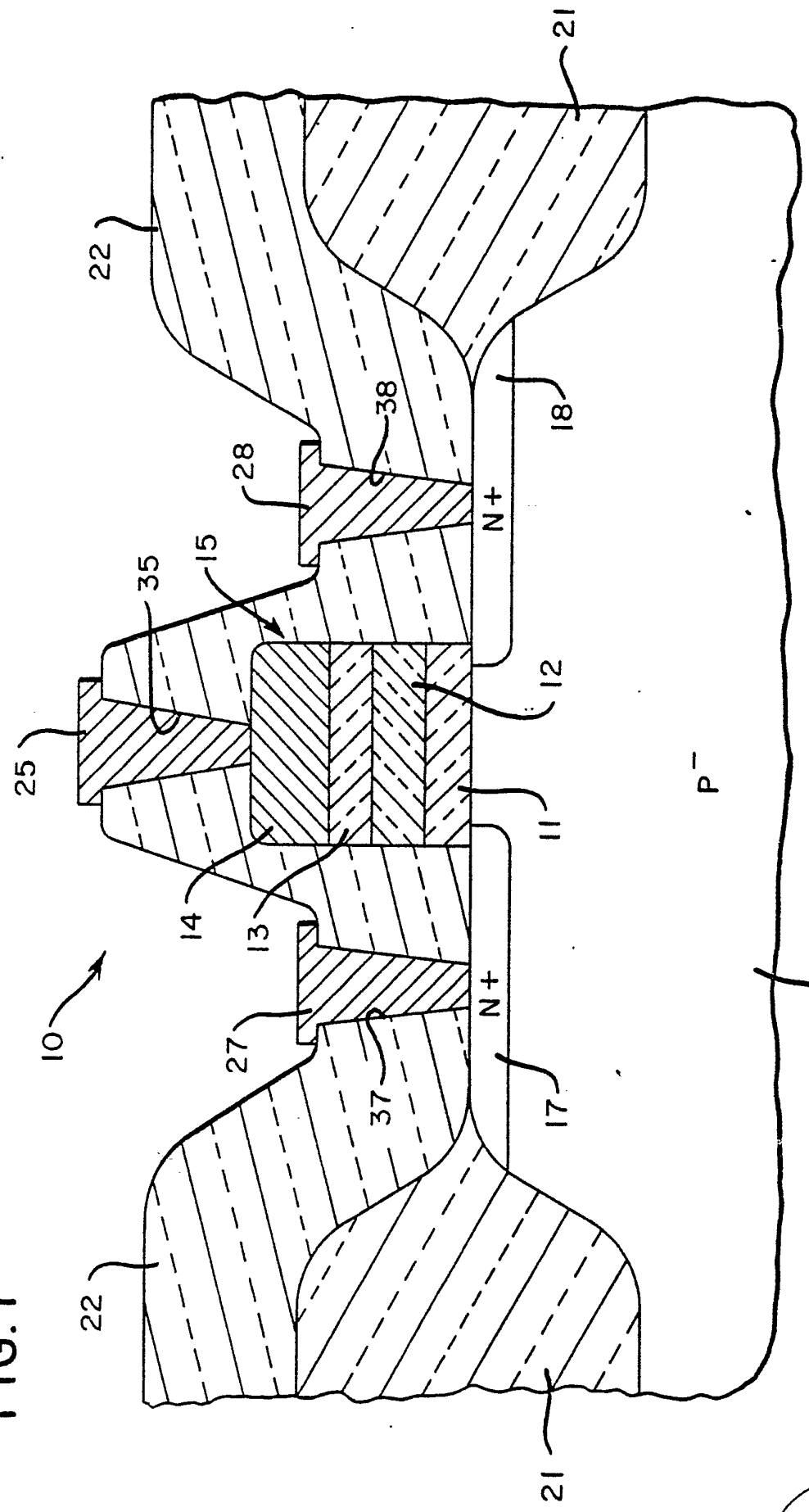


FIG. 1

FIG.2

REACTOR CHAMBER USED FOR H_2-ANNEAL

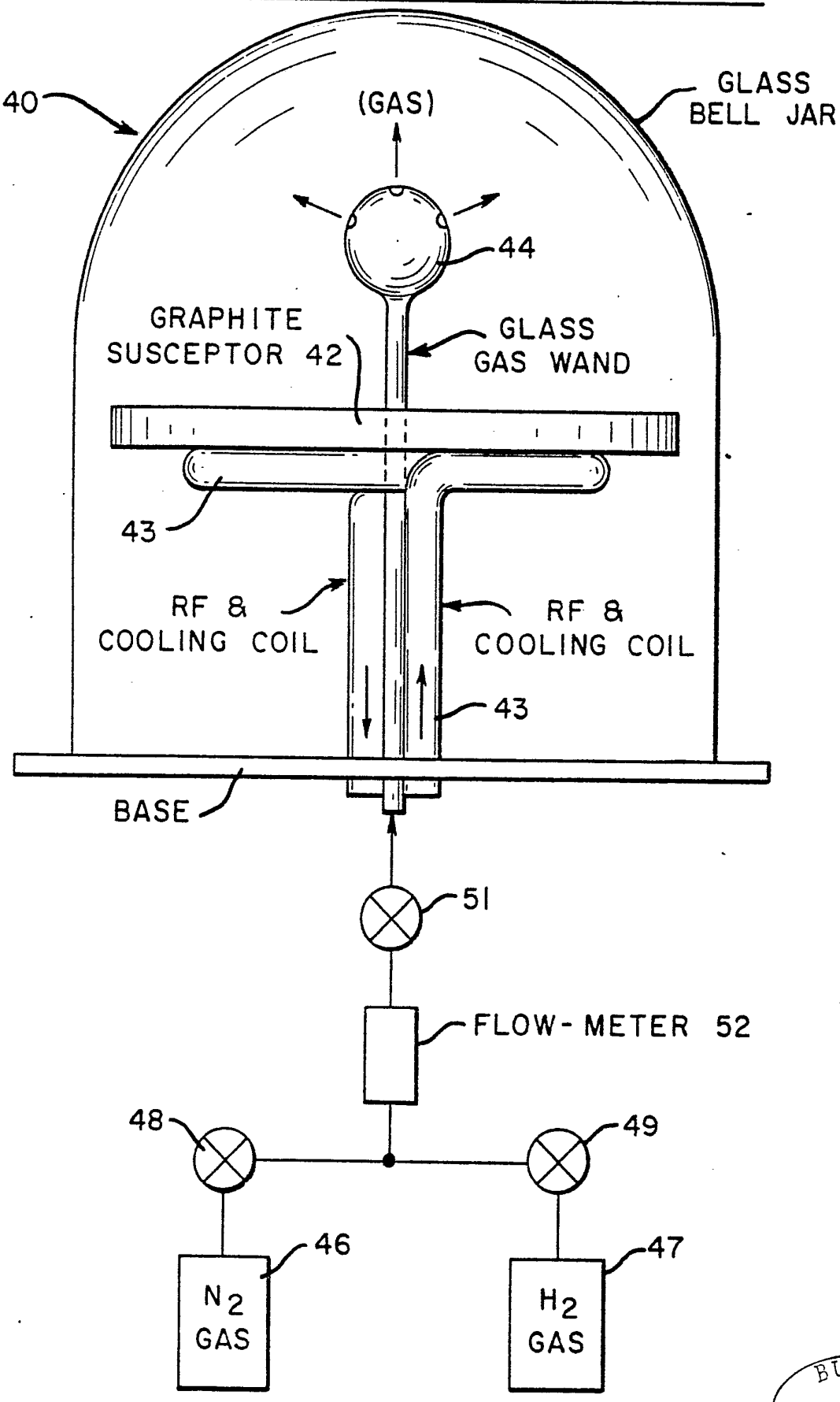


FIG. 3

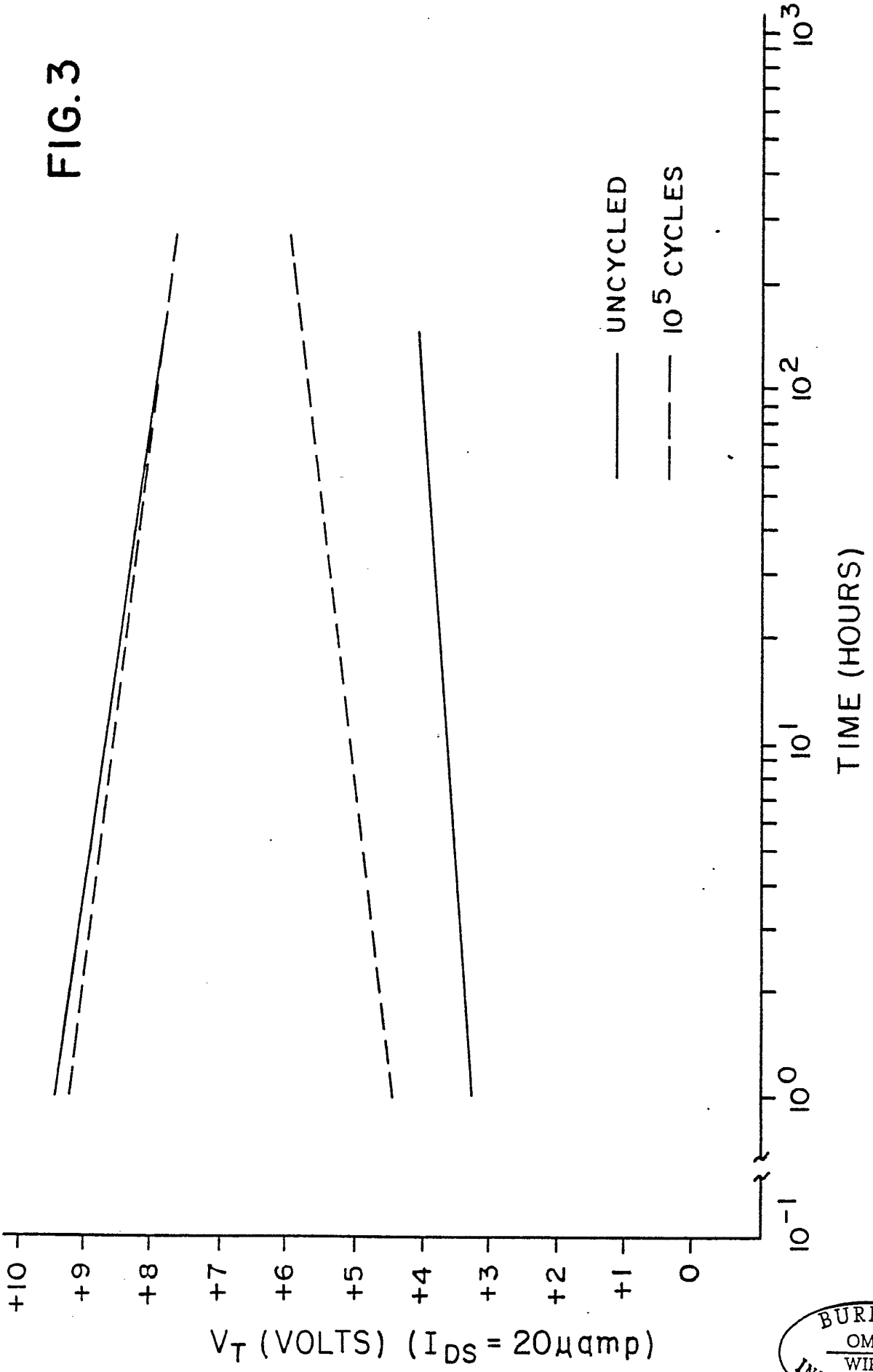
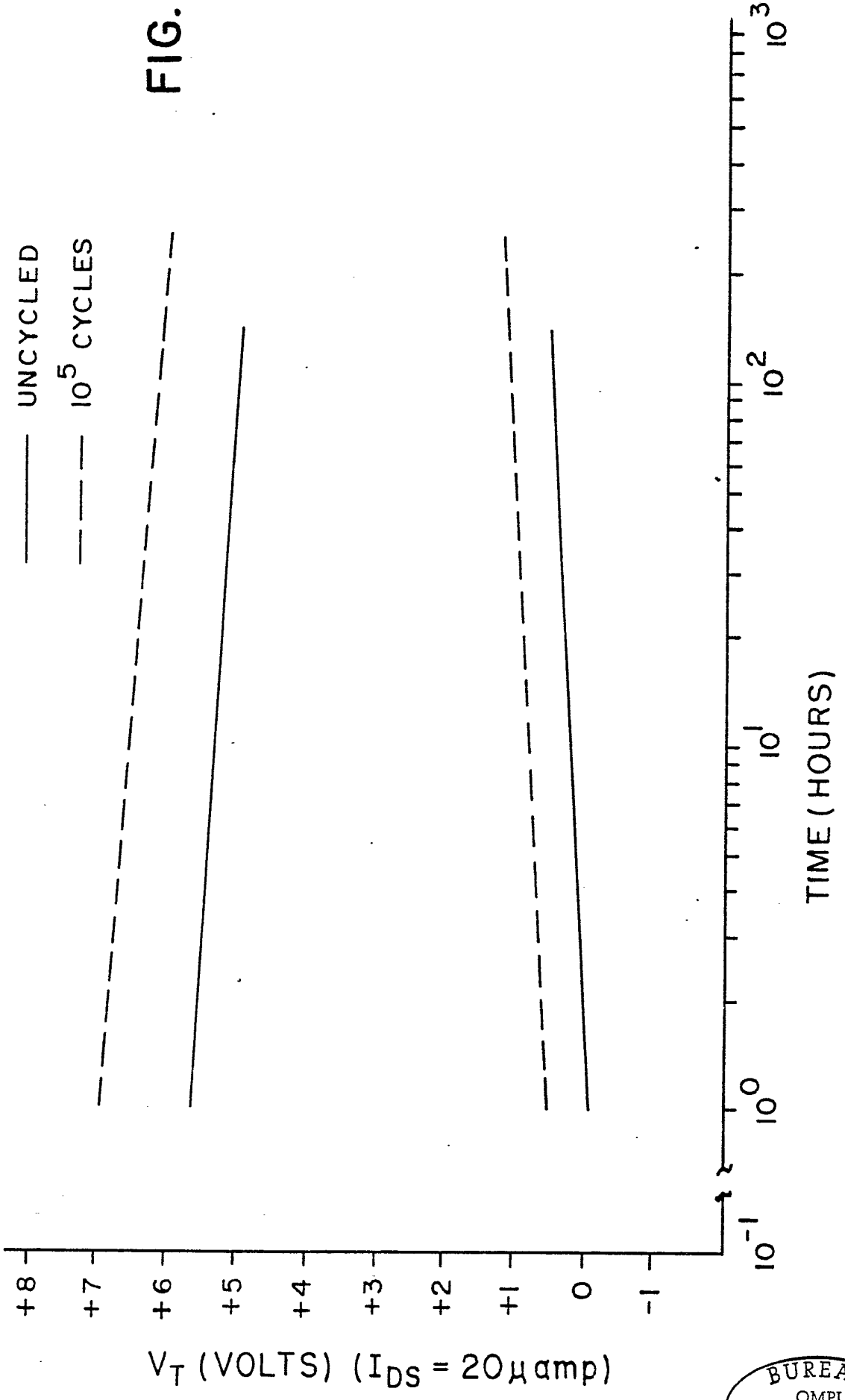


FIG. 4



INTERNATIONAL SEARCH REPORT

International Application No PCT/US 80/01020

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.3 H01L 21/324, H01L 21/477

US. CL. 29/571, 148/1.5, 187 357/23, 52, 54 427/93, 94

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	148/1.5, 187 29/571, 427/93, 94 357/23, 52, 54

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
A	US, E, Re 28,386, Published, 08 April 1975, Heiman et al	1-10
X	US, A, 3,615,873, Published, 26 October 1971, Sluss et al	1-7,10
A	US, A, 3,653,978, Published, 04 April 1972, Robinson et al	1-10
A	US, A, 3,719,866, Published, 06 March 1973, Naber et al	1-10
A	US, A, 3,867,196, Published, 18 February 1975 Richman	1-10
A	US, A, 4,027,380, Published, 07 June 1977, Deal et al	1-10
X	US, A, 4,097,314, Published, 27 June 1978, Schlesier et al	1,4,5,9
X	US, A, 4,151,007, Published, 24 April 1979, Levinstein et al	1,3-5,8-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
05 DECEMBER 1980	24 DEC 1980
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	William G. Saba WILLIAM G. SABA

Form PCT/ISA/210 (second sheet) (October 1977)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	US, N, Solid State Electronics, Vol. 13, pp. 1451-1459, Published, 1970, "Surface State Related 1/F Noise In MOS Transistors" By Hsu, S.T.	1-10
X	US, N, J. Electrochem. Soc., Vol. 118, No. 9, pp. 1463-1468, Published, September 1971, "High-Temperature Annealing Of Oxidized Silicon Surfaces" By Montillo et al	1-10
X	US, N, I.B.M. Technical Disclosure Bulletin, Vol. 18, No. 3 p. 753, Published, August 1975, "Post Oxidation Annealing Of Field-Effect Transistors To Reduce Fixed Charge Levels" By Burkhardt et al	1-10

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers _____, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [11]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.

Continuation From The Second Sheet

X	US, N, Electronic Engineering, Pages 41-43, Published, January 1976, "Threshold Voltage Shift Of MOS Transistor By Ion Implantation" By Runge, H.	1,3-5,8-10
A	US, N, IEEE Transactions On Electron Devices, Vol. ED-24, No. 5, Published, May 1977, Pages 584-586, "Threshold-Alterable Si-Gate MOS Device", By Chen, P.C.Y.	1-10
A	US, N, Applied Physics Letters, Vol. 31, No. 7 Published, 01 October 1977, Pages 475-476, "New Approach For The Floating-Gate MOS Non-volatile Memory" By Lee Han-Sheng	1-10
A	JA, A, 52-10079, Published, 26 January 1977	1-10