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(71) Applicant: **TOKYO ELECTRON LIMITED** [JP/JP]; Akasaka Biz Tower, 3-1 Akasaka 5-chome, Minato-ku, Tokyo 107-6325 (JP).

(71) Applicant *(for JP only)*: **TOKYO ELECTRON U.S. HOLDINGS, INC.** [US/US]; 2400 Grove Boulevard, Austin, Texas 78741 (US).

(72) Inventors: **YU, Kai-Hung**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **O'MEARA, David**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **JOY, Nicholas**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **PATTANAIK, Gyanaranjan**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **CLARK, Robert**; 2859 Bayview Dr., Fremont, California 94538 (US). **TAPILY, Kandabara**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **HAKAMATA, Takahiro**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **WAJDA, Cory**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US). **LEUSINK, Gerrit**; NanoFab 300 South, 255 Fuller Road, Suite 214, Albany, New York 12203 (US).

(74) Agent: **LUDVIKSSON, Audunn**; Tokyo Electron U.S. Holdings, Inc., 2400 Grove Blvd., Austin, Texas 78741 (US).

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(54) **Title:** METHOD FOR FILLING RECESSED FEATURES IN SEMICONDUCTOR DEVICES WITH A LOW-RESISTIVITY METAL

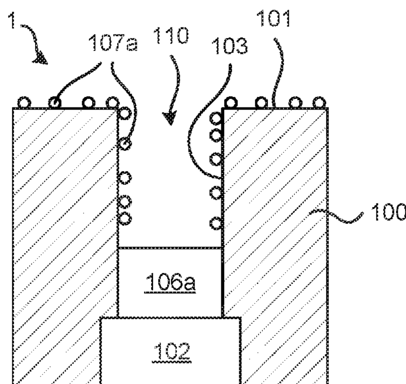


FIG. 1B

(57) **Abstract:** A method for filling recessed features with a low-resistivity metal. The method includes providing a patterned substrate containing a recessed feature formed in a first layer and a second layer that is exposed in the recessed feature, and pre-treating the substrate with a surface modifier that increases metal deposition selectivity on the second layer relative to on the first layer, depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the second layer in the recessed feature, and removing metal nuclei deposited on the first layer, including on a field area and on sidewalls of the first layer in the recessed feature, to selectively form the metal layer on the second layer in the recessed feature. The steps of pre-treating, depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

METHOD FOR FILLING RECESSED FEATURES IN SEMICONDUCTOR DEVICES WITH A LOW-RESISTIVITY METAL

CROSS-REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This application is related to and claims priority to United States Provisional Patent Application serial no. 62/744,038, filed on October 10, 2018, the entire contents of which are herein incorporated by reference.

FIELD OF THE INVENTION

10 **[0002]** The present invention relates to semiconductor processing and semiconductor devices, and more particularly, to a method for filling recessed features in semiconductor devices with a low-resistivity metal.

BACKGROUND OF THE INVENTION

15 **[0003]** Semiconductor devices contain filled recessed features such as trenches or vias that are formed in a dielectric material such as an interlayer dielectric (ILD). Selective metal filling of the recessed features is problematic due to finite metal deposition selectivity on a metal layer at the bottom of the recessed features relative to on the dielectric material. This makes it difficult to fully fill the recessed features with a metal in a bottom-up deposition process before the on-
20 set of unwanted metal nuclei deposition on the field area (horizontal area) around the recessed features and on the sidewalls of the recessed features.

SUMMARY OF THE INVENTION

[0004] Embodiments of the invention describe a method of filling recessed features in
25 semiconductor devices with a low-resistivity metal. According to one embodiment, the method includes providing a patterned substrate containing a recessed feature formed in a first layer and a second layer that is exposed in the recessed feature, and pre-treating the substrate with a surface modifier that increases metal deposition selectivity on the second layer relative to on the first layer. The method further includes depositing a metal layer on the substrate by vapor phase
30 deposition, where the metal layer is preferentially deposited on the second layer in the recessed feature, and removing metal nuclei deposited on the first layer, including on a field area and on sidewalls of the first layer in the recessed feature, to selectively form the metal layer on the

second layer in the recessed feature. The steps of pre-treating, depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

[0005] According to another embodiment, the method includes providing a patterned substrate containing a recessed feature formed in a first layer and a second layer that is exposed in the recessed feature, depositing a metal-containing layer on the substrate, including in the recessed feature, and anisotropically removing the metal-containing layer from a bottom of the recessed feature and from a field area around the recessed feature to form the metal-containing layer on sidewalls of the recessed feature. The method further includes pre-treating the substrate with a surface modifier that increases metal deposition selectivity on the metal-containing layer on the sidewalls of the recessed feature and on the second layer relative to on the first layer, depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the metal-containing layer on the sidewalls and on the second layer in the recessed feature relative to on the field area around the recessed feature, and removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature. The steps of pre-treating, depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

[0006] According to another embodiment, the method includes providing a patterned substrate containing a recessed feature formed in material, depositing a metal nitride layer on the substrate, including in the recessed feature and on a field area around the recessed feature, and oxidizing the metal nitride layer on the field area. The method further includes depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the metal nitride layer that is not oxidized in the recessed feature, and removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature. The steps of depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

[0007] According to another embodiment, the method includes providing a patterned substrate containing a recessed feature formed in material, depositing a metal oxide layer on the substrate, including in the recessed feature and on a field area around the recessed feature, nitriding the metal oxide layer on the field area and in the recessed feature, and oxidizing the nitrided metal oxide layer on the field area. The method further includes depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the nitrided metal oxide layer that is not oxidized in the recessed feature, and removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature. The steps

of depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

[0008] According to another embodiment, the method includes providing a patterned substrate containing a recessed feature formed in material, depositing a metal oxide layer on the substrate, including in the recessed feature and on a field area around the recessed feature, and nitriding the metal oxide layer on the field area. The method further includes depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the nitrided metal oxide layer on the field area, and removing metal nuclei deposited in the recessed feature to selectively form the metal layer on the field area. The steps of depositing and removing may be repeated at least once to increase a thickness of the metal layer in the recessed feature.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] A more complete appreciation of the invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0010] FIGS. 1A – 1F schematically show a method for selective metal formation in a recessed feature according to an embodiment of the invention;

[0011] FIGS. 2A – 2E schematically show a method for selective metal formation in a recessed feature according to another embodiment of the invention;

[0012] FIGS. 3A – 3E schematically show a method for selective metal formation in a recessed feature according to another embodiment of the invention;

[0013] FIGS. 4A – 4F schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention;

[0014] FIGS. 5A – 5E schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention;

[0015] FIGS. 6A – 6D schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention; and

[0016] FIG. 7 shows a SEM image with selective Ru metal formation in recessed features on a patterned substrate.

DETAILED DESCRIPTION OF SEVERAL EMBODIMENTS

[0017] Embodiments of the invention provide a method for selectively forming a low-resistivity metal in recessed features of a semiconductor device. The method can be used to fully fill the recessed features with the low-resistivity metal. According to one embodiment, metal deposition selectivity by vapor phase deposition increases in the order: Si-containing material < metal-containing layer < metal. The deposited metal can, for example, include Ru metal, Co metal, or W metal. An incubation time for metal deposition is shortest on a metal and longest on a Si-containing material. An incubation time refers to a delay until metal deposition starts on a surface during a deposition process. In one embodiment, this may be used to preferentially form a metal in a recessed feature relative to on surfaces above the recessed feature. The Si-containing material can include SiO_2, SiON, or SiN. The SiO_2 may be deposited as a layer or formed by oxidation of Si, for example by exposure to air, oxygen (O_2 or O), ozone, or H_2O. The SiN may be deposited as a layer or formed by nitridation of Si, for example by exposure to N or NH_3. The SiON may be deposited as a layer or formed by nitriding SiO_2, by oxidation of SiN, or by oxidation and nitridation of Si. The metal-containing layer can include a metal oxide, a metal nitride, a metal carbide, a metal silicide, a metal sulfide, or a metal phosphide. The metal silicide may be formed by metal deposition on Si or Si deposition on a metal, followed by a heat-treatment, or by formation of the metal silicide during a deposition process. The metal can, for example, include Ru metal, Co metal, or W metal.

[0018] FIGS. 1A – 1F schematically shows a method for selective metal formation in a recessed feature according to an embodiment of the invention. The metal can, for example, be selected from the group consisting of Ru metal, Co metal, and W metal. The patterned substrate 1 contains a field area 101 around a recessed feature 110 formed in a first layer 100. The recessed feature 110 contains sidewalls 103 and a second layer 102 that has an exposed surface 104.

[0019] According to one embodiment, the first layer 100 can include a dielectric material and the second layer 102 can include a metal layer. The dielectric material can, for example, contain SiO_2, a low dielectric constant (low-k) material such as fluorinated silicon glass (FSG), carbon doped oxide, a polymer, a SiCOH-containing low-k material, a non-porous low-k material, a porous low-k material, a CVD low-k material, a spin-on dielectric (SOD) low-k material, or any other suitable dielectric material, including a high dielectric constant (high-k) material. In some examples, a width (critical dimension (CD)) of the recessed feature 110 can be between about 10nm and about 100nm, between about 10nm and about 15nm, between about 20nm and about 90, or between about 40nm and about 80nm. In some examples, the depth of the recessed

feature 110 can between bout 40nm and about 200nm, between about 50nm and about 150, or between about 50nm and about 150nm. In some examples, and the recessed feature 110 can have an aspect ratio (depth/width) between about 2 and about 20, or between about 4 and about 6. The second layer 102 can include a low-resistivity metal such as Cu metal, Ru metal, Co
5 metal, W metal, or a combination thereof. In one example, the second layer 102 can include two or more stacked metal layers. Examples of the stacked metal layers include Co metal on Cu metal (Co/Cu) and Ru metal on Cu metal (Ru/Cu).

[0020] The method includes pre-treating the patterned substrate 1 with a surface modifier that adsorbs on the first layer 100 and thereby increases metal deposition selectivity on the second
10 layer 102 relative to on the first layer 100, including on the sidewalls 103 and on the field area 101. The presence of the surface modifier hinders deposition of the metal layer on first layer 100 but the second layer 102 is not modified. According to one embodiment, the patterned substrate 1 is pre-treated with a surface modifier by exposure to a reactant gas that contains a molecule that is capable of forming self-assembled monolayers (SAMs) on a substrate. SAMs
15 are molecular assemblies that are formed spontaneously on substrate surfaces by adsorption and are organized into more or less large ordered domains. The SAMs can include a molecule that possesses a head group, a tail group, and a functional end group, and SAMs are created by the chemisorption of head groups onto the substrate from the vapor phase at room temperature or above room temperature, followed by a slow organization of the tail groups. Initially, at small
20 molecular density on the surface, adsorbate molecules form either a disordered mass of molecules or form an ordered two-dimensional "lying down phase", and at higher molecular coverage, over a period of minutes to hours, begin to form three-dimensional crystalline or semicrystalline structures on the substrate surface. The head groups assemble together on the substrate, while the tail groups assemble far from the substrate. According to one embodiment,
25 the head group of the molecule forming the SAMs can include a thiol, a silane, or a phosphonate. Examples of silanes include molecule that include C, H, Cl, F, and Si atoms, or C, H, Cl, and Si atoms. Non-limiting examples of the molecule include perfluorodecyltrichlorosilane ($CF_3(CF_2)_7CH_2CH_2SiCl_3$), perfluorodecanethiol ($CF_3(CF_2)_7CH_2CH_2SH$), chlorodecyldimethylsilane ($CH_3(CH_2)_8CH_2Si(CH_3)_2Cl$), and
30 tertbutyl(chloro)dimethylsilane ($(CH_3)_3CSi(CH_3)_2Cl$)).

[0021] According to some embodiments of the invention, the reactant gas can contain a silicon-containing gas, including an alkyl silane, an alkoxysilane, an alkyl alkoxysilane, an alkyl siloxane, an alkoxysiloxane, an alkyl alkoxysiloxane, an aryl silane, an acyl silane, an aryl

siloxane, an acyl siloxane, a silazane, or any combination thereof. According to some embodiments of the invention, the reactant gas may be selected from dimethylsilane dimethylamine (DMSDMA), trimethylsilane dimethylamine (TMSDMA), bis(dimethylamino) dimethylsilane (BDMADMS), and other alkyl amine silanes. According to other embodiments, the reactant gas may be selected from N,O bistrimethylsilyltrifluoroacetamide (BSTFA) and trimethylsilyl-pyrrole (TMS-pyrrole).

[0022] According to some embodiments of the invention, the reactant gas may be selected from silazane compounds. Silazanes are saturated silicon-nitrogen hydrides. They are analogous in structure to siloxanes with --NH--- replacing --O--. An organic silazane precursor can further contain at least one alkyl group bonded to the Si atom(s). The alkyl group can, for example, be a methyl group, an ethyl group, a propyl group, or a butyl group, or combinations thereof. Furthermore, the alkyl group can be a cyclic hydrocarbon group such as a phenyl group. In addition, the alkyl group can be a vinyl group. Disilazanes are compounds having from 1 to 6 methyl groups attached to the silicon atoms or having 1 to 6 ethyl groups attached the silicon atoms, or a disilazane molecule having a combination of methyl and ethyl groups attached to the silicon atoms.

[0023] The method further includes depositing a metal layer 106a on the patterned substrate 1 by vapor phase deposition, where the metal layer 106a is preferentially deposited on the second layer 102 in the recessed feature 110. The metal layer 106a can, for example, be selected from the group consisting of Ru metal, Co metal, and W metal. According to one embodiment of the invention, Ru metal may be deposited by chemical vapor phase deposition (CVD) or atomic layer deposition (ALD). Examples of Ru-containing precursors include $Ru_3(CO)_{12}$, (2,4-dimethylpentadienyl) (ethylcyclopentadienyl) ruthenium (Ru(DMPD)(EtCp)), bis(2,4-dimethylpentadienyl) ruthenium ($Ru(DMPD)_2$), 4-dimethylpentadienyl) (methylcyclopentadienyl) ruthenium (Ru(DMPD)(MeCp)), and bis(ethylcyclopentadienyl) ruthenium ($Ru(EtCp)_2$), as well as combinations of these and other precursors.

[0024] As schematically shown in FIG. 1B, the metal deposition may not be completely selective and metal nuclei 107a may be deposited on the sidewalls 103 and on the field area 101. Unlike the metal layer 106a, the metal nuclei 107a may be form a non-continuous layer where the total amount of the metal in the metal nuclei 107a is less than the amount of the metal in the metal layer 106a.

[0025] In one example, Ru metal was deposited by CVD using a $Ru_3(CO)_{12}$ precursor in a CO carrier gas. After pre-treating the substrate with a surface modifier, Ru metal nuclei were

observed on a dielectric material after a thickness of about 15-20nm of Ru metal was deposited on a Cu metal layer at a bottom of a recessed feature in the dielectric material. This illustrates the limited selectivity of Ru metal deposition on different materials and the difficulty of selectively depositing and filling recessed features deeper than about 15-20nm with Ru metal before the onset of Ru metal deposition on dielectric surfaces. Ru metal deposition rates by CVD were observed to decrease in the order: metal > metal nitride or nitride metal oxide > metal oxide or oxidized metal nitride > ILD, where the Ru metal deposition rate is highest on a metal surface and lowest on an ILD surface. This may be utilized for preferential Ru metal deposition on the different materials. ILDs include dielectric compounds that contain silicon, carbon, or both silicon and carbon. Examples include SiO_2, SiON, SiN, SiCOH, Si, SiC, and C.

[0026] The method further includes removing the metal nuclei 107a from the patterned substrate 1 to selectively form the metal layer 106a on the second layer 102 in the recessed feature 110. This is schematically shown in FIG. 1C. It is may be preferable that the removal of the metal nuclei 107a be performed before they get too big and are more difficult to remove efficiently. In one example, Ru metal nuclei 107a may be removed by etching using reactive ion etching (RIE), for example using plasma-excited O_2 gas and optionally adding a halogen-containing gas (e.g., Cl_2).

[0027] The steps of pre-treating, depositing and removing may be repeated at least once to increase a thickness of the metal deposited in the recessed feature 110. This is schematically shown in FIG. 1D where additional metal layer 106b is preferentially deposited on the metal layer 106a and additional metal nuclei 107b are deposited on the sidewalls 103 and on the field area 101. Thereafter, as shown in FIG. 1E, the additional metal nuclei 107b are removed. In one example, the pre-treating, depositing and removing may be repeated until the recessed feature 110 is fully filled with the metal. This is schematically shown in FIG. 1F, where the recessed feature 110 is filled with metal layers 106a – 106c.

[0028] A process example for selective Ru metal formation in a recessed feature includes a pre-treatment using a TMSDMA gas exposure where TMSDMA liquid is vaporized and diluted with N_2 gas, a substrate temperature between about 180°C and about 250°C, a process chamber pressure of about 5Torr, and a 10sec exposure time with no plasma excitation. A Ru metal CVD process includes a process gas containing $Ru_3(CO)_{12}$ + CO (e.g., a gas flow ratio of about 1:100), a substrate temperature between about 135°C and about 180°C (for example about 160°C), a process chamber pressure between about 1mTorr and about 20mTorr (for example about 5mTorr), and a 400sec exposure without plasma excitation that deposits about 20nm of Ru

metal on a metal surface. A Ru metal removal process includes the use of an etching gas of containing O_2 and Cl_2 (e.g., a gas flow ratio of about 100:1), a substrate temperature between about room temperature and about 370°C (for example about 370°C), plasma excitation using a capacitively coupled plasma source with about 1200W of RF power applied to a top electrode and between about 0W and about 300W (for example 0W) of RF power applied to a bottom electrode (substrate holder), a process chamber pressure of about 5mTorr, and a 40sec exposure time to remove the equivalent of about 5nm of Ru metal nuclei.

[0029] FIG. 7 shows a SEM image with selective Ru metal formation in recessed features on a patterned substrate. The as-received patterned substrate contained raised SiO_2 features on a W metal film. The raised SiO_2 features were about 113nm tall, about 31nm wide, and were spaced apart by about 87nm. The raised SiO_2 features formed recessed features that were about 113nm deep and with a width of about 87nm. The figure shows the results following a deposition process that included pre-treating the patterned substrate with a surface modifier containing TMSDMA, a Ru metal CVD deposition step using $Ru_3(CO)_{12}$ + CO, and a Ru metal etching step using plasma-excited O_2 gas + Cl_2 gas that removed Ru metal nuclei from the sidewalls of the recessed features. The sequence of pre-treating, Ru metal depositing, and Ru metal nuclei removal was performed four times. The figure illustrates that Ru metal was selectively formed in the recessed features and no Ru metal nuclei were present on the sidewalls of the recessed features or on the top surfaces of the etched SiO_2 features. The thickness of the Ru metal formed in the recessed features was about 69nm and filled about 61% of the volume of the recessed features.

[0030] FIGS. 2A – 2F schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention. FIG. 1A has been reproduced as patterned substrate 2 in FIG. 2A. The method includes providing the patterned substrate 2 containing a recessed feature 110 formed in a first layer 100 and a second layer 102 that is exposed in the recessed feature 110. As shown in FIG. 2B, the method includes depositing a metal-containing layer 111 on the patterned substrate 2, including in the recessed feature 110 and on the field area 101 around the recessed feature 110. The metal-containing layer 111 may be conformal and in some examples, the metal-containing layer 111 can include a metal oxide, a metal nitride, or a combination thereof. The metal oxide can, for example, include Al_2O_3, TiO_2, HfO_2, or MnO_2, and the metal nitride can, for example, include AlN, TiN, HfN, or MnN.

[0031] Thereafter, as shown in FIG. 2C, the method further includes anisotropically removing the metal-containing layer 111 from a bottom of the recessed feature 110 and from the field area

101 around the recessed feature 110 to form the metal-containing layer 111 on the sidewalls 103 of the recessed feature 110. The method further includes pre-treating the patterned substrate 2 with a surface modifier that that adsorbs on the first layer 100, including on the field area 101, and thereby increases metal deposition selectivity on the metal-containing layer 111 on the sidewalls 103 of the recessed feature 110 and on the second layer 102 relative to on the first layer 100.

[0032] The method further includes depositing a metal layer 112 on the patterned substrate 2 by vapor phase deposition, where the metal layer 112 is preferentially deposited on the metal-containing layer 111 on the sidewalls 103 and on the second layer 102 at the bottom of the recessed feature 110, relative to on the field area 101 around the recessed feature 110. The metal layer 112 can, for example, be selected from the group consisting of Ru metal, Co metal, and W metal. As schematically shown in FIG. 2D, the metal deposition may not be completely selective and metal nuclei 113 may be deposited on the field area 101. Unlike the metal layer 112, the metal nuclei 113 may be form a non-continuous layer where the total amount of the metal in the metal nuclei 113 is less than the amount of the metal in the metal layer 112. According to the embodiment shown in FIG. 2D, the metal layer 112 may fully fill the recessed feature 110. As shown in FIG. 2E, the method further includes removing the metal nuclei 113 deposited on the field area 101 of the first layer 100 around the recessed feature 110 to selectively form the metal layer 112 in the recessed feature 110.

[0033] According to another embodiment, the metal layer 112 may not fully fill the recessed feature 110, and the pre-treating, depositing and removing may be repeated at least once to increase a thickness of the metal deposited in the recessed feature 110. According to one embodiment, the pre-treating, depositing and removing may be repeated until the recessed feature 110 is fully filled with the metal.

[0034] FIGS. 3A – 3E schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention. FIG. 1A has been reproduced as patterned substrate 3 in FIG. 3A. The method includes providing the patterned substrate 3 containing a recessed feature 110 formed in a material. In one example, the material can include a first layer 100 and a second layer 102 that is exposed in the recessed feature 110. As shown in FIG. 3B, the method further includes depositing a metal nitride layer 114 on the patterned substrate 3, including in the recessed feature 110 and on the field area 101 around the recessed feature 110. The metal nitride layer 114 may be conformal, and in some examples, the metal nitride layer 114 can include AlN, TiN, HfN, or MnN.

[0035] Thereafter, the method further includes oxidizing the metal nitride layer 114 on the field area 101 to form an oxidized metal nitride layer 115. As used herein, the oxidizing process incorporates oxygen into at least a surface region of the metal nitride layer 114. As schematically shown in FIG. 3C, the metal nitride layer 114 may also be oxidized in the recessed feature 110 near the opening of the recessed feature 110. The step of oxidizing the metal nitride layer 114 can be performed using plasma-excited O_2 gas, where the small opening of the recessed feature 110 limits the penetration of the plasma-excited O_2 gas into the recessed feature 110. This limits the oxidation of the metal nitride layer 114 to the field area 101 and an upper portion of the recessed feature 110.

[0036] The method further includes depositing a metal layer 116 on the substrate by vapor phase deposition, where the metal layer 116 is preferentially deposited on the metal nitride layer 114 that is not oxidized in the recessed feature 110. The preferential metal deposition is believed to be due to a shorter incubation time for the metal deposition on the metal nitride layer 114 relative to on the oxidized metal nitride layer 115. As schematically shown in FIG. 3D, the metal deposition may not be completely selective and metal nuclei 123 may be deposited on the field area 101. Unlike the metal layer 116, the metal nuclei 123 may be form a non-continuous layer where the total amount of the metal in the metal nuclei 123 is less than the amount of the metal in the metal layer 116.

[0037] According to the embodiment shown in FIG. 3D, the metal layer 116 may fully fill the recessed feature 110 where oxidation of the metal nitride layer 114 is avoided. As shown in FIG. 3E, the method further includes removing the metal nuclei 123 deposited on the field area 101 of the first layer 100 around the recessed feature 110 to selectively form the metal layer 116 in the recessed feature 110.

[0038] According to another embodiment, the metal layer 116 may not fully fill the recessed feature 110 where oxidation of the metal nitride layer 114 is avoided, and the steps of depositing and removing may be repeated at least once to increase a thickness of the metal layer 116 deposited in the recessed feature 110. According to one embodiment, the steps of depositing and removing may be repeated until the recessed feature 110 is fully filled with the metal layer 116.

[0039] FIGS. 4A – 4F schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention. FIG. 1A has been reproduced as patterned substrate 4 in FIG. 4A. The method includes providing the patterned substrate 4 containing a recessed feature 110 formed in a material. In one example, the material can include

a first layer 100 and a second layer 102 that is exposed in the recessed feature 110. As shown in FIG. 4B, the method further includes depositing a metal oxide layer 117 on the patterned substrate 4, including in the recessed feature 110 and on the field area 101 around the recessed feature 110. The metal oxide layer 117 may be conformal, and in some examples, the metal oxide layer 117 can include Al_2O_3, TiO_2, HfO_2, or MnO_2.

[0040] Thereafter, the method further includes nitriding the metal oxide layer 117 on the field area 101 and in the recessed feature 110 to form a nitrided metal oxide layer 118. As used herein, the nitriding process incorporates nitrogen into at least a surface region of the metal oxide layer 117. As schematically shown in FIG. 4C, the nitrided metal oxide layer 118 may be conformal. The step of nitriding the metal oxide layer 117 may be carried out using a thermal nitriding process (e.g., NH_3 anneal in the absence of a plasma) that effectively nitrides at least a portion of the thickness of the entire metal oxide layer 117, including in the recessed feature 110.

[0041] Thereafter, the method further includes oxidizing the nitrided metal oxide layer 118 on the field area 101 to form an oxidized nitrided metal oxide layer 119. As used herein, the oxidizing process incorporates oxygen into at least a surface region of the nitrided metal oxide layer 118. The step of oxidizing the nitrated metal oxide layer can be performed using plasma-excited O_2 gas, where the small opening of the recessed feature 110 limits the penetration of the plasma-excited O_2 gas into the recessed feature 110. This limits the oxidation of the nitrited metal oxide layer to the field area 101 and an upper portion of the recessed feature 110. This is schematically shown in FIG. 4D.

[0042] The method further includes depositing a metal layer 120 on the patterned substrate 4 by vapor phase deposition, where the metal layer 120 is preferentially deposited on the nitrided metal oxide layer 118 that is not oxidized in the recessed feature 110. The preferential metal deposition is believed to be due to a shorter incubation time for the metal deposition on the nitrated metal oxide layer relative to on the oxidized nitrided metal oxide layer 119.

[0043] As schematically shown in FIG. 4E, the metal deposition may not be completely selective and metal nuclei 121 may be deposited on the oxidized nitrided metal oxide layer 119 on the field area 101. Unlike the metal layer 120, the metal nuclei 121 may be form a non-continuous layer where the total amount of the metal in the metal nuclei 121 is less than the amount of the metal in the metal layer 120.

[0044] According to the embodiment shown in FIG. 4E, the metal layer 120 may fully fill the recessed feature 110 where oxidation of the nitrided metal oxide layer 118 is avoided. As shown

in FIG. 4F, the method further includes removing the metal nuclei 121 deposited on the field area 101 of the first layer 100 around the recessed feature 110 to selectively form the metal layer 120 in the recessed feature 110.

[0045] According to another embodiment, the metal layer 120 may not fully fill the recessed feature 110 where oxidation of the nitrided metal oxide layer 118 is avoided, and the steps of depositing and removing may be repeated at least once to increase a thickness of the metal layer 120 deposited in the recessed feature 110. According to one embodiment, the steps of depositing and removing may be repeated until the recessed feature 110 is fully filled with the metal layer 120.

[0046] FIGS. 5A – 5D schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention. FIG. 5A shows a patterned substrate 5 containing recessed features 510 formed in a material 500, where the recessed features contain sidewalls 503 and bottom 502. The method includes depositing a metal oxide layer 504 on the patterned substrate 5, including in the recessed features 510 and on a field area 501 around the recessed features 510. This is schematically shown in FIG. 5B.

[0047] The method further includes nitriding the metal oxide layer 504 on the field area 101. As used herein, the nitriding process incorporates nitrogen into at least a surface region of the metal oxide layer 504 to form a nitrided metal oxide layer 505. This is schematically shown in FIG. 5C. The step of nitriding the metal oxide layer 504 can be performed using plasma-excited nitrogen-containing gas (e.g., N_2 or NH_3), where the small openings of the recessed features 510 limit the penetration of the plasma-excited nitrogen-containing gas into the recessed features 510.

[0048] The method further includes depositing a metal layer 506 on the patterned substrate 5 by vapor phase deposition, where the metal layer 506 is preferentially deposited on the nitrided metal oxide layer 505 on the field area 501. As schematically shown in FIG. 5D, the metal deposition may not be completely selective and metal nuclei 507 may be deposited on the metal oxide layer 504 in the recessed features 510.

[0049] The method further includes removing the metal nuclei 507 deposited in the recessed features 510 to selectively form the metal layer 506 on the field area 501. This is schematically shown in FIG. 5E. The steps of depositing and removing may be repeated at least once to increase a thickness of the metal layer 506 on the field area 501.

[0050] FIGS. 6A – 6D schematically shows a method for selective metal formation in a recessed feature according to another embodiment of the invention. In one example, shown in FIG. 6A,

the patterned substrate 6 may include a portion of a 3D NAND device. The method include providing a patterned substrate 6 containing an etched vertical feature 610 and etched horizontal features 601 in a material 600. The etched vertical feature 610 may be tapered with a larger opening near the top than near the bottom. In one example, the material 600 may include SiO_2 or SiN. The method further includes nitriding the etched vertical feature 610 and the etched horizontal features 601 to form a nitrided layer 602. The process of nitriding can include a thermal nitriding process (e.g., NH_3 anneal in the absence of a plasma) that nitrides both the etched vertical feature 610 and etched horizontal features 601. Thereafter, the method includes a plasma treatment (e.g., an Ar plasma) that removes the nitrided layer 602 from the etched vertical feature 610, while retaining the nitrided layer 602 in the etched horizontal features 601. The resulting patterned substrate 6 is shown in FIG. 6B. The method further includes depositing a metal layer 603 on the patterned substrate 6 by vapor phase deposition, where the metal layer 603 is preferentially deposited on the nitrided layer 602 in the etched horizontal features 601 relative to on the etched vertical feature 610. This is shown in FIG. 6C. The vapor phase deposition is performed until the etched vertical feature 610 is also fully filled with a metal layer 604. The selective metal deposition is due to a higher metal deposition rate on the nitrided layer 602 than on the etched vertical feature 610 that is not nitrided. This allows for complete metal filling of the etched vertical feature 610 and the etched horizontal features 601 without any voids.

[0051] A method for filling recessed features in semiconductor devices with a low-resistivity metal has been disclosed in various embodiments. The foregoing description of the embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. This description and the claims following include terms that are used for descriptive purposes only and are not to be construed as limiting. Persons skilled in the relevant art can appreciate that many modifications and variations are possible in light of the above teaching. Persons skilled in the art will recognize various equivalent combinations and substitutions for various components shown in the Figures. It is therefore intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, the method comprising:

providing a patterned substrate containing a recessed feature formed in a first layer and a second layer that is exposed in the recessed feature;

pre-treating the substrate with a surface modifier that increases metal deposition selectivity on the second layer relative to on the first layer;

depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the second layer in the recessed feature; and

removing metal nuclei deposited on the first layer, including on a field area and on sidewalls of the first layer in the recessed feature, to selectively form the metal layer on the second layer in the recessed feature.

2. The method of claim 1, further comprising:

repeating the pre-treating, depositing and removing at least once to increase a thickness of the metal layer in the recessed feature.

3. The method of claim 1, wherein the pre-treating includes forming self-assembled monolayers (SAMs) on the first layer.

4. The method of claim 1, wherein the metal layer is selected from the group consisting of Ru metal, Co metal, and W metal, and the second layer is selected from the group consisting of Cu metal, Ru metal, Co metal, W metal, and a combination thereof.

5. A method of forming a semiconductor device, the method comprising:

providing a patterned substrate containing a recessed feature formed in a first layer and a second layer that is exposed in the recessed feature;

depositing a metal-containing layer on the substrate, including in the recessed feature;

anisotropically removing the metal-containing layer from a bottom of the recessed feature and from a field area around the recessed feature to form the metal-containing layer on sidewalls of the recessed feature;

pre-treating the substrate with a surface modifier that increases metal deposition selectivity on the metal-containing layer on the sidewalls of the recessed feature and on the second layer relative to on the first layer;

depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the metal-containing layer on the sidewalls and on the second layer in the recessed feature, relative to on the field area around the recessed feature; and

removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature.

6. The method of claim 5, further comprising:

repeating the pre-treating, depositing and removing at least once to increase a thickness of the metal layer in the recessed feature.

7. The method of claim 5, wherein the pre-treating includes forming self-assembled monolayers (SAMs) on the second layer.

8. The method of claim 5, wherein the metal layer is selected from the group consisting of Ru metal, Co metal, and W metal, and the second layer is selected from the group consisting of Cu metal, Ru metal, Co metal, W metal, and a combination thereof.

9. The method of claim 5, wherein the metal-containing layer contains a metal oxide, a metal nitride, or a combination thereof.

10. The method of claim 5, wherein the metal oxide includes Al_2O_3, TiO_2, HfO_2, or MnO_2, and the metal nitride includes AlN, TiN, HfN, or MnN.

11. A method of forming a semiconductor device, the method comprising:

providing a patterned substrate containing a recessed feature formed in material;

depositing a metal nitride layer on the substrate, including in the recessed feature and on a field area around the recessed feature;

oxidizing the metal nitride layer on the field area;

depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the metal nitride layer that is not oxidized in the recessed feature; and

removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature.

12. The method of claim 11, further comprising:

repeating the depositing and removing at least once to increase a thickness of the metal layer in the recessed feature.

13. The method of claim 11, wherein the metal layer is selected from the group consisting of Ru metal, Co metal, and W metal.

14. The method of claim 11, wherein the metal nitride layer includes AlN, TiN, HfN, or MnN.

15. A method of forming a semiconductor device, the method comprising:

providing a patterned substrate containing a recessed feature formed in material;

depositing a metal oxide layer on the substrate, including in the recessed feature and on a field area around the recessed feature;

nitriding the metal oxide layer on the field area and in the recessed feature;

oxidizing the nitrided metal oxide layer on the field area;

depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the nitrided metal oxide layer that is not oxidized in the recessed feature; and

removing metal nuclei deposited on the field area to selectively form the metal layer in the recessed feature.

16. The method of claim 15, further comprising:

repeating the depositing and removing at least once to increase a thickness of the metal layer in the recessed feature.

17. The method of claim 15, wherein the metal layer is selected from the group consisting of Ru metal, Co metal, and W metal.

18. The method of claim 15, wherein the metal oxide layer includes Al_2O_3, TiO_2, HfO_2, or MnO_2.

19. A method of forming a semiconductor device, the method comprising:

providing a patterned substrate containing a recessed feature formed in material;

depositing a metal oxide layer on the substrate, including in the recessed feature and on a field area around the recessed feature;

nitriding the metal oxide layer on the field area;

depositing a metal layer on the substrate by vapor phase deposition, where the metal layer is preferentially deposited on the nitrided metal oxide layer in the field area; and

removing metal nuclei deposited in the recessed feature to selectively form the metal layer on the field area.

20. The method of claim 19, further comprising:

repeating the depositing and removing at least once to increase a thickness of the metal layer on the field area.

21. The method of claim 19, wherein the metal layer is selected from the group consisting of Ru metal, Co metal, and W metal.

22. The method of claim 19, wherein the metal oxide layer includes Al_2O_3, TiO_2, HfO_2, or MnO_2.

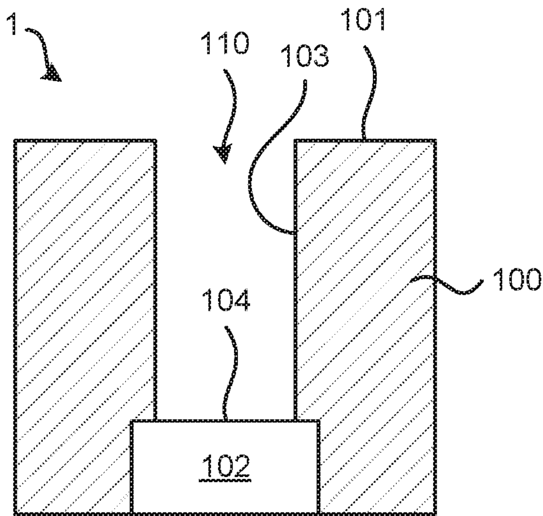


FIG. 1A

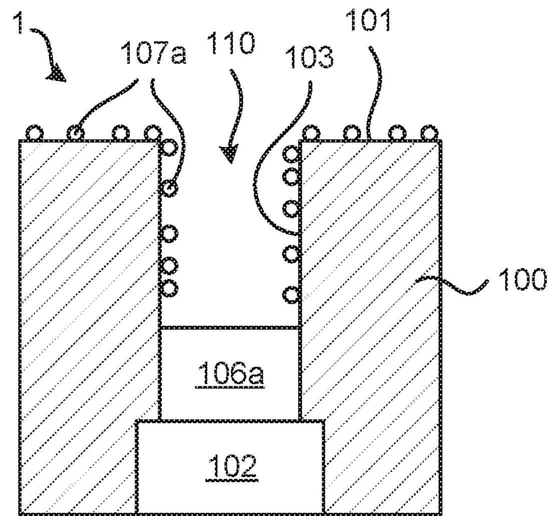


FIG. 1B

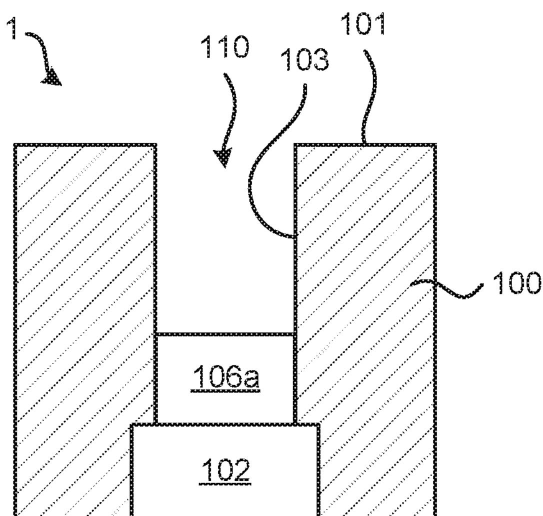


FIG. 1C

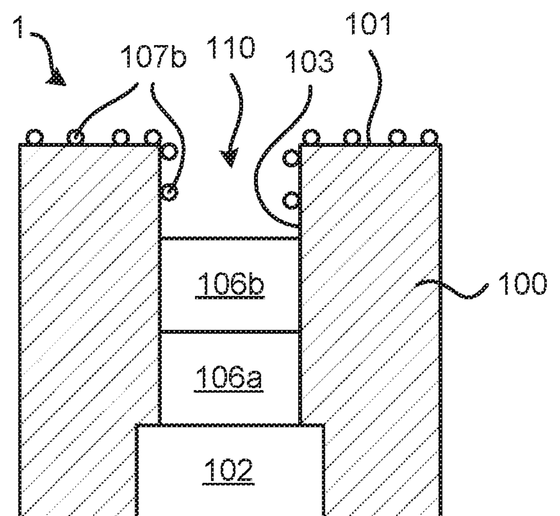


FIG. 1D

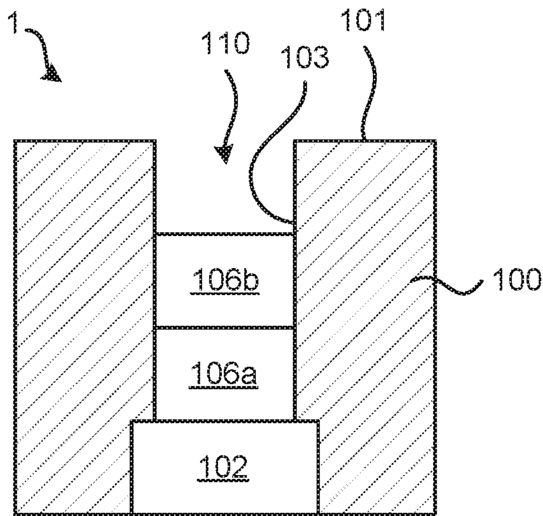


FIG. 1E

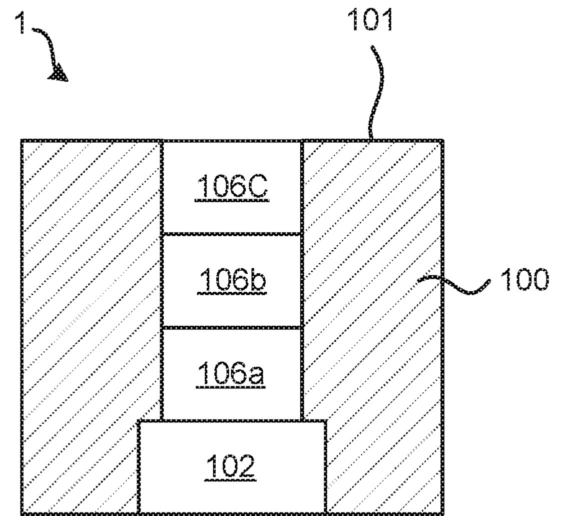


FIG. 1F

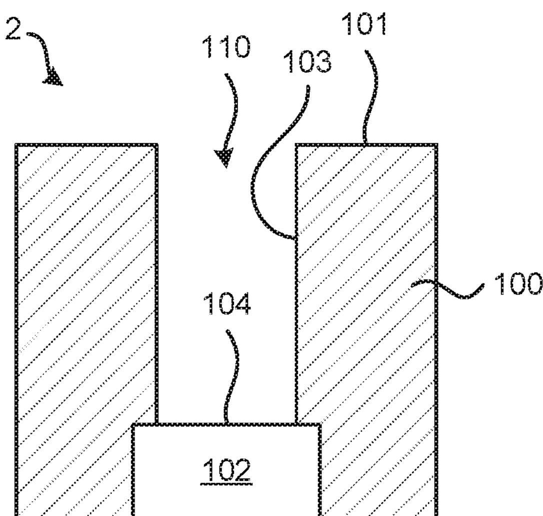


FIG. 2A

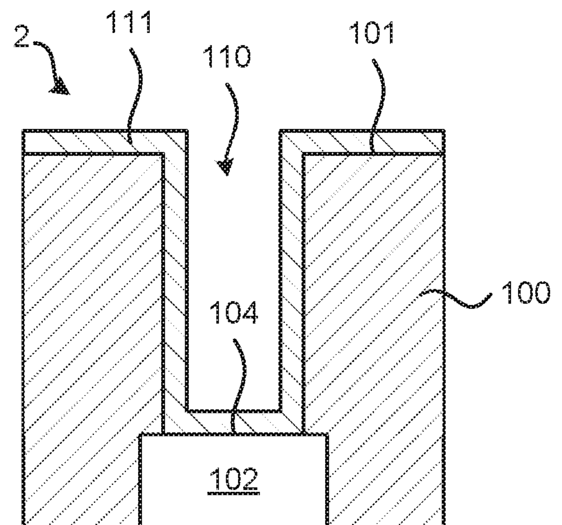


FIG. 2B

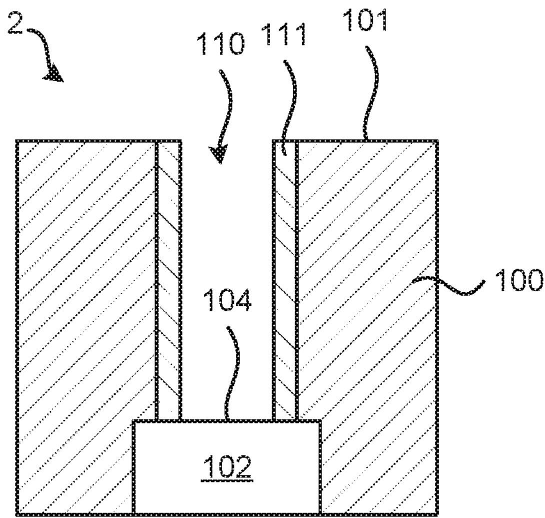


FIG. 2C

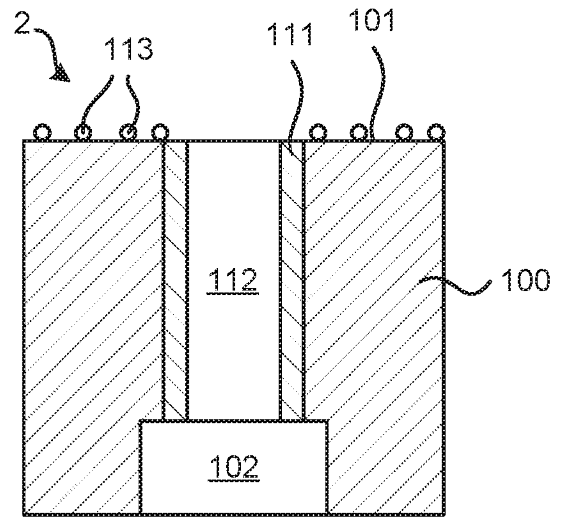


FIG. 2D

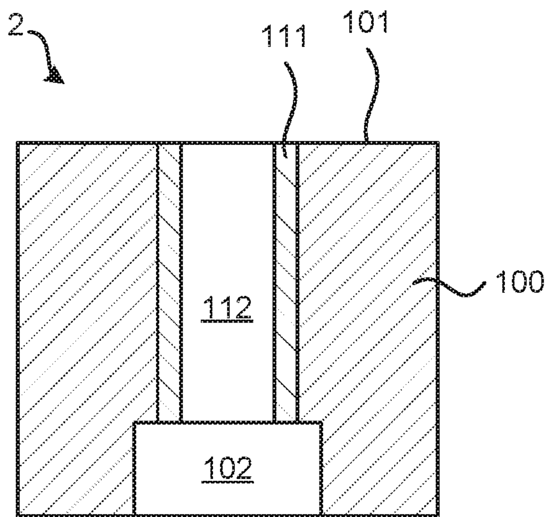


FIG. 2E

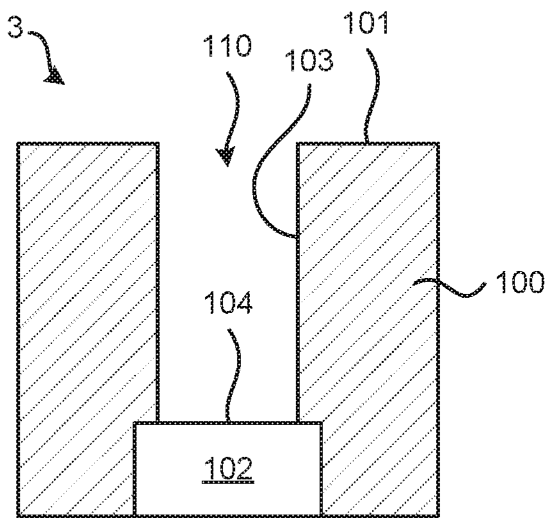


FIG. 3A

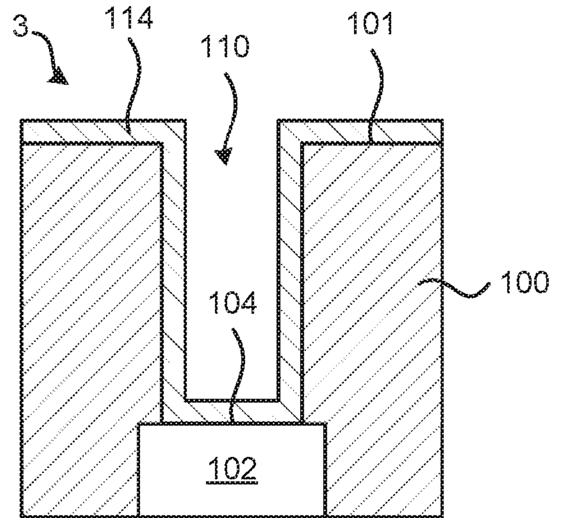


FIG. 3B

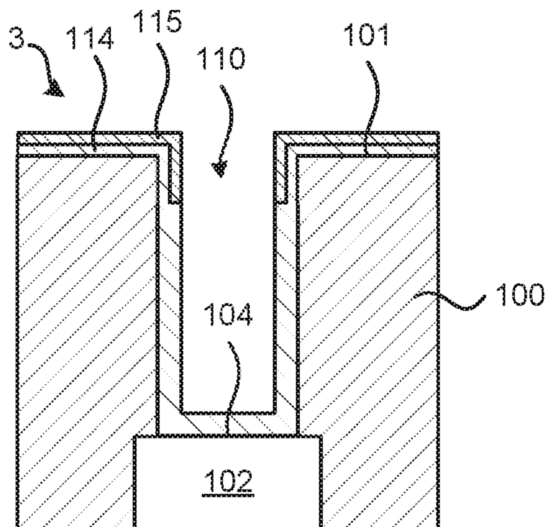


FIG. 3C

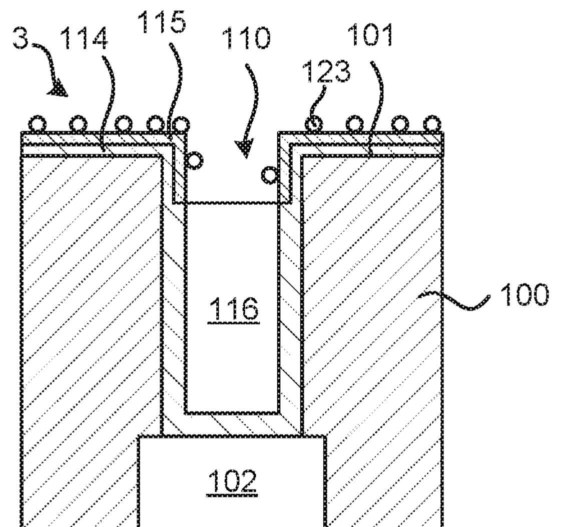


FIG. 3D

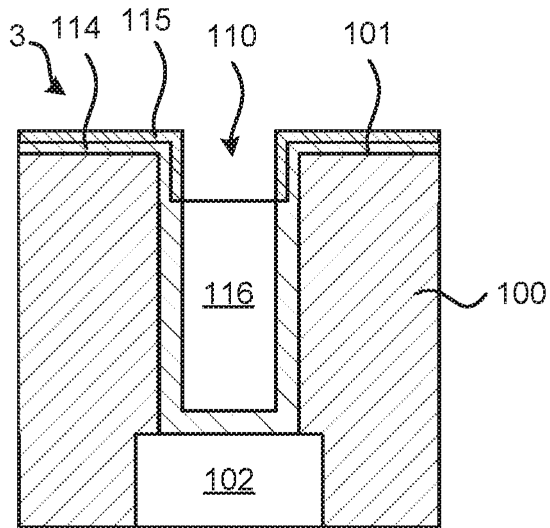


FIG. 3E

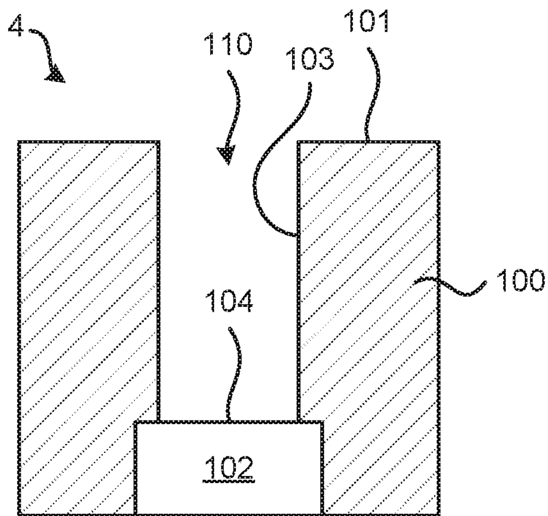


FIG. 4A

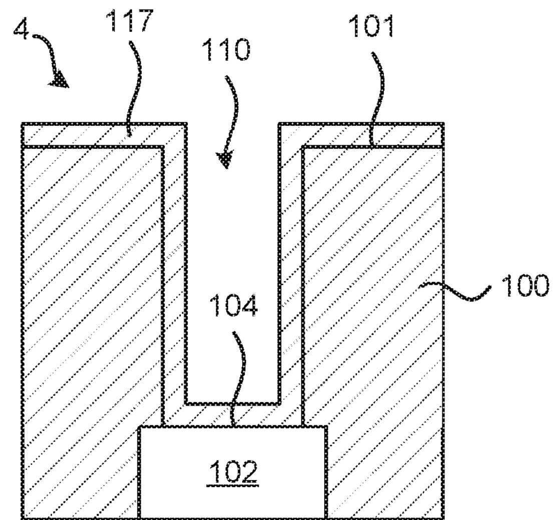


FIG. 4B

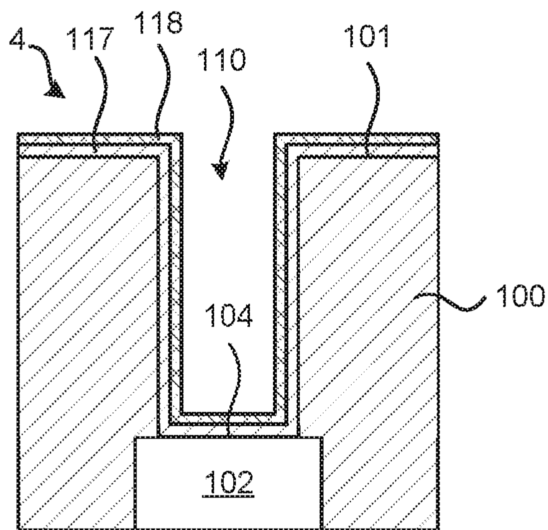


FIG. 4C

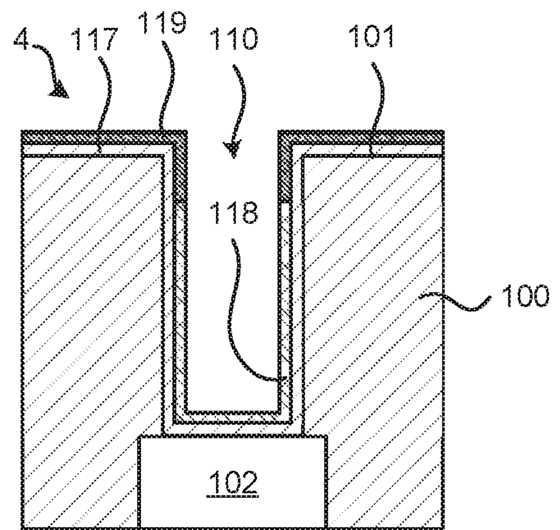


FIG. 4D

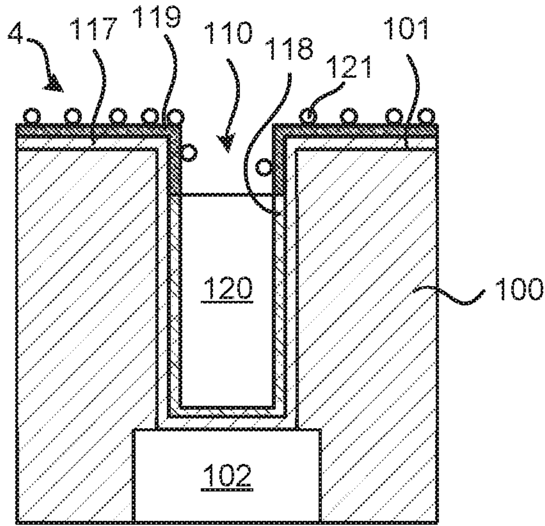


FIG. 4E

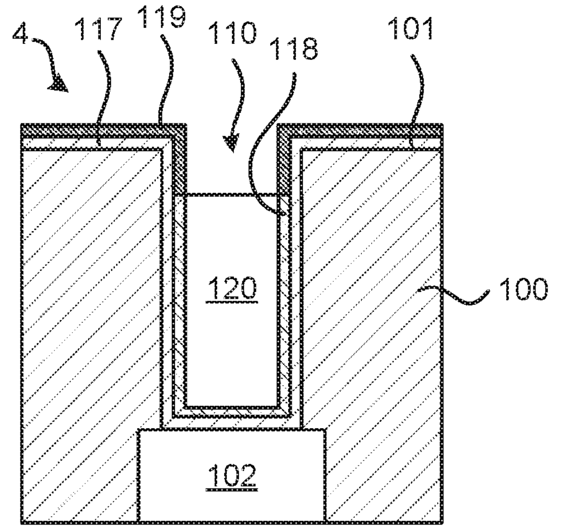


FIG. 4F

FIG. 6

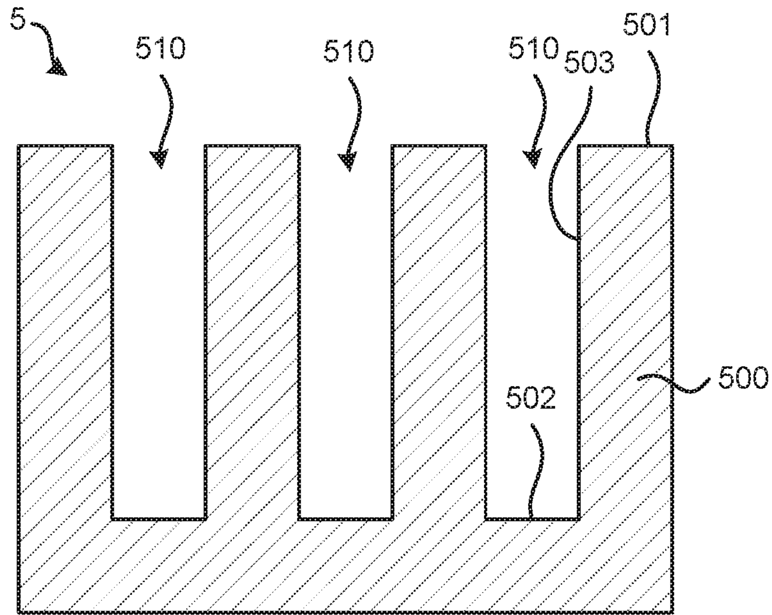


FIG. 5A

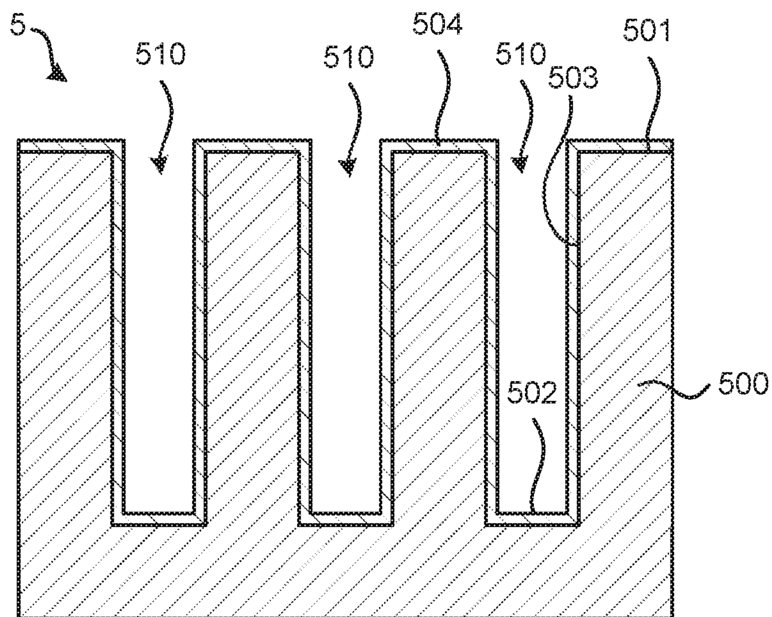


FIG. 5B

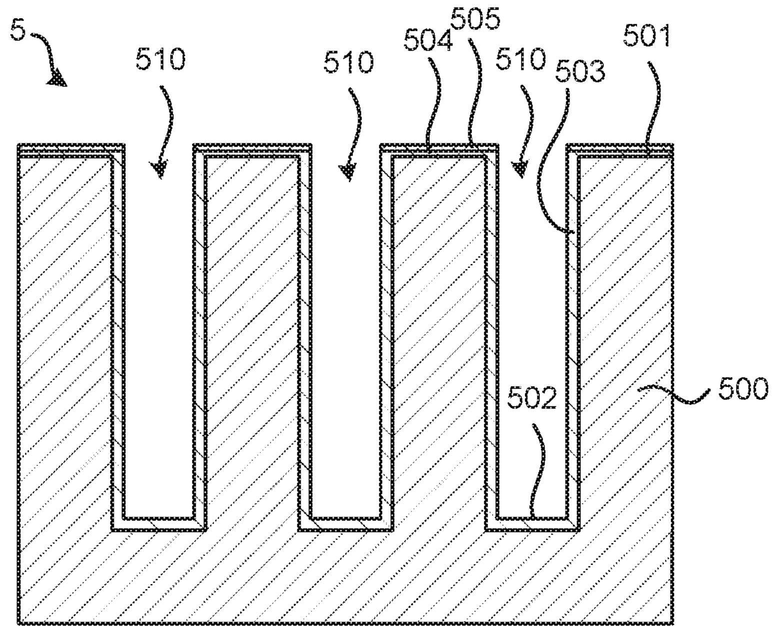


FIG. 5C

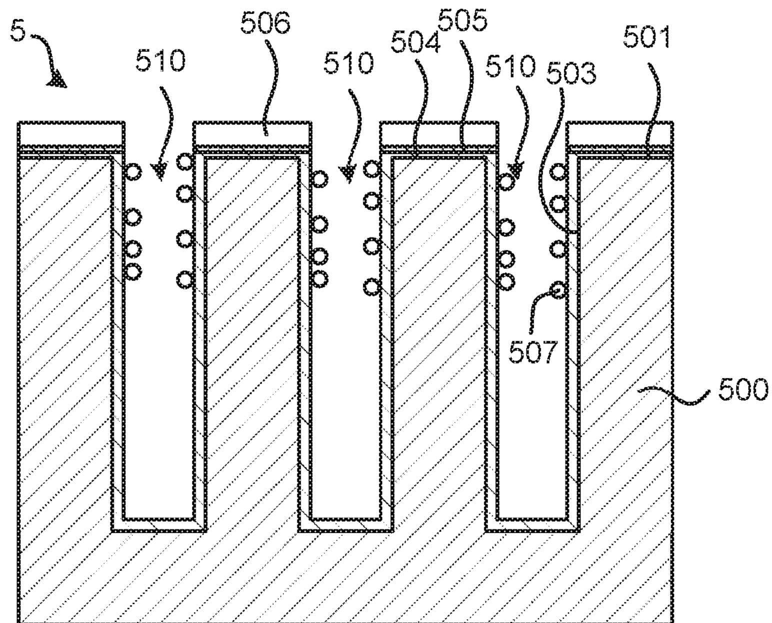


FIG. 5D

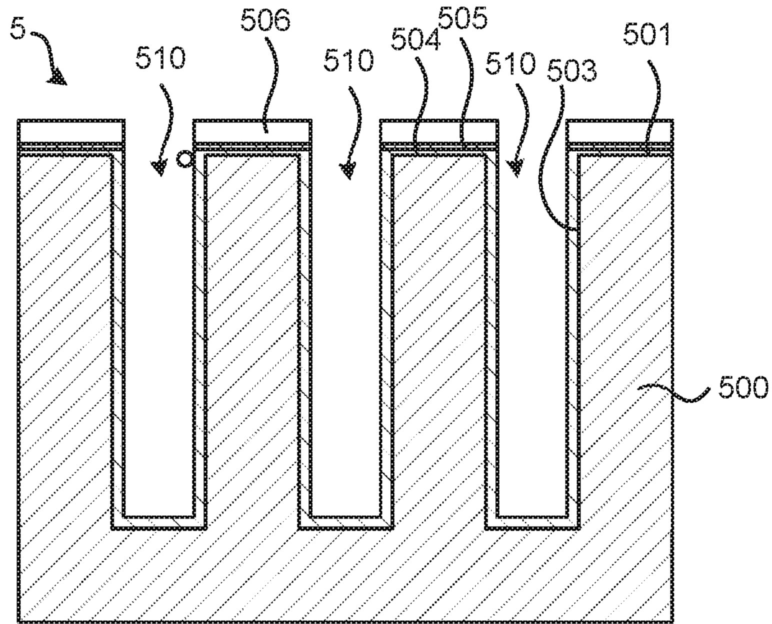


FIG. 5E

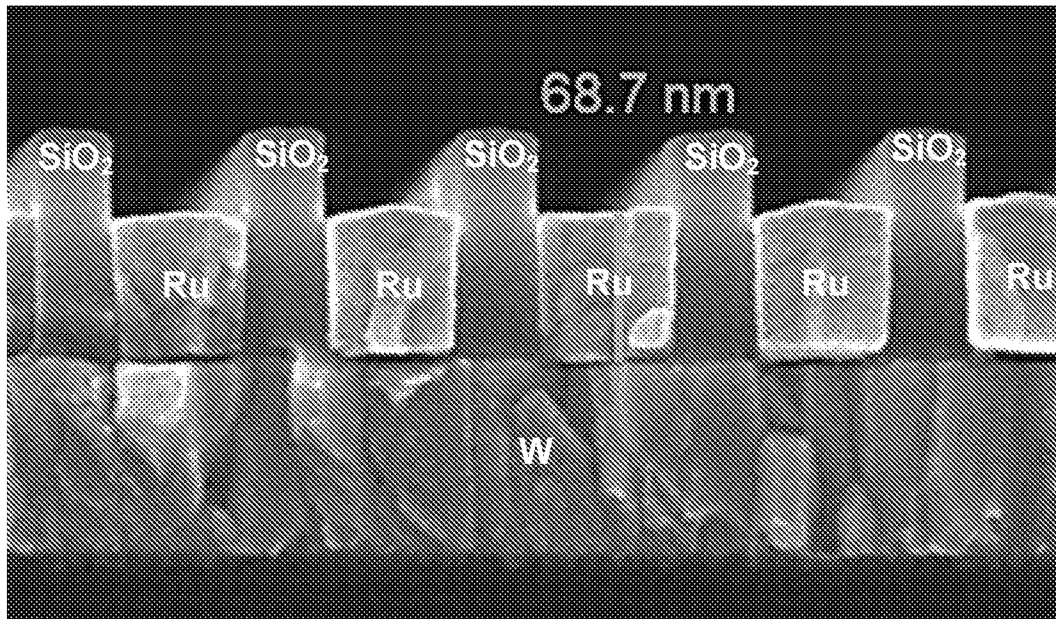


FIG. 7

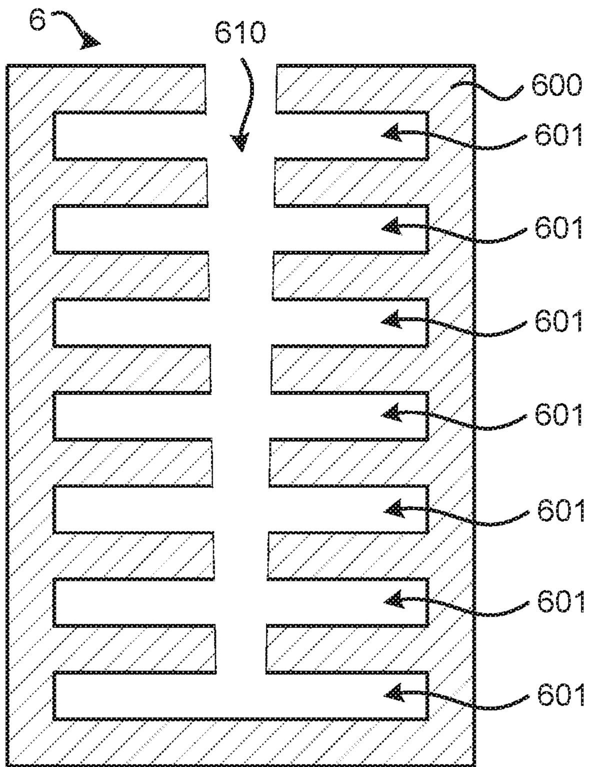


FIG. 6A

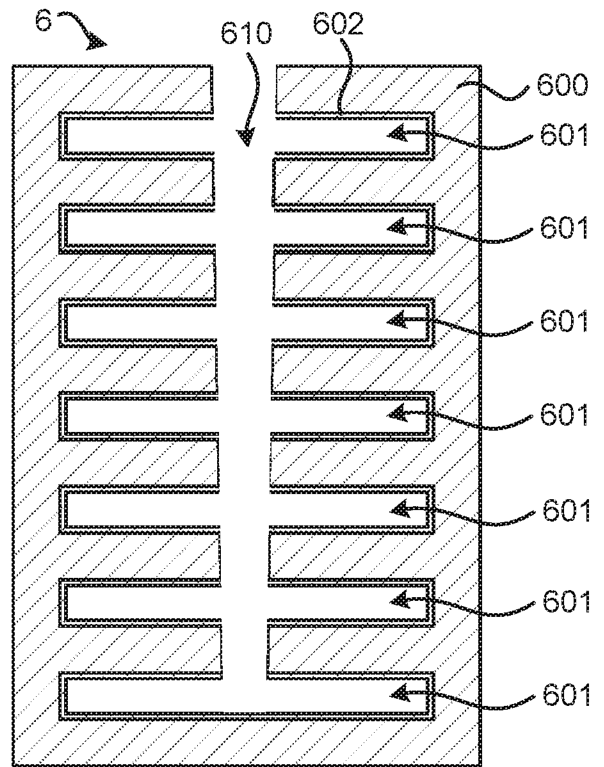


FIG. 6B

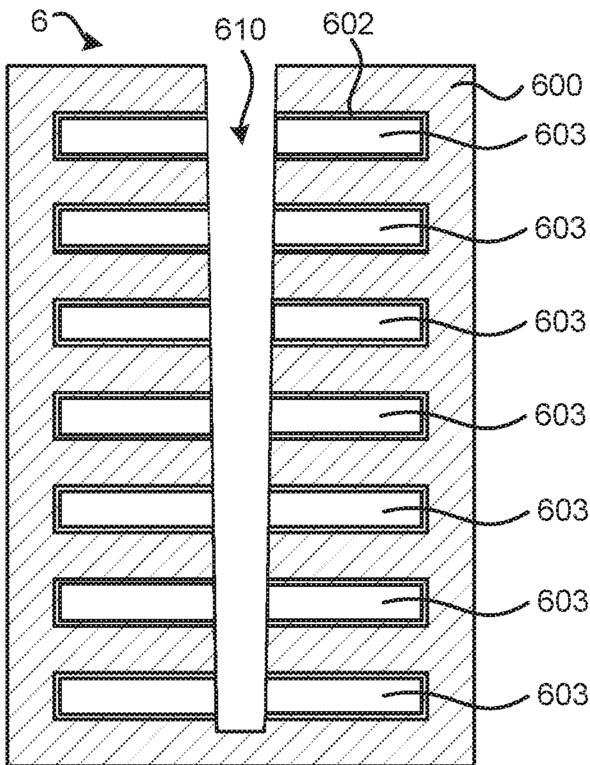


FIG. 6C

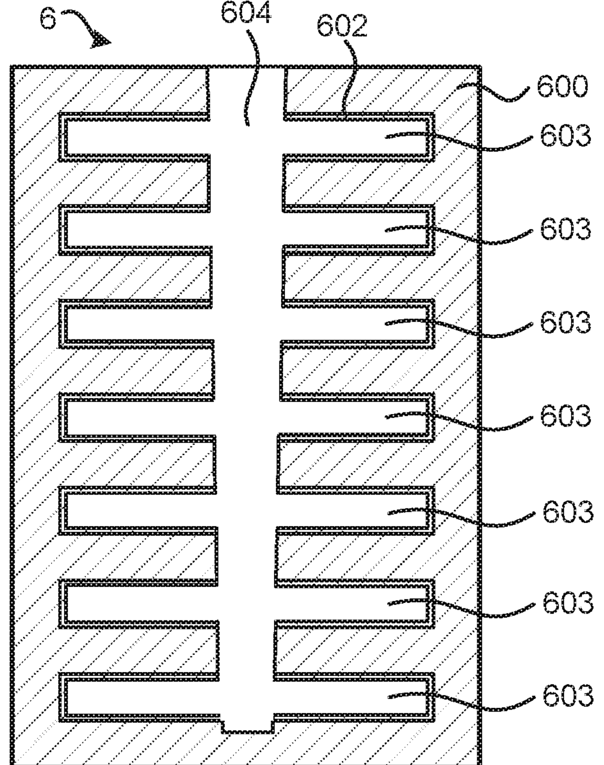


FIG. 6D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/055676

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; C23C 14/22; H01L 21/283; H01L 21/31; H01L 21/3205; H01L 2144

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: recessed feature, metal nuclei, deposition, remove, self-assembled monolayers

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2012-0302071 A1 (SANG IN LEE) 29 November 2012 See paragraphs [0020]-[0021], [0024], [0035]-[0036], [0046]-[0047], [0051]-[0053]; claim 1; and figures 2A-2I.	1-22
Y	US 6492263 B1 (HSIN-TANG PENG et al.) 10 December 2002 See column 3, lines 53-60; column 4, lines 15-20, 46-50; and figures 2a-2f.	1-22
Y	KR 10-1168768 B1 (NOVELLUS SYSTEMS, INC.) 07 March 2005 See paragraphs [0076], [0087]; claim 29; and figures 4a-4c.	3,7
A	KR 10-2014-0009354 A (VARIAN SEMICONDUCTOR EQUIPMENT ASSOCIATES, INC.) 22 January 2014 See paragraphs [0020]-[0023]; and figures 4-11.	1-22
A	KR 10-2008-0001254 A (SAMSUNG ELECTRONICS CO., LTD.) 03 January 2008 See claim 1; and figures 1a-1g.	1-22

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed

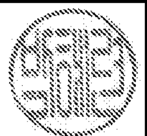
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search
31 January 2020 (31.01.2020)

Date of mailing of the international search report
05 February 2020 (05.02.2020)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. +82-42-481-8578

Authorized officer
PARK, Hye Lyun

Telephone No. +82-42-481-3463

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/055676

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2012-0302071 A1	29/11/2012	US 2010-0041179 A1	18/02/2010
		US 8263502 B2	11/09/2012
		US 8501633 B2	06/08/2013
US 6492263 B1	10/12/2002	TW 463307 B	11/11/2001
KR 10-1168768 B1	25/07/2012	KR 10-1383406 B1	17/04/2014
		KR 10-2005-0022261 A	07/03/2005
		KR 10-2007-0080235 A	09/08/2007
		KR 10-2011-0055496 A	25/05/2011
		US 2004-0142557 A1	22/07/2004
		US 2004-0202786 A1	14/10/2004
		US 2005-0031786 A1	10/02/2005
		US 2006-0094238 A1	04/05/2006
		US 2008-0045010 A1	21/02/2008
		US 2008-0124926 A1	29/05/2008
		US 2008-0254623 A1	16/10/2008
		US 2010-0035427 A1	11/02/2010
		US 2011-0223763 A1	15/09/2011
		US 2013-0168864 A1	04/07/2013
		US 2015-0279732 A1	01/10/2015
		US 6635965 B1	21/10/2003
		US 7005372 B2	28/02/2006
		US 7141494 B2	28/11/2006
		US 7262125 B2	28/08/2007
		US 7589017 B2	15/09/2009
		US 7691749 B2	06/04/2010
		US 7754604 B2	13/07/2010
		US 7955972 B2	07/06/2011
		US 8048805 B2	01/11/2011
		US 8409985 B2	02/04/2013
		US 9076843 B2	07/07/2015
		US 9583385 B2	28/02/2017
		WO 2005-027211 A1	24/03/2005
KR 10-2014-0009354 A	22/01/2014	CN 103380494 A	30/10/2013
		JP 2014-507074 A	20/03/2014
		TW 201246361 A	16/11/2012
		US 2012-0213941 A1	23/08/2012
		WO 2012-116044 A1	30/08/2012
		WO 2012-116056 A1	30/08/2012
KR 10-2008-0001254 A	03/01/2008	None	