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(54) **LOW CEILING TEMPERATURE PROCESS FOR A PLASMA REACTOR WITH HEATED SOURCE OF A POLYMER-HARDENING PRECURSOR MATERIAL**

(52) **U.S. Cl.** 216/68; 216/72; 216/79; 438/710; 438/714; 438/723; 438/729; 438/735; 438/743

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(57) **ABSTRACT**

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A high plasma density etch process for etching an oxygen-containing layer overlying a non-oxygen containing layer on a workpiece in a plasma reactor chamber, by providing a chamber ceiling overlying the workpiece and containing a semiconductor material, supplying into the chamber a process gas containing etchant precursor species, polymer precursor species and hydrogen, applying plasma source power into the chamber, and cooling the ceiling to a temperature range at or below about 150 degrees C. The etchant and polymer precursor species contain fluorine, and the chamber ceiling semiconductor material includes a fluorine scavenger precursor material. Preferably, the process gas includes at least one of CHF_3 and CH_2F_2 . Preferably, the process gas further includes a species including an inert gas, such as He , H_2 or Ar . If the chamber is of the type including a heated fluorine scavenger precursor material, this material is heated to well above the polymer condensation temperature, while the ceiling is cooled. In some cases, the plasma source power applicator is an inductive antenna overlying the semiconductor ceiling, and the ceiling has a cooling/heating apparatus contacting the ceiling through semiconductor rings. The inductive antenna in this case constitutes inductive elements between adjacent ones of the semiconductor rings.

(*) **Notice:** This is a publication of a continued prosecution application (CPA) filed under 37 CFR 1.53(d).

(21) **Appl. No.: 09/008,151**

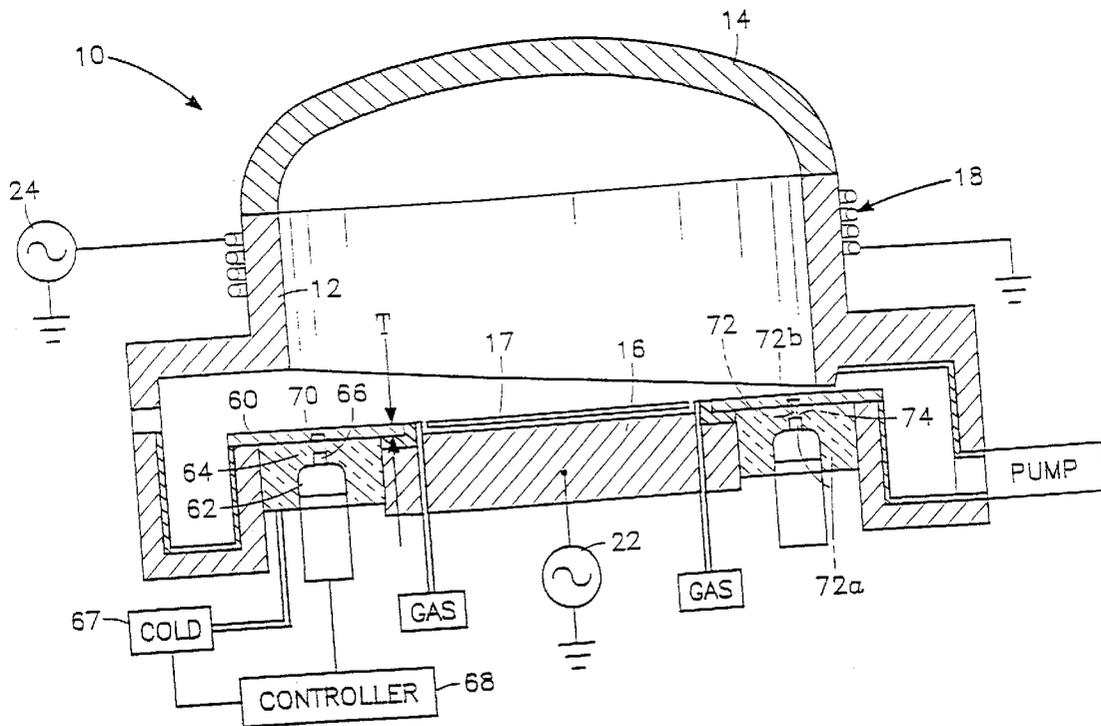
(22) **Filed: Jan. 16, 1998**

Related U.S. Application Data

(63) Continuation-in-part of application No. 08/734,797, filed on Oct. 23, 1996, now Pat. No. 6,024,826, which is a continuation of application No. 08/648,256, filed on May 13, 1996, now Pat. No. 6,036,877.

Publication Classification

(51) **Int. Cl.⁷ B44C 1/22**



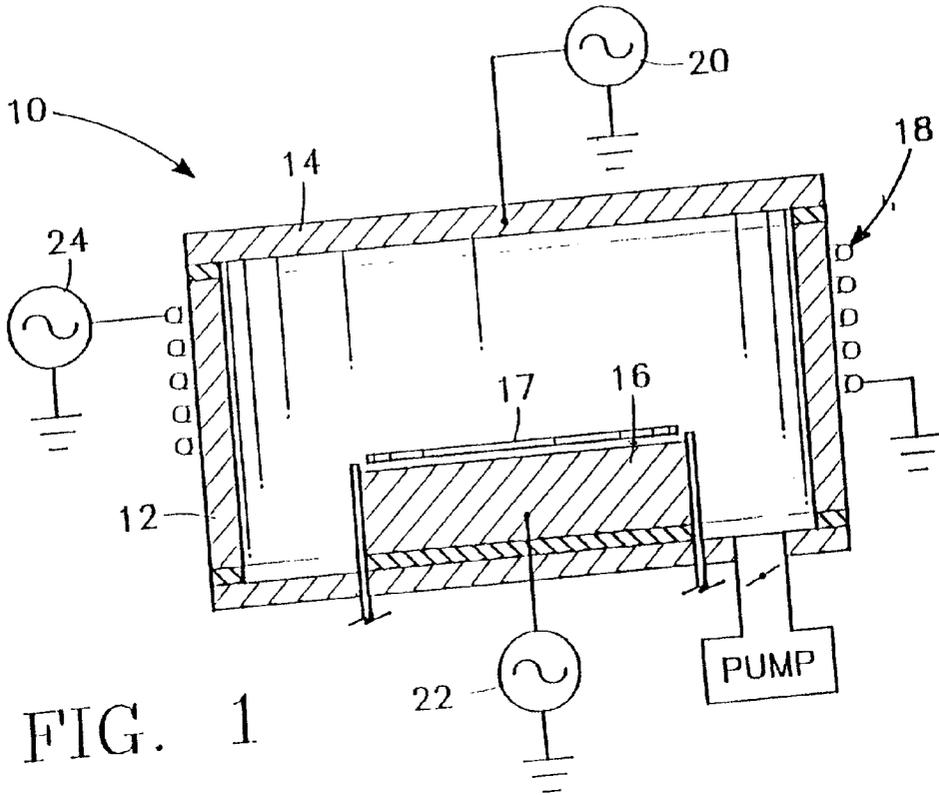


FIG. 1

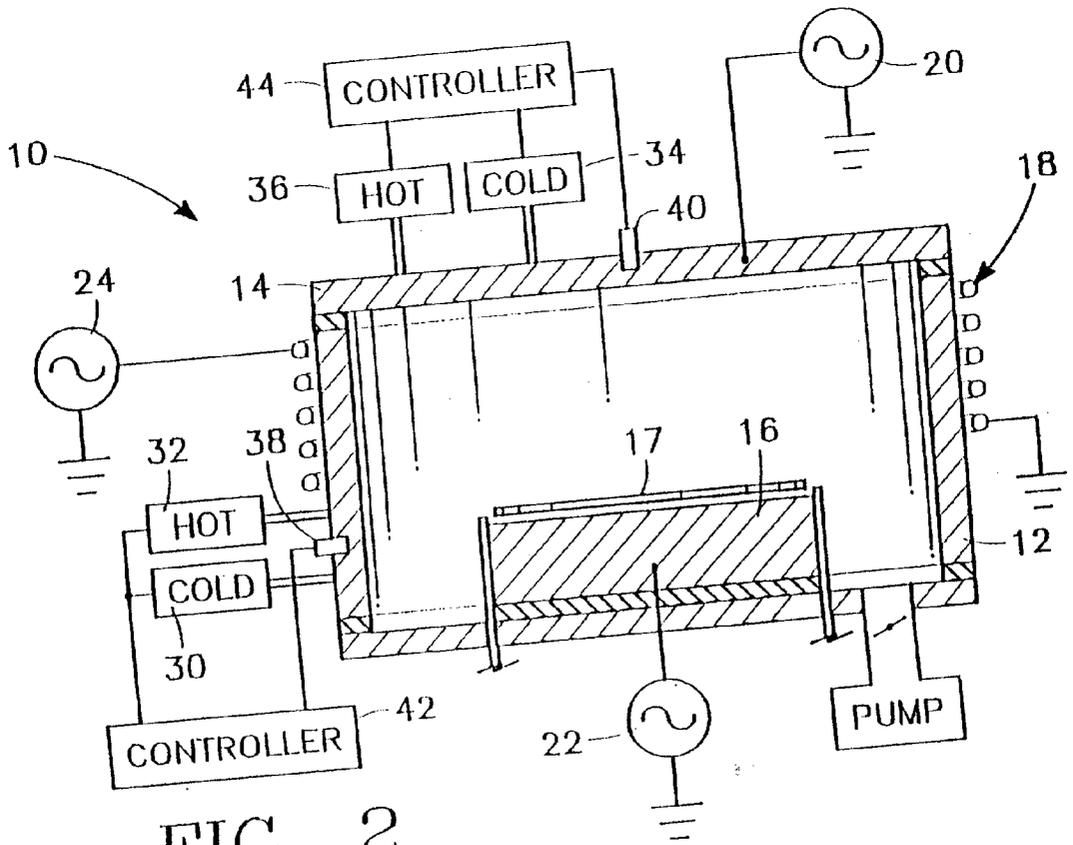


FIG. 2

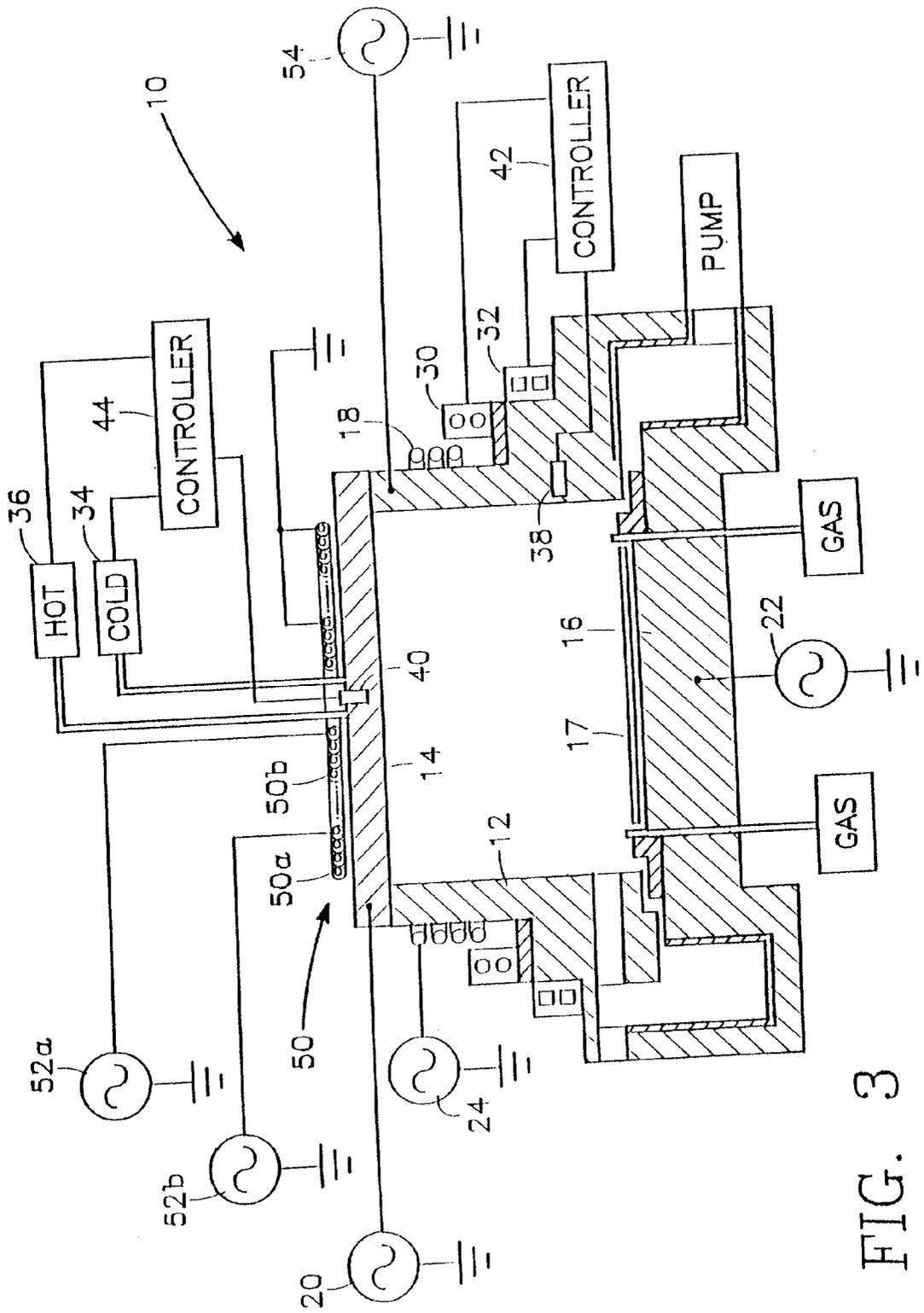


FIG. 3

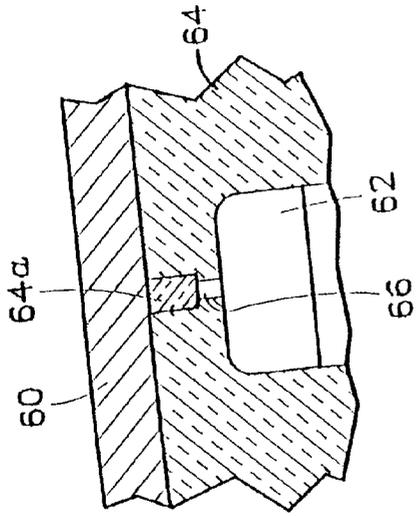


FIG. 4D

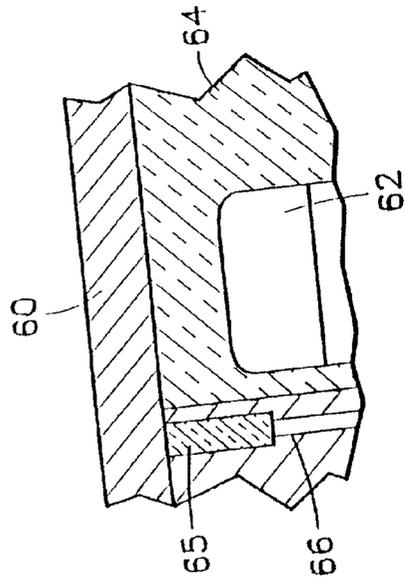


FIG. 4E

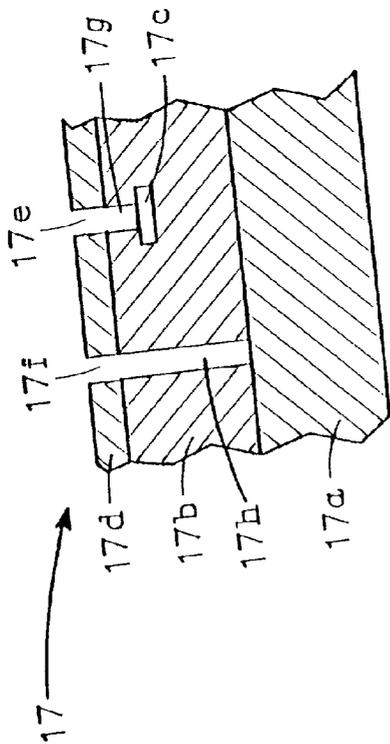


FIG. 4B

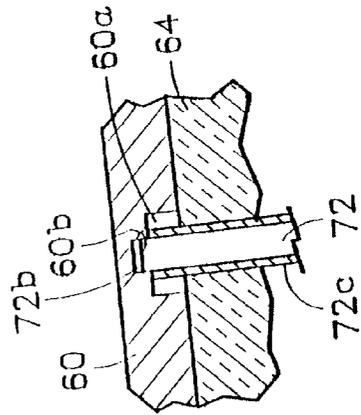


FIG. 4C

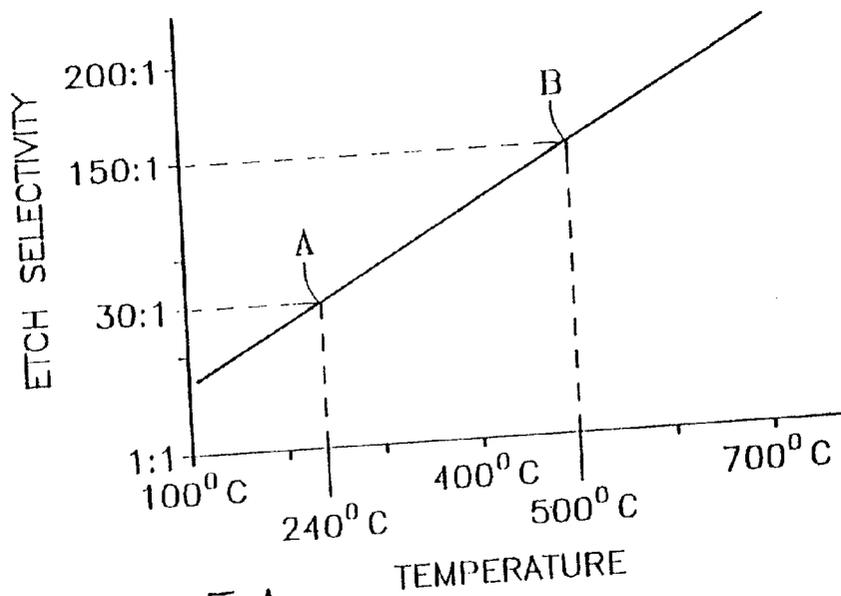


FIG. 5A

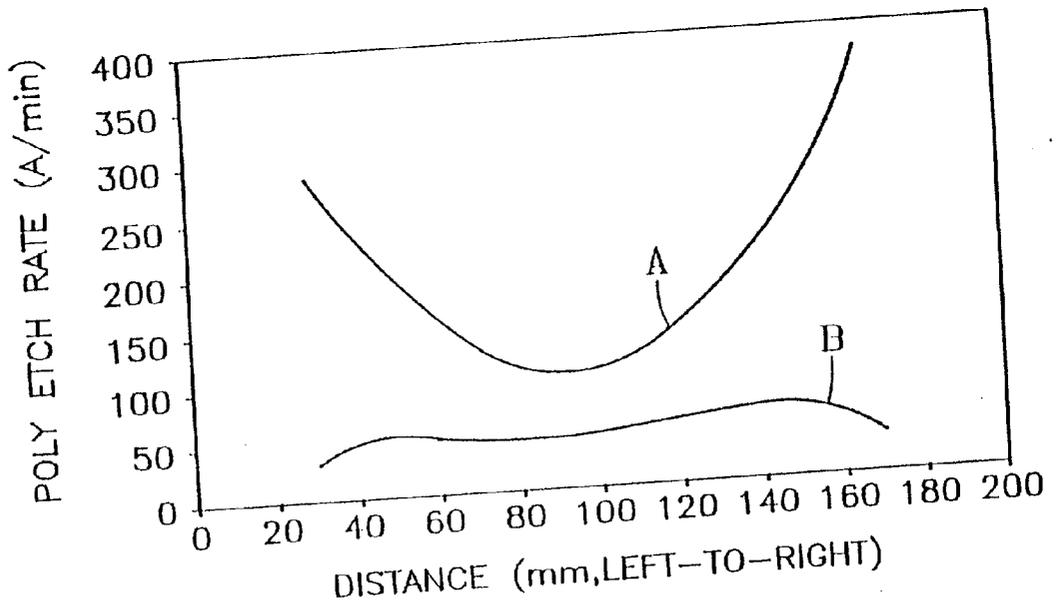


FIG. 5B

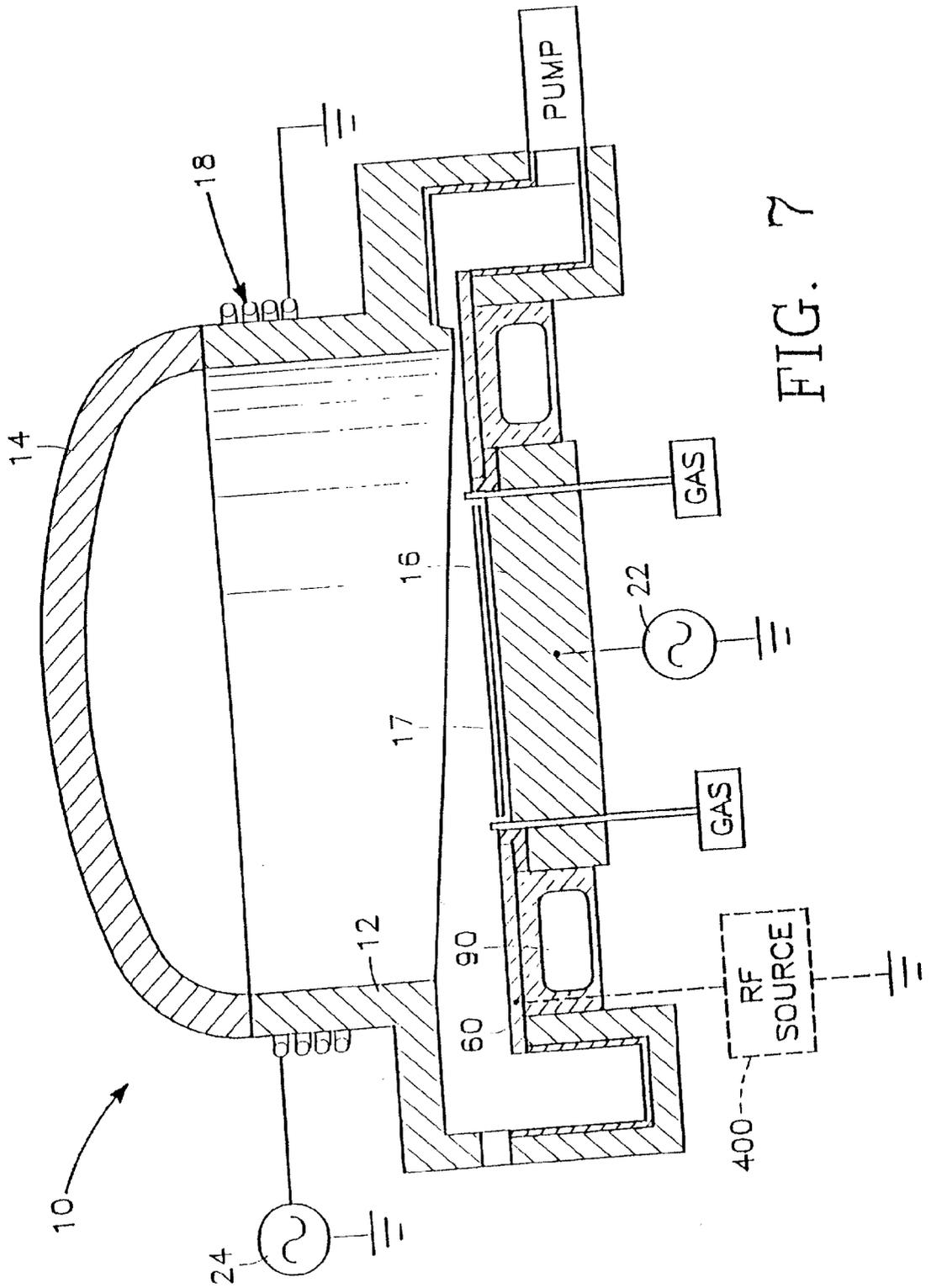


FIG. 7

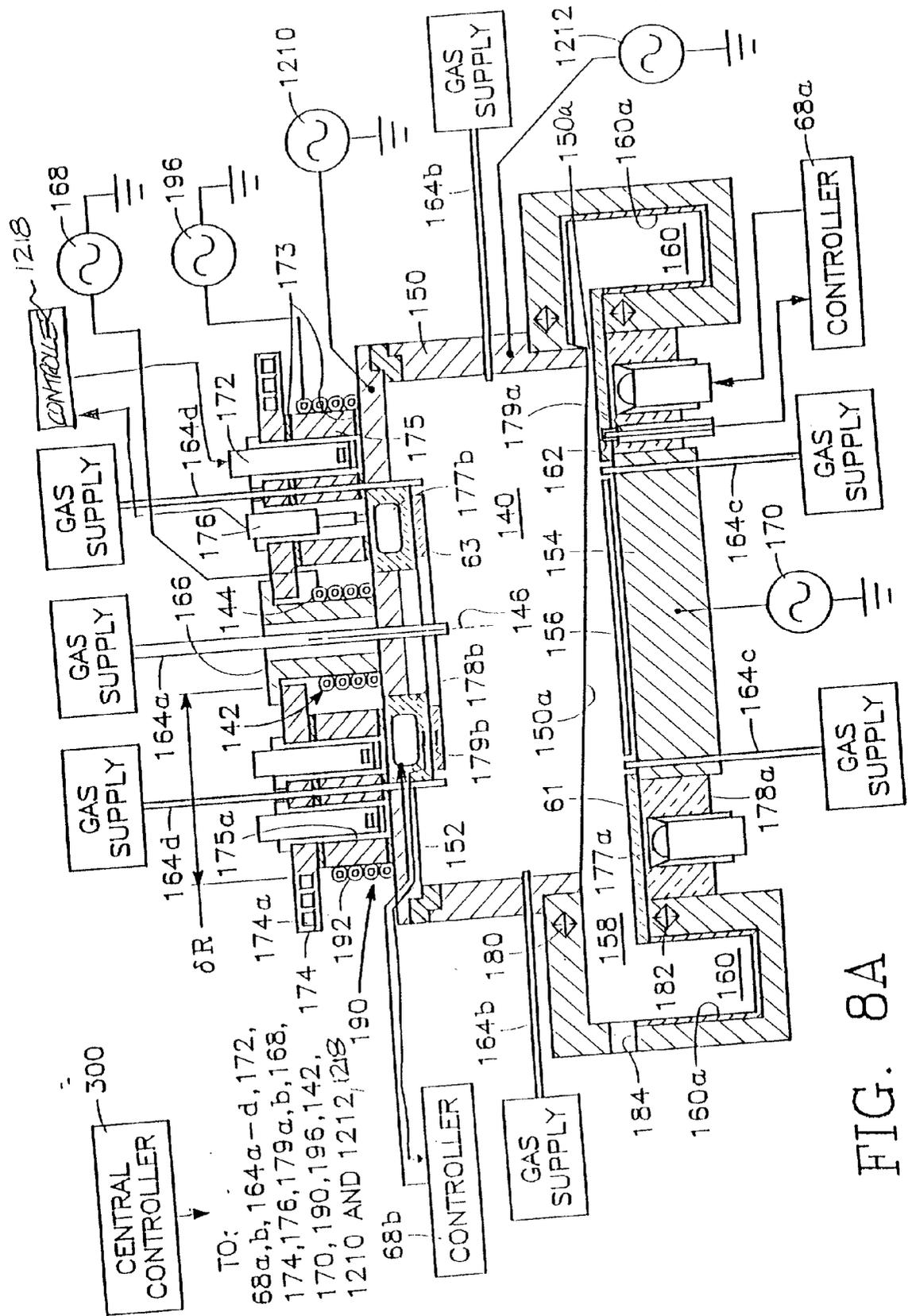


FIG. 8A

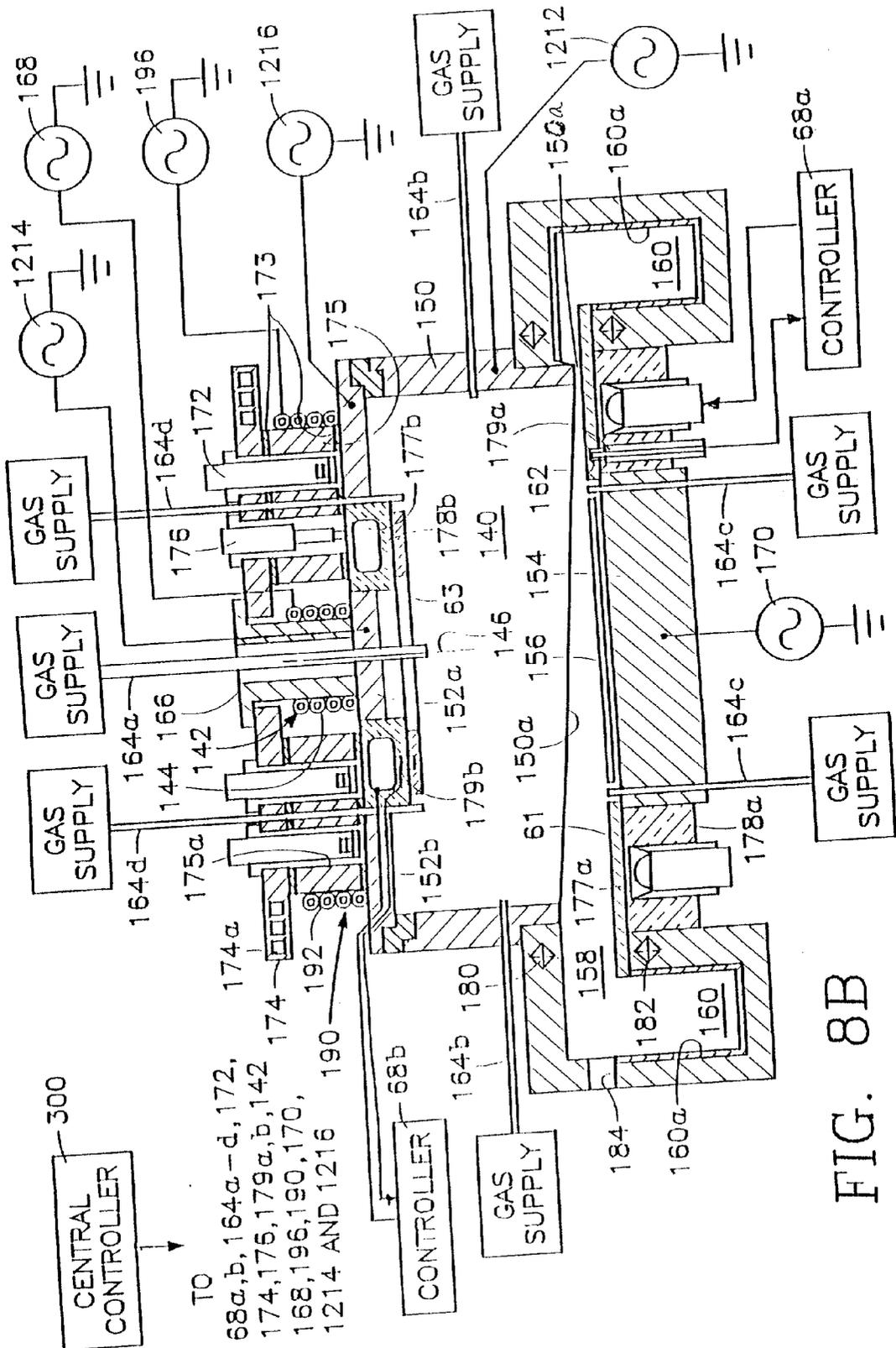


FIG. 8B

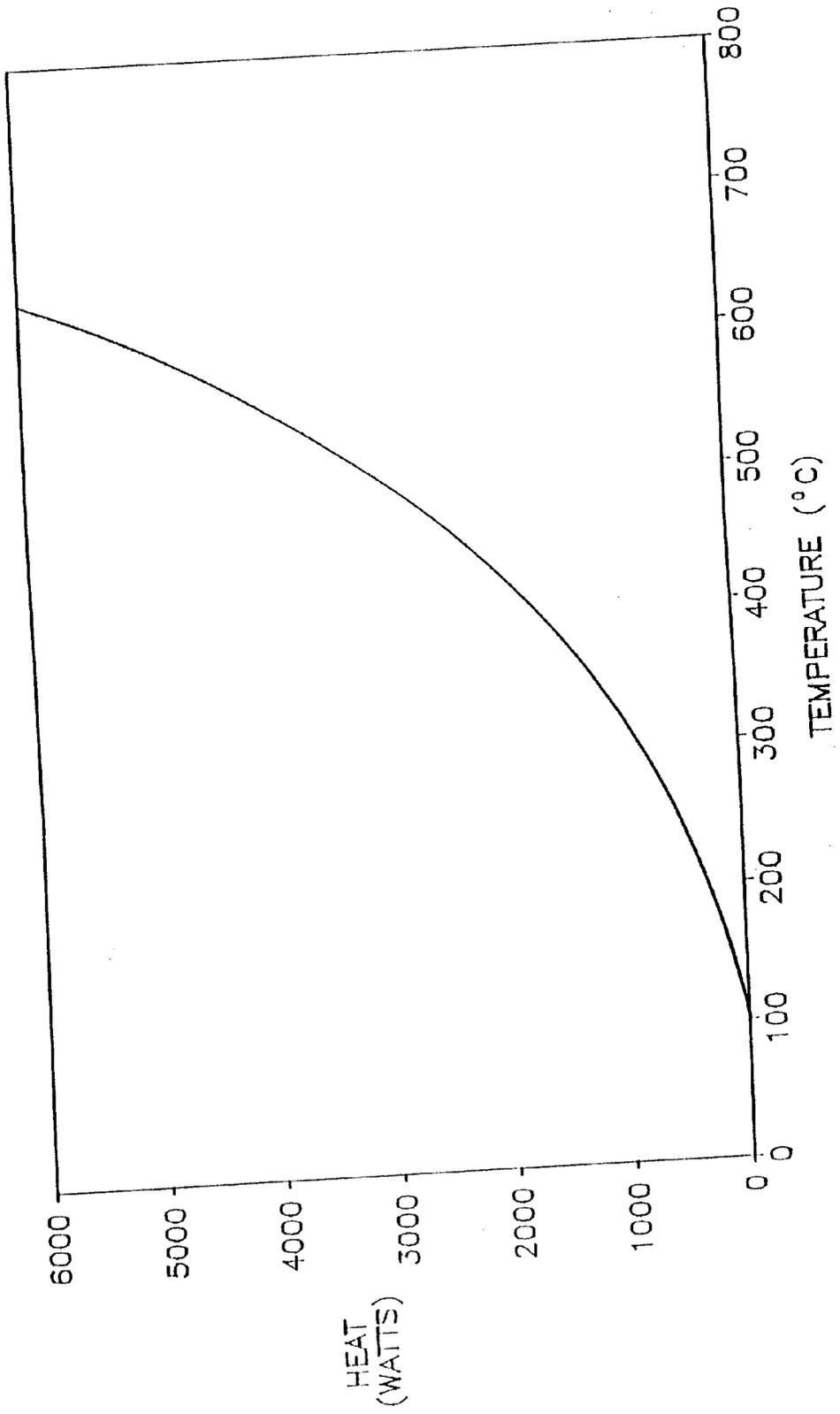


FIG. 10

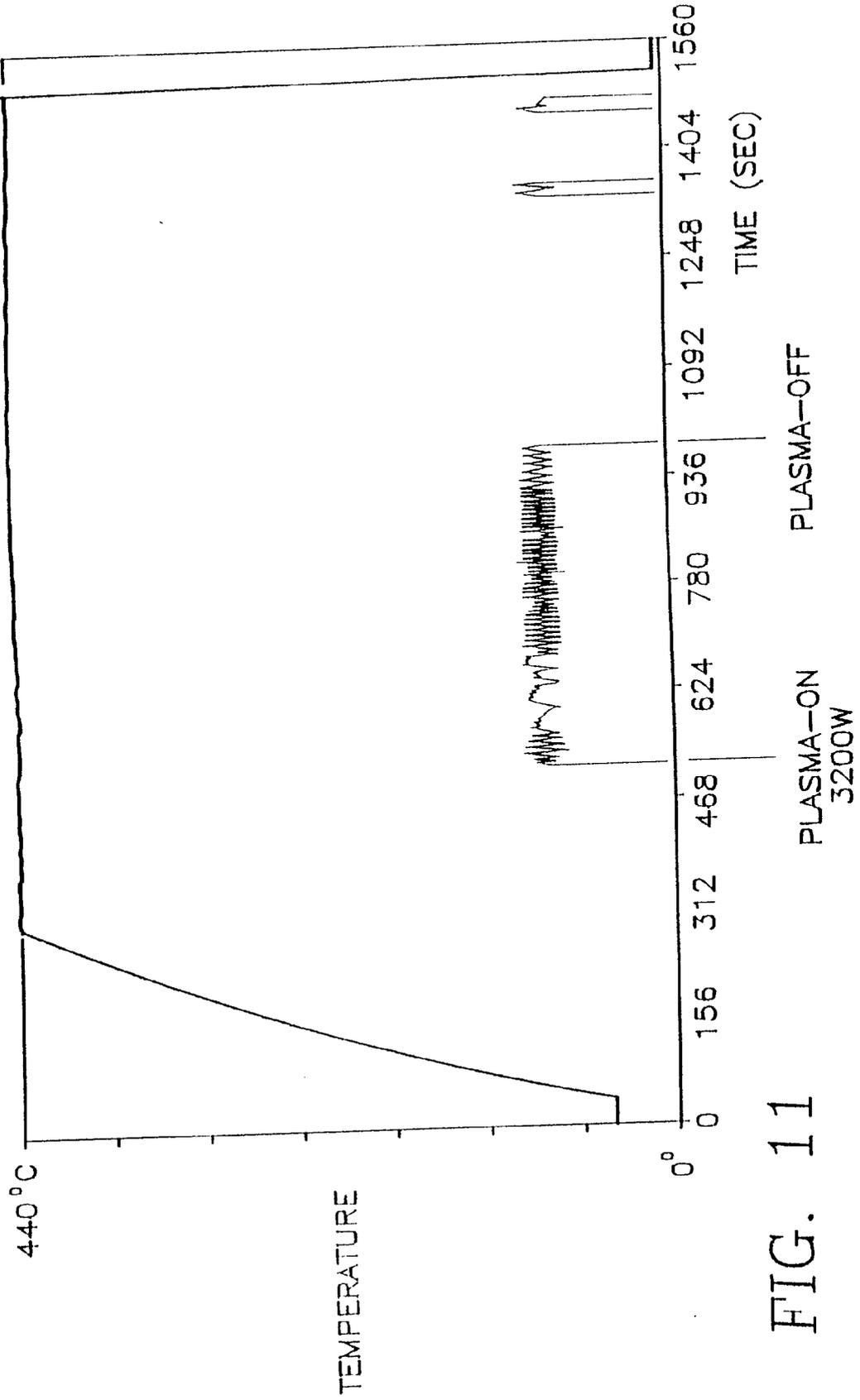


FIG. 11

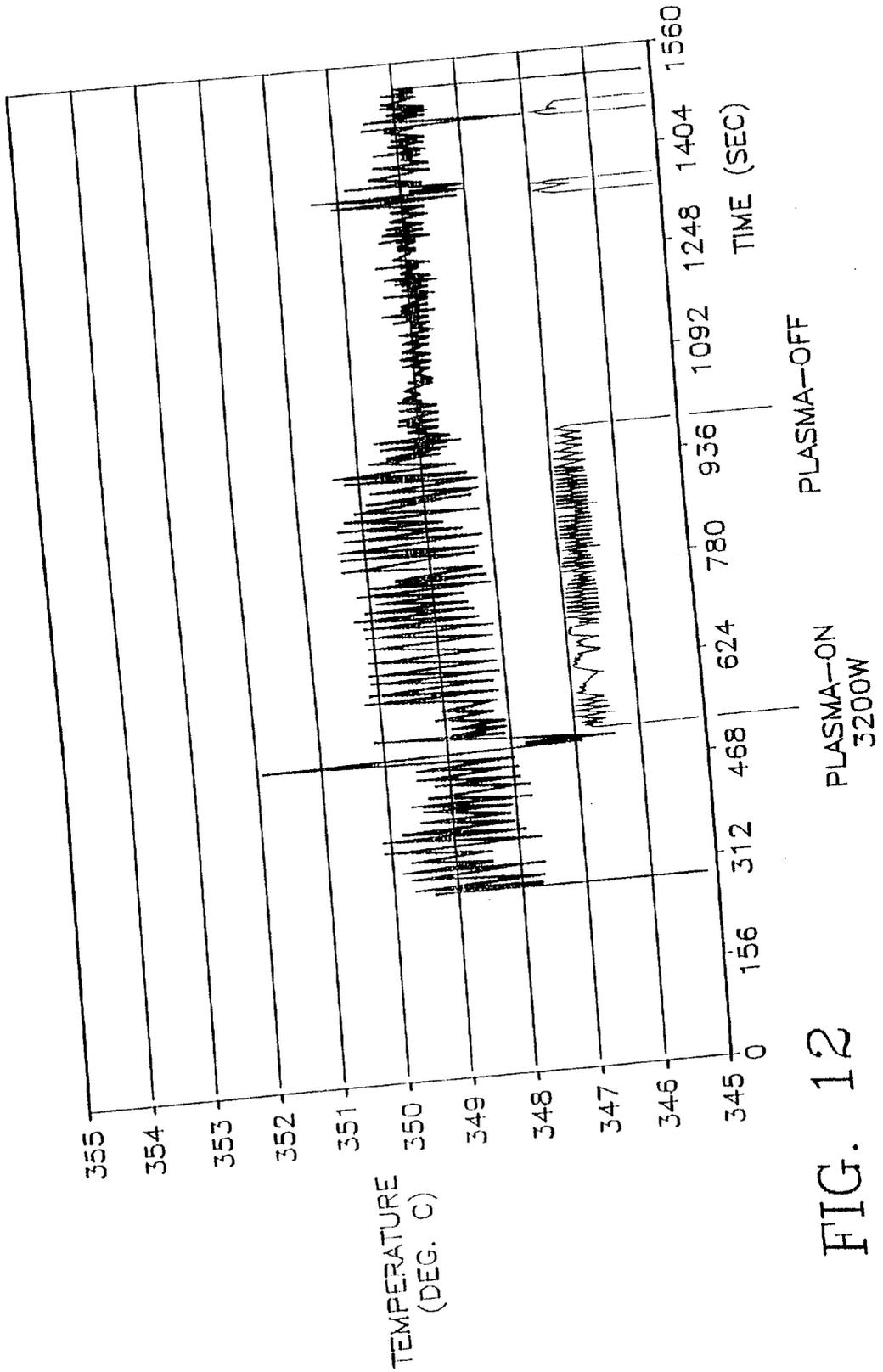


FIG. 12

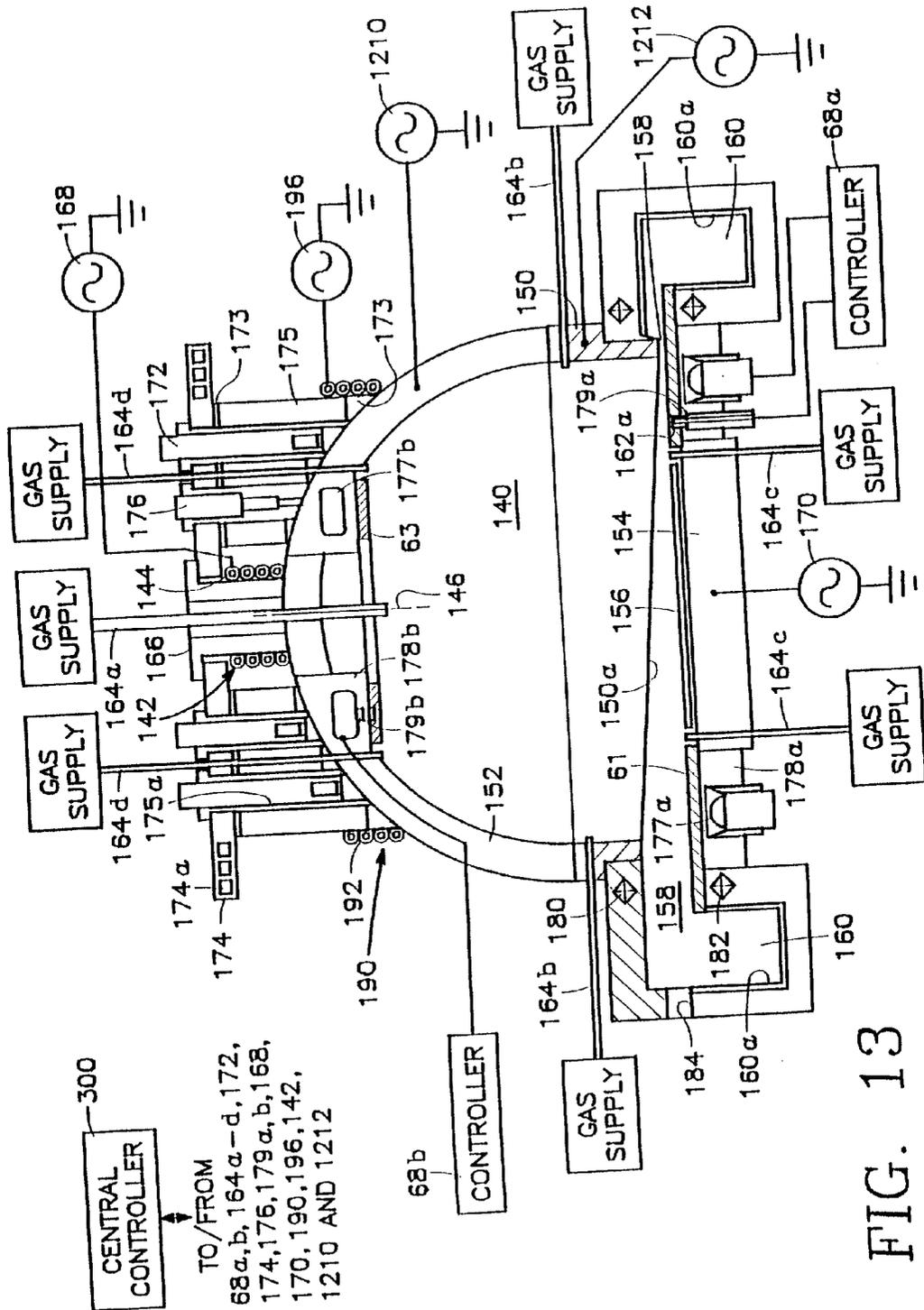


FIG. 13

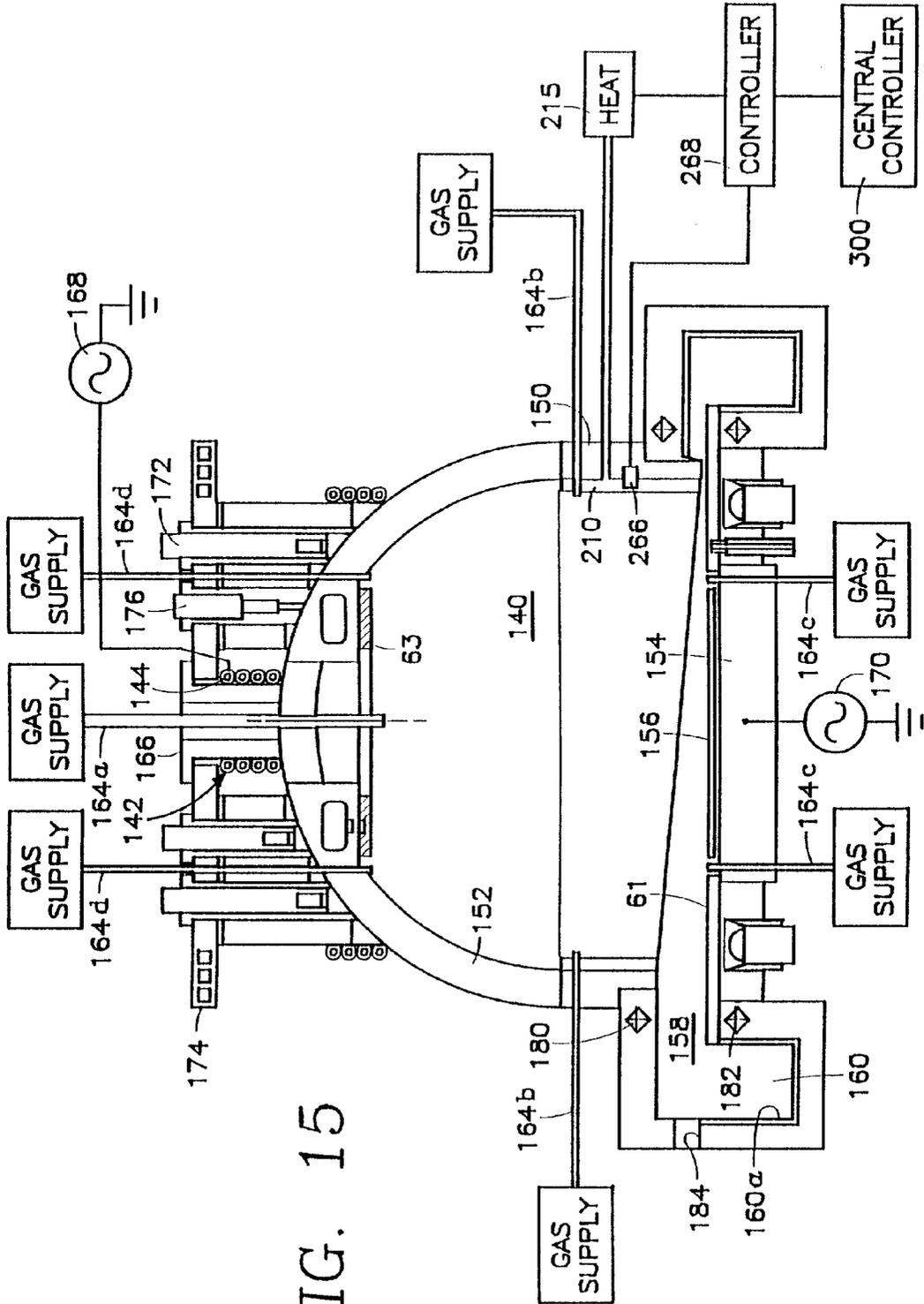


FIG. 15

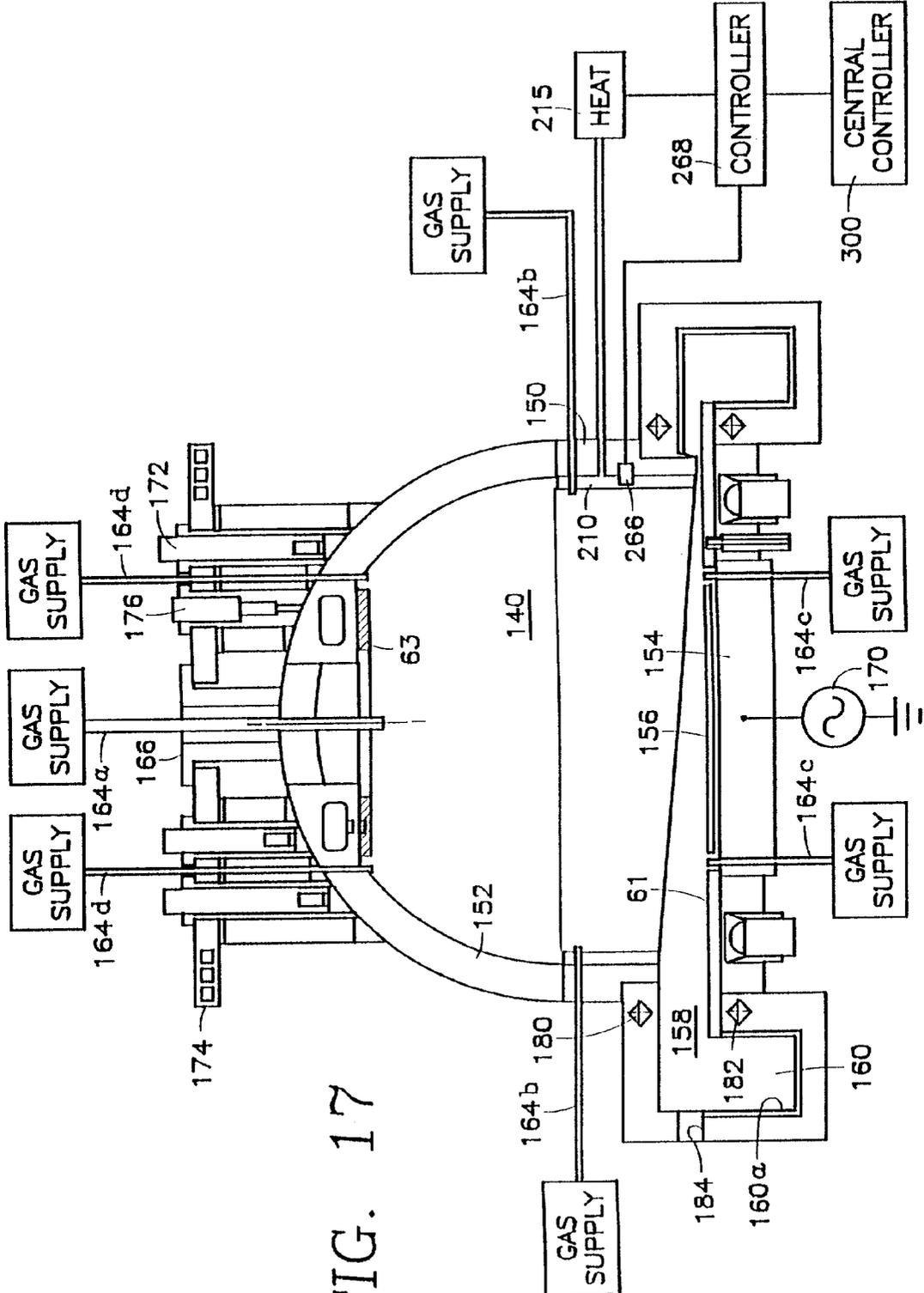


FIG. 17

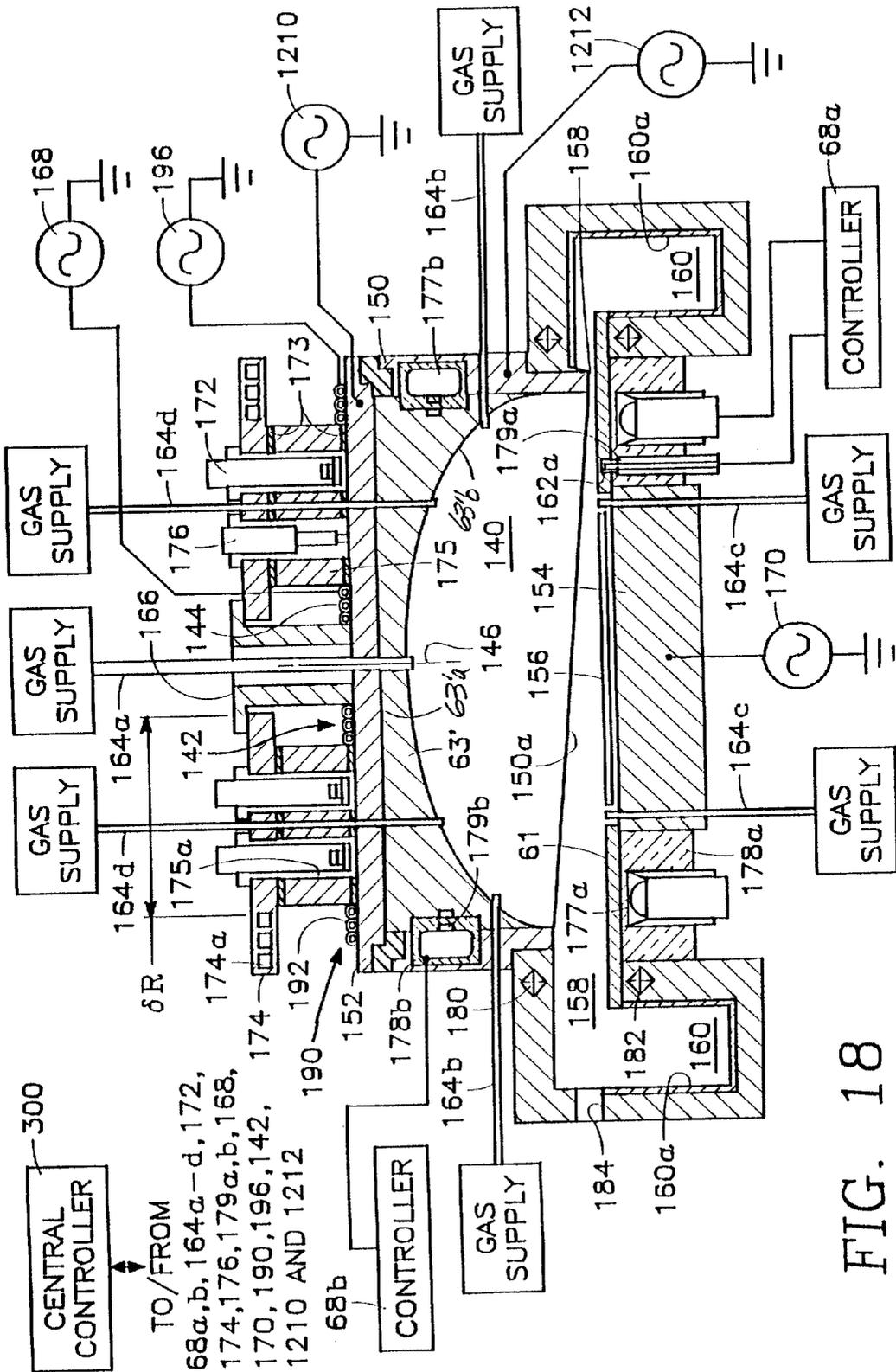


FIG. 18

LOW CEILING TEMPERATURE PROCESS FOR A PLASMA REACTOR WITH HEATED SOURCE OF A POLYMER-HARDENING PRECURSOR MATERIAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Ser. No. 08/734,797 filed Oct. 23, 1996 by Kenneth S. Collins et al., which is a continuation-in-part of U.S. Ser. No. 08/648,256 filed May 13, 1996 by Kenneth S. Collins et al., which is a continuation-in-part of the following co-pending U.S. applications, the disclosures of which are incorporated herein by reference:

[0002] (a) Ser. No. 08/580,026 filed Dec. 20, 1995 by Kenneth S. Collins et al. which is a continuation of Ser. No. 08/041,796 filed Apr. 1, 1993 which is a continuation of Ser. No. 07/722,340 filed Jun. 27, 1991;

[0003] (b) Ser. No. 08/503,467 filed Jul. 18, 1995 by Michael Rice et al. which is a divisional of Ser. No. 08/138,060 filed Oct. 15, 1993; and

[0004] (c) Ser. No. 08/597,577 filed Feb. 2, 1996 by Kenneth Collins, which is a continuation-in-part of Ser. No. 08/521,668 filed Aug. 31, 1995 (now abandoned), which is a continuation-in-part of Ser. No. 08/289,336 filed Aug. 11, 1994, which is a continuation of Ser. No. 07/984,045 filed Dec. 1, 1992 (now abandoned). In addition, U.S. application Ser. No. 08/648,254 filed May 13, 1996 by Kenneth S. Collins et al. entitled "Inductively Coupled RF Plasma Reactor Having Overhead Solenoidal Antenna" discloses related subject matter.

BACKGROUND OF THE INVENTION

[0005] 1. Technical Field

[0006] The invention is related to a plasma reactor for processing a workpiece such as a semiconductor wafer with a process employing an etch selectivity-enhancing precursor material such as polymer precursor gases.

[0007] 2. Background Art

[0008] 1. Background Art Relating to the Parent Application

[0009] High density RF plasma reactors for etching contact openings through silicon dioxide layers to underlying polysilicon conductor layers and/or to the silicon substrate of a semiconductor wafer are disclosed in the above-referenced application by Collins et al. Ideally, such a reactor carries out an etch process which quickly etches the overlying silicon dioxide layer wherever a contact opening is to be formed, but stops wherever and as soon as the underlying polysilicon or silicon material (or other non-oxygen-containing material such as silicon nitride) is exposed, so that the process has a high oxide-to-silicon etch selectivity. Such reactors typically include a vacuum chamber, a wafer support within the chamber, process gas flow inlets to the chamber, a plasma source coil adjacent the chamber connected to an RF power source usually furnishing plasma source power and another RF power source connected to the wafer support usually to furnish plasma bias power. For a

silicon oxide etch process, a process gas including an etchant such as a fluorine-containing substance is introduced into the chamber. The fluorine in the process gas freely dissociates under typical conditions so much that the etch process attacks not only the silicon oxide layer through which contact openings are to be etched, but also attacks the underlying polysilicon or silicon material as soon as it is exposed by the etch process. Thus, a typical etch process carried out by such a reactor is not the ideal process desired and has a lower oxide-to-silicon etch selectivity. As employed in this specification, the term "etch selectivity" refers to the ratio between the etch rates of two different materials, such as silicon dioxide and silicon (either crystalline silicon or polycrystalline silicon hereinafter referred to as "polysilicon"). A low etch selectivity can cause punch through. In etching shallow contact openings to intermediate polysilicon layers while simultaneously etching deep contact openings to the underlying silicon substrate, the etch process first reaches and will punch through the intermediate polysilicon layer before reaching the silicon substrate. A very high oxide-to-silicon etch selectivity is necessary to prevent the punchthrough, depending upon the ratio between the depths of the silicon substrate and the intermediate polysilicon layer through the silicon oxide. For example, if (a) the deep contact opening through the oxide to the substrate is 1.0 micron deep and is to be 50% overetched, (b) the intermediate polysilicon layer is 0.4 microns deep (below the top of the oxide layer) and (c) if not more than 0.01 microns of the intermediate polysilicon layer are to be removed (to avoid punch-through), then an oxide-to-silicon etch selectivity of at least 110:1 is required.

[0010] It is known that oxide-to-silicon etch selectivity is enhanced by a polymer film which forms more readily over silicon and polysilicon or other non-oxygen-containing layers than over silicon dioxide or other oxygen-containing layers. In order to form such a selectivity-enhancing polymer film, the fluorine-containing substance in the process gas is a fluorocarbon or a fluoro-hydrocarbon. Some of the fluorine in the process gas is consumed in chemically etching the silicon dioxide layer on the wafer. Another portion of the fluorine reacts with other species including carbon contained in the process gas to form a polymer on the surface of the wafer. This polymer forms more rapidly and strongly on any exposed silicon and polysilicon surfaces (or other non-oxygen-containing surfaces) than on silicon dioxide (or other oxygen-containing surfaces), thus protecting the silicon and polysilicon from the etchant and enhancing etch selectivity. Etch selectivity is further improved by improving the strength of the polymer formed on polysilicon surfaces. The polymer is strengthened by increasing the proportion of carbon in the polymer relative to fluorine, which can be accomplished by decreasing the amount of free fluorine in the plasma. For this purpose, a fluorine scavenger, such as a silicon piece, can be provided in the reactor chamber and heated to avoid being covered with polymer and additionally to permit silicon ions, radicals and/or neutral species to be removed therefrom and taken into the plasma. The silicon atoms removed from the scavenger combine with some of the free fluorine in the plasma, thereby reducing the amount of fluorine available to polymerize and increasing the proportion of carbon in the polymer formed on the wafer.

[0011] While the use of a fluorine scavenger such as a heated silicon piece inside the reactor chamber enhances

etch selectivity by strengthening the polymer formed on the wafer, even the etch selectivity so enhanced can be relatively inadequate for a particular application such as the simultaneous etching of contact holes of very different depths. Therefore, it would be desirable to increase the polymer strength beyond that achieved by the improved scavenging technique described above.

[0012] Another problem is that the rate of removal of silicon from the scavenger piece required to achieve a substantial increase in polymer strength is so great that the silicon piece is rapidly consumed and the consequent need for its replacement exacts a price in loss of productivity and increased cost. Typically the scavenger piece is a piece of silicon in the reactor chamber ceiling or wall or a piece of silicon near the reactor chamber ceiling. The rate of removal of silicon therefrom is enhanced by applying an RF bias potential to the silicon piece while its temperature is carefully controlled to prevent polymer deposition thereon and to control the rate of silicon removal therefrom. As disclosed in the above-referenced U.S. application Ser. No. 08/543,067, silicon is added into the plasma by a combination of applied RF bias and heating of the scavenger piece. The temperature control apparatus is integrated with the silicon piece so that replacement of the silicon piece (e.g., a silicon ceiling) is relatively expensive. In U.S. application Ser. No. 08/597,577 referenced above, an all-silicon reactor chamber is disclosed in which the walls and ceiling are silicon, and any fluorine scavenging is done by consuming the silicon ceiling or walls, requiring their replacement at periodic intervals with a concomitant increase in cost of operation and decrease in productivity. Thus, not only is it desirable to increase the polymer strength but it is also desirable to decrease the rate at which silicon must be removed from the scavenger to achieve a desired etch selectivity.

[0013] 2. Background Art Relating to the Present Application

[0014] The reactor structure described in the detailed description below in this specification includes a fluorine-scavenger precursor material (such as silicon or silicon carbide) either in the form of a ceiling or a disposable ring around the pedestal, or both. In order to readily provide a fluorine-scavenging species to the plasma, this material is heated to a desired temperature (generally above the condensation temperature of the polymer formed from the fluorine and carbon species in the plasma). While this has provided significant process advantages as described below, the continuing trend of ever smaller semiconductor device critical dimensions and greater competition in semiconductor price require more improvements in process performance and cost effectiveness. Specifically, it is now desired to obtain a deeper (high aspect ratio) etch depth at a faster etch rate. A deeper etch depth is required to meet continuing reductions in critical dimension or opening size, while the faster etch rate is required to meet higher production through-put demands for lower device cost. It is also desired to improve photoresist facet selectivity in silicon oxide plasma etching. Such an improvement would provide a greater margin of safety against removal of silicon dioxide material at the edge of an opening due removal ("faceting") of photoresist at the edge. It is further desired to better control the etch profile to obtain a 90° taper of the vertical walls of the etched opening. It is also desired to critical dimension variance across the wafer surface (e.g., center to

edge) to as low as 0.05 microns or less and to minimize silicon loss at the bottom of each etched opening to 800 angstroms or less. As yet another way of reducing costs, it is desired to reduce the cost of consumable materials in the reactor (such as the fluorine-scavenging precursor material of the ceiling). The present invention described below accomplishes all of the foregoing simultaneously.

[0015] For reactors of the type lacking a silicon or silicon-carbide ring around the pedestal as the fluorine-scavenger precursor material, the only fluorine-scavenger precursor material is a silicon reactor ceiling. In attempting to address the problem of through-put, the etch rate could be increased, theoretically, by reducing the ceiling temperature to reduce fluorine scavenging, thereby increasing the fluorine content of the plasma as well as the fluorine content of the protective polymer deposited on the wafer. A sufficient reduction in ceiling temperature would cause more polymer to deposit on the ceiling, thereby reducing the polymer deposition rate on the wafer. With such changes, the plasma would etch the silicon oxide layers faster and the high-fluorine content polymer itself would etch the silicon oxide layers, the combined effect of which is to significantly increase the rate at which silicon oxide is etched. However, this approach has not seemed feasible because the oxide etch selectivity would decrease due to the increase in fluorine content of the polymer condensed onto non-oxygen-containing surfaces. A polymer based upon C—F bonding is weaker than a polymer based primarily upon pure C—C bonding, so that a polymer containing more fluorine is weaker and provides less oxide-to-silicon selectivity. This latter disadvantage could be addressed by decreasing the plasma source power in order to enhance the oxide selectivity, but it would seem such a decrease would reduce the etch rate, so as to offset whatever etch rate gain was obtained by decreasing the roof temperature. Thus, a practical solution has not seemed to be attainable.

SUMMARY OF THE INVENTION

[0016] A high plasma density etch process for etching an oxygen-containing layer overlying a non-oxygen containing layer on a workpiece in a plasma reactor chamber, by providing a chamber ceiling overlying the workpiece and containing a semiconductor material, supplying into the chamber a process gas containing etchant precursor species, polymer precursor species and hydrogen, applying plasma source power into the chamber, and cooling the ceiling to a temperature range at or below about 150 degrees C. The etchant and polymer precursor species contain fluorine, and the chamber ceiling semiconductor material includes a fluorine scavenger precursor material. Preferably, the process gas includes at least one of CHF_3 and CH_2F_2 . Preferably, the process gas further includes a species including an inert gas, such as HeH_2 or Ar. If the chamber is of the type including a heated fluorine scavenger precursor material, this material is heated to well above the polymer condensation temperature, while the ceiling is cooled. In some cases, the plasma source power applicator is an inductive antenna overlying the semiconductor ceiling, and the ceiling has a cooling/heating apparatus contacting the ceiling through semiconductor rings. The inductive antenna in this case constitutes inductive elements between adjacent ones of the semiconductor rings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 is a simplified cut-away side view of a plasma reactor of the type disclosed in a first one of the co-pending applications referred to above.

[0018] FIG. 2 is a simplified cut-away side view of a plasma reactor of the type disclosed in a second one of the co-pending applications referred to above.

[0019] FIG. 3 is a simplified cut-away side view of a plasma reactor of the type disclosed in a third one of the co-pending applications referred to above.

[0020] FIG. 4A is a cut-away side view of a plasma reactor in accordance with a preferred embodiment of the present invention employing inductive heating of an expendable polymer-hardening precursor piece.

[0021] FIG. 4B is an enlarged cross-sectional view of the workpiece processed in a working example of the embodiment of FIG. 4, illustrating the multi-layer conductor structure of the workpiece.

[0022] FIG. 4C is an enlarged view corresponding to FIG. 4A illustrating a sleeve and counterbore in which an optical fiber is inserted.

[0023] FIG. 4D is an enlarged view corresponding to FIG. 4A illustrating a long wavelength optical window inside a heat transparent window.

[0024] FIG. 4E is an enlarged view corresponding to FIG. 4A illustrating a long wavelength window separate from a heat transparent window.

[0025] FIG. 5A is a graph illustrating oxide-to-silicon etch selectivity as a function of temperature of a polymer-hardening precursor ring.

[0026] FIG. 5B is a graph illustrating radial distribution of the polysilicon etch rate in angstroms/minute at temperatures of 240° C. and 500° C., respectively.

[0027] FIG. 6 is a cut-away view of a plasma reactor in accordance with another preferred embodiment of the invention employing radiant or infrared heating of an expendable polymer-hardening precursor piece.

[0028] FIG. 7 is a cut-away view of a plasma reactor in accordance with a preferred embodiment of the invention in which an expendable polymer-hardening precursor piece is heated in an all-semiconductor reactor chamber.

[0029] FIG. 8A is a cut-away side view of a plasma reactor in accordance with a preferred embodiment employing heated polymer-hardening precursor pieces at separate radial locations relative to the wafer being processed.

[0030] FIG. 8B corresponds to the embodiment of FIG. 8A in which the ceiling is divided into inner and outer portions.

[0031] FIG. 9 illustrates an embodiment of the invention in which the expendable polymer-hardening precursor piece is a removable liner abutting the cylindrical chamber side wall.

[0032] FIG. 10 is a graph illustrating the performance of a working example of a temperature control system in a reactor embodying the invention.

[0033] FIG. 11 is a graph illustrating the closed loop response of the temperature system whose performance is depicted in FIG. 10.

[0034] FIG. 12 is an enlarged view of a portion of the graph of FIG. 11.

[0035] FIG. 13 illustrates an embodiment corresponding to FIG. 8A but having a dome-shaped ceiling.

[0036] FIG. 14 illustrates an embodiment corresponding to FIG. 8B but having a dome-shaped ceiling.

[0037] FIG. 15 illustrates an embodiment corresponding to FIG. 9 but having a dome-shaped ceiling.

[0038] FIG. 16 illustrates an embodiment corresponding to FIG. 8A in which plasma source power is capacitively coupled rather than inductively coupled.

[0039] FIG. 17 illustrates an embodiment corresponding to FIG. 9 in which plasma source power is capacitively coupled rather than inductively coupled.

[0040] FIG. 18 illustrates a modification of the embodiment of FIG. 8A in which the polymer-hardening precursor ring is replaced by a polymer-hardening precursor chamber liner over the chamber ceiling.

[0041] FIG. 19 illustrates a modification of the embodiment of FIG. 18 adopting the feature of FIG. 8B in which the ceiling is divided into radially inner and outer (disk and annular) portions.

[0042] FIG. 20 illustrates a modification of the embodiment of FIG. 18 replacing the solenoid antenna coils with the flat antenna coils of the embodiment of FIG. 3.

[0043] FIG. 21 illustrates a modification of the embodiment of FIG. 20 adopting the feature of FIG. 8B in which the ceiling is divided into radially inner and outer (disk and annular) portions.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0044] 1. Description of the Parent Application

[0045] Referring to FIG. 1, the above-referenced co-pending U.S. application Ser. No. 08/580,026 discloses a plasma reactor chamber 10 having a cylindrical side wall 12, a flat ceiling 14, a wafer support pedestal 16 for supporting a workpiece 17 being processed such as a semiconductor wafer, an inductive side coil 18 wound around the cylindrical side wall 12 and independent RF power sources 20, 22, 24 connected to the ceiling 14, the pedestal 16 and the inductive coil 18, respectively. In particular, the co-pending application of Collins et al. discloses that the ceiling 14 may comprise silicon in order to provide a fluorine scavenger. For this purpose, RF power is applied to the silicon ceiling 14 by the RF power source 20 to enhance the removal of silicon therefrom.

[0046] Referring to FIG. 2, the above-referenced co-pending application by Rice et al. discloses that the side wall 12 is quartz and provides a temperature control system for controlling the temperature of the quartz side wall 12 and the temperature of the silicon ceiling 14. The temperature control system includes a cooling source 30 and heating source 32 coupled to the quartz side wall 12 and a cooling source 34 and heating source 36 coupled to the silicon ceiling 14.

Temperature sensors **38**, **40** coupled to the side wall **12** and ceiling **14**, respectively, are monitored by controllers **42**, **44**, respectively. The controller **42** governs the cooling source **30** and heating source **32** of the quartz side wall **12** while the controller **44** governs the cooling source **34** and heating source **36** of the silicon ceiling. The purpose for controlling the temperature of the silicon ceiling **14** is, at least in part, to prevent polymer accumulation on the ceiling **14** which would otherwise prevent the ceiling **14** from donating scavenger silicon to the plasma. Therefore, controller **44** maintains the ceiling temperature somewhat above the polymer condensation (or polymerization) temperature, or about 170° C. depending upon processing conditions. At the same time, the RF power source **20** applies sufficient RF power to the silicon ceiling **14** in order promote removal of silicon from the ceiling **14** by the plasma at a sufficient rate to scavenge the desired amount of fluorine for enriching the carbon content of the polymer formed on the wafer to enhance etch selectivity. In fact, the combination of elevated temperature and applied RF bias overcomes the energy threshold below which interaction between the plasma and the ceiling **14** causes polymer deposition and above which the interaction causes etching of the ceiling **14**.

[0047] Referring to FIG. 3, the above-referenced co-pending application Ser. No. 08/597,577 by Kenneth S. Collins discloses that both the ceiling **14** and the side wall **12** are a semiconductor such as silicon and that they can act as windows to permit inductive coupling of RF source power through themselves to the plasma. For this reason, either one or both the side coil **18** and an overhead inductor **50** may be employed and couple RF source power to the plasma through the silicon side wall **12** and the silicon ceiling **14**. U.S. application Ser. No. 08/597,577 disclosed a planar overhead coil and such would be suitable for carrying out the present invention. However, the overhead inductor **50** of the embodiment of FIG. 3 includes inner and outer solenoids **50a**, **50b** (of the type disclosed in above-referenced co-pending U.S. application Ser. No. by Kenneth S. Collins et al. entitled "Inductively Coupled RF Plasma Reactor Having Overhead Solenoidal Antenna") separately powered by independent RF power sources **52a**, **52b** to facilitate process uniformity control. Furthermore, both the ceiling **14** and side wall **12** can be employed as separate electrodes, so that RF power is applied to the silicon side wall **12** by a separate RF power source **54**. Sufficient RF power is applied to either or both the silicon ceiling **14** and the silicon side wall **12** to promote removal of silicon therefrom for scavenging fluorine. The side wall **12** and ceiling **14** are preferably maintained above the polymer condensation temperature to permit their use as silicon scavenger precursors and to avoid the usual requirement for frequent chamber cleaning operations to remove polymer and associated contaminant deposits.

[0048] A first embodiment of the present invention is a process which does not merely enrich the carbon content of the carbon-fluorine polymer, but actually forms a different kind of polymer which more strongly adheres to the underlying silicon, polysilicon or similar non-oxygen-containing surfaces to be protected. The result is a revolutionary improvement in etch selectivity. It is a discovery of the invention that certain materials in a class including silicon, silicon carbide, graphite, silicon nitride, when raised to a higher temperature range (e.g., well above the polymer condensation temperature) become polymer-hardening pre-

cursors in which they change the chemical structure of the polymer, resulting in a polymer which is far more resistant to etching than has been provided in the prior art. The process is carried out by maintaining the temperature of a polymer-hardening precursor material inside the reactor chamber at a higher temperature range (e.g., 180° C. to 220° C. for a silicon precursor material whose potential is floating and in any case substantially above the applicable polymer condensation temperature). This higher temperature range varies greatly with the applied RF bias potential on the polymer-hardening precursor material and with the selection of the material itself.

[0049] In a second embodiment of the invention, the polymer-hardening precursor material is held in a maximum temperature range at which an even greater polymer hardness is achieved. The maximum temperature range for a silicon precursor material held at a floating potential is above 220° C. and is preferably in the range from about 300° C. to about 700° C. This maximum temperature range varies greatly with the RF bias applied to the polymer-hardening precursor material. While not necessarily subscribing to any particular theory in this specification, it is felt that, in some case but not necessarily all, at the maximum temperature range of the polymer-hardening precursor material, the polymer-hardening precursor (e.g., silicon) material removed therefrom by the plasma bonds with the fluorine, carbon and hydrogen atoms (assuming a fluoro-hydrocarbon gas is employed) as they polymerize, the material (e.g., silicon) thus added providing a different kind of polymer having an optimum resistance to etching. In some cases, the polymer thus produced in this second embodiment is distinguished by a shiny surface.

[0050] At the higher temperature range, the heated polymer-hardening precursor material (e.g., in the silicon ceiling **14** in the present example): (1) reduces free fluorine in the plasma by providing scavenging fluorine to the plasma, (2) changes the relative concentrations of carbon to fluorine and hydrogen in the plasma, (3) changes the relative concentrations of etchant species and polymer precursor species in the plasma near the wafer surface. At the maximum temperature range, the heated polymer-hardening precursor material performs (1)-(3) above and (4) contributes polymer-hardening precursor (silicon) material into the polymer, producing a polymer having a resistance to etching beyond what has been heretofore attained in the art.

[0051] Efficacy of the invention is seen, for example, in the photoresist selectivity achieved by the invention, although similar improvement in silicon-to-silicon oxide selectivity is also achieved (as described later in this specification). When the polymer hardening precursor material (silicon) is heated to 300° C., sputtering effects are observed at the photoresist facets or corners of features covered by photoresist, and the etch selectivity of oxide to photoresist (the "photoresist selectivity") is only about 3:1. If the polymer hardening precursor material is heated further to about 430° C., then the photoresist selectivity jumps to about 5:1, a significant improvement. If the polymer hardening precursor material temperature is increased even further to about 560° C., then the photoresist selectivity increases to about 6:1.

[0052] Carrying out the invention in the reactor chamber of FIGS. 1, 2 or 3 can be accomplished by employing the

silicon ceiling 14 or silicon side wall or skirt 12 as the polymer-hardening precursor material and increasing the temperature of the silicon ceiling 14 of FIGS. 1, 2 or 3 (and/or the silicon side wall 12 of FIG. 3) to the requisite temperature. The silicon ceiling 14 (and/or silicon side wall 12), when heated to the higher temperature range of the present invention, becomes a polymer-hardening precursor.

[0053] One problem in using the silicon ceiling 14 (or silicon side wall 12) as a fluorine scavenger precursor is that it is consumed at a rate determined at least in part by the amount of RF power coupled to it and must therefore be replaced at more frequent intervals. (RF power can be coupled to the scavenger precursor either directly from an RF power generator or indirectly by capacitive coupling from other chamber surfaces having RF power applied directly thereto.) Because the ceiling 14 (and/or side wall 12) is integrated with the temperature control system described above, its replacement entails loss of productivity due to the amount of labor required to remove and replace it, as well as a cost to acquire a new silicon ceiling 14 connectable to the temperature control apparatus. The present invention solves this problem because the process of the invention can further include reducing the RF bias applied by the RF power source 20 to the ceiling 14 (or reducing the RF power applied by the RF power source 22 to the silicon side wall of FIG. 3) while further increasing the silicon ceiling (and/or side wall) temperature to compensate for the reduction in RF bias power. The advantage of this latter feature is that the rate at which silicon is removed from the ceiling 14 (and/or side wall 12) is reduced with the reduction in applied RF power to the ceiling. In one example, the RF power applied by the RF power source 20 to the ceiling 14 may be reduced four-fold while the temperature of the ceiling 14 is increased only moderately from about 200° C. to about 240° C. Thus, the invention provides dual advantages of (a) revolutionary improvement in polymer resistance to etching and (b) reduced consumption rate of the silicon material in the ceiling or side wall. The increased polymer durability results in an increased etch selectivity while the decreased silicon consumption rate results in decreased cost of operation and decreased loss in productivity.

[0054] Even though the invention permits a reduction in consumption rate of the polymer-hardening precursor piece (e.g., the silicon ceiling), its replacement is nevertheless expensive and time-consuming due at least in part to its integration with the temperature control apparatus for maintaining the requisite temperature of the piece in accordance with the polymer-hardening process of the present invention. However, the invention is preferably carried out with a separate cheaply fabricated quickly replaceable polymer-hardening precursor piece, to avoid consuming any of the integral parts of the reactor chamber such as the chamber side wall or the chamber ceiling. Such a replaceable polymer-hardening precursor piece can be of any suitable easily fabricated shape (e.g., planar annulus, planar ring, solid ring, cylinder, plate, and so forth) and placed at any suitable location within the reactor chamber. However, in the embodiment of FIG. 4A, the expendable polymer-hardening precursor piece is a thin planar annular ring 60 of a polymer-hardening precursor material (such as silicon) surrounding a peripheral portion of the wafer pedestal 16. While the ring 60 can lie in any suitable plane within the chamber, in order to permit access to the wafer by a conventional wafer

transfer mechanism the silicon ring 60 lies slightly below or nearly in the plane of the wafer 17 held on the wafer pedestal 16.

[0055] In order to eliminate any necessity of integrating or mechanically coupling the polymer-hardening precursor ring 60 with a direct temperature control apparatus, heating by a method other than direct conduction (e.g., radiant heating or inductive heating) is preferably employed. A radiant heat source such as a tungsten halogen lamp or an electric discharge lamp may be employed. A radiant or inductive heat source can be internal—unseparated from the ring 60, or it can be external—separated from the ring 60 by a transmissive window for example. In the embodiment of FIG. 4A, an external inductive heater is employed constituting an inductive coil 62 separated from the polymer-hardening precursor ring 60 by a window 64 of a material such as quartz which is at least nearly transparent for purposes of inductive coupling. In order to provide the most efficient inductive heating, the polymer-hardening precursor ring 60 is formed of silicon having a sufficiently low resistivity, for example on the order of 0.01 Ω -cm. The following is an example illustrating how to select the resistivity of a silicon version of the ring 60. If: (a) the thickness T of the ring 60 must be about 0.6 cm (0.25 in) for structural-mechanical purposes, (b) the inductive heater coil 62 is driven at a frequency of 1.8 Mhz, (c) an RF skin depth $\delta = \Gamma T$ (for example, $\Gamma = 1$) is desired for optimum absorption efficiency, and (d) the silicon ring 60 has a magnetic permeability μ , then the maximum resistivity of the silicon ring 60 is given by:

$$\rho = \delta^2 \pi f \mu$$

[0056] which in the foregoing example is 0.029 Ω -cm. The present invention has been implemented using 0.01 Ω -cm silicon. In the case of a semiconductor such as silicon, there is no risk of falling short of the minimum resistivity in this case and so no computation of the minimum resistivity is given here.

[0057] In a working example corresponding to the embodiment of FIG. 4A, 4000 Watts of source power at 2.0 Mhz was applied to the inductive coil 18, 1400 Watts of bias power at 1.8 Mhz was applied to the wafer pedestal 16, process gases of CHF_3 and CO_2 were introduced into the reactor chamber at flow rates of 120 sccm and 46 sccm, respectively, while the chamber pressure was maintained at 50 Mtorr, the ceiling temperature was maintained at 200° C. and the side wall temperature was maintained at 220° C. The polymer-hardening precursor ring 60 was crystalline silicon and reached a temperature in the range of between 240° C. and 500° C. The polymer deposited onto the silicon and polysilicon surfaces on the wafer 17 was characterized by the shinier appearance of a polymer hardened by the process of the present invention.

[0058] The semiconductor wafer 17 processed in this working example had the multi-layer conductor structure illustrated in FIG. 4B consisting of a silicon substrate 17a, a silicon dioxide layer 17b and a polysilicon conductor line 17c, the etch process being facilitated by a photoresist layer 17d having mask openings 17e, 17f defining the openings 17g, 17h etched through the silicon dioxide layer 17b down to the polysilicon conductor 17c and the substrate 17a, respectively. A very high oxide-to-silicon etch selectivity is necessary to prevent the punchthrough, depending upon the

ratio between the depths of the silicon substrate and the intermediate polysilicon layer through the silicon oxide. For the case in which the deep contact opening **17h** through the oxide to the substrate is 1.0 micron deep and is to be 50% overetched, the intermediate contact opening **17g** to the polysilicon layer is 0.4 microns deep and not more than 0.01 microns of the intermediate polysilicon conductor layer **17c** are to be removed (to avoid punch-through), then an oxide-to-silicon etch selectivity of at least 110:1 is required.

[0059] By increasing the temperature of the silicon ring **60** over the processing of successive wafers, it was found that oxide-to-silicon etch selectivity generally increased with temperature in the manner illustrated in the graph of **FIG. 5A**. The two data points A and B of **FIG. 5A** correspond to the curves A and B of **FIG. 5B** illustrating radial distribution of the polysilicon etch rate in angstroms/minute at temperatures of 240° C. and 500° C., respectively. The etch selectivities of data points A and B of **FIG. 5A** were computed from the oxide etch rate of 9,000 angstroms/minute observed at both temperatures as an etch selectivity of 30:1 at 240° C. and 150:1 at 500° C. Thus, increasing the temperature to 500° C. provides a selectivity well-above the 110:1 minimum selectivity required in the above-given working example of **FIG. 4B**.

[0060] In the embodiment of **FIG. 4A**, the temperature of the polymer-hardening precursor ring **60** is sensed by a temperature-sensing device **66** which is not attached to the silicon ring **60**. A controller **68** governing the current or power flow through the inductor **62** monitors the output of the temperature-sensing device **66** in order to maintain the temperature of the polymer-hardening precursor ring **60** at the desired temperature. Preferably, the temperature-sensing device **66** is a radiant temperature sensor which responds to radiation from the ring **60** within a particular wavelength range. Such a radiant temperature sensor may be an optical pyrometer responsive to thermal radiation or a fluoro-optical probe which responds to optical pulse-stimulated emission. For this purpose, the window **64** is of a material which is at least sufficiently transmissive within the wavelength range of the sensor **66** to provide an optical signal-to-noise ratio adequate to enable temperature control of the ring **60**. Preferably, and in addition, the material of the window **64** (over its range of operating temperatures) does not thermally radiate strongly (relative to the radiation from the silicon ring **60**) within the wavelength range of the sensor **66**, so that the radiation of the window **64** is practically invisible to the sensor **66** so as to not interfere with its measurement of the silicon ring temperature.

[0061] If the polymer-hardening precursor ring **60** is silicon, then one difficulty in measuring its temperature by an optical pyrometer is that the thermal emissivity of silicon varies with temperature. (The silicon emissivity also happens to vary with wavelength and doping level, although it is the temperature dependence of the emissivity that is addressed here.) One solution to this problem is to bond a small piece **70** of a black-body or gray-body radiating material such as silicon nitride to the ring **60**. Preferably an optical fiber **72** (indicated in dashed line) is placed with one end **72a** facing a sensing portion **74** of the sensor **66** and the other end **72b** facing the gray-body radiator piece **70** bonded to the ring **60**. (If a black-body or gray-body radiating material is not added, then the long-wavelength radiation emitted by the silicon ring **60** at lower (e.g., room) tempera-

tures can be carried by the optical fiber **72** provided the fiber **72** is a long wavelength material such as sapphire or zinc selenide in lieu of the usual optical fiber material of quartz.) Since the temperature measurement by the sensor **66** can be degraded by background radiation from the plasma, it is preferred to provide a counter-bore **60a** in the ring **60** to shield the optical fiber end **72b** from background radiation (e.g., from heated chamber surfaces and from the plasma itself) without requiring any contact between the optical fiber **72** and the ring **60**. In addition to or instead of providing the counter-bore **60a** to shield the optical fiber end **72b** from plasma or background radiation, the wavelength of the sensor **66** can be selected to lie outside the plasma emission band (4 microns to 8 microns). The optical fiber **72** may be employed with or without the gray-body radiator piece **70**. The window **64** passes heat to the ring **60** while the optical fiber **72** passes emission from the ring **60** to the temperature sensor **66**.

[0062] If the temperature measurement is made directly of the silicon (i.e., without the intervening gray-body radiator piece **70**), then it is preferable to use a material such as sapphire for the optical fiber **72** which is highly transmissive at the emission wavelength of silicon, and to shield the optical fiber **72** with an opaque shield. Moreover, the problem of the silicon's emissivity varying with temperature may be ameliorated as shown in **FIG. 4C** by providing, in registration with the counterbore **60a**, a hole **60b** which is a relatively deep and narrow with a high (e.g., 5:1) aspect ratio, the optical fiber **72** being sunk into the counterbore **60a** to prevent background optical noise from entering the fiber end and an opaque shield **72c** surrounding the remainder of the optical fiber **72**. Such a deep hole may extend axially in the silicon ring **60** but preferably it extends radially from the circumferential edge of the silicon ring **60**. In this implementation, virtually none of the optical radiation from a heater lamp or from the plasma itself can enter the optical fiber **72** to interfere with the temperature measurement.

[0063] If the ring temperature is to be sensed through the window **64** in the absence of the optical fiber **72**, then another difficulty with measuring the temperature of the silicon ring **60** is that below 200° C. its peak thermal emission wavelength is shifted to a very long wavelength, well outside the optical passband of typical materials such as quartz that can be used for the window **64**. Quartz typically is transparent between about 300 nm and 3 microns, while silicon's peak thermal emission wavelength varies from 4 microns at 400° C. to 10 microns at room temperature. Thus, the range of directly measurable the silicon ring temperatures is limited, since silicon below about 200° C. does not appreciably radiate within the optical passband of quartz. One solution illustrated in **FIG. 4D** is to employ a small port **64a** within the quartz window **64**, the small port **64a** being of a material which is transparent at the long wavelengths emitted by silicon at cooler temperatures down to room temperature. The small port **64a** can be sapphire or zinc selenide. The radiant temperature sensor **66** would be selected to be responsive at the longer wavelengths passed by the small port **64a**. Alternatively, instead of the small long-wavelength port **64a** within the window **64**, a separate long-wavelength port **65** illustrated in **FIG. 4E** outside of the window **64** may be employed and may be made of sapphire or zinc selenide. The long wavelength port **65** may

be replaced by its equivalent, a long wavelength version of the optical fiber 72, such as a sapphire optical fiber.

[0064] If the sensor 66 is a fluoroptical probe, then it is unaffected by the thermal emissivity of the ring 60. In this case, a fluorescent substance or powder is immersed in the surface of a small region of the ring 60 aligned with the optical fiber end 72b. An optical pulse is applied periodically to the other fiber end 72a and the resulting optical pulse-stimulated emission from the fluorescent powder (in the ring 60) travels from the fiber end 72b to the fiber end 72a to be analyzed by the sensor 66 to determine the ring temperature. A counterbore in the ring 60 shields the optical fiber end 72b from background radiation.

[0065] In order to radiantly cool the ring 60, the window 64 may be cooled by conventional means, for example by providing a cold sink for radiant cooling of the polymer-hardening precursor ring 60. In this case, the rate at which the polymer-hardening precursor ring 60 is cooled is a function of $[T_{\text{ring}}]^4 - [T_{\text{window}}]^4$, where T_{ring} and T_{window} are the absolute temperatures (Kelvin), respectively, of the polymer-hardening precursor ring 60 and the cooled window 64. Efficient radiant cooling of the ring 60 is attained by maintaining a 200° C. temperature difference between the silicon ring 60 and the window 64, which is readily accomplished by conventional liquid or gas cooling apparatus 67 in contact with the window 64, provided the ring 60 is maintained within the preferred temperature range of 300° C. and 700° C. However, the ring may instead be cooled using any one of a number of conventional techniques. For example, it may be cooled in the manner that the wafer is typically cooled.

[0066] Whether the ring 60 is conductively cooled by a conventional cold plate or is radiantly cooled by the window 64, in some cases it may not be necessary to provide a heat source (such as the tungsten halogen lamps). Instead, heating by the plasma itself may be more than sufficient to heat the ring 60, in conjunction with the conductive or radiant cooling, to maintain stable temperature control of the ring 60 within the requisite temperature range. Thus, in an alternative embodiment, no heat source is provided.

[0067] In the embodiment of FIG. 6, the inductive heating coil 62 is replaced by a radiant heater 80 such as a tungsten-halogen lamp or an electric discharge lamp which emits electromagnetic radiation of a wavelength within the optical transmission band of the quartz window 64 (to avoid heating the window 64) and within the absorption band of the polymer-hardening precursor ring 60. Preferably, the wavelength of the emission from the radiant heater 80 differs from the wavelength of the emission from the polymer-hardening precursor ring 60 in order to avoid interfering with the temperature measurement performed by the optical pyrometer 66. However, if the optical fiber 72 is sunk into the counterbore 60a and if the optical fiber is completely shielded by the opaque shield 72c that extends down to the top of the counterbore 60a, then the radiant heater emission cannot interfere with the temperature measurement, and so it is not required, in this case, that the radiant heater emission wavelength differ from the emission wavelength of the (silicon) ring 60. In fact, this is advantageous since a number of commercially available detectors that could be installed at the output end of the optical fiber are more stable near the short emission wavelength range (1-2 μ) of silicon. In this

case, the temperature measurement is performed at shorter wavelengths so that the long wavelength port 64a or 65 or long wavelength (e.g., sapphire) optical fiber is not required.

[0068] To summarize the requirements for optimum radiant heating and radiant temperature sensing: (a) the material of the window 64 is highly transmissive at the wavelength of the radiant heat source 80 and either the window 64 itself or a small assigned portion of it or an optical fiber through it is highly transmissive at the wavelength to which the temperature sensor 66 is responsive but is not itself highly radiant at that wavelength; (b) the polymer-hardening precursor ring 60 is highly absorbing at the wavelength of the radiant heater 80 and either the ring 60 itself or a material embedded in or on it is radiant at the wavelength at which the sensor 66 responds; and (c) the wavelength of the radiant heater 80 does not coincide with the wavelength at which the sensor 66 is responsive and yet lies within the absorption spectrum of the polymer precursor ring 60 and outside the absorption spectrum of the window 64.

[0069] The foregoing requirements can be met in various ways, for example by first specifying the materials of the polymer-hardening precursor ring 60 and then selecting a compatible material for the window 64 and then finally selecting the wavelengths of the radiant heater and the sensor 66 by process of elimination, or else specifying the wavelengths of the sensor 66 and the radiant heater and then selecting the materials by process of elimination. The foregoing requirements may be relaxed to an extent depending upon the sensitivity of the temperature measurement and temperature control precision desired.

[0070] If radiant cooling is desired, then further requirements are imposed upon the window 64: (a) in the portion of the window 64 through which the sensor 66 views the ring 60 the window 64 is at least nearly transparent to the wavelength of radiation emitted by the heated ring 60 (as stated above), while (b) in other portions of the window 64 not used by the sensor 66 to view the ring 60 the window 64 has an absorption spectrum which includes the re-radiation wavelength of the radiantly heated polymer-hardening precursor ring 60, so as to absorb heat therefrom to provide radiant cooling.

[0071] One way of reducing the number simultaneous constraints on the material of the window 64 is to not require the window 64 to transmit both heat to the ring 60 and the ring's thermal emission to the sensor 66. This is accomplished by employing the small long-wavelength (zinc selenide or sapphire) port 64a or auxiliary window 65 for exclusive use by the sensor 66 or to employ the optical fiber 72 for exclusive use by the sensor 66, in either case reducing the function of the window 64 to transmitting radiation from the heat source only. In this case, if radiant cooling is desired, then the only other constraint on the window is that it absorb emission from the ring 60. This is possible as long as the emission wavelength of the radiant heat source 80 and the ring emission are of different wavelengths. Furthermore, it is preferred that the sensor 66 is not responsive at the wavelengths emitted by the radiant heat source 80.

[0072] In one working example, the polymer-hardening precursor ring 60 was crystalline silicon with a resistivity of 0.01 Ω -cm and an average emissivity between 0.3 and 0.7, the window 64 was quartz with an optical passband between 300 nm and 3 microns, the sensor 66 was an optical

pyrometer that sensed radiation through an optical fiber (corresponding to the optical fiber **72**) in a wavelength range of 4-10 microns and the radiant heater **80** was a 3000° K tungsten-halogen lamp with a peak power emission wavelength range of 0.9-1.0 micron. It should be noted that optical pyrometry in either a visible or non-visible wavelength range may be employed in carrying out the invention.

[0073] Referring now to a preferred embodiment illustrated in **FIG. 7**, an expendable polymer-hardening precursor ring **60** of silicon is added to the all-semiconductor (silicon) reactor chamber of **FIG. 3** and heated by a heating device **90** which may be either an induction heater or a radiant heater. Optionally, and in addition, a separate RF bias source **400** may be connected to the ring **60** to help, along with the heating of the ring **60**, to maintain the ring **60** reactive with the plasma and furnish polymer-hardening precursor material therefrom into the plasma. The advantage is that none of the silicon window electrodes (e.g., the silicon side wall **12** or the silicon ceiling **14**) are used to provide silicon to the polymer chemistry and therefore they need not be heated to the elevated temperatures (e.g., over 200° C. to 700° C.) to which a polymer-hardening precursor must be heated. Moreover, the RF bias power applied to the silicon wall **12** and the silicon ceiling **14** need not be so high as to promote consumption of the silicon material thereof. In fact, it may be preferable to apply no bias to the walls and ceiling. Preferably, the temperature of the silicon ceiling **14** and of the silicon side wall **12** and the RF power applied thereto are selected to minimize consumption thereof by etching, sputtering or ion bombardment thereof while maintaining their surfaces relatively free of polymer accumulation, to avoid frequent chamber cleaning operations. The best mode for accomplishing this is the light deposition mode referred to earlier in this specification. In a light deposition mode carried out during a two-minute plasma etch/polymer deposition process, the silicon wall temperature is maintained near 100° C.-150° C., and the resulting polymer deposition thereon is sufficiently light so that it can be removed subsequently by a 10 to 20 second exposure to a high density oxygen plasma temporarily generated in the chamber following etching of the wafer. Alternatively, but not preferably, a heavy deposition mode may be employed in which the silicon chamber walls are held near room temperature (for example) during the etch process.

[0074] Referring to **FIG. 8A**, separate independently controllable polymer-hardening precursor rings **61**, **63** are placed at different radial locations relative to the wafer to permit further compensation for radially non-uniform processing conditions. The separate outer and inner polymer-hardening precursor rings **61**, **63** of **FIG. 8A** are independently controlled by respective inductive or radiant heaters **80a**, **80b**, respective sensors **66a**, **66b** with respective windows **64a**, **64b** and respective temperature controllers **68a**, **68b**. In order to compensate for processing conditions giving rise to different etch selectivities at different radial locations on the wafer **17**, the user may select different polymer-hardening precursor ring temperatures to be maintained by the different temperature controllers **68a**, **68b**.

[0075] While any suitable reactor configuration may be employed in carrying out an embodiment having the separately controlled outer and inner polymer-hardening precursor rings **61**, **63**, the implementation illustrated in **FIG. 8A** employs a reactor having a solenoidal antenna over a heated

semiconductor window electrode ceiling of the type disclosed in above-referenced co-pending U.S. application Ser. No. _____ by Kenneth S. Collins et al. entitled "Inductively Coupled RF Plasma Reactor Having Overhead Solenoidal Antenna". Notably, the presently preferred implementation of the present invention employs the reactor of the above-referenced co-pending application but with only the outer polymer-hardening precursor ring **61**. The reactor of the above-referenced co-pending application includes a cylindrical chamber **140** having a non-planar coil antenna **142** whose windings **144** are closely concentrated in non-planar fashion near the center axis **146** of the cylindrical chamber **140**. While in the illustrated embodiment the windings **144** are symmetrical and have an axis of symmetry coinciding with the center axis of the chamber, the invention may be carried out differently. For example, the windings may not be symmetrical and/or their axis of symmetry may not coincide with the center of the chamber or the workpiece center. Close concentration of the windings **144** about the center axis **146** is accomplished by vertically stacking the windings **144** in the manner of a solenoid so that they are each a minimum distance from the chamber center axis **146**. This increases the product of current (**I**) and coil turns (**N**) near the chamber center axis **146** where the plasma ion density has been the weakest for short workpiece-to-ceiling heights. As a result, the RF power applied to the non-planar coil antenna **142** produces greater induction $[d/dt][N \cdot I]$ near the chamber center axis **146** (relative to the peripheral regions) and therefore greater plasma ion density in that region, so that the resulting plasma ion density is more nearly uniform despite the small workpiece-to-ceiling height. Thus, the invention provides a way for reducing the ceiling height for enhanced plasma process performance without sacrificing process uniformity.

[0076] In order that the windings **144** be at least nearly parallel to the plane of the workpiece **156**, they preferably are not wound in the usual manner of a helix but, instead, are preferably wound so that each individual turn is parallel to the (horizontal) plane of the workpiece **156** except at a step or transition between turns (from one horizontal plane to the next).

[0077] The cylindrical chamber **140** consists of a cylindrical side wall **150** and a circular ceiling **152** which can be integrally formed with the side wall **150** so that the side wall **150** and ceiling **152** can constitute a single piece of material, such as silicon. However, the preferred embodiment illustrated **FIG. 8A** has the side wall **150** and ceiling **152** formed as separate pieces. The circular ceiling **152** may be of any suitable cross-sectional shape such as planar, dome, conical, truncated conical, cylindrical or any combination of such shapes or curve of rotation. Generally, the vertical pitch of the solenoid **142** (i.e., its vertical height divided by its horizontal width) exceeds the vertical pitch of the ceiling **152**, even for ceilings defining 3-dimensional surfaces such as dome, conical, truncated conical and so forth. A solenoid having a pitch exceeding that of the ceiling is referred to herein as a non-conformal solenoid, meaning that, in general, its shape does not conform with the shape of the ceiling, and more specifically that its vertical pitch exceeds the vertical pitch of the ceiling.

[0078] A pedestal **154** at the bottom of the chamber **140** supports a workpiece **156**, such as a semiconductor wafer, which is to be processed. The chamber **140** is evacuated by

a pump (not shown in the drawing) through an annular passage 158 to a pumping annulus 160 surrounding the lower portion of the chamber 140. The interior of the pumping annulus may be lined with a replaceable metal liner 160a. The annular passage 158 is defined by the bottom edge 150a of the cylindrical side wall 150 and a planar ring 162 surrounding the pedestal 154. Process gas is furnished into the chamber 140 through any one or all of a variety of gas feeds. In order to control process gas flow near the workpiece center, a center gas feed 164a can extend downwardly through the center of the ceiling 152 toward the center of the workpiece 156. In order to control gas flow near the workpiece periphery, plural radial gas feeds 164b, which can be controlled independently of the center gas feed 164a, extend radially inwardly from the side wall 150 toward the workpiece periphery, or base axial gas feeds 164c extend upwardly from near the pedestal 154 toward the workpiece periphery, or ceiling axial gas feeds 164d can extend downwardly from the ceiling 152 toward the workpiece periphery. Etch rates at the workpiece center and periphery can be adjusted independently relative to one another to achieve a more radially uniform etch rate distribution across the workpiece by controlling the process gas flow rates toward the workpiece center and periphery through, respectively, the center gas feed 164a and any one of the outer gas feeds 164b-d. This feature of the invention can be carried out with the center gas feed 164a and only one of the peripheral gas feeds 164b-d.

[0079] The solenoidal coil antenna 142 is wound around a housing 166 surrounding the center gas feed 164. A plasma source RF power supply 168 is connected across the coil antenna 142 and a bias RF power supply 170 is connected to the pedestal 154.

[0080] Confinement of the overhead coil antenna 142 to the center region of the ceiling 152 leaves a large portion of the top surface of the ceiling 152 unoccupied and therefore available for direct contact with temperature control apparatus including, for example, plural radiant heaters 172 such as tungsten halogen lamps and a water-cooled cold plate 174 which may be formed of copper or aluminum for example, with coolant passages 174a extending therethrough. Preferably the coolant passages 174a contain a coolant of a known variety having a high thermal conductivity but a low electrical conductivity, to avoid electrically loading down the antenna or solenoid 142. The cold plate 174 provides constant cooling of the ceiling 152 while the maximum power of the radiant heaters 172 is selected so as to be able to overwhelm, if necessary, the cooling by the cold plate 174, facilitating responsive and stable temperature control of the ceiling 152. The large ceiling area irradiated by the heaters 172 provides greater uniformity and efficiency of temperature control. (It should be noted that radiant heating is not necessarily required in carrying out the invention, and the skilled worker may choose to employ an electric heating element instead, as will be described later in this specification.) If the ceiling 152 is silicon, as disclosed in co-pending U.S. application Ser. No. 08/597,577 filed Feb. 2, 1996 by Kenneth S. Collins et al., then there is a significant advantage to be gained by thus increasing the uniformity and efficiency of the temperature control across the ceiling. Specifically, where a polymer precursor and etchant precursor process gas (e.g., a fluorocarbon gas) is employed and where the etchant (e.g., fluorine) must be scavenged, the rate of polymer deposition across the entire ceiling 152 and/or

the rate at which the ceiling 152 furnishes a fluorine etchant scavenger material (silicon) into the plasma is better controlled by increasing the contact area of the ceiling 152 with the temperature control heater 172. The solenoid antenna 142 increases the available contact area on the ceiling 152 because the solenoid windings 144 are concentrated at the center axis of the ceiling 152.

[0081] The increase in available area on the ceiling 152 for thermal contact is exploited in a preferred implementation by a highly thermally conductive torus 175 (formed of a ceramic such as aluminum nitride, aluminum oxide or silicon nitride or of a non-ceramic like silicon either lightly doped or undoped) whose bottom surface rests on the ceiling 152 and whose top surface supports the cold plate 174. One feature of the torus 175 is that it displaces the cold plate 174 well-above the top of the solenoid 142. This feature substantially mitigates or nearly eliminates the reduction in inductive coupling between the solenoid 142 and the plasma which would otherwise result from a close proximity of the conductive plane of the cold plate 174 to the solenoid 142. In order to prevent such a reduction in inductive coupling, it is preferable that the distance between the cold plate 174 and the top winding of the solenoid 142 be at least a substantial fraction (e.g., one half) of the total height of the solenoid 142. Plural axial holes 175a extending through the torus 175 are spaced along two concentric circles and hold the plural radiant heaters or lamps 172 and permit them to directly irradiate the ceiling 152. For greatest lamp efficiency, the hole interior surface may be lined with a reflective (e.g., aluminum) layer. The ceiling temperature is sensed by a sensor such as a thermocouple 176 extending through one of the holes 175a not occupied by a lamp heater 172. For good thermal contact, a highly thermally conductive elastomer 173 such as silicone rubber impregnated with boron nitride is placed between the ceramic torus 175 and the copper cold plate 174 and between the ceramic torus 175 and the silicon ceiling 152.

[0082] In the embodiment of FIG. 8A, the chamber 140 may be an all-semiconductor chamber, in which case the ceiling 152 and the side wall 150 are both a semiconductor material such as silicon. Controlling the temperature of, and RF bias power applied to, either the ceiling 152 or the wall 150 regulates the extent to which it furnishes fluorine scavenger precursor material (silicon) into the plasma or, alternatively, the extent to which it is coated with polymer. The material of the ceiling 152 is not limited to silicon but may be, in the alternative, silicon carbide, silicon dioxide (quartz), silicon nitride or a ceramic.

[0083] The chamber wall or ceiling 150, 152 need not be used as the source of a fluorine scavenger material. Instead, a disposable silicon member can be placed inside the chamber 140 and maintained at a sufficiently high temperature to prevent polymer condensation thereon and permit silicon material to be removed therefrom into the plasma as fluorine scavenging material. In this case, the wall 150 and ceiling 152 need not necessarily be silicon, or if they are silicon they may be maintained at a temperature (and/or RF bias) near or below the polymer condensation temperature (and/or a polymer condensation RF bias threshold) so that they are coated with polymer from the plasma so as to be protected from being consumed. While the disposable silicon member may take any appropriate form, in the embodiment of FIG. 8A the disposable or expendable silicon member is an annular

ring 162 surrounding the pedestal 154. Preferably, the annular ring 162 is high purity silicon and may be doped to alter its electrical or optical properties. In order to maintain the silicon ring 162 at a sufficient temperature to ensure its favorable participation in the plasma process (e.g., its contribution of silicon material into the plasma for fluorine scavenging), plural radiant (e.g., tungsten halogen lamp) heaters 177 arranged in a circle under the annular ring 162 heat the silicon ring 162 through a quartz window 178. As described in the above-referenced co-pending application, the heaters 177 are controlled in accordance with the measured temperature of the silicon ring 162 sensed by a temperature sensor 179 which may be a remote sensor such as an optical pyrometer or a fluoro-optical probe. The sensor 179 may extend partially into a very deep hole 162a in the ring 162, the deepness and narrowness of the hole tending at least partially to mask temperature-dependent variations in thermal emissivity of the silicon ring 162, so that it behaves more like a gray-body radiator for more reliable temperature measurement.

[0084] As described in U.S. application Ser. No. 08/597, 577 referred to above, an advantage of an all-semiconductor chamber is that the plasma is free of contact with contaminant producing materials such as metal, for example. For this purpose, plasma confinement magnets 180, 182 adjacent the annular opening 158 prevent or reduce plasma flow into the pumping annulus 160. To the extent any polymer precursor and/or active species succeeds in entering the pumping annulus 160, any resulting polymer or contaminant deposits on the replaceable interior liner 160a may be prevented from re-entering the plasma chamber 140 by maintaining the liner 160a at a temperature significantly below the polymer condensation temperature, for example, as disclosed in the referenced co-pending application.

[0085] A wafer slit valve 184 through the exterior wall of the pumping annulus 160 accommodates wafer ingress and egress. The annular opening 158 between the chamber 140 and pumping annulus 160 is larger adjacent the wafer slit valve 184 and smallest on the opposite side by virtue of a slant of the bottom edge of the cylindrical side wall 150 so as to make the chamber pressure distribution more symmetrical with a non-symmetrical pump port location.

[0086] Maximum inductance near the chamber center axis 146 is achieved by the vertically stacked solenoidal windings 144.

[0087] A second outer vertical stack or solenoid 1120 of windings 1122 at an outer location (i.e., against the outer circumferential surface of the thermally conductive torus 175) is displaced by a radial distance δR from the inner vertical stack of solenoidal windings 144. Note that confinement of the inner solenoidal antenna 142 to the center and the outer solenoidal antenna 1120 to the periphery leaves a large portion of the top surface of the ceiling 152 available for direct contact with the temperature control apparatus 172, 174, 175. An advantage is that the larger surface area contact between the ceiling 152 and the temperature control apparatus provides a more efficient and more uniform temperature control of the ceiling 152.

[0088] For a reactor in which the side wall and ceiling are formed of a single piece of silicon for example with an inside diameter of 12.6 in (32 cm), the wafer-to-ceiling gap is 3 in (7.5 cm), and the mean diameter of the inner solenoid

was 3.75 in (9.3 cm) while the mean diameter of the outer solenoid was 11.75 in (29.3 cm) using $\frac{3}{16}$ in diameter hollow copper tubing covered with a 0.03 thick teflon insulation layer, each solenoid consisting of four turns and being 1 in (2.54 cm) high. The outer stack or solenoid 1120 is energized by a second independently controllable plasma source RF power supply 196. The purpose is to permit different user-selectable plasma source power levels to be applied at different radial locations relative to the workpiece or wafer 56 to permit compensation for known processing non-uniformities across the wafer surface, a significant advantage. In combination with the independently controllable center gas feed 164a and peripheral gas feeds 164b-d, etch performance at the workpiece center may be adjusted relative to etch performance at the edge by adjusting the RF power applied to the inner solenoid 142 relative to that applied to the outer solenoid 190 and adjusting the gas flow rate through the center gas feed 164a relative to the flow rate through the outer gas feeds 164b-d. While the present invention solves or at least ameliorates the problem of a center null or dip in the inductance field as described above, there may be other plasma processing non-uniformity problems, and these can be compensated in the versatile embodiment of FIG. 8A by adjusting the relative RF power levels applied to the inner and outer antennas. For effecting this purpose with greater convenience, the respective RF power supplies 168, 196 for the inner and outer solenoids 142, 190 may be replaced by a common power supply 197a and a power splitter 197b which permits the user to change the relative apportionment of power between the inner and outer solenoids 142, 190 while preserving a fixed phase relationship between the fields of the inner and outer solenoids 142, 190. This is particularly important where the two solenoids 142, 190 receive RF power at the same frequency. Otherwise, if the two independent power supplies 168, 196 are employed, then they may be powered at different RF frequencies, in which case it is preferable to install RF filters at the output of each RF power supply 168, 196 to avoid off-frequency feedback from coupling between the two solenoids. In this case, the frequency difference should be sufficient to time-average out coupling between the two solenoids and, furthermore, should exceed the rejection bandwidth of the RF filters. A preferred mode is to make each frequency independently resonantly matched to the respective solenoid, and each frequency may be varied to follow changes in the plasma impedance (thereby maintaining resonance) in lieu of conventional impedance matching techniques. In such implementations, the frequency ranges of the two solenoids should be mutually exclusive. Alternatively, the two solenoids are driven at the same RF frequency and in this case it is preferable that the phase relationship between the two be such as to cause constructive interaction or superposition of the fields of the two solenoids. Generally, this requirement will be met by a zero phase angle between the signals applied to the two solenoids if they are both wound in the same sense. Otherwise, if they are oppositely wound, the phase angle is preferably 180°. In any case, coupling between the inner and outer solenoids can be minimized or eliminated by having a relatively large space between the inner and outer solenoids 142, 190, as will be discussed below in this specification.

[0089] The range attainable by such adjustments is increased by increasing the radius of the outer solenoid 910 to increase the spacing between the inner and outer sole-

noids **142**, **190**, so that the effects of the two solenoids **142**, **190** are more confined to the workpiece center and edge, respectively. This permits a greater range of control in superimposing the effects of the two solenoids **142**, **190**. For example, the radius of the inner solenoid **142** should be no greater than about half the workpiece radius and preferably no more than about a third thereof. (The minimum radius of the inner solenoid **142** is affected in part by the diameter of the conductor forming the solenoid **142** and in part by the need to provide a finite non-zero circumference for an arcuate—e.g., circular—current path to produce inductance.) The radius of the outer coil **190** should be at least equal to the workpiece radius and preferably 1.5 or more times the workpiece radius. With such a configuration, the respective center and edge effects of the inner and outer solenoids **142**, **190** are so pronounced that by increasing power to the inner solenoid the chamber pressure can be raised into the hundreds of Mt while providing a uniform plasma, and by increasing power to the outer solenoid **190** the chamber pressure can be reduced to on the order of 0.01 Mt while providing a uniform plasma. Another advantage of such a large radius of the outer solenoid **190** is that it minimizes coupling between the inner and outer solenoids **142**, **190**.

[0090] In the embodiment of FIG. 8A, the ceiling **152** and side wall **150** are separate semiconductor (e.g., silicon) pieces insulated from one another having separately controlled RF bias power levels applied to them from respective RF sources **1210**, **1212** to enhance control over the center etch rate and selectivity relative to the edge. As set forth in greater detail in above-referenced U.S. application Ser. No. 08/597,577 filed Feb. 2, 1996 by Kenneth S. Collins et al., the ceiling **152** may be a semiconductor (e.g., silicon) material doped so that it will act as an electrode capacitively coupling the RF bias power applied to it into the chamber and simultaneously as a window through which RF power applied to the solenoid **142** may be inductively coupled into the chamber. The advantage of such a window-electrode is that an RF potential may be established directly over the wafer (e.g., for controlling ion energy) while at the same time inductively coupling RF power directly over the wafer. This latter feature, in combination with the separately controlled inner and outer solenoids **142**, **190** and center and peripheral gas feeds **164a**, **164b** greatly enhances the ability to adjust various plasma process parameters such as ion density, ion energy, etch rate and etch selectivity at the workpiece center relative to the workpiece edge to achieve an optimum uniformity. In this combination, pressure and/or gas volume through individual gas feeds is individually and separately controlled to achieve such optimum uniformity of plasma process parameters.

[0091] The lamp heaters **172** may be replaced by electric heating elements. The disposable silicon member is an annular ring **62** surrounding the pedestal **54**. Preferably, the annular ring **62** is high purity silicon and may be doped to alter its electrical or optical properties. In order to maintain the silicon ring **62** at a sufficient temperature to ensure its favorable participation in the plasma process (e.g., its contribution of silicon material into the plasma for fluorine scavenging), plural radiant (e.g., tungsten halogen lamps) heaters **177** arranged in a circle under the annular ring **62** heat the silicon ring **62** through a quartz window **178**. As described in the above-referenced co-pending application, the heaters **177** are controlled in accordance with the mea-

sured temperature of the silicon ring **62** sensed by a temperature sensor **179** which may be a remote sensor such as an optical pyrometer or a fluoro-optical probe. The sensor **179** may extend partially into a very deep hole **162a** in the ring **62**, the deepness and narrowness of the hole tending at least partially to mask temperature-dependent variations in thermal emissivity of the silicon ring **62**, so that it behaves more like a gray-body radiator for more reliable temperature measurement.

[0092] FIG. 8B illustrates another variation in which the ceiling **152** itself may be divided into an inner disk **152a** and an outer annulus **152b** electrically insulated from one another and separately biased by independent RF power sources **1214**, **1216** which may be separate outputs of a single differentially controlled RF power source.

[0093] In accordance with an alternative embodiment, a user accessible central controller **1300** shown in FIGS. 8A and 8B, such as a programmable electronic controller including, for example, a conventional microprocessor and memory, is connected to simultaneously control gas flow rates through the central and peripheral gas feeds **164a**, **164b**, RF plasma source power levels applied to the inner and outer antennas **142**, **190** and RF bias power levels applied to the ceiling **152** and side wall **150** respectively (in FIG. 8A) and the RF bias power levels applied to the inner and outer ceiling portions **152a**, **152b** (in FIG. 8B), temperature of the ceiling **152** and the temperature of the silicon ring **62**. A ceiling temperature controller **1218** governs the power applied by a lamp power source **1220** to the heater lamps **172** by comparing the temperature measured by the ceiling temperature sensor **176** with a desired temperature known to the controller **1300**. The master controller **1300** governs the desired temperatures of the temperature controllers **1218** and **68a**, **68b**, the RF power levels of the solenoid power sources **168**, **196**, the RF power levels of the bias power sources **1210**, **1212** (FIG. 8A) or **1214**, **1216** (FIG. 8B), the wafer bias level applied by the RF power source **170** and the gas flow rates supplied by the various gas supplies (or separate valves) to the gas inlets **164a-d**. The key to controlling the wafer bias level is the RF potential difference between the wafer pedestal **154** and the ceiling **152**. Thus, either the pedestal RF power source **170** or the ceiling RF power source **1212** may be simply a short to RF ground. With such a programmable integrated controller, the user can easily optimize apportionment of RF source power, RF bias power and gas flow rate between the workpiece center and periphery to achieve the greatest center-to-edge process uniformity across the surface of the workpiece (e.g., uniform radial distribution of etch rate and etch selectivity). Also, by adjusting (through the controller **1300**) the RF power applied to the solenoids **142**, **190** relative to the RF power difference between the pedestal **154** and ceiling **152**, the user can operate the reactor in a predominantly inductively coupled mode or in a predominantly capacitively coupled mode.

[0094] While the various power sources connected in FIG. 8A to the solenoids **142**, **190**, the ceiling **152**, side wall **150** (or the inner and outer ceiling portions **152a**, **152b** as in FIG. 8B) have been described as operating at RF frequencies, the invention is not restricted to any particular range of frequencies, and frequencies other than RF may be selected by the skilled worker in carrying out the invention.

[0095] In a preferred embodiment of the invention, the high thermal conductivity spacer 175, the ceiling 152 and the side wall 150 are integrally formed together from a single piece of crystalline silicon.

[0096] While the expendable polymer-hardening precursor piece has been described as a planar ring 60 in the wafer support pedestal top surface plane, it may be of any shape and at any location, provided that it is not too distant from the heat source to be efficiently heated thereby and provided that it shields the plasma processing region of the chamber from the heat source (so as to avoid diversion of power from the heat source to plasma generation in the chamber). In the preferred embodiment some shielding of the plasma from energy of the heat source (in addition to that provided by the silicon ring 60 itself) is provided by a pair of ring magnets 100, 102 that prevent plasma flow between the plasma processing region of the chamber and the pumping annulus.

[0097] Another embodiment that provides the requisite shielding and close proximity of the expendable polymer-hardening precursor piece to a remote heat source is illustrated in FIG. 9 in which the expendable piece is a cylindrical silicon liner 110 abutting the cylindrical chamber side wall interior surface. A peripheral heat source 115 adjacent the outside of the cylindrical side wall heats the silicon liner 110 through the side wall. The peripheral heat source 115 may be an induction heater, in which case the cylindrical chamber wall is either an insulator such as quartz or is a semiconductor such as silicon of sufficiently high resistivity to minimize absorption and maximize transmission of the induction field of the heat source 115 to the liner 110. Alternatively, the peripheral heat source 115 is a radiant heater such as a tungsten halogen lamp or an electric discharge lamp. A temperature sensor 166 and temperature controller 168 governing operation of the peripheral heater 115 perform temperature control in the manner of the sensor 66 and controller 68 of the embodiment of FIG. 8A. In the embodiment of FIG. 9, the master controller 300 governs the temperature controller 168.

[0098] The graph of FIG. 10 illustrates the performance of a temperature control system implemented in the embodiment of FIG. 6. The horizontal axis is the steady state temperature in degrees Celsius at which the temperature controller 68 has been commanded to hold the silicon ring 60, while the vertical axis is the applied power in Watts required to maintain the selected ring temperature. The graph of FIG. 11 illustrates the closed loop temperature response of the system of FIG. 6, the horizontal axis being time in seconds and the vertical axis being the ring temperature in degrees Celsius. In the graph of FIG. 11, the ring 60 begins at an initial temperature near room temperature and, after about 30 seconds, the controller 68 is commanded to put the ring temperature at 440° C. This temperature is reached at about 310 seconds with no overshoot and only a trace amount of system noise. At about 550 seconds a plasma is ignited in the chamber and is extinguished at about 1000 seconds, the effect on the ring temperature being almost unobservable in FIG. 11. This latter event proves the stability of the temperature control system and its responsiveness. FIG. 12 is a greatly enlarged view of a portion of the graph of FIG. 11 in the neighborhood of the time window from 301 seconds (when the target temperature is reached with no overshoot) and including 550 seconds (when the plasma is temporarily turned on). The plasma was

ignited with 3.2 Kwatts of source power at 550 seconds and the enlarged view of FIG. 12 reveals a short spike in the ring temperature coincident with that event. This data was obtained using the fluoro-optical probe version of the sensor 66 and the optical fiber 72.

[0099] In lieu of heating the polymer hardening precursor piece (e.g., the silicon ring 60), RF bias power may be applied from a source 400 (indicated in dashed line in FIG. 7) to the piece to achieve a desired effect in increasing polymer resistance to etching. The skilled worker can readily ascertain the requisite RF bias power level for this application by increasing the RF bias power on the piece (e.g., the silicon ring 60) until polymer deposition no longer accumulates thereon and the surface of the piece remains free for interaction with the plasma. While this may be practiced as an alternative mode of the invention, it is not the most preferable mode because: (a) the consumption of the polymer hardening precursor piece will be higher, and (b) some electrical (RF) coupling to the polymer hardening precursor piece must be provided to impose the requisite RF bias power on it, complicating its structure. In yet another alternative mode, heating and RF biasing of the polymer hardening precursor piece may be combined.

[0100] FIG. 13 illustrates how the embodiment of FIG. 8A may be modified to provide it with a dome-shaped monolithic ceiling. In particular, the ceiling 152, which may have a multiradius dome shape, is hemispherical in the illustrated embodiment. FIG. 14 illustrates an embodiment corresponding to FIG. 8B in that the dome-shaped ceiling 152 is divided into plural disk and annular sections 152a, 152b which are electrically separate and may be connected to separate RF power sources. FIG. 15 illustrates an embodiment corresponding to FIG. 9 in that the dome-shaped ceiling is combined with the feature of an expendable polymer-hardening precursor piece in the form of a vertical cylindrical liner 210 adjacent the vertical cylindrical chamber side wall. In order to maintain the polymer-hardening precursor liner at the requisite temperature, a heater 215 (such as an electric heater) provides heat to the liner 210. A temperature sensor 266 monitors the temperature of the liner 210. The output of the sensor 266 is connected to a controller 268 governing electric current supplied to the heater 215. The controller 268 is of the conventional type which can be programmed with a selected temperature. The controller 268 increases or decreases the electric current supplied to the heater 215 depending upon whether the sensor 266 senses a liner temperature which is below or above the selected temperature, respectively.

[0101] In accordance with the methodology of the invention, process uniformity across the wafer surface is optimized by adjusting the radial density distribution across the wafer surface of either or both etchant precursor species and deposition precursor species in the plasma. This is accomplished in the invention by any one or some or all of several methods. A first method is to divide the ceiling 152 into plural radially disposed separate sections (as illustrated in FIG. 8B for example) and changing the RF power applied to one section relative to the other. A second method is to change the radial distribution of temperature across the ceiling. As discussed above, this can be accomplished by separately controlling the heaters 172 disposed at different

radial locations. A third method is to separately adjust the process gas flow rate in the radially inner and outer gas flow inlets **164a**, **164b**, **164d**.

[0102] While the expendable temperature-regulated polymer-hardening precursor piece has been disclosed in combination with an inductively coupled plasma reactor, other applications are useful. For example, the polymer-hardening precursor piece may be used in a capacitively coupled plasma reactor. Such an application is illustrated in **FIG. 16**. In **FIG. 16** the ceiling **152** is driven by the RF power source **1210** to provide plasma source power into the chamber. No inductive antenna is necessary (e.g., the solenoid antennas **142**, **190**) although an inductive antenna may be present even through the reactor is operated in a predominantly capacitive coupling mode. If there is no inductive antenna over the ceiling **152**, then it is not absolutely required for the ceiling to be a semiconductor material although such a feature is advantageous in any case for the reasons described previously herein. If indeed the ceiling is not a semiconductor, the heaters **172** and the associated control apparatus may be eliminated if desired. In the capacitive coupling mode, the plasma source power is applied predominantly between the ceiling **152** and the wafer pedestal **154**, so that one of the two RF power sources **1210** and **170** may be eliminated as redundant. (In the inductive coupling mode, having two separate sources **1210**, **170** is not necessarily redundant since the source **170** provides independent RF bias controlling ion energy near the wafer while the source **1210** controls the bombardment or activation of the ceiling **152**.) **FIG. 17** illustrates how the feature of an expendable polymer-hardening precursor piece in the form of a vertical cylindrical liner **210** on the chamber side wall interior may be combined with a capacitively coupled plasma reactor.

[0103] **FIG. 18** illustrates how the plasma reactor of **FIG. 8A** may be modified so that the polymer-hardening precursor ring **63** is replaced by a polymer-hardening precursor chamber liner **63'** near chamber ceiling. In this embodiment, the liner **63'** has an outer surface **63'a** that fits the square corner between the flat ceiling **152** and the cylindrical sidewall **150** and an inner surface **63'b** which is three-dimensionally shaped and confines the plasma processing region to the three-dimensional shape. In the embodiment of **FIG. 18**, the liner interior surface **63'b** forms at least a portion of the ceiling of the chamber confining the plasma to a volume whose top has the three dimensional (e.g., dome) shape. In the drawing of **FIG. 18**, this three-dimensional shape is a multi-radius dome shape having a radius of curvature which increases from a minimum radius value at the circumferential periphery of the liner **63'** to a maximum radius value at the center. However, the shape may be a single-radius shape or a hemispherical shape. **FIG. 19** illustrates how the embodiment of **FIG. 18** may be modified to adopt the feature of **FIG. 8B** in which the ceiling **152** is divided into radially inner and outer (disk and annular) portions **152a**, **152b** which are driven with independent RF power levels and/or RF frequencies.

[0104] **FIG. 20** illustrates how the embodiment of **FIG. 18** may be modified to replace the solenoid antenna coils **142**, **190** with the flat antenna coils **50a**, **50b** of the embodiment of **FIG. 3**. **FIG. 21** illustrates how the embodiment of **FIG. 20** may be modified to adopt the feature of **FIG. 8B** in which the ceiling **152** is divided into radially inner and outer (disk

and annular) portions **152a**, **152b** which are driven with independent RF power levels and/or RF frequencies.

[0105] In the embodiments of **FIGS. 20** and **21**, the heating and cooling apparatus is distributed across a large proportion of the top surface of the ceiling, so that only a relatively small number of windings are accommodated in the flat coils **50a**, **50b**. In order to increase the number of flat coil windings, a simpler heating and cooling apparatus may be employed in the manner of **FIG. 3**, in order to accommodate a greater number of flat coil windings.

[0106] In each of the embodiments disclosed in this specification in which the ceiling **152** is driven with RF power, the RF plasma source power has been described as being inductively coupled by an inductor or inductors, such as the inner and outer solenoid antennas **142**, **190**. However, RF plasma source power may instead be capacitively coupled from the ceiling **152** (or ceiling portions **152a**, **152b**) applying sufficient RF power to the ceiling **152** with the wafer support or pedestal **154** being connected as an RF return path for the power applied to the ceiling **152**, while very little or no RF power is applied to the inductors **142**, **190** or such inductors are eliminated.

[0107] 2. Description of Relating to the Present Invention

[0108] It is now desired to obtain a deeper etch depth at a faster etch rate than was heretofore attainable. A deeper etch depth is required to meet continuing reductions in critical dimension or opening size, while the faster etch rate is required to meet higher production through-put demands for lower device cost. It is also desired to improve photoresist facet selectivity in silicon oxide plasma etching. Such an improvement would provide a greater margin of safety against removal of silicon dioxide material at the edge of an opening due removal ("faceting") of photoresist at the edge. It is further desired to better control the etch profile to obtain a 90% taper of the vertical walls of the etched opening. It is also desired to critical dimension variance across the wafer surface (e.g., center to edge) to as low as 0.05 microns or less and to minimize silicon loss at the bottom of each etched opening to 800 angstroms or less. As yet another way of reducing costs, it is desired to reduce the cost of consumable materials in the reactor (such as the fluorine-scavenger precursor material). The present invention described below accomplishes all of the foregoing simultaneously.

[0109] For reactors of the type lacking a silicon or silicon-carbide ring around the pedestal as the fluorine-scavenger precursor material, the only fluorine-scavenger precursor material is a silicon reactor ceiling. In attempting to address the problem of through-put, the etch rate could be increased, theoretically, by reducing the ceiling temperature to reduce fluorine scavenging, thereby increasing the fluorine content of the plasma as well as the fluorine content of the protective polymer deposited on the wafer. A sufficient reduction in ceiling temperature would cause more polymer to deposit on the ceiling, thereby reducing the polymer deposition rate on the wafer. With such changes, the plasma would etch the silicon oxide layers faster and the high-fluorine content polymer itself would etch the silicon oxide layers, the combined effect of which is to significantly increase the rate at which silicon oxide is etched. However, this approach has not seemed feasible because the oxide etch selectivity would decrease due to the increase in fluorine content of the polymer condensed onto non-oxygen-containing surfaces. A

polymer based upon C—F bonding is weaker than a polymer based primarily upon pure C—C bonding, so that a polymer containing more fluorine is weaker and provides less oxide-to-silicon selectivity. This latter disadvantage could be addressed by decreasing the plasma source power in order to enhance the oxide selectivity, but it would seem such a decrease would reduce the etch rate, so as to offset whatever etch rate gain was obtained by decreasing the roof temperature.

[0110] In meeting all of the foregoing problems, the present invention exploits the large effect ceiling temperature has on the etch process. In the type of reactor having both a silicon ceiling and a silicon (or silicon carbide) ring, the process characteristics are far more affected by the ceiling temperature than the ring temperature, due mainly to the greater surface area of the ceiling. Thus, for example, it has already been disclosed in this specification that only the silicon (or silicon carbide) ring is heated (to on the order of 300 degrees C., for example) while the silicon ceiling is maintained at a much cooler temperature (as low as 100 degrees C. or even room temperature). In this way, the advantages of improved polymer quality and etch selectivity obtained by raising the temperature of the silicon ring are at least partly realized while the ceiling temperature is reduced in applying the process of the present invention to gain additional advantages, which will be discussed below. As for a reactor lacking the heated silicon (or silicon carbide) ring around the pedestal, the process of the present invention including a reduced ceiling temperature provides additional advantages and the desired enhancements in performance discussed previously herein.

[0111] The low ceiling-temperature process of the present invention includes cooling the ceiling sufficiently to (a) reduce the rate at which polymer forms on the wafer by increasing the rate at which it condenses onto the ceiling, and (b) increase the fluorine content of the plasma (due to the decrease in scavenging species taken into the plasma from the ceiling), so that the plasma etches silicon oxide at a significantly faster rate.

[0112] In accordance with the preferred embodiment of the present invention, the increase in etch rate and etch depth is accomplished without surrendering other advantages, such as photoresist selectivity, oxide/silicon selectivity, etch profile and center-to-edge etch uniformity. In order to reduce damaging or faceting of the photoresist, the plasma source power (applied to the overhead inductive antenna elements) is reduced. This overcomes the greater tendency of a fluorine-rich plasma to attack photoresist. In order to provide greater oxide/silicon etch selectivity, a hydrogen-containing polymer precursor and etchant precursor species, such as CHF₃, is added to the conventional etchant gas, typically C₂F₆. The addition of hydrogen to the plasma in this manner causes polymer with more C—H or C—H—F bonds to form on the wafer. This type of polymer deposits more rapidly (on non-oxygen containing surfaces), thereby increasing oxide/silicon etch selectivity. As an additional advantage, a C—H or C—H—F polymer tends to form more strongly on the side walls of etched openings. This improves the etch profile, providing the desired wall taper of between 85 degrees and 90 degrees.

[0113] Another advantage of adding the hydrogen-containing polymer and etchant precursor gas (e.g., CHF₃) is

that some of the hydrogen disassociated from the added gas forms HF, which promote the silicon dioxide etch rate, thereby further enhancing the process performance.

[0114] In one embodiment, another gas is added to the mixture described above, containing a compound of hydrogen and an inert species. One example is HeH₂.

[0115] One advantage provided by the greater fluorine content of the plasma (due to the lower silicon ceiling temperature) is that photoresist faceting is reduced because the greater fluorine content produces more Si_xF_y species or radicals in the plasma. Such species emit ultraviolet wavelength radiation, which makes chemical changes in the outermost photoresist layers tending to harden those outer layers. In this way, the photoresist acquires a hardened shell which is more difficult for the plasma to attack, so that there is less faceting, and the entire photoresist layer is etched uniformly.

[0116] The low ceiling-temperature process described here may be used in a plasma reactor of the type illustrated in FIGS. 1 and 2, for example, in which plasma source power is applied by a cylindrical inductive coil wound around the chamber side walls and having a silicon (or other fluorine scavenger precursor material) ceiling, which, as shown in FIG. 2, may be heated or cooled. The invention is equally applicable to a plasma reactor of the type illustrated in FIG. 8A in which plasma source power is applied by an inductive antenna overlying the silicon ceiling, where the ceiling can act as a window electrode—being a window through which source power is coupled and an electrode which can be grounded or RF-driven, the reactor further including a heated silicon ring. As already described above in this specification, the ceiling can be maintained at a relatively cool temperature while the silicon ring can be heated to a relatively hot temperature.

WORKING EXAMPLE NO. 1

[0117] A working example of a process of the present invention applied to a reactor of the type illustrated in FIG. 2 is as follows: C₂F₆ was fed into the chamber at rate of between 35 sccm and 15 sccm, CHF₃ was fed into the chamber at a rate of between 25 sccm and 50 sccm at a chamber pressure of about 17 Mt. The ratio of C₂F₆ to CHF₃ depended upon the desired etch rate and etch selectivity. HeH₂ was supplied into the chamber at a rate of between 200 sccm and 300 sccm. The resist selectivity improved with greater amount of HeH₂, with little observable effect on etch rate. 1400 Watts of plasma source power was applied to the coil antenna, 1100 Watts of plasma bias power was applied to the wafer pedestal. The chamber side wall was maintained at about 160 degrees while the ceiling was cooled to 115 degrees C. The etch rate was found to lie in a range of about 8,000 to 12,000 angstroms per minute through an etch depth of over 2.5 microns.

WORKING EXAMPLE NO. 2

[0118] An embodiment of the low ceiling-temperature process of the present invention is suitable for use with a reactor of the type illustrated in FIG. 8A for etching a high aspect ratio opening through silicon dioxide. A working example of such a process is as follows: The gas flow rates were 110 sccm of CHF₃, 15 sccm of CH₂F₂, 400 sccm of Ar. The chamber pressure was maintained near 110 Mt. The

silicon ring was heated to 350 degrees C. while the silicon ceiling was cooled to 120 degrees C. 790 Watts of source power was applied to the inner inductive coil while 2610 of plasma source power was applied to the outer inductive coil. An etch rate of about 1.1 micron per minute was achieved, with an etch profile having a 90 angle. The photoresist selectivity was about 4.5:1.

WORKING EXAMPLE NO. 3

[0119] Another embodiment of the low ceiling-temperature process of the present invention is suitable for use with a reactor of the type illustrated in **FIG. 8A** for etching a bi-level device. A bi-level device has at least two conductive layers, and a single etch step may be required to simultaneously open contacts to both layers without overetching the upper conductor layer and without underetching the opening to the lower conductor layer. The process of the present invention can be readily tailored to meet such stringent requirements. An example of such a process is as follows: The gas flows were 90 sccm of CHF_3 , 10 sccm of CH_2F_2 , 400 sccm of Ar. The chamber pressure was about 88 Mt. 830 Watts of source power was applied to the inner coil antenna and 2450 Watts to the outer coil antenna. 1400 Watts of plasma bias power was applied to the wafer pedestal. The silicon ring was heated to 350 degrees C. while the silicon ceiling was cooled to 150 degrees C. The result was that the etch profile had a taper of between 88 and 90 degrees, as desired, the etch rate was about one micron per minute. The photoresist facet selectivity was about 5.5:1.

[0120] It was observed that decreasing plasma source power reduced photoresist faceting but did not improve photoresist etch selectivity. From the foregoing examples, it is seen that the hydrogen-containing polymer- and etchant-precursor gas may be selected from among CHF_3 , CH_2F_2 and similar gases. The hydrogen-inert gas compound was added only in Working Example No. 1 in the reactor of **FIG. 1** (lacking an overhead coil and a heated silicon ring), but may be useful in carrying out the invention in a reactor of type of **FIG. 8A** having an overhead coil and a heated silicon ring.

[0121] Another advantage following directly from the reduction in ceiling temperature was a proportional reduction in cost of consumables, a significant advantage of the invention. At the lower ceiling temperature the ceiling was worn away at a much lower rate, reducing its frequency of replacement and thereby reducing the per-wafer cost of consumables. The ceiling must be replaced once its interior surface has been worn by sputtering to the point the process can no longer be easily controlled within a desired window. The process of the present invention greatly lengthens the longevity of the ceiling.

[0122] In summary, the high plasma density silicon dioxide etch process of the invention includes cooling the ceiling to 150 degrees C. or below (as low as room temperature, for example), reducing the plasma source power (e.g., to a range of 1400 Watts to 2500 Watts), maintaining the RF bias power on the wafer at approximately 1000-1500 Watts, and employing a process gas mixture which provides etchant precursor species, polymer precursor species, hydrogen and an inert gas species. The process is applicable to either the type of reactor illustrated in **FIG. 2** in which the plasma source power applicator is a cylindrical inductor wound

around the chamber side wall or the type of reactor illustrated in **FIG. 8A** in which the plasma source power applicator is an overhead inductive antenna coupling power through the semiconductor ceiling. The latter type of reactor may further include a disposable heated semiconductor ring adjacent the wafer pedestal, which is preferably heated well above the polymer condensation temperature (e.g., to 350 degrees C.). One preferred process gas providing etchant precursor species, polymer precursor species and hydrogen is CHF_3 . The chamber pressure is maintained in a range of about 15 mT to 125 mT.

[0123] While the invention has been described in detail by specific reference to preferred embodiments thereof, it is understood that variations and modifications thereof may be made without departing from the true spirit and scope of the invention.

What is claimed is:

1. A high plasma density etch process for etching an oxygen-containing layer overlying a non-oxygen containing layer on a workpiece in a plasma reactor chamber, said process comprising:

providing a chamber ceiling overlying said workpiece and containing a semiconductor material;

supplying into said chamber a process gas containing etchant precursor species, polymer precursor species and hydrogen;

applying plasma source power into said chamber; and

cooling said ceiling to a temperature range at or below about 150 degrees C.

2. The process of claim 1 wherein said etchant and polymer precursor species contain fluorine, and wherein said chamber ceiling semiconductor material comprises a fluorine scavenger precursor material.

3. The process of claim 2 wherein said process gas comprises at least one of CHF_3 and CH_2F_2 .

4. The process of claim 3 wherein said process gas further comprises a non-hydrogen containing etchant and polymer precursor gas.

5. The process of claim 4 wherein said non-hydrogen containing etchant and polymer precursor gas comprises C_2F_6 .

6. The process of claim 3 wherein said process gas further comprises a species including an inert gas.

7. The process of claim 6 wherein said species including an inert gas comprises one of HeH_2 or Ar.

8. The process of claim 2 wherein said source power applicator comprises an inductive antenna overlying said ceiling, whereby said ceiling is a window to said inductive antenna, said process further comprising:

applying RF bias power to said workpiece; and

controlling the RF potential of said ceiling.

9. The process of claim 8 wherein controlling the RF potential of said ceiling comprises one of:

(a) holding said ceiling at an RF ground potential;

(b) applying an RF bias signal to said ceiling.

10. The process of claim 8 further comprising:

providing a fluorine scavenger precursor material in said chamber separate from said ceiling; and

- heating said fluorine scavenger precursor material to an elevated temperature above a condensation temperature of a polymer formable from said polymer precursor species of said process gas.
- 11.** The process of claim 10 wherein said elevated temperature is above 170 degrees C.
- 12.** The process of claim 10 wherein said elevated temperature is above 270 degrees C.
- 13.** The process of claim 10 wherein said elevated temperature is near 350 degrees C.
- 14.** The process of claim 10 wherein said heated fluorine scavenger precursor material comprises a semiconductor ring concentric with and adjacent said workpiece.
- 15.** The process of claim 10 wherein said heated fluorine scavenger precursor material comprises an interior semiconductor liner adjacent a wall of said chamber.
- 16.** The process of claim 1 further comprising providing a cooling apparatus over said ceiling for carrying out the cooling of said ceiling.
- 17.** The process of claim 16 wherein said cooling apparatus comprises:
- plural semiconductor rings overlying and contacting said ceiling;
 - a chilled plate overlying and contacting said plural semiconductor rings, wherein said plasma source power applicator comprises inductive elements overlying said ceiling between adjacent ones of said plural semiconductor rings.
- 18.** The process of claim 17 wherein said inductive elements comprise solenoidal elements.
- 19.** The process of claim 17 wherein said inductive elements comprise coil windings.
- 20.** The process of claim 1 further comprising maintaining said chamber at a pressure between about 15 mT and 115 Mt.
- 21.** The process of claim 1 wherein applying plasma source power comprises:
- providing plural respective inductive elements at respective radial locations overlying said ceiling; and
 - applying different plasma RF source power levels to said respective inductive elements to optimize etch uniformity across said workpiece.
- 22.** The process of claim 21 further comprising providing a cooling apparatus over said ceiling for carrying out the cooling of said ceiling, comprising:
- plural semiconductor rings overlying and contacting said ceiling;
 - a chilled plate overlying and contacting said plural semiconductor rings, wherein said respective inductive elements overlie said ceiling between adjacent ones of said plural semiconductor rings.
- 23.** A high plasma density etch process for etching a silicon oxide layer overlying a silicon layer on a workpiece in a plasma reactor chamber, said process comprising:
- providing a chamber ceiling overlying said workpiece and containing a semiconductor material comprising silicon;
 - supplying into said chamber a process gas containing carbon, fluorine and hydrogen species, said species constituting etchant precursor species and polymer precursor species;
 - inductively coupling plasma source power into said chamber through said ceiling to maintain a plasma in said chamber; and
 - cooling said ceiling sufficiently to reduce fluorine scavenging silicon species in said chamber and increase silicon oxide etch rate to on the order of approximately 1 micron of silicon oxide per minute.
- 24.** The process of claim 23 wherein said cooling cools said ceiling to a temperature range at or below about 150 degrees C.
- 25.** The process of claim 23 wherein said process gas comprises at least one of CHF_3 and CH_2F_2 .
- 26.** The process of claim 25 wherein said process gas further comprises a non-hydrogen containing etchant and polymer precursor gas.
- 27.** The process of claim 26 wherein said non-hydrogen containing etchant and polymer precursor gas comprises C_2F_6 .
- 28.** The process of claim 26 wherein said process gas further comprises a species including an inert gas.
- 29.** The process of claim 28 wherein said species including an inert gas comprises one of HeH_2 or Ar.
- 30.** The process of claim 23 further comprising:
- applying RF bias power to said workpiece; and
 - controlling the RF potential of said ceiling.
- 31.** The process of claim 30 wherein controlling the RF potential of said ceiling comprises one of:
- (a) holding said ceiling at an RF ground potential;
 - (b) applying an RF bias signal to said ceiling.
- 32.** The process of claim 23 further comprising:
- providing a fluorine scavenger precursor material in said chamber separate from said ceiling; and
 - heating said fluorine scavenger precursor material to an elevated temperature above a condensation temperature of a polymer formable from said polymer precursor species of said process gas.
- 33.** The process of claim 32 wherein said elevated temperature is above 170 degrees C.
- 34.** The process of claim 32 wherein said elevated temperature is above 270 degrees C.
- 35.** The process of claim 32 wherein said elevated temperature is near 350 degrees C.
- 36.** The process of claim 32 wherein said heated fluorine scavenger precursor material comprises a semiconductor ring concentric with and adjacent said workpiece.
- 37.** The process of claim 32 wherein said heated fluorine scavenger precursor material comprises an interior semiconductor liner adjacent a wall of said chamber.
- 38.** The process of claim 23 further comprising providing a cooling apparatus over said ceiling for carrying out the cooling of said ceiling.
- 39.** The process of claim 38 wherein said cooling apparatus comprises:
- plural semiconductor rings overlying and contacting said ceiling;
 - a chilled plate overlying and contacting said plural semiconductor rings, wherein said plasma source power applicator comprises inductive elements overlying said ceiling between adjacent ones of said plural semiconductor rings.

40. The process of claim 39 wherein said inductive elements comprise solenoidal elements.

41. The process of claim 39 wherein said inductive elements comprise coil windings.

42. The process of claim 23 wherein said ceiling has a three-dimensionally shaped interior surface facing the interior of said chamber.

43. The process of claim 42 wherein said interior surface is dome shaped.

44. The process of claim 42 wherein said interior surface is hemispherical.

45. The process of claim 42 wherein said interior surface has a multiradius dome shape having a maximum radius at a periphery thereof and a minimum radius at the center thereof.

46. The process of claim 23 wherein said semiconductor ceiling is divided into plural electrically separate concentric sections, said process further comprising:

applying respective plasma RF source power levels to said separate section so as to optimize etch uniformity across said workpiece.

47. The process of claim 23 wherein said ceiling is divided into plural concentric sections, said process further comprising:

separately controlling respective temperatures of said plural concentric sections so as to optimize etch uniformity across said workpiece.

48. The plasma reactor of claim 23 further comprising:

providing process gas inletting apparatus comprising plural process gas inlets at respective radial locations; and furnishing said process gas through said plural gas inlets at respective gas flow rates to optimize etch uniformity across said workpiece.

49. The process of claim 32 further comprising heating said fluorine scavenging precursor material to a temperature at which polymer-hardening precursor material is provided therefrom into the plasma.

50. A plasma etch process comprising:

providing a chamber within which to carry out said process, including a semiconductor ceiling;

supporting an article to be processed on a support in the chamber;

supplying a process gas containing at least etchant and polymer precursor materials;

providing, in addition to said process gas, a source material of silicon or carbon in said chamber;

generating a plasma within said chamber;

heating said source material sufficiently to at least maintain a surface of said source reactive with said plasma;

cooling said ceiling to a temperature range below a polymer condensation temperature; and

adjusting the radial distribution of plasma ion density across said article to be processed.

51. The process of claim 50 wherein said ceiling is cooled to a temperature range between room temperature and about 150 degrees C.

52. The process of claim 50 wherein the generating of a plasma comprises applying RF plasma source power into said chamber and wherein said adjusting comprises adjusting the radial RF power distribution in said chamber.

53. The process of claim 52 wherein said reactor comprises an inductive antenna for the applying of RF plasma source power, said antenna being divided into concentric electrically separate antenna sections, and the adjusting of radial RF power distribution in said chamber comprises adjusting separate RF power levels applied to said separate antenna sections.

54. The process of claim 50 wherein the adjusting of radial distribution of plasma ion density comprises adjusting radial distribution of process gas in said chamber.

55. The process of claim 54 wherein said reactor comprises plural process gas inlets disposed at different radial locations for the supplying of process gas, and wherein said adjusting of radial distribution of process gas in said chamber comprises adjusting different gas flow rates to respective ones of said gas inlets at different radial locations.

56. The process of claim 50 wherein said chamber comprises a semiconductor ceiling facing said support and wherein the adjusting of radial distribution of plasma ion density comprises adjusting temperatures of different radial zones of said ceiling.

57. The process of claim 50 wherein said chamber comprises a ceiling facing said support and said ceiling comprises plural electrically separate concentric ceiling sections, and the adjusting of radial distribution of plasma ion density comprises adjusting different RF power levels applied to respective ones of said plural concentric sections of said ceiling.

58. The process of claim 50 wherein said chamber comprises plural electrically separate concentric chamber enclosure sections, and the adjusting of radial distribution of plasma ion density comprises adjusting different RF power levels applied to respective ones of said plural concentric enclosure sections.

59. The process of claim 50 wherein the step of heating comprises heating said source material to at least a polymer condensation temperature.

60. The process of claim 59 wherein said etch process etches first and second different materials on said article at first and second etch rates respectively, said first etch rate being greater than said second etch rate corresponding to an etch selectivity of said first material to said second material which is a function of said first and second etch rates, and wherein said heating step further comprises:

increasing a temperature of said source material into a temperature range above said polymer condensation temperature to increase said etch selectivity.

61. The process of claim 60 wherein said first material overlies said second material and said etchant creates openings through said first material to a expose portions of said second material.

62. The process of claim 61 wherein:

said polymer precursor material provides material for polymer deposition on the exposed portions of said second material;

said etchant precursor material provides material for etching said article; and

said polymer deposition reduces etching of said second material to enhance etch selectivity.

63. The process of claim 62 wherein:

a photoresist mask layer over said first material has openings therethrough defining said openings; and

said polymer deposition reduces etching of said second material and of said photoresist material to enhance etch selectivity.

64. The process of claim 62 wherein said first material comprises an oxygen-containing material and said second material comprises a non-oxygen containing material.

65. The process of claim 60 wherein said heating step further comprises:

increasing a temperature of said source material into a temperature range above said polymer condensation temperature.

66. The process of claim 65 wherein said temperature range is one wherein polymer formed on said wafer contains an amount of said source material.

67. The process of claim 61 wherein said first material comprises an oxide, said second material comprises silicon or polysilicon, an etchant precursor of said process gas comprises fluorine, a polymer precursor of said process gas comprises at least fluorine and carbon and said source material comprises silicon.

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