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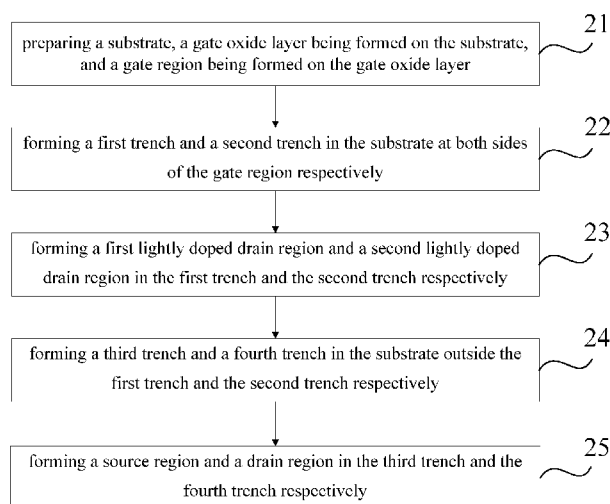


Fig. 1

(57) Abstract: A method for fabricating a small-scale MOS device, including: preparing a substrate; forming a first trench in the substrate along a first side of the gate region and forming a second trench in the substrate along a second side of the gate region, the first side of the gate region opposite the second side of the gate region; forming a first lightly doped drain region and a second lightly doped drain region in the first trench and the second trench, respectively; forming a third trench in the substrate overlapping at least a first portion of the first lightly doped drain region and a fourth trench in the substrate overlapping at least a first portion of the second lightly doped drain region; and forming a source region and a drain region in the third trench and the fourth trench, respectively.

METHOD FOR FABRICATING SMALL-SCALE MOS DEVICE

BACKGROUND

[0001] Field of the Invention

5 [0002] The present invention relates to the field of semiconductor fabrication technique, and more particular to a method for fabricating a small-scale metal-oxide-semiconductor MOS device.

[0003] Description of the Related Art

[0004] With the ever increasing development of Integrated Circuit (IC) fabrication
10 process/device technology, the degree of IC integration is becoming higher, and thus the size of MOS devices is required to be smaller.

[0005] The process for fabricating, for example, a NMOS type MOS device generally includes the following steps; (i) growing a screen oxide layer on a substrate, (ii) performing photolithography and P-type ion implantation to form a P well, (iii) growing a
15 gate oxide layer, (iv) depositing polysilicon and performing photolithography and etching to form a gate region, (v) performing photolithography and implantation to form a N-type Lightly Doped Drain (LDD), (vi) depositing Tetraethyl Ortho Silicate (TEOS) and performing photolithography and etching to form a side wall, (vii) performing
photolithography and implantation for the source/drain (S/D) regions, (viii) thermally
20 annealing the S/D implant to form the S/D regions, (ix) depositing an Salicide Blocking (SAB) material layer, (x) performing photolithography and etch on the Salicide Blocking (SAB) material layer, and (xi) processing Silicide by metal processing to form a metal contact.

[0006] To obtain a small scale MOS device, the depth of the S/D junction must be made
25 shallow during fabrication, which requires high performance control for the implanting apparatus used in the S/D implanting process.

[0007] An existing ion implanter is a high-current and low-energy apparatus. Thus, under low energy and high productivity, it is difficult to implement a super-shallow junction technique with this apparatus. Therefore, a shallow S/D junction is difficult to

obtain with conventional implantation processing. Further, following the S/D implantation process, the thermal anneal process performed by existing fabrication techniques impedes further scaling of small-scale MOS devices.

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SUMMARY

[0008] In view of this, the present invention provides a method for fabricating a small-scale MOS device to obtain a shallow source/drain junction, and thus enable further MOS device scaling.

[0009] To achieve the above object, the present invention provides following technique solutions. According to one embodiment of the present invention, a method for fabricating a small-scale metal-oxide-semiconductor (MOS) device includes preparing a substrate of a first conductivity type, a gate oxide layer being formed on the substrate, and a gate region being formed on the gate oxide layer. The method further includes forming a first trench in the substrate along a first side of the gate region and forming a second trench in the substrate along a second side of the gate region, the first side of the gate region being opposite the second side of the gate region. The method further includes forming a first lightly doped drain region and a second lightly doped drain region in the first trench and the second trench, respectively. The method further includes forming a third trench in the substrate overlapping at least a first portion of the first lightly doped drain region and a fourth trench in the substrate overlapping at least a first portion of the second lightly doped drain region. The method further includes forming a source region and a drain region in the third trench and the fourth trench, respectively.

[0010] According to one specific embodiment, the method for fabricating a small-scale MOS device further includes forming metal silicide on the source region and the drain region respectively. According to another specific embodiment, the step of forming the first trench and forming the second trench further includes forming a photoresist layer having a first trench pattern and a second trench pattern on the gate oxide layer. The step further includes forming the first trench and the second trench by etching through the gate oxide layer and etching into the substrate, the etching being prevented under the photoresist layer and the gate region, and removing the photoresist layer.

[0011] According to another specific embodiment, the step of forming the first lightly doped drain region and a second lightly doped drain region further includes filling the first trench with the first lightly doped drain region and filling the second trench with the second lightly doped drain region, the first lightly doped drain region and the second lightly doped drain region being of a second conductivity type.

[0012] According to another specific embodiment, the step of forming the third trench and the fourth trench further includes forming a first side wall on the first side of the gate region and forming a second side wall on the second side of the gate region, depositing a salicide blocking (SAB) material layer over the substrate, and forming a photoresist layer having a third trench pattern and a fourth trench pattern on the SAB material layer. The step further includes forming the third trench and the fourth trench by etching through the SAB material layer, etching the first portion of the first lightly doped drain region, etching the first portion of the second lightly doped drain region, and etching into the substrate. The etching is prevented under the photoresist layer, the first side wall, the second side wall, and the gate region. Then, the photoresist layer is removed.

[0013] According to one specific embodiment, the step of forming the source region and the drain region further includes filling the third trench with the source region and filling the fourth trench with the drain region, the source region and the drain region being of the second conductivity type. According to another specific embodiment, the step of forming metal silicide on the source region and the drain region respectively further includes, depositing a metal over the substrate and on the SAB material layer, annealing the metal and forming metal silicide except over the SAB material layer, and removing the metal over the SAB material layer.

[0014] According to another specific embodiment, the step of preparing a substrate, a gate oxide layer being formed on the substrate, and a gate region being formed on the gate oxide layer, further includes (i) preparing a substrate, (ii) forming a screen oxide layer on the substrate, (iii) forming a well region of the first conductivity type in the substrate, (iv) removing the screen oxide layer, (v) forming a gate oxide layer on the substrate, and (vi) forming a gate region on the gate oxide layer.

[0015] According to another specific embodiment, the step of forming the first side wall and forming the second side wall includes depositing a dielectric layer over the substrate,

and etching back the dielectric layer by an anisotropic etch process. According to another specific embodiment, the gate region is SrTiO_3 , HfO_2 , ZrO_2 , or polysilicon. According to another specific embodiment, the depths of the third trench and the fourth trench are less than $0.1\mu\text{m}$. According to another specific embodiment, the depths of the third trench and the fourth trench are greater than the depths of the first trench and the second trench.

[0016] According to another specific embodiment, an upper surface of the first lightly doped drain region and an upper surface of the second lightly doped drain region are substantially at the same plane as an upper surface of the substrate. According to another specific embodiment, the step of filling the first trench and filling the second trench is by selective epitaxial growth in the first trench and in the second trench. According to another specific embodiment, an upper surface of the source region and an upper surface of the drain region are substantially at the same plane as an upper surface of the substrate. According to another specific embodiment, the step of filling the third trench and filling the fourth trench is by selective epitaxial growth in the third trench and in the fourth trench.

[0017] It may be seen from the above technical solutions that, according to the present invention, a first trench and a second trench are formed in the substrate at both sides of a gate region respectively, and a first lightly doped drain region and a second lightly doped drain region are formed respectively in the first trench and the second trench; similarly, a third trench and a fourth trench are formed in the substrate outside the first trench and the second trench respectively, and a source region and a drain region are formed in the third trench and the fourth trench respectively. Compared with the existing implanting technique in the prior art, the method for implementing according to the present invention forms four trenches in the substrate sequentially, depth of which may be controlled accurately by etching time, and the depths of the third trench and the fourth trench correspond to the depth of a source/drain junction formed later, and thus a shallow source/drain junction may be formed by controlling the etching time to fabricate a small-scale MOS device.

[0018] Furthermore, in the method provide by the present invention, implanting process is not performed for the source/drain formation; therefore a source/drain annealing process is omitted in the following steps, thus decreasing the steps in the technology flow and simplifying the process for fabricating a small-scale MOS device.

[0019] A better understanding of the nature and advantages of the embodiments of the present invention may be gained with reference to the following detailed description and the accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0020] Figure 1 is a flow chart showing a method for fabricating a small-scale MOS device, in accordance with an embodiment of the present invention; and

[0021] Figure 2 to Figure 10 are simplified cross sectional views showing a process for fabricating a small-scale MOS device, in accordance with embodiments of the present invention.

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DETAILED DESCRIPTION

[0022] To make the above objects, features and advantages more apparent to be understood, embodiments of the present invention will be further described in detail in conjunction with the drawings hereinafter.

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[0023] To facilitate the sufficient understanding of the invention, many details are explained in the following descriptions, however the present invention may be implemented in other manners than those described herein, and similar extensions may be made by those skilled in the art without deviating from the spirit of the present invention, therefore the present invention is not restricted by the embodiments disclosed hereinafter.

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[0024] Furthermore, the present invention is described in detail in conjunction with the simplified cross sectional views. In describing the embodiments of the present invention, to facilitate the description, sectional views showing structures of the device are magnified locally without conforming to a general scaling, and the mentioned simplified cross sectional views are only examples and should not restrict the scope of protection of the present invention. Moreover, three-dimensional size, i.e. the length, the width and the depth, should be given in view of practical implementation.

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[0025] According to embodiments of the present invention, a method for fabricating a

small-scale MOS device is provided to obtain a shallow source/drain junction, and thus enable further MOS device scaling. The S/D formation may be accomplished by etching trenches in the substrate that are self-aligned to the gate region. The trenches are then filled using in-situ- doped, selective epitaxy to grow the LDD and S/D regions in the trenches, without using ion implantation and the associated thermal annealing steps for activating the implant. The trench depth may be more accurately controlled by the trench etch process and the thermal budget for the fill process may be lower than processing by known implantation and thermal annealing techniques. Thus, greater MOS device size reduction is enabled.

10 [0026] Figure 1 is a flow chart showing a method for fabricating a small-scale MOS device, in accordance with an embodiment of the present invention, which shows the following steps. A substrate of a first conductivity type is prepared 21, a gate oxide layer being formed on the substrate, and a gate region being formed on the gate oxide layer. For example, the conductivity type of the substrate may, be p-type for an NMOS device.

15 [0027] The step 21 may also include the following steps. Figure 2 to Figure 10 are simplified cross sectional views showing a process for fabricating a small-scale MOS device, in accordance with embodiments of the present invention. Referring to Figure 2, a substrate 1 is prepared. The substrate prepared in this embodiment may include a body layer and an epitaxial layer (not shown), wherein the body layer is P-type monocrystalline silicon; and the epitaxial layer is lightly doped monocrystalline silicon growing on the
20 P-type monocrystalline silicon. Compared with the body layer, the epitaxial layer has the same lattice structure, a higher purity and fewer lattice defects. In other embodiments, the body layer may also be other semiconductor materials such as germanium, indium phosphide, or gallium arsenide.

25 [0028] A screen oxide layer 2 is formed on the substrate. The screen oxide layer may be grown on the substrate by a thermal oxidation process, and the screen oxide layer is silicon dioxide in this embodiment. The screen oxide layer is provided to reduce defect formation in the substrate during subsequent ion implantation of the well region, and thus the thickness of the screen oxide may be thin, which is generally approximately 150Å.

30 [0029] A well region of the first conductivity type is formed in the substrate. Referring to Figure 2, in accordance with an embodiment of the present invention, photoresist is spin

coated on screen oxide layer 2; next, the photoresist is exposed using a corresponding photomask, and then the development is performed; and a photoresist layer 3 with a well region pattern is formed on screen oxide layer 2. A well region 4 is formed in substrate 1 using ion implantation, by using the photoresist layer 3 with the well region pattern as a mask. In the present invention, the implanted ion is Boron B ion, and the formed well region 4 is P well. After removing photoresist layer 3, annealing is performed on the substrate to remove crystal lattice damage due to the ion implantation and to activate the implanted ions. After the annealing process is performed, well region 4 is formed. Then screen oxide layer 2 is removed from substrate 1.

10 [0030] Referring to Figure 3, in accordance with an embodiment of the present invention, a gate oxide layer 5 is formed over substrate 1 and on the well region 4 by thermal oxidization processes, and the thickness of gate oxide layer 5 may be between approximately 20 Å to hundreds of Å. In this embodiment, gate oxide layer 5 is silicon dioxide. The gate region is formed next on the gate oxide layer.

15 [0031] Referring to Figure 4, in accordance with an embodiment of the present invention, a gate region material layer is deposited on gate oxide layer 5. In this embodiment, the gate region material is SrTiO₃, and in other embodiments, the gate region material may also be material with high dielectric constant, such as HfO₂ or ZrO₂, and may also be material such as polysilicon. Then, photoresist is spin coated on the gate region material layer; next the photoresist is exposed using a corresponding photomask, and then the development is performed to form a photoresist layer with a gate region pattern on the gate region material layer. Then the gate region material layer is etched using the photoresist layer with the gate region pattern as a mask, and thus a gate region 6 is formed on gate oxide layer 5. After the gate region 6 is formed, the photoresist is removed.

25 [0032] Referring back to Figure 1, Step 22 shows forming a first trench and a second trench in the substrate at both sides of the gate region, respectively. In other words, step 22 shows forming a first trench in the substrate along a first side of the gate region and forming a second trench in the substrate along a second side of the gate region, the first side of the gate region being opposite the second side of the gate region. Step 22 may include the steps of forming a photoresist layer having a first trench pattern and a second trench pattern on the gate oxide layer; forming the first trench and the second trench by

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etching through the gate oxide layer and etching into the substrate, the etching being prevented under the photoresist layer and the gate region; and removing the photoresist layer.

[0033] Referring to Figure 5, in accordance with an embodiment of the present invention, photoresist is spin coated over the substrate 1, on gate oxide layer 5 and the gate region. The photoresist is exposed using a corresponding photomask. After the exposure, the development is performed to form a photoresist layer with a first trench pattern and a second trench pattern. The patterning for the photoresist may be adapted to merge the pattern for the first trench pattern and the second trench pattern into one region, which substantially overlaps the gate region. A first trench 7 and a second trench 8 are formed respectively in well 4 in substrate 1 at both sides of the gate region 6 through etching processes by using the photoresist layer with the first trench pattern and the second trench pattern as a mask. Further, the gate region also serves as a mask. Thus, first trench 7 may be formed self-aligned to the first side of gate region 6, and second trench 8 may be formed self-aligned to the second side of gate region 6. The first trench 7 and the second trench 8 are located in the well region 4, and the depths of the first trench 7 and the second trench 8 are substantially the same. After a first trench 7 and a second trench 8 are formed, the photoresist is removed. The first trench 7 and the second trench 8 are located close to both sides of the gate region 6, and the depths thereof are controlled accurately by etching time.

[0034] Referring again to Figure 1, Step 23 shows forming a first lightly doped drain region and a second lightly doped drain region in the first trench and the second trench, respectively. The step of forming the first lightly doped drain region and a second lightly doped drain region may further include filling the first trench with the first lightly doped drain region and filling the second trench with the second lightly doped drain region, the first lightly doped drain region and the second lightly doped drain region being of a second conductivity type. An upper surface of the first lightly doped drain region and an upper surface of the second lightly doped drain region may be formed substantially at the same plane as an upper surface of the substrate. The step of filling the first trench and filling the second trench may be by selective epitaxial growth in the first trench and in the second trench.

[0035] Referring now to Figure 6, in accordance with an embodiment of the present invention, a lightly doped drain epitaxial growth is performed in the first trench and the second trench by epitaxial growth processes. Because the substrate 1 outside the first trench and the second trench (i.e. at the sides far away from gate region 6) is coated with gate oxide layer 5, the epitaxial growth is selective epitaxial growth, i.e., the epitaxial growth is performed only in the first trench and the second trench. Therefore, the result of the selective epitaxial growth is that a first lightly doped drain region 9 and a second lightly doped drain region 10 are formed at both sides of gate region 6, respectively. In this embodiment, first lightly doped drain region 9 and the second lightly doped drain region 10 are both N-type LDDs. Furthermore, in this embodiment, the epitaxial growth may use low temperature selective epitaxial growth, in which the low temperature is about between 600°C to 800°C. Doping concentration may be non-uniform if the temperature is too high. First lightly doped drain region 9 and a second lightly doped drain region 10 may be formed using in-situ doping during epitaxy formation. The fill heights of first lightly doped drain region 9 and second lightly doped drain region 10 formed by epitaxial growth in the trenches may be substantially kept at a same plane with the surface of substrate 1.

[0036] Referring again to Figure 1, Step 24 shows forming a third trench and a fourth trench in the substrate outside the first trench and the second trench, respectively. In other words, Step 24 shows forming a third trench in the substrate overlapping at least a first portion of the first lightly doped drain region and a fourth trench in the substrate overlapping at least a first portion of the second lightly doped drain region.

[0037] Step 24 may include forming a first side wall on the first side of the gate region and forming a second side wall on the second side of the gate region. The step of forming the first side wall and forming the second side wall may include depositing a dielectric layer over the substrate, and etching back the dielectric layer by an anisotropic etch process. A dielectric layer is deposited over the substrate, and the dielectric layer spreads all over the surface of the gate region, the first lightly doped drain region, the second lightly doped drain region, and over the gate oxide layer 5. In this embodiment, the dielectric layer is silicon dioxide..

[0038] The dielectric layer is etched back by dry etching process. In this embodiment,

the etching back process is performed by an anisotropic plasma etcher, which does not need a mask. Referring to Figure 7, in accordance with an embodiment of the present invention, the result of the etching back process is that a first side wall 11 is formed on the first side of the gate region 6, and a second side wall 12 is formed on the second side of the gate region 6. First side wall 11 and second side wall 12 are located at opposite sides of the gate region 6 to avoid source-drain punch through that may be induced by a following step of forming the sources and drains.

[0039] Step 24 may further include depositing a salicide blocking (SAB) material layer over the substrate. In this embodiment, the SAB material layer is silicon dioxide. Then, a photoresist layer is formed having a third trench pattern and a fourth trench pattern on the SAB material layer. Step 24 may further include forming the third trench and the fourth trench by etching through the SAB material layer, etching the first portion of the first lightly doped drain region, etching the first portion of the second lightly doped drain region, and etching into the substrate. The etching is prevented under the photoresist layer, the first side wall, the second side wall, and the gate region. Then the photoresist layer is removed

[0040] Referring to Figure 8, in accordance with an embodiment of the present invention, photoresist is spin coated over the substrate 1 on the SAB material layer. The photoresist is exposed using an existing S/D (or SAB) photomask. After the exposure, the development is performed to form a photoresist layer 16 with a third trench pattern and a fourth trench pattern over the substrate 1 on the SAB material layer. The patterning for the photoresist may be adapted to merge the pattern for the third trench pattern and the fourth trench pattern into one region, which substantially overlaps the gate region.

[0041] A third trench 13 and a fourth trench 14 are formed respectively in well region 4 in substrate 1 outside first side wall 11 and outside second side wall 12 using etching processes, by using the photoresist layer 16 with the third trench pattern and the fourth trench pattern as a mask. Further, the first side wall, the second side wall, and the gate region also serve as masks against the etching. Thus, third trench 13 may be formed self-aligned to both first side wall 11 and the first side of gate region 6, and fourth trench 14 may be formed self-aligned to both second side wall 12 and the second side of gate region 6.

[0042] The etching of trench 13, may also remove a portion of first LDD region 9 furthest away from the first side of gate region 6. Similarly, the etching of trench 14, may also remove a portion of second LDD region 10 furthest away from the second side of gate region 6. Thus, trench 13 and 14 are self-aligned to first LDD region 9 and second LDD region 10, respectively. At the same time, a SAB material layer 15 is left formed on the substrate 1 under patterned photoresist layer 16. The third trench and the fourth trench are located in the well region 4, the depths thereof are substantially the same, which may be greater than the depths of the first trench and the second trench. The depths of the third trench 13 and the fourth trench 14 are controlled accurately by etching time, and are less than $0.1\mu\text{m}$ in this embodiment. And then the photoresist layer 16 is removed.

[0043] Referring again to Figure 1, Step 25 shows forming a source region and a drain region in the third trench and the fourth trench respectively. The step of forming the source region and the drain region further may further include filling the third trench with the source region and filling the fourth trench with the drain region, the source region and the drain region being of the second conductivity type. An upper surface of the source region and an upper surface of the drain region may be formed substantially at the same plane as an upper surface of the substrate. The step of filling the third trench and filling the fourth trench may be by selective epitaxial growth in the third trench and in the fourth trench.

[0044] Referring to Figure 9, in accordance with an embodiment of the present invention, a source/drain epitaxial growth is performed in the third trench and the fourth trench by epitaxial growth processes. Because the substrate 1 outside the third trench and the fourth trench (i.e. at the sides far away from the gate region 6) is coated with the SAB material layer 15, the epitaxial growth is selective epitaxial growth, i.e., the epitaxial growth is performed only in the third trench and the fourth trench. Therefore, the result of the selective epitaxial growth is that a source region 17 and a drain region 18 are formed respectively self-aligned to first lightly doped drain region 9 and second lightly doped drain region 10 at the sides further out from gate region 6. In this embodiment, source region 17 and drain region 18 are N-type source/drain. Furthermore, in this embodiment, the epitaxial growth is low temperature selective epitaxial growth, in which the low temperature is about between 600°C to 800°C . Doping concentration may be non-uniform if the temperature is too high. The fill heights of source region 17 and drain

region 18 formed by epitaxial growth in the trenches may be substantially kept at a same plane with the surface of the substrate 1. Source region 17 and drain region 18 may be formed using in-situ doping during epitaxy formation. The doping concentrations of source region 17 and drain region 18 may be greater than those of first lightly doped drain region 9 and second lightly doped drain region 10.

[0045] It may be seen from the above embodiments that the depths of the third trench and the fourth trench are corresponding to the depths of junctions of the source region and the drain region formed later, and the depths of the third trench and the fourth trench may be controlled accurately by etching time. Therefore, a source/drain shallow junction may be formed by controlling the etching time, so as to fabricate a small-scale MOS device.

[0046] Furthermore, in the method provided by the present invention, the processes of forming the lightly doped drain region, the source region and the drain region do not adopt the implantation process used in conventional process, and thus the annealing process is omitted, so as to simplify the whole process flow.

[0047] In accordance with an embodiment of the present invention, the method for fabricating a small-scale MOS device may further include forming metal silicide on the source region and the drain region, respectively. Metal silicide may be optionally formed on portions of the first LDD region and the second LDD region that extend out from under first sidewall 11 and second sidewall 12, respectively. The step of forming metal silicide on the source region and the drain region respectively may further include; depositing a metal over the substrate and on the SAB material layer, annealing the metal and forming metal silicide except over the SAB material layer, and removing the metal over the SAB material layer.

[0048] When the third trench and the fourth trench are formed in the substrate in the SAB material layer is left on the substrate. In this embodiment, metal is deposited over the substrate and on the SAB material layer by sputtering process, wherein the metal may be Ti, Co or other metal. Then an annealing process may be performed on the metal, and the metal does not react with the silicon oxide (the SAB material layer). Therefore, those two materials will not be chemical bonded and physically aggregated. However, the metal will react with silicon in the substrate during the annealing to generate a corresponding metal silicide, such as TiSi_2 or CoSi_2 . Thus, after the annealing process is

performed on the metal, metal silicide is formed on the source region and the drain region respectively, and optionally formed on portions of the first LDD region and the second LDD region that extend out from under first sidewall 11 and second sidewall 12, respectively.

5 [0049] Because that the metal does not react with the SAB material layer on the substrate, the metal that is not subjected to the reaction may be etched off easily. That is to say, the metal on regions of the substrate except the source region and the drain region and optionally on portions of the first LDD region and the second LDD region that extend out from under first sidewall 11 and second sidewall 12, respectively, is removed. Then, the
10 SAB material layer on the substrate may be removed.

[0050] Figure 10, in accordance with an embodiment of the present invention, shows metal silicide 19 on the source region 17 and the drain region 18. Whether metal silicide is formed on the gate region may be determined as required.

[0051] In accordance with an embodiment of the present invention, metal silicide is
15 formed on the source region and the drain region by means of the SAB material layer, which was defined by the photolithography step used to define the third and the fourth trench regions. Compared with the conventional silicide process technique, a photolithography process step is omitted, i.e., source/drain process and SAB process may be performed by photolithography once, so that the cost is decreased and the production
20 efficiency is improved.

[0052] It is noted that, in the present invention, relation terms such as “first” and “second” are used only to distinguish one entity or operation from the other entity or operation, but not sure to demand or indicate that there are those actual relations or orders among those entities and operations. Furthermore, the terms “including”, “comprising”, or
25 any other grammatical variations are used in the inclusive sense of “comprising” with non-excludability, so that process, method, article or device that includes series of the elements include not only those elements but also other elements that are not listed, or further include inherent elements of this process, method, article or device. In the case of no more restriction, an element defined by the sentence “including one ...” does not
30 indicate that there are no other same elements in the process, method, article or device that includes said element.

[0053] In the present specification, the embodiments are described in progression, each embodiment mainly focuses on the difference between itself and other embodiments, therefore the description is brief, and references may be made to those similar parts in the description of the method.

- 5 [0054] Embodiments of the present invention provide an apparatus and a method for fabricating MOS devices. It will be apparent to those with skill in the art that modifications to the above methods and apparatuses may occur without deviating from the scope of the present invention. The embodiments of the present invention are not limited by the type of transistor, PMOS, NMOS or otherwise, used to fabricating MOS devices.
- 10 The embodiments of the present invention are not limited by the type of integrated circuit in which the present invention may be disposed. Nor are the embodiments of the present invention limited to any specific type of process technology, e.g., CMOS, Bipolar, or BICMOS that may be used to manufacture MOS devices. Accordingly, the disclosures and descriptions herein are intended to be illustrative, but not limiting, of the scope of the
- 15 invention, which is set forth in the following claims along with their full scope of equivalents.

WHAT IS CLAIMED IS:

1. A method for fabricating a small-scale metal-oxide-semiconductor (MOS) device comprising:

5 preparing a substrate of a first conductivity type, a gate oxide layer being formed on the substrate, and a gate region being formed on the gate oxide layer;

forming a first trench in the substrate along a first side of the gate region and forming a second trench in the substrate along a second side of the gate region, the first side of the gate region being opposite the second side of the gate region;

10 forming a first lightly doped drain region and a second lightly doped drain region in the first trench and the second trench, respectively;

forming a third trench in the substrate overlapping at least a first portion of the first lightly doped drain region and a fourth trench in the substrate overlapping at least a first portion of the second lightly doped drain region; and

15 forming a source region and a drain region in the third trench and the fourth trench, respectively.

2. The method according to claim 1, further comprising forming metal silicide on the source region and the drain region respectively.

20 3. The method according to claim 1, wherein the step of forming the first trench and forming the second trench further comprises:

forming a photoresist layer having a first trench pattern and a second trench pattern on the gate oxide layer;

25 forming the first trench and the second trench by etching through the gate oxide layer and etching into the substrate, the etching being prevented under the photoresist layer and the gate region; and

removing the photoresist layer.

30 4. The method according to claim 1, wherein the step of forming the first lightly doped drain region and a second lightly doped drain region further comprises filling the

first trench with the first lightly doped drain region and filling the second trench with the second lightly doped drain region, the first lightly doped drain region and the second lightly doped drain region being of a second conductivity type.

5 5. The method according to claim 4, wherein the step of forming the third trench and the fourth trench further comprises:

 forming a first side wall on the first side of the gate region and forming a second side wall on the second side of the gate region;

 depositing a salicide blocking (SAB) material layer over the substrate;

10 forming a photoresist layer having a third trench pattern and a fourth trench pattern on the SAB material layer;

 forming the third trench and the fourth trench by etching through the SAB material layer, etching the first portion of the first lightly doped drain region, etching the first portion of the second lightly doped drain region, and etching into the substrate, the etching
15 being prevented under the photoresist layer, the first side wall, the second side wall, and the gate region, and

 removing the photoresist layer.

 6. The method according to claim 1, wherein the step of forming the source region
20 and the drain region further comprises filling the third trench with the source region and filling the fourth trench with the drain region, the source region and the drain region being of the second conductivity type.

 7. The method according to claim 5, wherein the step of forming metal silicide on the
25 source region and the drain region respectively further comprises:

 depositing a metal over the substrate and on the SAB material layer;

 annealing the metal and forming metal silicide except over the SAB material layer;
and

 removing the metal over the SAB material layer.

30

 8. The method according to claim 1, wherein the step of preparing a substrate, a gate

oxide layer being formed on the substrate, and a gate region being formed on the gate oxide layer, further comprises:

preparing a substrate;

forming a screen oxide layer on the substrate;

5 forming a well region of the first conductivity type in the substrate;

removing the screen oxide layer;

forming a gate oxide layer over the substrate and on the well region; and

forming a gate region on the gate oxide layer.

10 9. The method according claim 5, wherein the step of forming the first side wall and forming the second side wall comprises:

depositing a dielectric layer over the substrate; and

etching back the dielectric layer by an anisotropic etch process.

15 10. The method according to any one of claims 1 to 9, wherein the gate region is SrTiO_3 , HfO_2 , ZrO_2 , or polysilicon.

11. The method according to any one of claims 1 to 9, wherein the depths of the third trench and the fourth trench are less than $0.1\mu\text{m}$.

20

12. The method according to any of claims 1 to 9, wherein the depths of the third trench and the fourth trench are greater than the depths of the first trench and the second trench.

25 13. The method according claim 4, wherein an upper surface of the first lightly doped drain region and an upper surface of the second lightly doped drain region are substantially at the same plane as an upper surface of the substrate.

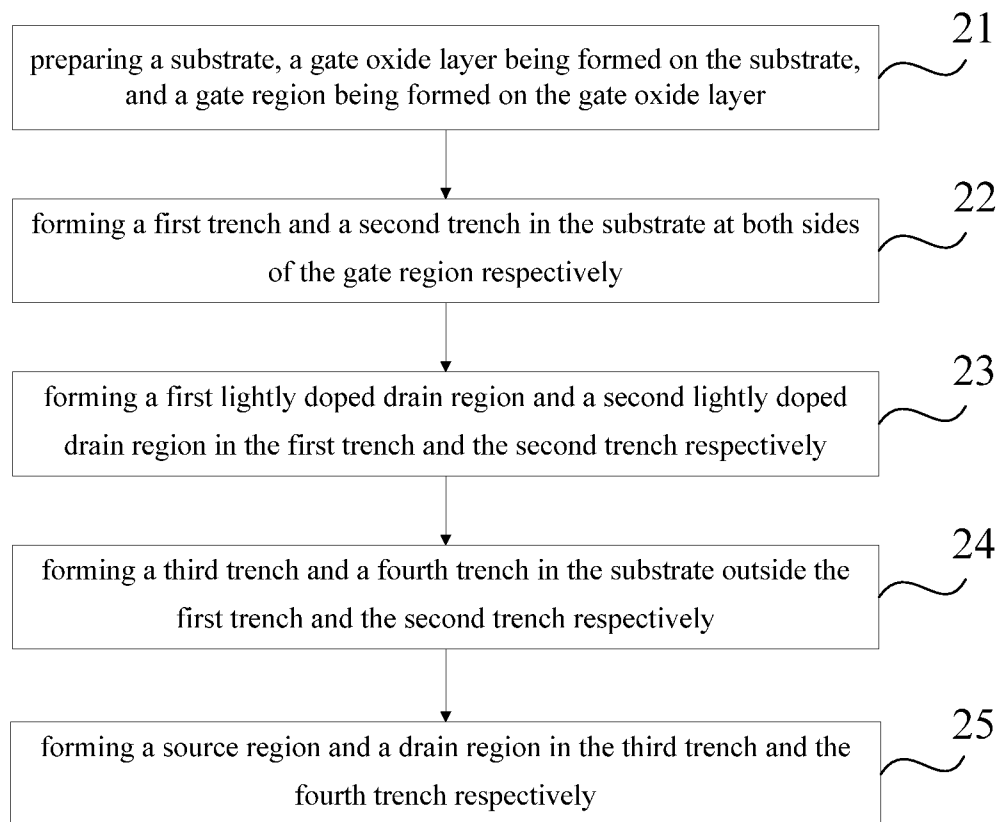
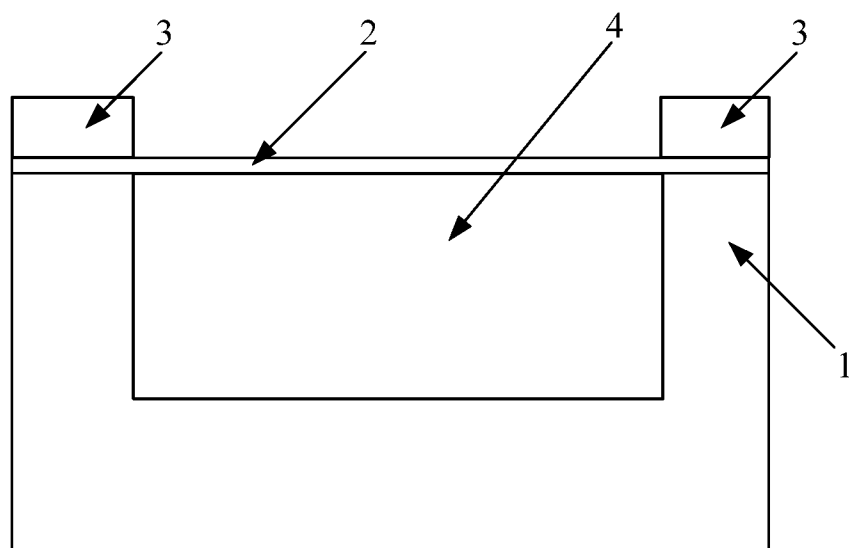
30 14. The method according claim 4, wherein the step of filling the first trench and filling the second trench is by selective epitaxial growth in the first trench and in the

second trench.

15. The method according claim 6, wherein an upper surface of the source region and
an upper surface of the drain region are substantially at the same plane as an upper surface
5 of the substrate.

16. The method according claim 6, wherein the step of filling the third trench and
filling the fourth trench is by selective epitaxial growth in the third trench and in the fourth
trench.

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**Fig. 1****Fig. 2**

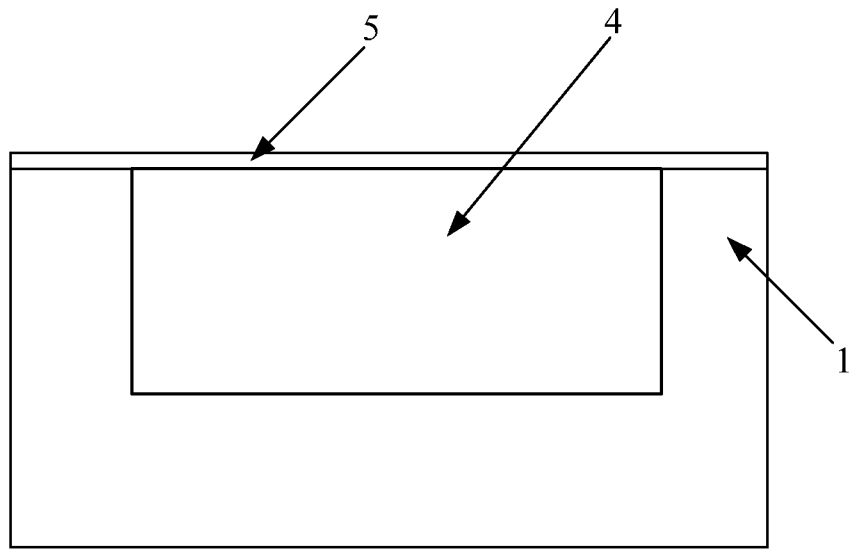


Fig. 3

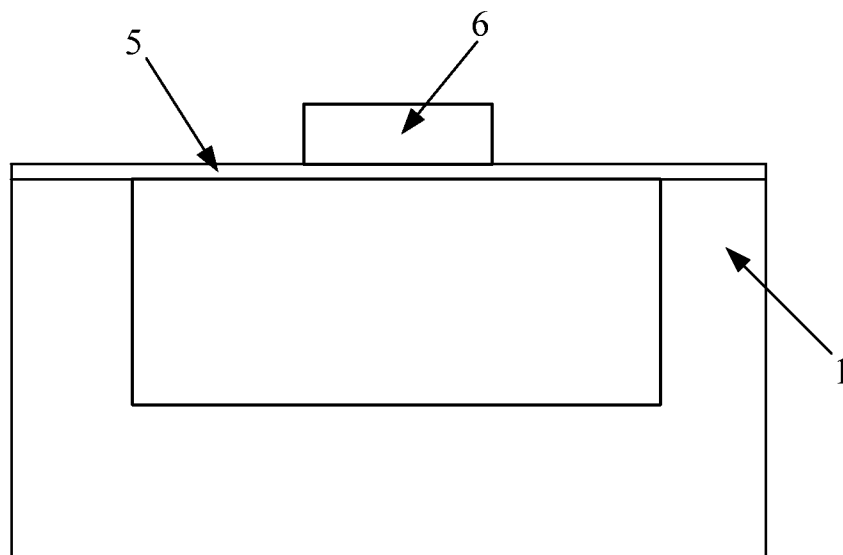


Fig. 4

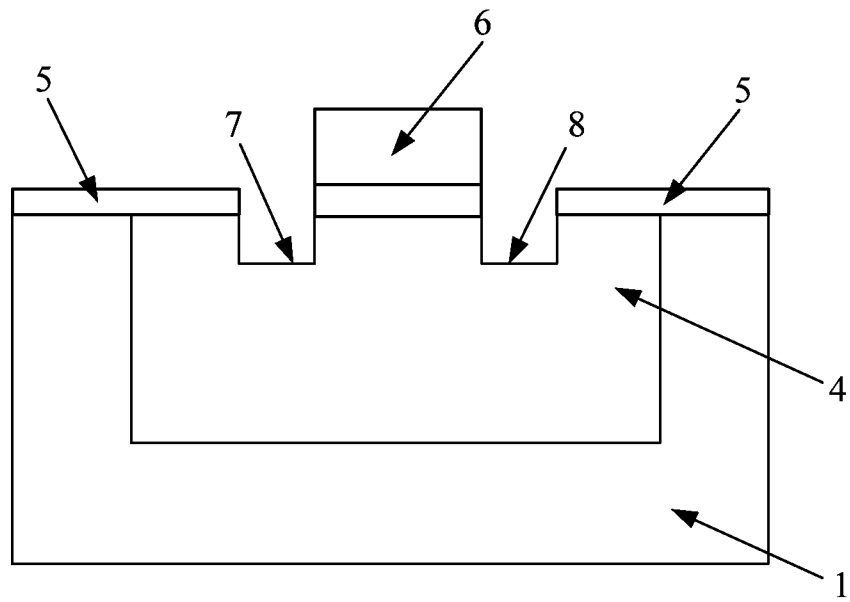


Fig. 5

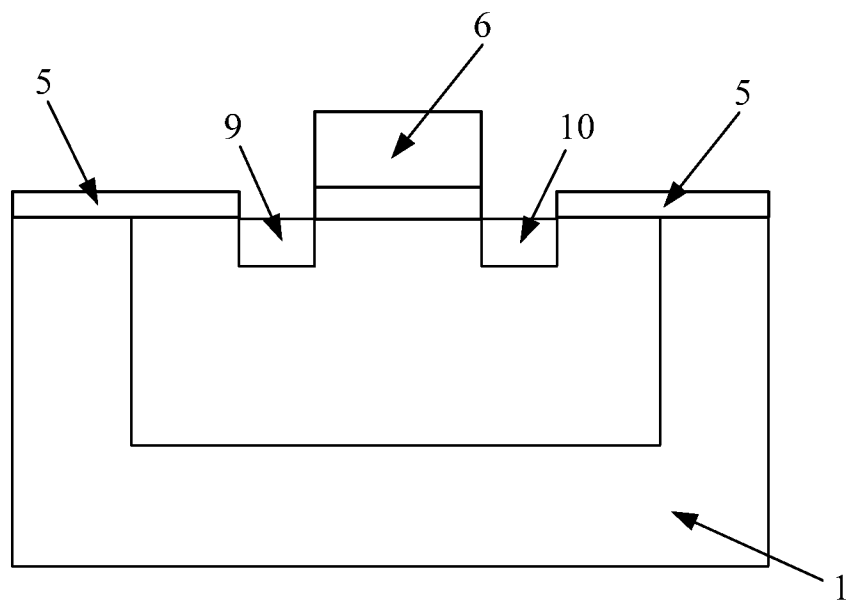


Fig. 6

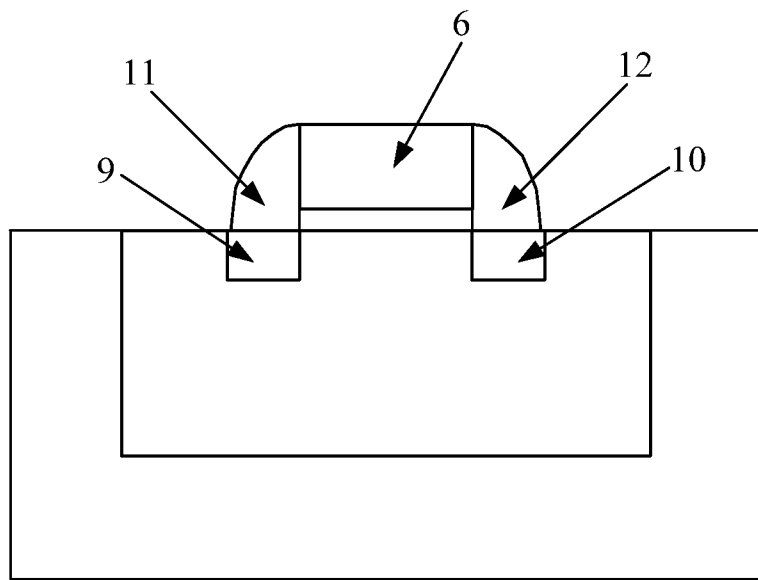


Fig. 7

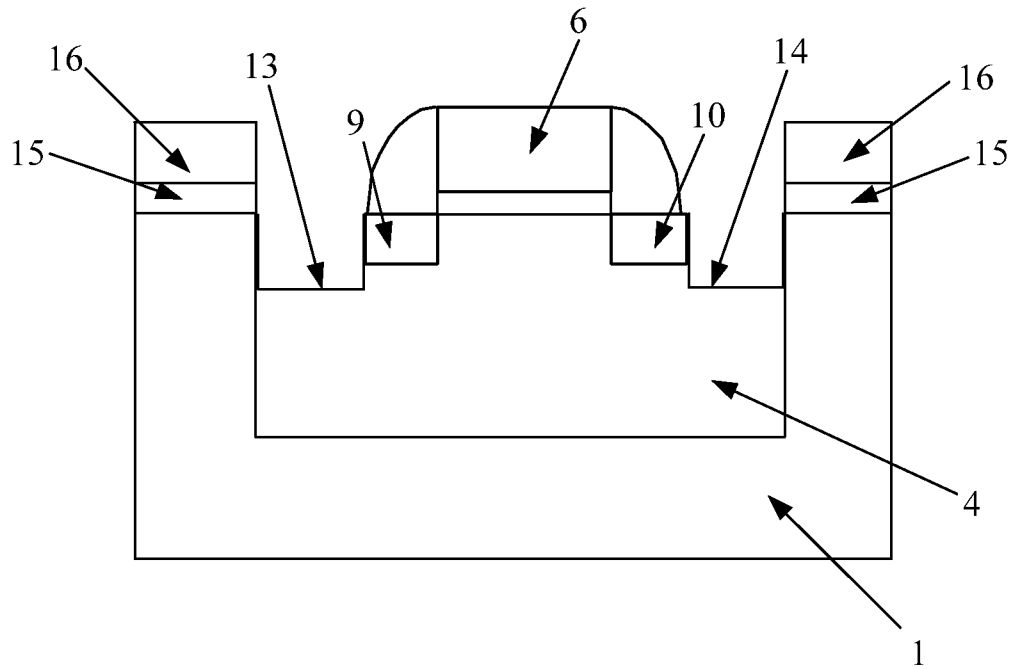


Fig. 8

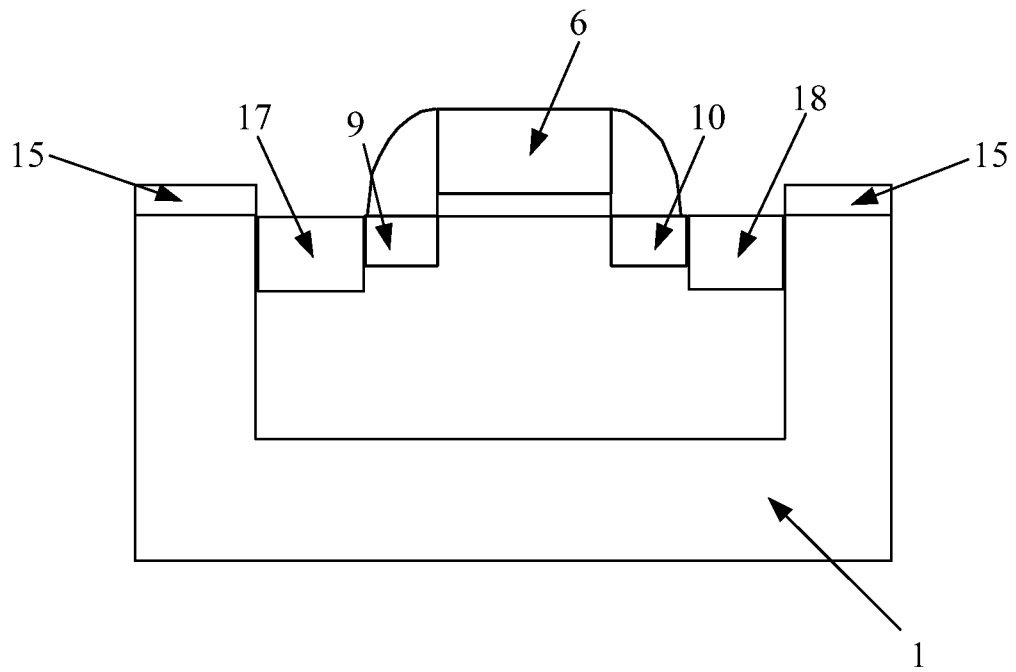


Fig. 9

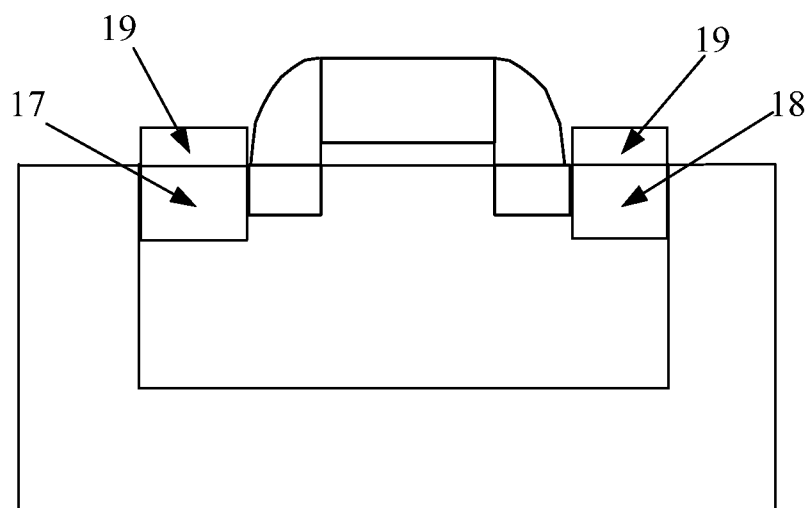


Fig. 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/080557

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L21/-, H01L29/-, H01L27/-

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, EPDOC, CNPAT, CNKI: MOS, transistor, LDD, lightly, dope, drain, trench, groove, selective, epitaxial growth, size

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US5598021A (LSI LOGIC CORPORATION) 28 Jan. 1997(28.01.1997) the whole document	1-16
A	CN101388415A (HONGLI SEMICONDUCTOR MFR CO., LTD.)18 Mar. 2009(18.03.2009) the whole document	1-16
A	US5538909A (UNITED MICROELECTRONICS CORPORATION) 23 Jul. 1996(23.07.1996) the whole document	1-16

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:	“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“A” document defining the general state of the art which is not considered to be of particular relevance	“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“E” earlier application or patent but published on or after the international filing date	“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“L” document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)	“&” document member of the same patent family
“O” document referring to an oral disclosure, use, exhibition or other means	
“P” document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 28 Dec. 2011(28.12.2011)	Date of mailing of the international search report 19 Jan. 2012 (19.01.2012)
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer XIE, Chaofang Telephone No. (86-10)62411899

International application No.
PCT/CN2011/080557

Form PCT/ISA /210 (patent family annex) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2011/080557

CLASSIFICATION OF SUBJECT MATTER

H01L 21/336 (2006.01) i

H01L 21/265 (2006.01) i