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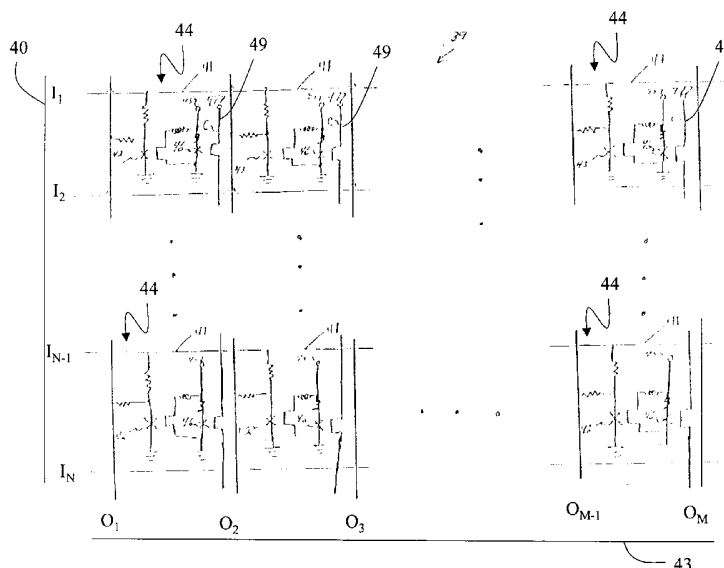
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(54) Title: SUPERCONDUCTIVE CROSSBAR SWITCH



(57) Abstract: A superconductor crossbar switch for connecting a plurality of inputs with a plurality of outputs, including a switching cell having an input, an output and a circuit for connecting the input with the output for bidirectionally transmitting data therebetween. The connection of the retaining and releasing circuitry of a plurality of cells enables the switch to simultaneously retain a selected cell or cells of a group of cells and disable the remaining cells of that group, whereby a subsequent query on a disabled cell is inoperative until the selected cell or cells is released. The crossbar switch is characterized by latency on the order of nanoseconds, a data rate per channel on the order of gigabits per second, essentially zero crosstalk, and detection of contention in nanoseconds or less and resolution of contention in nanoseconds or less.



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**TITLE OF THE INVENTION****SUPERCONDUCTIVE CROSSBAR SWITCH**

This application claims priority from U.S. Provisional Application Serial  
5 No. 60/306,880 filed July 23, 2001. The entirety of that provisional application is  
incorporated herein by reference.

**BACKGROUND OF THE INVENTION****Field of the Invention**

The present invention relates to superconductive switching devices, and in  
10 particular to a superconducting crossbar switch for bidirectionally connecting a  
plurality of inputs with a plurality of outputs.

**Background of the Technology**

Advances in high performance computing are being pursued in many  
different directions. The technology thrust has been directed toward very high  
15 speed, high circuit density chips which are of low power (to permit small volume  
packaging) and organized into a small number of processors. Another thrust  
involves the use of many processors, tens to perhaps thousands, working in concert  
to perform the computation. In this case, the stress on the individual elements is  
relieved and there is greater computational power, but interconnection problems  
20 that arise with the added software complexity must be solved.

One of the configurations for a massively parallel computing system calls  
for a large number of processors to be connected to a large shared memory system  
on an equal access basis. The demands placed upon the interconnection switch are  
formidable, in terms of complexity, speed, and intelligence. For example, the  
25 switch must have a short latency time and must establish the requested connection  
very quickly, ideally within a small fraction of the processor clock time. The data  
rate per channel must also be very high. For example, for a 32 bit word machine  
with a 30 nanosecond clock, a data rate of  $10^9$  bits/second (i.e., gigabits/second)

per processor is required. Once established, the data path must be immune to noise, and crosstalk must be kept to a minimum. The established link must be inviolate during the processor transaction time and releasable very quickly, ideally within a clock cycle.

5           There is a need to inform the processor of successful connection. The time during which two or more processors contend for the same memory port needs to be minimized with fast resolution of these contentions. Finally, data needs to be transferred in both directions. Although there are a number of switch architecture solutions, it is generally accepted that the best solution is a crossbar, which is a  
10           switch that allows the requesters equal access at the same level to any output line.

Computer systems also need high bandwidth and short access times to carry out data exchange between memory and processors, and among processors.

#### **Related Art**

          Crossbar switches are well-known in the prior art, as evidenced by U.S.  
15           Patent No. 3,539,730 to Imamura, which discloses a crossbar switch used in a two-stage link connection system. Each switch is divided into two parts, in accordance with vertical groups. The parts of the switch are assigned to primary and secondary lattices, respectively, with links between the lattices being formed by connecting the outgoing lines from the primary lattice of one switch with the  
20           secondary lattice of another switch.

          Also known in the art are polarity switching circuits which utilize Josephson junction devices (e.g., interferometers) and superconducting interconnections coupled to a utilization circuit, including one or more memory cells or logic circuits. Such circuits are disclosed, for example, in U.S. Patent No.  
25           4,210,921 to Faris.

          Prior switching circuits possess certain inherent drawbacks that render them unsuitable for use with large numbers of computing elements. As a result, they cannot meet all of the requirements set forth above for a massively parallel computing system.

### SUMMARY OF THE INVENTION

The present invention overcomes the above identified drawbacks of the prior switching circuits, as well as others, by providing a modular crossbar switch that is extendable in size, operates under low power with low latency, and detects and resolves conflicts that arise when two or more processors contend for the same memory port. The switch of the present invention is capable of interconnecting N computers or processors with M memories, or other processors or computers where N and M can be of the order of 1000 or more. One embodiment of the present invention is also modular, in that small crossbars can easily be extended to become very large ones, (e.g., 32 x 32 can grow into 1000 x 1000). In addition, if the computer data rate exceeds that of one channel, paralleling of channels is easily performed. The switch is also suitable for general communications network usage, as well.

An embodiment of the present invention includes a crossbar switch for connecting a plurality of input devices with a plurality of output devices, and a switching cell having an input, an output, and an apparatus for connecting the output for bi-directionally transmitting data therebetween. The connecting apparatus includes a superconductive device having zero resistance and negligible crosstalk, and a control device to control operation of the connecting apparatus. The connecting apparatus provides a connection for a plurality of processors or functional units to be connected to one another. For example, a configuration of adders, multipliers, and dividers can be switched, such that data can be routed sequentially from one function to another with arbitrary freedom.

Another embodiment of the present invention includes a second superconductive device and a second control device to retain and release the operation of the first superconductive device.

An additional embodiment of the present invention includes a plurality of inputs, a plurality of outputs, and a plurality of cells arranged in a matrix, with the inputs coupled to one plurality of cells and the outputs connected to another plurality of cells, so as to define a superconducting device matrix. In an

embodiment of the present invention, the cells are connected in parallel with the inputs and outputs.

In a further embodiment of the present invention, each output includes a summing device for summing output voltages or currents of the cells connected therewith, in order to accommodate the inputs and to render the matrix extendable in numbers of inputs and outputs. The summing device may include a summing amplifier or an additional superconductive device. In another embodiment of the present invention, the switching cells include a feedback mechanism connected to the outputs which feeds data to the outputs and acknowledges pulses back to a requestor.

In yet another embodiment of the present invention, retaining and releasing devices for the cells are connected to the outputs and are interconnected and operable to simultaneously retain a selected cell of the plurality of cells, and disable the remaining cells of the plurality of cells, whereby a subsequent query on a disabled cell is inoperative until the selected cell is released. The crossbar also allows multicast or broadcast operation wherein any one input may be connected simultaneously or in arbitrary order to more than one or all of the output ports.

In a further embodiment of the invention, a sensing apparatus is connected with each of the outputs for detecting simultaneous queries to cells of the respective groups of cells and for generating to the processors via the cells an indication of conflict from the simultaneous queries as well as resolving these conflicts while preventing further interference.

Additional advantages and novel features of the invention will be set forth in part in the description that follows, and in part will become more apparent to those skilled in the art upon examination of the following or upon learning by practice of the invention.

### **BRIEF DESCRIPTION OF THE FIGURES**

In the drawings:

FIG. 1 illustrates a prior art Josephson junction device;

FIG. 2 is a graph illustrating the operation of the Josephson junction device of FIG. 1;

FIG. 3 is a simplified perspective view of a prior art Josephson junction device with a magnetic field control line;

5           FIG. 4 shows prior art operation of Josephson junctions in which a resistor is placed between the electrode and the counter-electrode for the device shown in FIG. 1;

FIG. 5 is a schematic representation of a prior art Superconducting Quantum Interference Device (SQUID) device;

10           FIG. 6 is a graph representing the operation of the SQUID device of FIG. 5;

FIG. 7 illustrates a matrix of cells comprising a superconductive crossbar switch, in accordance with an embodiment of the present invention;

15           FIGs. 8 and 9 illustrate use of the superconductive crossbar switch, in accordance with an embodiment of the present invention;

FIGs. 10 and 11 illustrate use of the superconductive crossbar switch, connected to a summing device, in accordance with an embodiment of the present invention;

20           FIG. 12 is a schematic representation of a switch illustrating a plurality of summing devices, and the clamping and crossbar cell memory circuit, in accordance with an embodiment of the present invention;

FIG. 13 is a schematic representation of the cell circuits and clamp circuit and their operation in the situation of no contention, in accordance with an embodiment of the present invention;

25           FIG. 14 is a flow diagram illustrating operation of the circuits of FIG. 12, in accordance with an embodiment of the present invention;

FIG. 15 is a timing diagram illustrating the operation of the circuits of FIG. 13, and a situation of non-simultaneous request (no contention) for a memory line, in accordance with an embodiment of the present invention;

FIG. 16 is a schematic representation of the cell circuits in the situation of two simultaneous requests for the same memory line, in accordance with an embodiment of the present invention;

5 FIG. 17 is a timing diagram illustrating the operation of two processors contending for the same output line, in accordance with an embodiment of the present invention;

FIG. 18 illustrates a representative physical layout of a 128 x 128 crossbar switch, in accordance with an embodiment of the present invention; and

10 FIG. 19 illustrates a representation of a crossbar switch chip, including separate decoders and the switching matrix, in accordance with an embodiment of the present invention.

### **DETAILED DESCRIPTION OF THE INVENTION**

15 FIG. 1 illustrates a Josephson tunnel junction device known in the prior art. The Josephson tunnel junction device includes top and bottom layers 20, 21 of superconductor material sandwiching a thin insulating film 22. If a voltage  $V$  is applied between the top and bottom layers through a resistance  $R$ , there is a range of current in which zero resistance current up to  $I_m$ , can be transported between the two elements.

20 FIG. 2 illustrates the behavior of the circuit current  $I$  as the input voltage  $V$  is increased for a representative resistance  $R$ , in the Josephson tunnel junction device shown in FIG. 1. The voltage  $V_j$  across the device will be zero until the device current exceeds  $I_m$ , at which point the junction will switch to the voltage state consistent with the circuit load resistor  $R$  and the device's own voltage-current curve  $J$ , determined by the physics and manufacturing art.

25 FIG. 3 illustrates a Josephson junction device 29 known in the prior art, in which switching occurs by imposing a magnetic field into a junction via a control line placed above it. The current  $I$  to be controlled is carried through a first layer of superconducting material 30 on a substrate 31. A thin film of insulator 32 separates the first superconducting material 30 from a second layer of  
30 superconducting material 33. An insulator layer 35 separates layer 33 from a third

layer of superconducting material 36. When a control current  $I_c$ , passes through layer 36, a magnetic field 37 is created at the junction, which reduces the maximum allowed zero resistance current. Thus, if the device's transport current  $I$  is greater than the new allowed value, the device will switch into the voltage state, similar to as described above with regard to FIGs. 1 and 2. The device can be fabricated to switch with picosecond rise times, with its final voltage state in the millivolts range for presently available materials. The currents that are switched are most often in the hundreds of microamperes range. The power dissipation per unit is in the microwatt range.

10 The prior art also includes fabrication of Josephson Junctions in which the device has the current versus voltage curve represented by FIG. 4, as compared with FIG. 2. This behavior may be acquired by a resistor being placed between the electrode and the counter-electrode of the device in FIG. 1. Or, equivalently, one may achieve such a "weak link" behavior by fabricating the Josephson device with a conductor between the two electrodes of FIG. 1. It is also well known that such behavior is a standard property of so-called "high temperature" superconductive Josephson Junctions. The effect of such a device is to provide a voltage, when switched, which is dependent upon the resistors in the circuit. Nevertheless, the circuits required can still be made from such junctions.

20 If one connects a Josephson junction in parallel with an inductance, the closed loop forms a Superconducting Quantum Interference Device (SQUID), which is also known in the prior art. Insertion of a second junction into this loop, as illustrated in FIG. 5, also produces a SQUID, but with device properties that are very advantageous in switching applications. In particular, if an input current  $I_g$  is inserted and divided between the two junctions,  $J_1$  and  $J_2$ , that zero resistance transport current can be controlled by introducing magnetic flux into the closed loop via the control current,  $I_c$ . FIG. 6 shows the curve of allowed zero resistance current,  $I_g$ , as a function of the imposed control current,  $I_c$ .  $I_m$  represents the maximum gate current  $I_g$  as a function of the control current  $I_c$ . In particular, if an input current  $I_g$  is inserted, it will be divided into two paths according to the size of the inductors  $L_1$ , and  $L_2$  and the maximum critical currents of  $J_1$  and  $J_2$ , as well as

by the control line current  $I_c$ , which is magnetically coupled to the loop. FIG. 6 represents the joint values of  $I_g$  and  $I_c$ , for which current  $I_g$  can be transported through the loop with zero resistance. This region is represented by the shaded area. Joint values of  $I_g$  and  $I_c$ , which are above this area, will result in non-zero voltage transport of  $I_g$ . A control line can thus be used to change the maximum zero resistance current of a two terminal Josephson junction, or SQUID. The detailed properties depend upon the inductance, critical currents of the device, and insertion point(s) of the currents. (A more detailed explanation of the structure and operation of the Josephson junction and the SQUID is found in the IBM Journal of Research and Development, vol. 24, No. 2 (March 1980), which is hereby incorporated by reference.)

### **Superconductive Crossbar Switch**

FIG. 7 illustrates a superconductive crossbar switch, in accordance with an embodiment of the present invention. The superconductive crossbar switch 39 includes at least one cell 41 in a matrix, which are arranged in rows and columns in accordance with the number of input lines  $I_i$  40 and output lines  $O_i$  43. For example, there are N inputs and M outputs for coupling, such as via or including wired, wireless, or fiberoptic connections, N processors with M memories. The number of inputs and outputs need not be equal. In one embodiment of the present invention, the superconductive crossbar switch 39 is extendable to accommodate large numbers of processors and memories. Thus, for example, the module can easily be extended from a 32 input x 32 output to a 1024 input x 1024 output configuration, as is further described below.

Each input port connects to a row of cells 41 via an input line  $I_i$  40. Each cell 41 includes a connecting circuit 44, which connects the input line  $I_i$  to a selected output line  $O_i$  for bidirectionally transmitting data therebetween. The connecting circuit includes a first superconductive device 42, which has zero-resistance. A first control signal applied to a first terminal 45 controls the first superconductive device 42 externally on command, for controlling operation of the

superconductive crossbar switch 39. In one embodiment, the first control signal comprises an electrical current.

Each cell 41 also includes a retaining and releasing circuit for retaining (i.e., clamping) and releasing the operation of the first superconductive device 42. The retaining and releasing circuit includes a second superconductive device 46 and a second control signal, delivered through a clamp line 49 at a second terminal 47, for controlling the second superconductive device 46 and the devices 46 of the cells 41 in the same column of cells 41, as shown in FIG. 7.

The first and second superconductive devices 42 and 46 can also be addressed by optical illumination, in another embodiment of the present invention. For example, if the first superconductive device 42 is optically illuminated, the switch cell connection from input to output will be maintained for the duration of the optical signal. In effect, the optical beam has "enabled" the desired connection. If the second superconductive device 46 is addressed by the optical beam, the current will be steered into the control line for the first superconductive device 42. Alternatively, an electron beam could be used instead of an optical beam.

When the cells 41 are arranged in a matrix as shown in FIG. 7, each input line  $I_i$  40 is coupled to a cell 41 (e.g., a row of cells), thereby to define a matrix of cells.

#### 20 **Method of Using the Superconductive Crossbar Switch**

FIGs. 8 and 9 illustrate use of the superconductive crossbar switch 39, in accordance with an embodiment of the present invention. Referring to FIG. 8, the processors and memories coupled to the input lines 40 ( $I_i = I_4, I_5, I_6$ ) and output lines 43 ( $O_i = O_8, O_9, O_{10}$ ), respectively, need not be synchronously clocked, but instead may be run independently. The operation will be described for the example of a 32 input x 32 output crossbar chip organized as shown in FIG. 8, but it should be understood that any number of inputs 40 and outputs 43 may be provided. In this example, each of the 32 input lines from the 32 processors transmits a serial bit stream. The first serial bit word, or part of it, from a processor (or other source), contains the address of the specific memory line which the processor is attempting

to acquire. In addition, the address bits are followed by a "FLAG" bit, a "one."  
This first word carrying the destination address and the FLAG bit is input to the  
requesting processor's data line. The decoder selects the appropriate 1<sup>st</sup> control  
line (45a) and powers it, thereby permitting the FLAG bit to proceed to the output  
5 line.

The initial state of each cell is a zero current condition in the first address  
terminals 45a, 45b, 45c, and 45d, corresponding to the first terminal 45 in FIG. 7.  
As there is no current in the address lines, all the devices 42a, 42b, 42c, and 42d  
will short the processor pulses on input lines 40 to ground and therefore no output  
10 is observed at output lines 43.

If now the processor coupled to input line  $I_4$  attempts to access the memory  
coupled to output line  $O_8$ , the process of FIG. 9 is followed. The processor  
decoder selects the address line for the output line  $O_8$ , contained in the processor's  
request word (step 905 of FIG. 9). After the address line is found (decoded), it is  
15 determined if there is a control current for the address line (step 910 of FIG. 9).

If there is a control current (step 910 of FIG. 9), a decoder current is  
impressed at terminal 45a, which depresses the zero resistance current threshold of  
superconductive device 42a, thereby allowing input pulses to be transferred across  
the superconductive device 42a (step 915 of FIG. 9). Subsequent pulses from the  
20 processor or input line  $I_4$  are then fed into the output line  $O_8$ , and thus, for example,  
into a summing circuit 50.

If there is no control current for the address line (step 910 of FIG. 9), the  
input pulses on input line  $I_5$  are not transferred to output line  $O_8$  (step 920 of FIG.  
9), but are shorted to ground by the superconductive device 42b, as shown in FIG.  
25 8. Thus, the input pulses from another processor do not interfere with the data  
pulses from input line  $I_4$  on output line  $O_8$ .

Correspondingly, if, for example, input line  $I_5$  seeks to send data to output  
line  $O_9$ , then a current is impressed at terminal 45d by the processor decoder and  
the input data pulse stream is then imposed upon output line  $O_9$ , with no  
30 interference from the processor coupled to input line  $I_4$  because its control line 45b  
is not driven.

### Superconductive Crossbar Switch Coupled to Summing Device

FIGs. 10 and 11 illustrate use of an example superconductive crossbar switch 39 coupled to a summing device 68, in accordance with an embodiment of the present invention. Referring to FIG. 10, each cell 41 is similar to the cells 41 shown in FIG 8. In addition, each output line 43 is coupled to a summing device 68 containing a third superconductive device 51 controlled by the control line 65. An input driver circuit 52 couples each input line to its corresponding processor.

FIG. 11 illustrates an exemplary process for using the superconductive crossbar switch 39, coupled to a summing device 68, as shown in FIG. 10. In FIG. 10, pulses  $\underline{a}$  from the processor drive additional superconductive devices 55 into the voltage state and thereby impress a voltage on the input line 40 (step 1105 of FIG. 11), which is coupled to all the row cells accessed by that processor. The impressed voltage causes a current to flow through the resistor 57 to be shorted to ground via the first superconductive device 42 (step 1110 of FIG. 11).

It is determined if the control signal provided at terminal 45 is powered (step 1115 of FIG. 11). If yes, that control signal can be made sufficient to reduce the critical current through first superconductive device 42, such that it exhibits a "gap" voltage (step 1120 of FIG. 11). The pulse current passing through the first superconductive device 42 will exceed the maximum zero resistance current and the first superconductive device 42 will switch into the voltage state, thereby impressing its "gap" voltage upon the cell tie point between resistors 57 and 62.

If the control signal is not powered (step 1115 of FIG. 11), the superconductive device 42 may be operated such that it transfers to a resistive state, or the superconductive device 42 itself may be fabricated such that it does not exhibit a "gap" voltage (step 1125 of FIG. 11). This voltage will cause a current to flow through resistor 62 down to the output line 63 through control 65 and additional superconductive devices 66. This current will be insufficient to switch additional superconductive devices 66, and therefore, since control 65 is of very low inductance, the voltage across control 65 and additional superconductive devices 66 will be very small and will decay very rapidly, such that the current through resistor 62 will predominately go through control 65 and only a negligible

amount will pass through resistor 67, and eventually all current will pass through control 65 and additional superconductive devices 66.

The current through control 65 depresses the maximum allowed zero resistance current of superconductive device 51, which then triggers and produces a signal for transfer to the memory circuits (step 1130 of FIG. 11). In an alternative embodiment, other equivalent sensing circuits may be used instead. The pulse sensed by the memory circuit is inverted, amplified, and fed back via terminal 70 (step 1135 of FIG. 11) after an appropriate delay, with sufficient current to exceed the allowed maximum current through superconductive devices 66 and thereby impose a voltage on the output line 43, which will cause current to flow through resistors 62 and 67. However, only superconductive device 42 has a suppressed maximum current, and therefore only line 56 will experience a current back into control 71 via resistor 57; input line 72 will not. As before, control 71 will control superconductive device 75 and the current through superconductive devices 55 will be too small to switch superconductive devices 55 into the voltage state. The input pulse  $\underline{a}$  will be returned as an 'acknowledge' pulse  $\underline{t}$  only to the processor 61, which generated pulse  $\underline{a}$  (step 1140 of FIG. 11), and to no other, provided that the selected cell 41 is the only one energized. This return path is also valid for transfers of data from memory back to the processor 61.

#### 20 **Superconductive Crossbar Switch with Summing Devices**

With reference to FIG. 12, there is shown a crossbar switch 39 having a number of summing devices 78, represented in this embodiment by amplifiers  $M_i$ , coupled to each output line 43 (e.g.,  $O_3, O_9, O_{10}$ ). The summing amplifier  $M_9$  is coupled to output line  $O_9$ , and so on. The summing devices 78 are operable for summing the output voltages of the cells coupled to the respective output line  $O_i$ . Summing the input voltages in this manner enables the crossbar switch to accommodate a plurality of inputs and thus renders the matrix extendable in numbers of inputs and outputs. This comes about because the input terminal of the amplifier is summed to zero voltage, thereby producing no crosstalk from the selected processor to the other processors.

**Superconductive Crossbar Switch with Additional Junction and Control Line**

In order to prevent interference by other processors after an output line has been acquired, an additional junction and control line is provided as is illustrated in FIG. 13. The operation of this device will also be described below with reference to FIGs. 14 and 15. In the crossbar's initial state, current is applied to clamp line C<sub>8</sub>, thereby depressing the maximum zero resistance current of superconductive device 46a (step 1405 of FIG. 14). When terminal 45a is activated, current will be caused to flow through inductor 106 and control line 107, because the critical current of superconductive device 46a has been reduced to below the imposed decoder current level. This will occur because the clamp current C suppresses the maximum zero resistance current of device 46a.

With respect to cell 41b, current at terminal 45b will initially flow into inductor 108 because the inductance of inductor 108 is required to be lower than the inductance of inductor 106 (step 1410 of FIG. 14). However, since superconductive device 46a has its maximum zero resistance current reduced because of the signal imposed at C<sub>8</sub>, superconductive device 46a will switch to the voltage state, and all the current imposed on terminal 45b will be directed through inductor 106 and control line 107.

After the decoder has applied its current at terminal 45b, a flag pulse or set of pulses is inserted into the processor datastream at I<sub>4</sub> (step 1415 of FIG. 14). These pulses would normally immediately follow those that select the address. When these flag pulses are detected on the output line O<sub>8</sub> for the cell, the CLAMP current on C<sub>8</sub> will be dropped (step 1420 of FIG. 14). Now, if decoder power to terminal 45b is removed, the flux stored in inductor 106 will be maintained by a circulating current in the loop comprising inductors 106, 108 and device 46a. This action of dropping the clamp signal succeeds in not only retaining the usage of the output line in cell 41a after the decoder is powered down, but it also prohibits interference by other requesters for the same output line (e.g., in cell 41c).

With reference to cell 45c of FIG. 13, the initial state has the CLAMP line C<sub>8</sub> energized, similar to as described above with regard to FIG. 7. Removal of the CLAMP current at C<sub>8</sub> causes the critical current of device 46a to no longer be

depressed (step 1425 of FIG. 14). Decoder power applied to terminal 45c, will then flow predominately through inductor 111, which is required to have much smaller inductance than the inductance of inductor 112.

5 The resulting current through inductor 112, and thus control line 113, will be insufficient to depress the critical current of device 116 enough for it to switch when data current flows through resistor 117. This, in effect, prevents interference by the processor (step 1430 of FIG. 14) coupled to line  $I_5$ , with the output line  $O_8$  already in use. By extension, this operation will hold for all late requesters for an output line.

10 FIG. 15 summarizes the above described behavior. Processor 1 is shown having powered its decoder output, thereby permitting its flag bit to be sent to the SENSE circuits. At a later time, this causes the CLAMP to be dropped at time C from OPEN to CLAMPED at the cell location. Processor 2 thus is unable to insert its flag pulse onto the output line. Finally, the "acknowledge" return pulse is  
15 received by only processor 1, as processor 2 connection is not enabled.

### **Contention Situation**

If two processors request the same memory line at the "same time," a contention situation occurs. For example, in FIG. 16, if the address lines 45b and 45d are "simultaneously" powered, contention will occur between the processors  
20 coupled via inputs  $I_4$  and  $I_5$  for the memory coupled to output line  $O_9$ . This will cause the memory acquisition to "flag" bits from both the processors coupled to  $I_4$  and  $I_5$ , and thus to drive the output line at the same time. This will produce two units of current in the control line 91, which triggers the "contention" sensor 92. Detection of this event will cause the support electronics to ignore the SENSE  
25 signal and to keep the CLAMP line on current HIGH. This function may also be provided by cryogenic circuitry. No return "acknowledge" pulse is sent, thereby, by its absence, informing the requesting sources of their failure to acquire the requested output line.

### Situation Where Two Processors Have Requested Memory

FIG. 17 depicts the situation wherein processors 1 and 2 have requested the memory at the same time. In that event, the clamp line is not dropped at C, the crossbar cells on that memory line stay available, and no "acknowledge" pulse is returned to the requesters. This silence advises them to retry. If processor 2 requests the memory line at a time between a and C, the electronics can still keep CLAMP high, withhold "acknowledge," and thereby maintain availability to other requesters. This may be done at cryogenic temperature or at room temperature.

### Example of 128 x 128 Switch

FIG. 18 shows an example of a 128 input x 128 output crossbar switch embodying the features of the present invention. In this example, 64 processors 126-126 are coupled to a processor glue chip 127 and 64 memories 128-128 are each coupled to a memory glue chip 131. There are 64 more processors 136-136 coupled to a second processor glue chip 137 and an additional 64 memories 132-132 coupled to a second memory glue chip 133. Connected between these glue chips is a crossbar switch 138 essentially comprising a plurality of interconnecting matrices of cells S1-S16, each of which is a 32 x 32 crossbar matrix. Each of the 64 processors 126-126 is coupled via an input data line 141 to processor glue chip 127, to which each of the 64 processors 126-126 transmits serial bit data. Processor glue chip 127 outputs and receives that data into chips S1, S2, S5, S6 for transactions to and from memories 128-128 by the 64 processors 126-126. It also outputs and receives the data into chips S9, S10, S13, S14 for transactions to and from memories 132-132 by the same 64 processors 126-126. Likewise, chips S3, S4, S7, S8 connect processors 136-136 to memories 128-128 while chips S11, S12, S15, S16 connect processors 136-136 to memories 132-132.

The selection of a memory line by a given processor is accomplished by including a destination memory address in that processor's submitted data word and clocking it via the appropriate input clock line on the proper crossbar chip (i.e., the required input processor and sought-for-output memory line). The destination

address may also be introduced by an external controller and may also be decoded by an external decoder.

The return data from the interrogated memory line is fed into the corresponding memory glue chip as DRIVE, returned in parallel to the crossbar bank and is transferred to only the activated and locked processor line. From there, it continues to the corresponding processor glue chip and on to the originating processor. Clamping is accomplished by controlling a separate line (not shown), which disables access of all the unselected processors to the activated memory line. Contention is separately detected on the memory glue chip.

### 10 **Switch Chip**

FIG. 19 illustrates an embodiment of a switch chip that interconnects 32 input lines to 32 output lines via the previously described matrix of cells. In this example, each processor is assigned and coupled to its own decoder, which decodes the destination address that was requested by that processor and activates the address line of the proper cell in the matrix, as previously described. Such a chip may be replicated to populate the 128 x 128 matrix described in FIG. 17.

Example embodiments of the present invention have been described in accordance with the above advantages. It will be appreciated that these examples are merely illustrative of the invention. Many variations and modifications will be apparent to those skilled in the art.

**WHAT IS CLAIMED IS:**

1. A superconducting crossbar switch, comprising:  
a plurality of input lines;  
a matrix of a plurality of cells, each of the plurality of cells being coupled to  
5 one of the plurality of input lines, wherein each cell includes:  
a first circuit portion containing a first superconducting switch; and  
a second circuit portion, wherein a first signal via the second circuit  
portion triggers the first superconducting switch;  
a plurality of output lines, each of the plurality of output lines coupled to one  
10 of the plurality of cells.
2. The switch of Claim 1, wherein the second circuit portion includes a  
second superconducting switch.
3. The switch of Claim 2, wherein the second circuit portion comprises a  
first leg and a second leg, the second leg including the second superconducting  
15 switch, wherein a signal via the first leg of the second circuit portion triggers the  
first superconducting switch.
4. The switch of Claim 3, wherein each cell of the plurality of cells further  
includes:  
a third circuit portion, wherein a second signal via the third circuit portion  
20 triggers the second superconducting switch.
5. The switch of Claim 1, wherein the first circuit portion includes a first  
resistor in series with the first superconducting switch.
6. The switch of Claim 5, wherein the first superconducting switch is in  
series with a coupling to a first ground connection.
- 25 7. The switch of Claim 6, wherein the first circuit portion includes a second  
resistor coupled in series with the first resistor.
8. The switch of Claim 7, wherein the second resistor is in series with a  
coupling to one from the plurality of output lines.
9. The switch of Claim 4, wherein the first leg of the second circuit portion  
30 includes an inductor.

10. The switch of Claim 4, wherein the second leg of the second circuit portion is in series with a coupling to a second ground connection.
11. The switch of Claim 1, wherein the first signal is produced via a first current in the second circuit portion.
- 5 12. The switch of Claim 4, wherein the second signal is produced via a second current in the third circuit portion.
13. The switch of Claim 1, wherein the first signal is an optical signal.
14. The switch of Claim 4, wherein the second signal is an optical signal.
15. The switch of Claim 1, wherein the matrix of a plurality of cells  
10 includes 32 rows and 32 columns of cells, and wherein the plurality of input lines includes 32 input lines and the plurality of output lines includes 32 output lines.
16. The switch of Claim 1, further comprising a plurality of summing devices, wherein each of the plurality of output lines is coupled in series with one from the plurality of summing devices.
- 15 17. The switch of Claim 16, wherein each of the plurality of summing devices includes a third superconducting switch.
18. The switch of Claim 16, wherein each of the plurality of summing devices includes a first summing device circuit portion and a second summing device circuit portion.
- 20 19. The switch of Claim 18, wherein the second summing device circuit portion includes a third superconducting device, and wherein a third signal via the first summing device circuit portion triggers the third superconducting device.
20. The switch of Claim 19, wherein each of the plurality of summing devices includes a summing device output.
- 25 21. The switch of Claim 20, wherein the triggering of the third superconducting device produces an output signal via the summing device output.
22. The switch of Claim 20, wherein the summing device output is coupled to a memory device.
23. The switch of Claim 22, wherein each of the plurality of summing  
30 devices includes a summing device input.

24. The switch of Claim 23, wherein the summing device input is coupled to the first summing device circuit.

25. The switch of Claim 24, wherein the first summing device circuit includes at least a fourth superconducting device.

5           26. The switch of Claim 25, wherein each of the at least a fourth superconducting device is coupled in series to a third ground connection.

27. The switch of Claim 25, wherein the at least a fourth superconducting device includes the fourth superconducting device and a fifth superconducting device.

10           28. The switch of Claim 26, wherein the summing device input is coupled to the memory device.

29. The switch of Claim 26, wherein each of the at least a fourth superconducting switch are coupled in series between the coupling to the third ground connection and a point at which the summing device input is coupled to the first summing device circuit.

15           30. The switch of Claim 16, wherein each of the plurality of output lines is capable of bidirectionally transmitting a signal.

31. The switch of Claim 22, further comprising a plurality of input drivers coupled in series with each of the plurality of input lines.

20           32. The switch of Claim 23, wherein each of the plurality of input drivers includes a sixth superconducting switch.

33. The switch of Claim 31, wherein each of the plurality of input drivers includes a first input driver circuit portion and a second input driver circuit portion.

25           34. The switch of Claim 33, wherein the second input driver circuit portion includes a sixth superconducting device, and wherein a fourth signal via the first input driver circuit portion triggers the sixth superconducting device.

35. The switch of Claim 34, wherein the input driver includes an input driver output.

30           36. The switch of Claim 35, wherein the triggering of the sixth superconducting device produces an output signal via the input driver output.

37. The switch of Claim 35, wherein the input driver output is coupled to a processor.

38. The switch of Claim 37, wherein each of the plurality of input drivers includes an input driver input.

5           39. The switch of Claim 38, wherein the input driver input is coupled to the first input driver circuit.

40. The switch of Claim 39, wherein the first input driver circuit includes at least a seventh superconducting device.

10           41. The switch of Claim 40, wherein each of the at least a seventh superconducting device is coupled in series to a fourth ground connection.

42. The switch of Claim 41, wherein the at least a seventh superconducting device includes the seventh superconducting device and an eighth superconducting device.

15           43. The switch of Claim 42, wherein the input driver input is coupled to the processor.

44. The switch of Claim 41, wherein each of the at least a seventh superconducting switch are coupled in series between the coupling to the fourth ground connection and a point at which the input driver input is coupled to the first input driver circuit.

20           45. The switch of Claim 16, wherein each of the plurality of summing devices includes an amplifier.

46. The switch of Claim 18, wherein each of the plurality of summing devices includes a third summing device circuit portion.

25           47. The switch of Claim 46, wherein the third summing device circuit portion includes a ninth superconducting device, and wherein a fifth signal via the first summing device circuit portion triggers the ninth superconducting device.

48. The switch of Claim 47, wherein each of the plurality of summing devices includes a summing device contention output.

30           49. The switch of Claim 48, wherein the triggering of the ninth superconducting device produces an output signal via the summing device contention output.

50. A superconducting crossbar switch, comprising:  
a matrix of a plurality of cells, wherein each cell includes:  
a first circuit portion containing a first superconducting switch; and  
a second circuit portion, wherein a first signal via the second circuit  
5 portion triggers the first superconducting switch.
51. A superconducting crossbar switch, comprising:  
a matrix of a plurality of cells, wherein each cell includes:  
a first circuit portion containing a first superconducting switch; and  
a second circuit portion, wherein a first signal via the second circuit  
10 portion triggers the first superconducting switch;  
first and second processor glue chips coupled to the matrix of a plurality of  
cells;  
first and second memory glue chips coupled to the matrix of a plurality of  
cells;  
15 a first plurality of processors coupled to the first glue chip via a first input  
data line;  
a second plurality of processors coupled to the second glue chip;  
a first plurality of memory devices coupled to the first memory glue chip;  
and  
20 a second plurality of memory devices coupled to the second memory glue  
chip.
52. A crossbar switch for connecting a plurality of inputs with a plurality of  
outputs, comprising:  
at least one switching cell, comprising:  
25 at least one input device;  
at least one output device; and  
at least one connecting switch for bi-directionally transmitting data  
between the at least one input device and the at least one output device, each of the  
at least one connecting switch comprising:  
30 a first superconductive switch; and

a first control switch to control operation of the connecting switch.

53. The crossbar switch of Claim 52, wherein the first superconductive switch has zero resistance and negligible crosstalk.

5 54. The crossbar switch of Claim 52, wherein the connecting switch allows connection among a plurality of functional units.

55. The crossbar switch of Claim 52, further comprising:  
a second superconductive switch; and  
a second control switch for retaining and releasing operation of the first  
10 superconductive switch.

56. The crossbar switch of Claim 52, further comprising:  
a switching cell, comprising:  
a plurality of cells arranged in a matrix with the at least one input  
device coupled to the plurality of cells, and the at least one output device coupled  
15 to the plurality of cells.

57. The crossbar switch of Claim 56, wherein the switching cell further  
comprises:  
a feedback mechanism.

58. The crossbar switch of Claim 57, wherein the plurality of cells further  
20 comprise:  
retaining and releasing devices connected to the at least one output device to  
simultaneously retain a selected cell of the plurality of cells and disable the  
remaining cells of the plurality of cells, whereby a subsequent transmission to a  
disabled cell is inoperative until the selected cell is released.

25 59. The crossbar switch of Claim 52, wherein the at least one output device  
comprises:  
a summing device for summing output currents.

60. The crossbar switch of Claim 59, wherein the summing device  
comprises at least one selected from:  
30 a summing amplifier; and  
an additional superconductive switch.

61. The crossbar switch of Claim 52, further comprising:  
a sensing apparatus coupled to the at least one connecting switch for  
detecting simultaneous pulses to cells, generating an indication of conflict from the  
simultaneous pulses, and resolving the conflict.
- 5           62. A method for transmitting information via a superconducting crossbar  
switch, the switch including a plurality of cells, each of the cells including a first  
superconducting switch in a first circuit portion, a coupling to an input line, a  
coupling to an output line, and a second circuit portion, the method comprising:  
transmitting a control signal to the second circuit portion;  
10           the second circuit portion producing a first switching signal in response to  
receiving the control signal;  
the first switching signal triggering the first superconducting switch; and  
the triggering of the first superconducting switch allowing transmission of  
an output signal via the output line.
- 15           63. The method of Claim 62, wherein the switching signal comprises an  
electrical signal.
64. The method of Claim 62, wherein the switching signal comprises an  
optical signal.
65. The method of Claim 62, wherein the second circuit portion includes a  
20           second superconducting switch, and wherein each of the cells includes a third  
circuit portion, the method further comprising:  
transmitting a clamp line signal to the third circuit portion;  
the third circuit portion producing a second switching signal in response to  
receiving the clamp line signal;  
25           the second switching signal triggering the second superconducting switch;  
and  
the triggering of the second superconducting switch allowing the second  
circuit portion to produce the first switching signal.
66. The method of Claim 62, further comprising:  
30           transmitting an input to the superconducting crossbar switch; and  
the transmission input producing the output signal via the output line.

67. The method of Claim 66, wherein a plurality of output lines are associated with the plurality of cells, and wherein transmitting an input to the superconducting crossbar switch includes:

5 selecting one from the plurality of output lines for which data is to be transmitted; and

identifying at least one from the plurality of cells corresponding to the selected one from the plurality of output lines.

68. The method of Claim 66, wherein each output line for the plurality of cells is coupled to a summing device, the summing device including a first circuit portion and a second circuit portion, wherein the second circuit portion includes a third superconducting switch, the method further comprising:

10 transmitting the output signal via the output line to the first circuit portion of the summing device;

15 the first circuit portion of the summing device producing a summing device control line signal;

the control line signal triggering the third superconducting switch; and

the triggering of the third superconducting switch producing a transmission to a memory input.

69. The method of Claim 68, wherein each input line for the plurality of cells is coupled to an input driver, the input driver including a first circuit portion and a second circuit portion, wherein the input driver second circuit portion includes a fourth superconducting switch, and wherein the input driver first circuit portion includes at least a fifth superconducting switch, the method further comprising:

25 the input driver first circuit portion receiving a signal; and

the received input driver first circuit portion signal driving each of the at least a fifth superconducting switch into a voltage state.

70. The method of Claim 68, wherein the summing device first circuit portion includes at least a sixth superconducting switch, the method further comprising:

30

transmitting an inverted amplified signal corresponding to the memory input to the summing device first circuit portion;

the inverted amplified signal driving each of the at least a sixth superconducting switch into a voltage state; and

5 transmitting the inverted amplified signal via at least one of the plurality of cells to the input driver first circuit portion.

71. The method of Claim 70, wherein the inverted amplified signal received by the input driver first circuit portion comprises an acknowledge signal.

72. A method for resolving contention in a crossbar switch having a  
10 plurality of inputs, at least one output, a plurality of switching devices, and at least one contention sensor, wherein each of the switching devices is coupled to at least one of the plurality of inputs, and wherein each of the at least one contention sensor is coupled to one of the at least one output, the method comprising:

a first one of the plurality of inputs transmitting a first input signal to a first  
15 one of the plurality of switching devices;

a second one of the plurality of inputs, concurrently with transmission of the first input signal, transmitting a second input signal to a second one of the plurality of switching devices;

20 transmitting a combined switch output from the first and the second switching devices to one of the at least one output;

the contention sensor sensing the combined switch output; and

upon sensing the combined switch output, the contention sensor preventing generation of an output signal via the one of the at least one output.

73. The method of Claim 72, wherein preventing generation of an output  
25 signal via the one of the at least one output further includes:

preventing generation of an acknowledgment signal to each of the first one and the second one of the plurality of inputs.

74. The method of Claim 72, wherein each of the plurality of switching devices comprises a switching device superconducting switch.

30 75. The method of Claim 72, wherein the contention sensor comprises a contention sensor superconducting device.

76. The method of Claim 73, further comprising:  
determining absence of an acknowledgment signal;  
upon determining absence of an acknowledgment signal, the first one of the  
plurality of inputs retransmitting the first input signal, and the second one of the  
5 plurality of inputs retransmitting the second input signal.

77. A method for providing a broadcast signal via a crossbar switch having  
a plurality of inputs, at least one output, and a plurality of switching devices,  
wherein each of the switching devices is coupled to at least one of the plurality of  
inputs, the method comprising:  
10 transmitting a control signal to each of the plurality of switching devices  
from which a switch output is to be transmitted;  
transmitting an input signal to at least one of the plurality of switching  
devices; and  
for each of the plurality of switching devices receiving the control signal and  
15 receiving the input signal, the switching device generating an output signal to any  
of the at least one output.

78. The method of Claim 77, wherein each of the plurality of switching  
devices comprises a superconducting switch.

79. The method of Claim 78, wherein the switching device preventing  
20 generation of an output signal to any of the at least one output includes:  
generating a current in the switching device; and  
the generated current causing the superconducting switch to conduct.

80. A method for transmitting a signal via a crossbar switch having a  
plurality of inputs, at least one output, and a plurality of switching devices,  
25 wherein each of the switching devices is coupled to at least one of the plurality of  
inputs, the method comprising:  
transmitting an input signal to each of the plurality of switching devices;  
transmitting a control signal to each of the at least one of the plurality of  
switching devices from which an output is to be generated; and

for each of the plurality of switching devices receiving the control signal and receiving the input signal, the switching device generating an output signal to one of the at least one output.

5 81. The method of Claim 80, wherein, each of the plurality of switching devices receiving the input signal and receiving no control signal is prevented from generating the output signal to any of the at least one output.

82. The method of Claim 81, wherein each of the plurality of switching devices comprises a superconducting switch.

10 83. The method of Claim 82, wherein, the superconducting switch in the plurality of switching devices is coupled to ground, and wherein each of the plurality of switching devices preventing generation of the output signal to any of the at least one output includes:

the input signal generating a current in the switching device; and  
conducting the generated current via the superconducting switch to the  
15 ground.

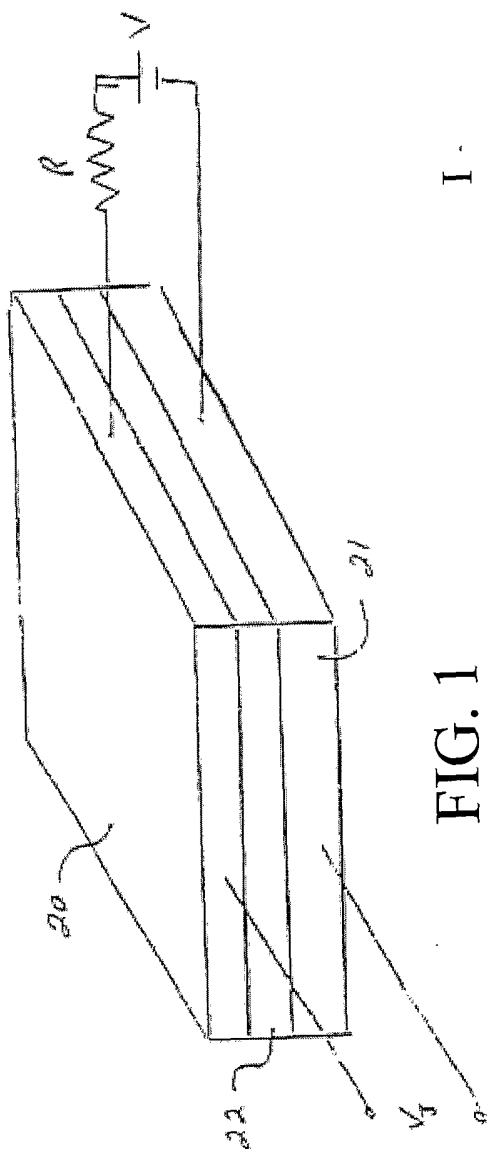


FIG. 1  
(PRIOR ART)

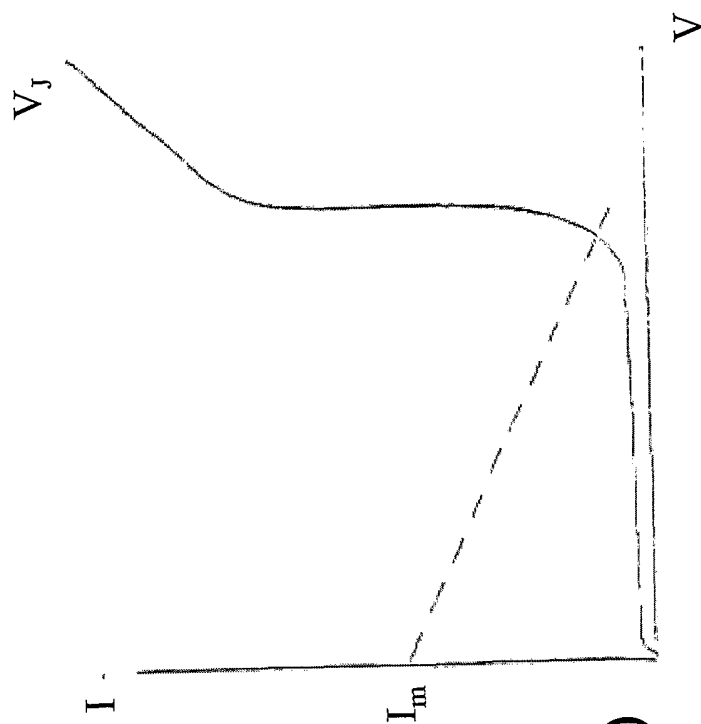


FIG. 2  
(PRIOR ART)

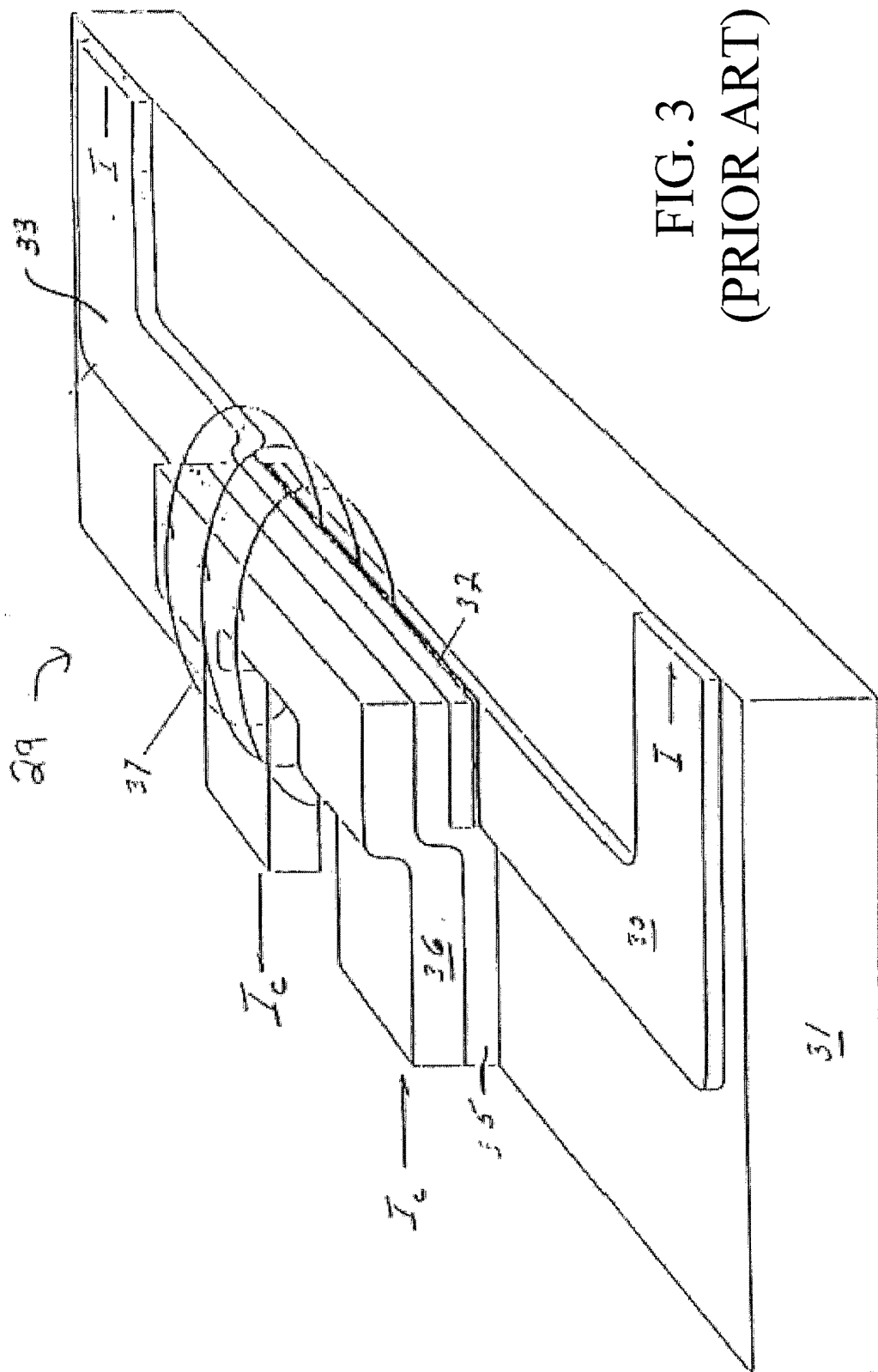


FIG. 3  
(PRIOR ART)

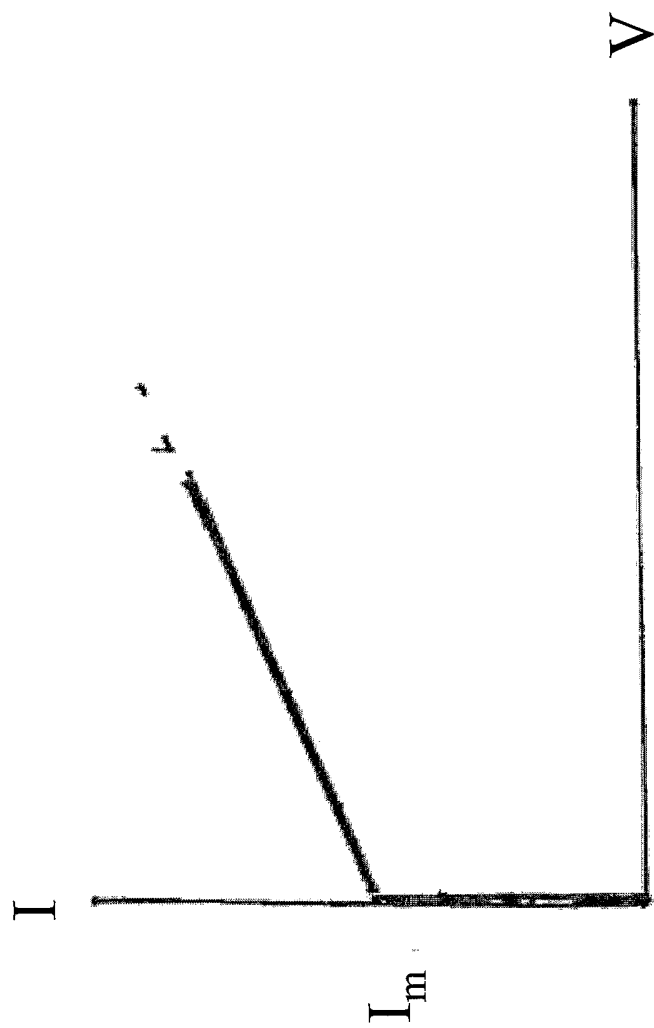


FIG. 4  
(PRIOR ART)

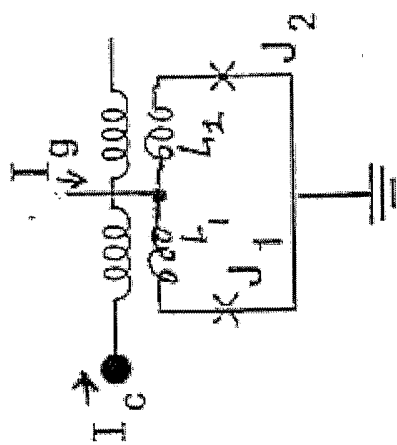


FIG. 5  
(PRIOR ART)

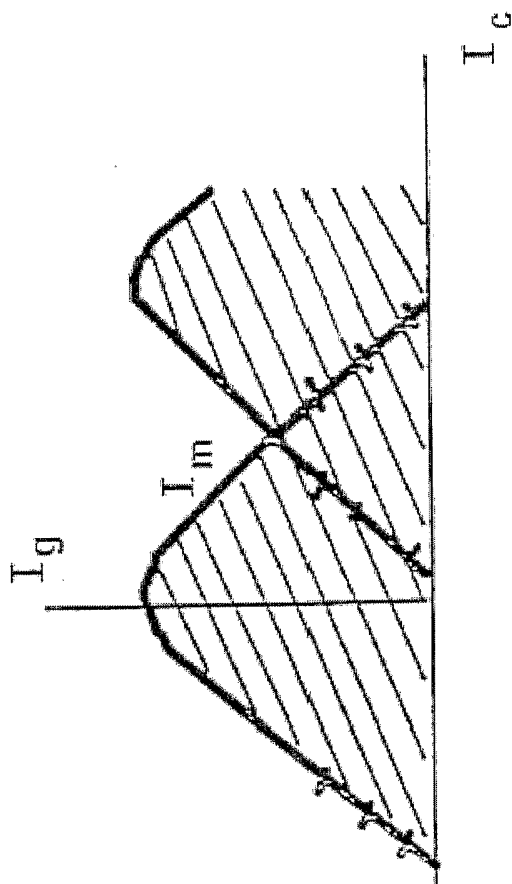


FIG. 6  
(PRIOR ART)

FIG. 7

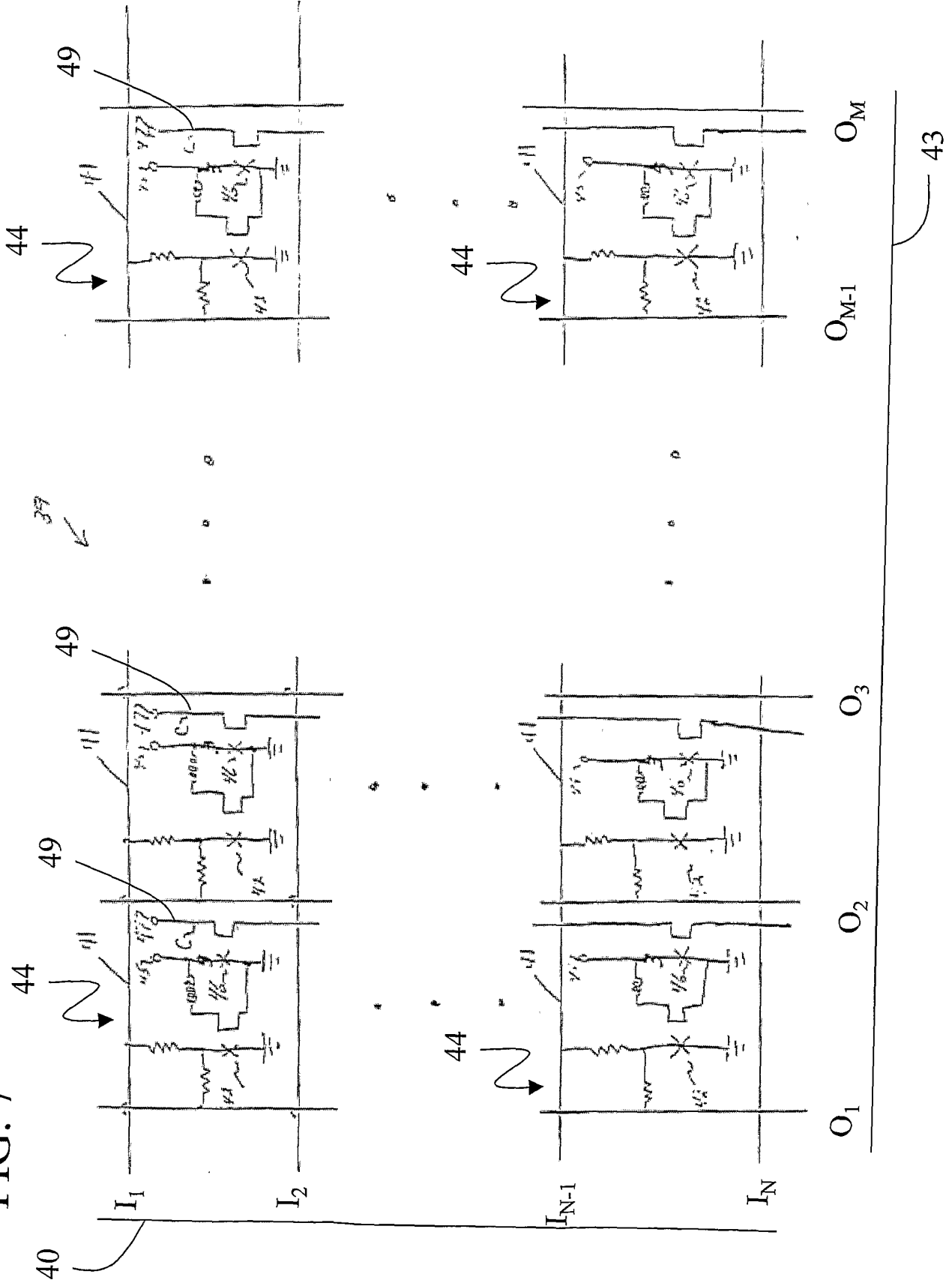


FIG. 8

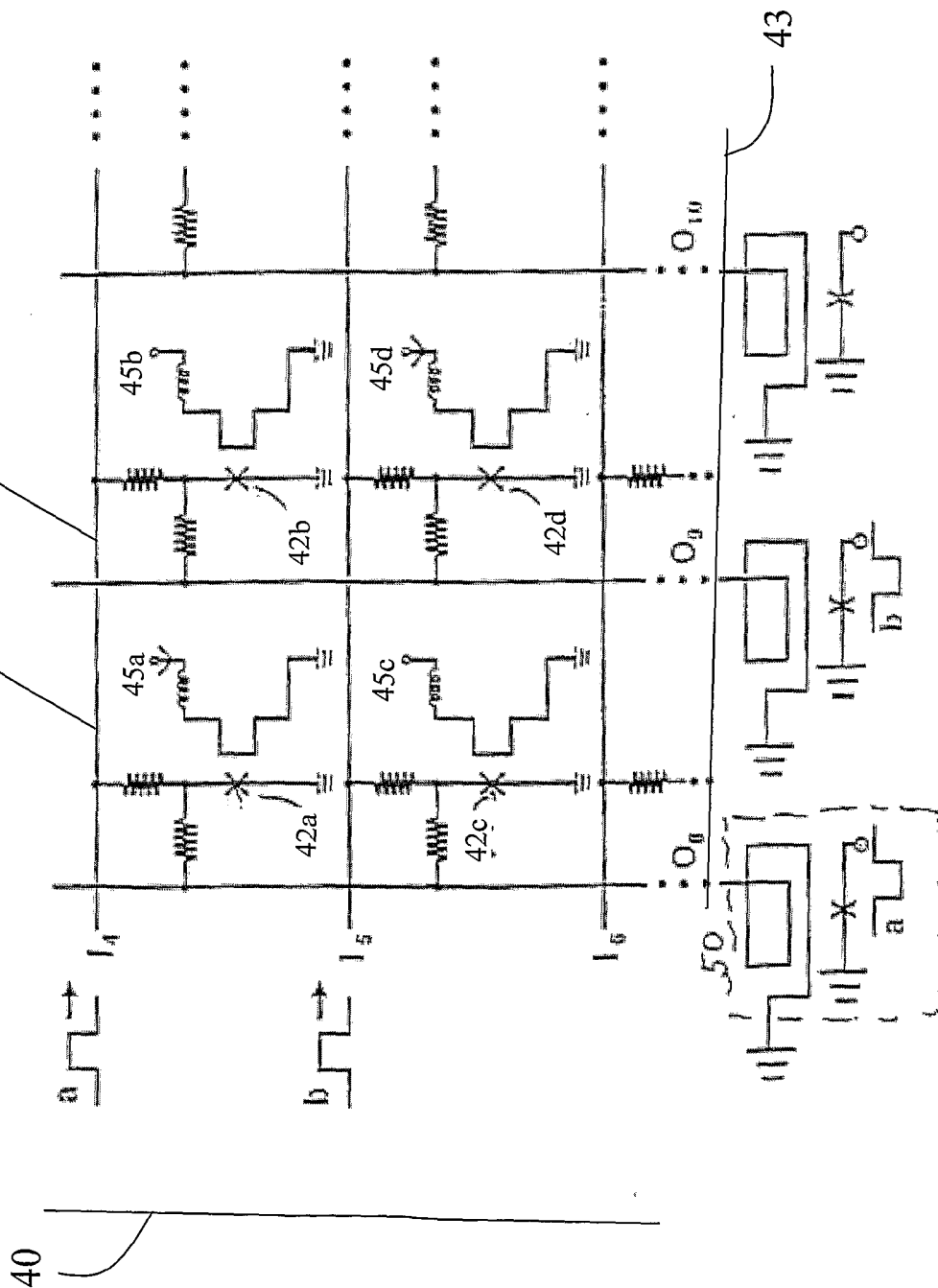
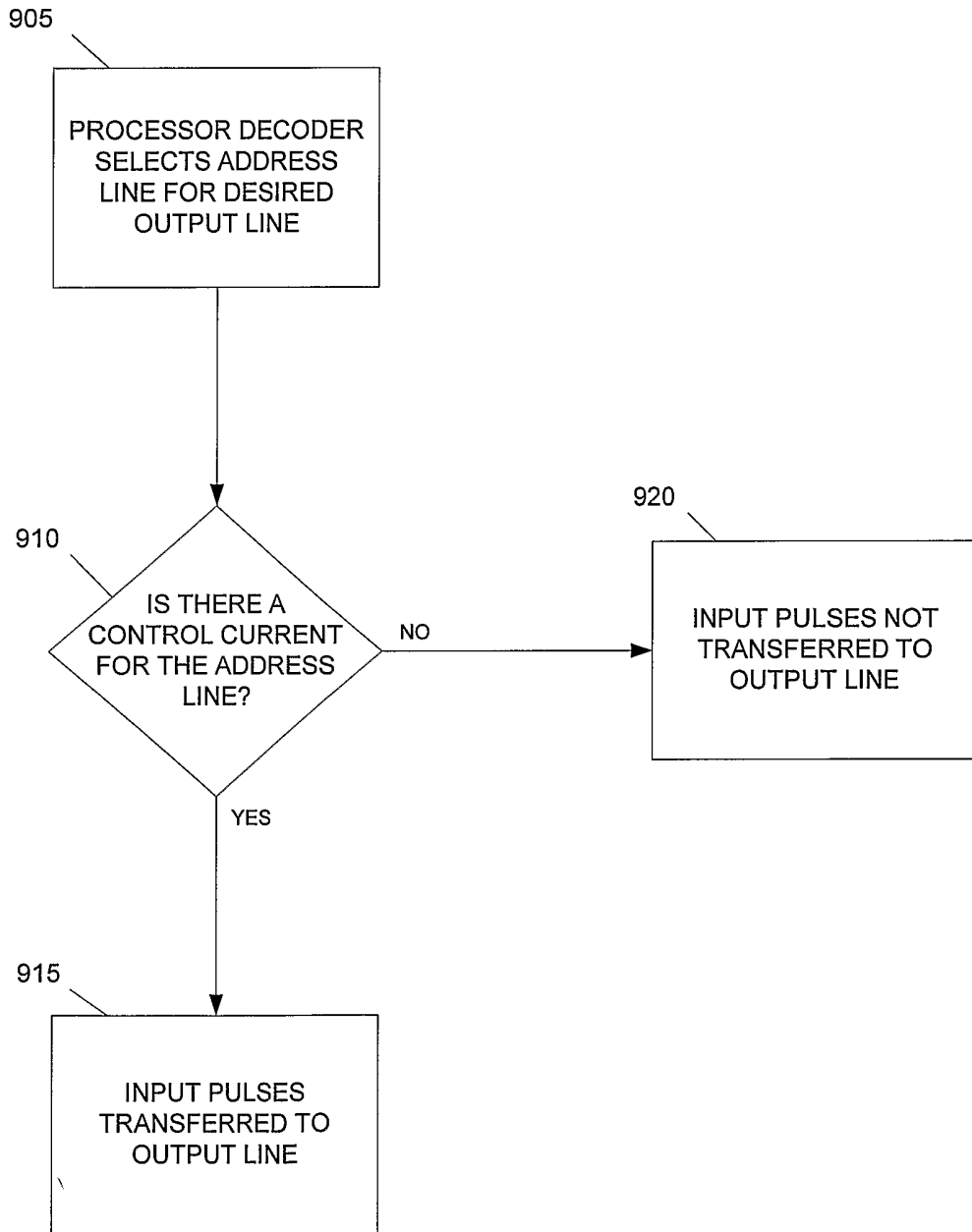


FIG. 9



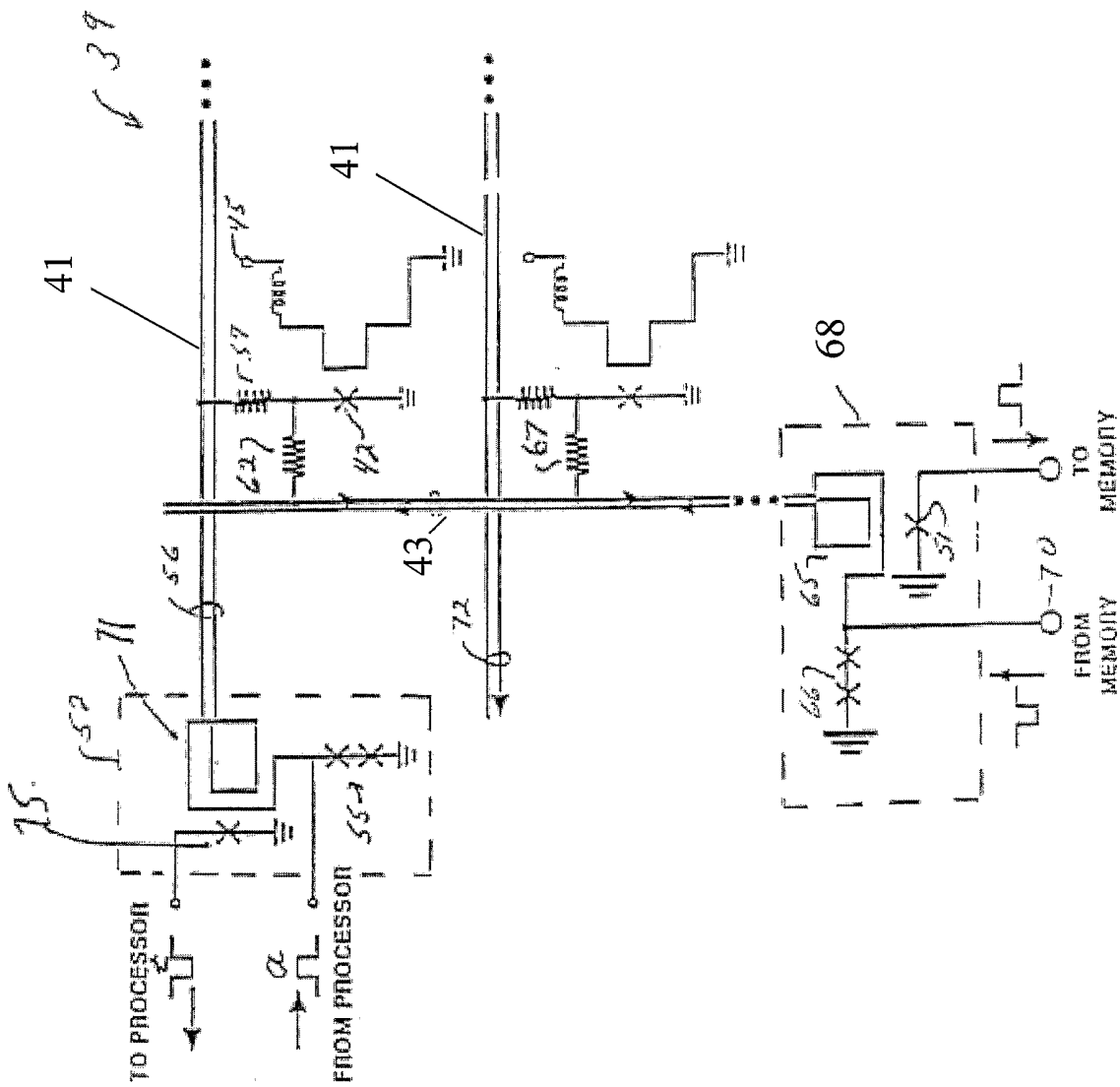


FIG. 10

FIG. 11

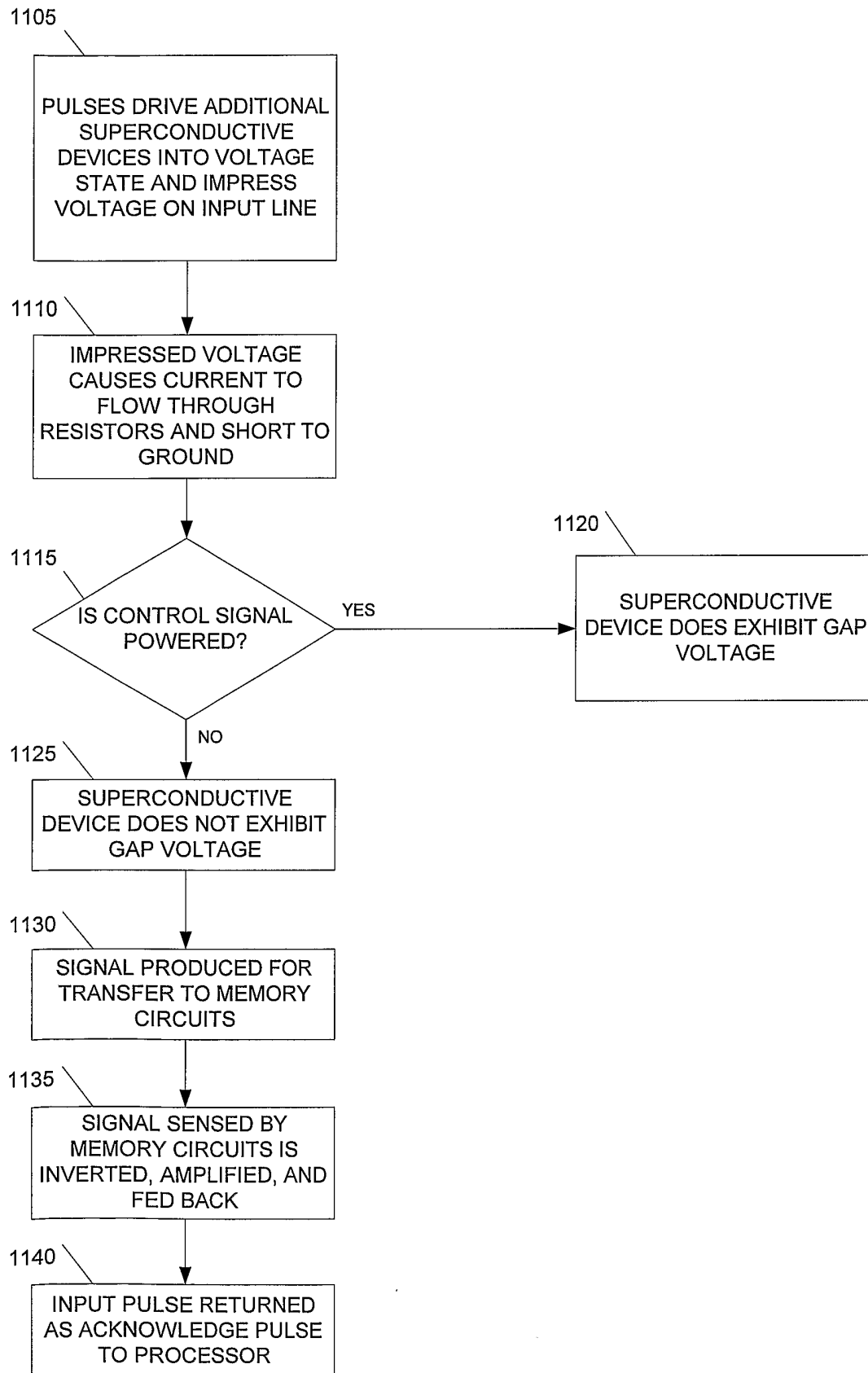


FIG. 12

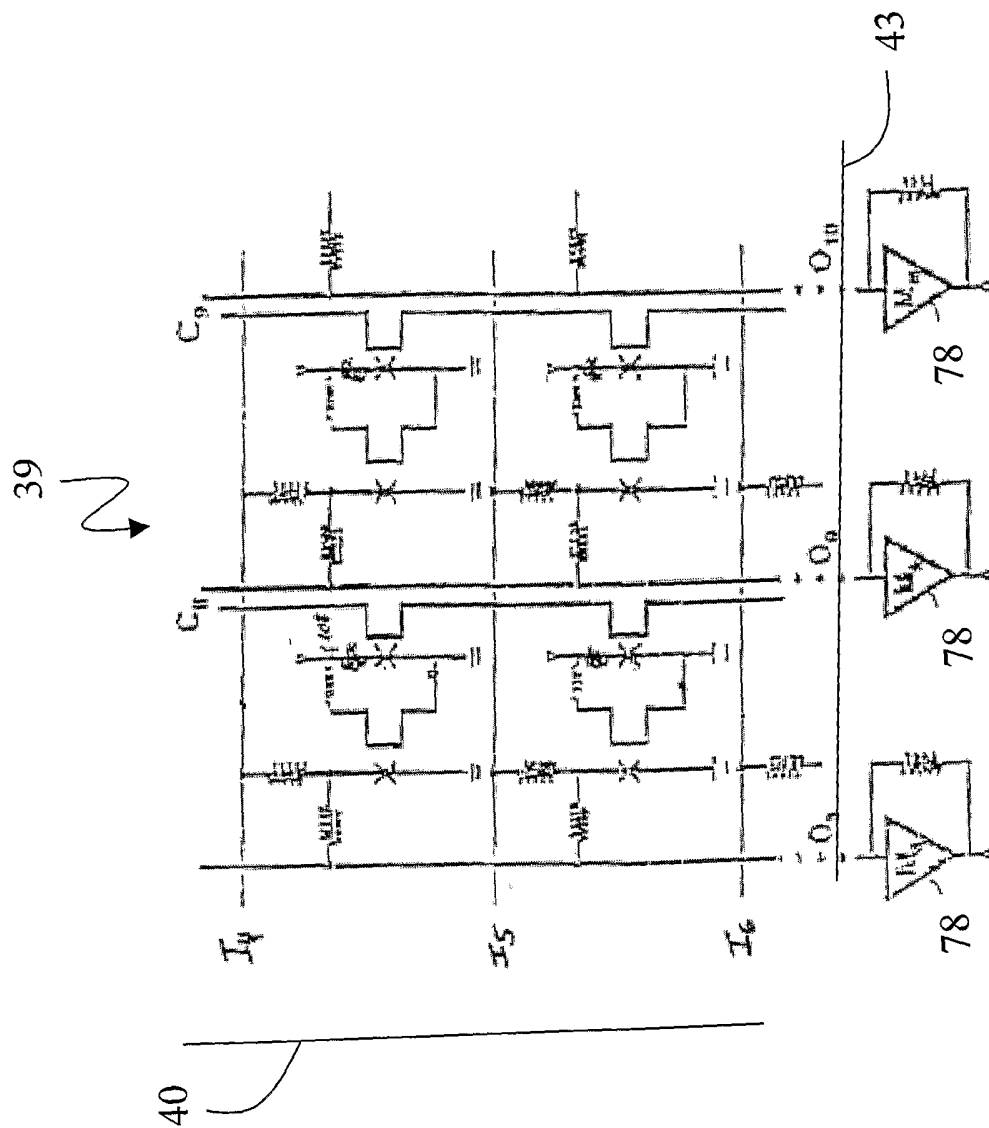


FIG. 13

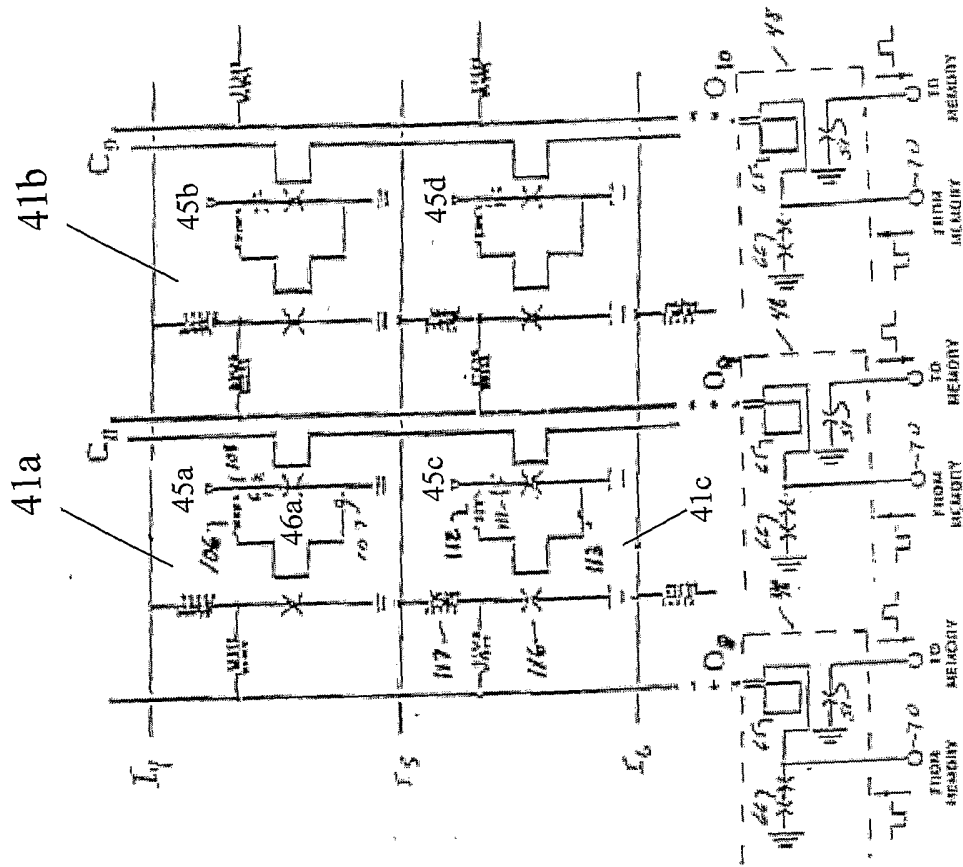


FIG. 14

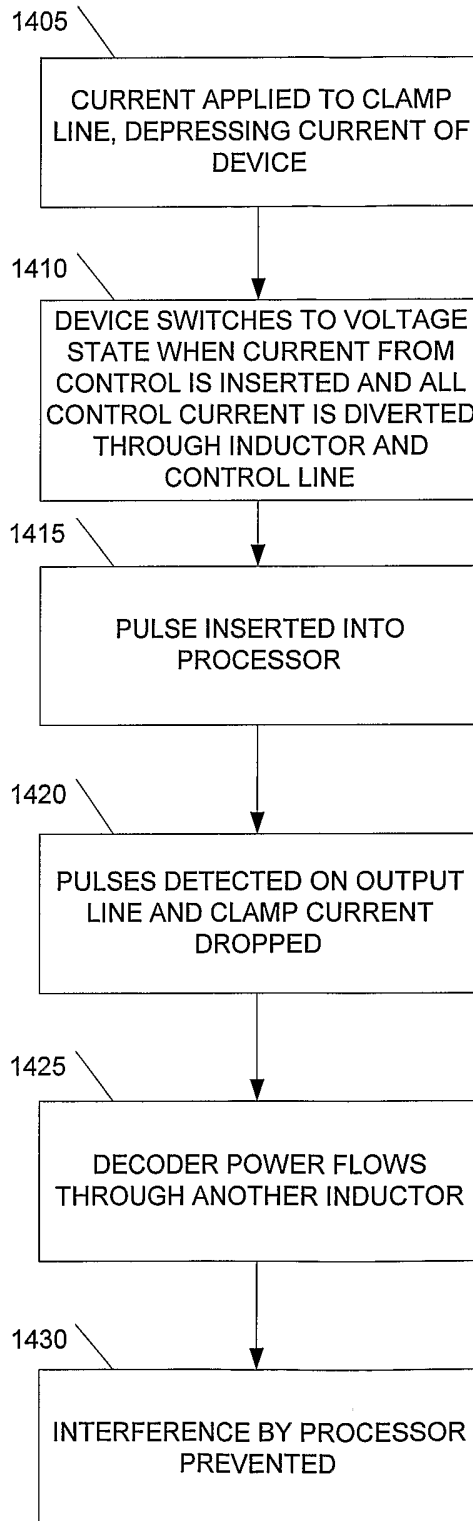


FIG. 15

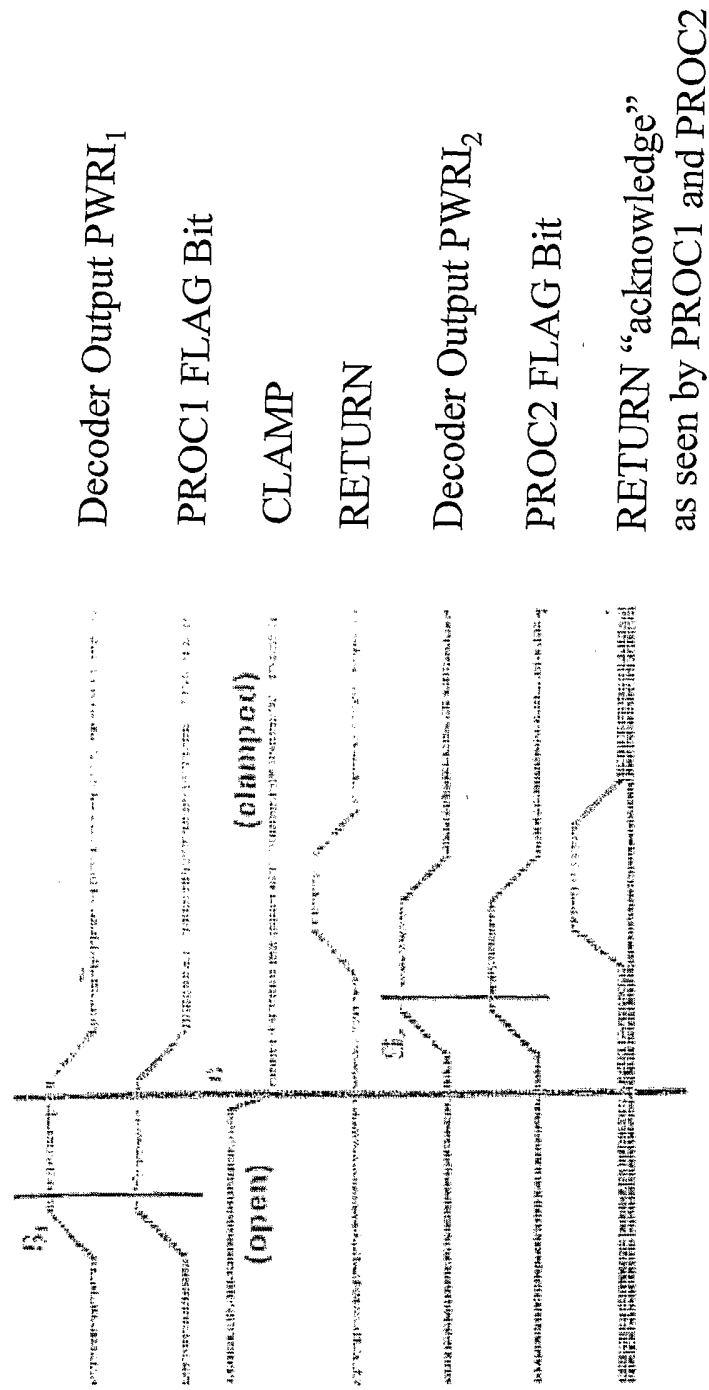


FIG. 16

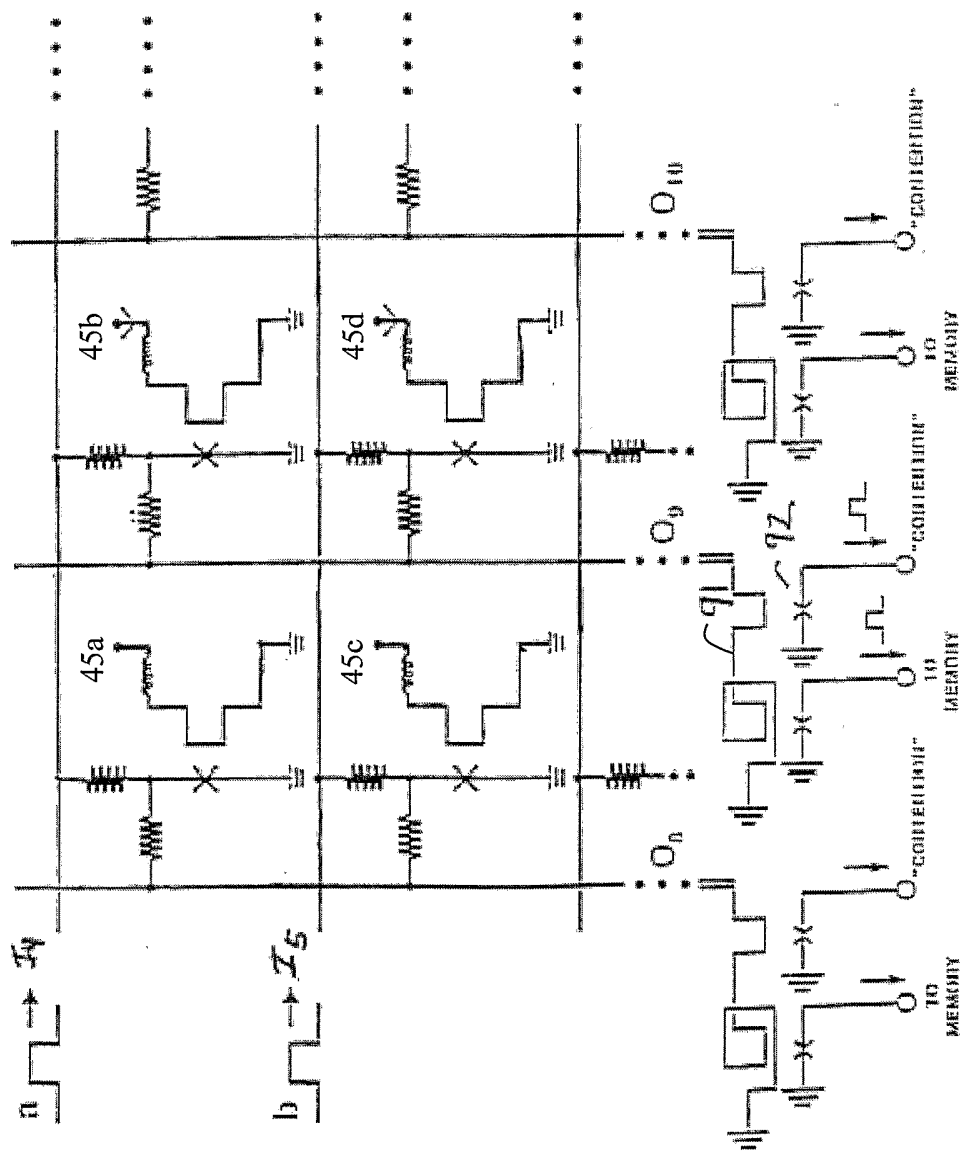


FIG. 17

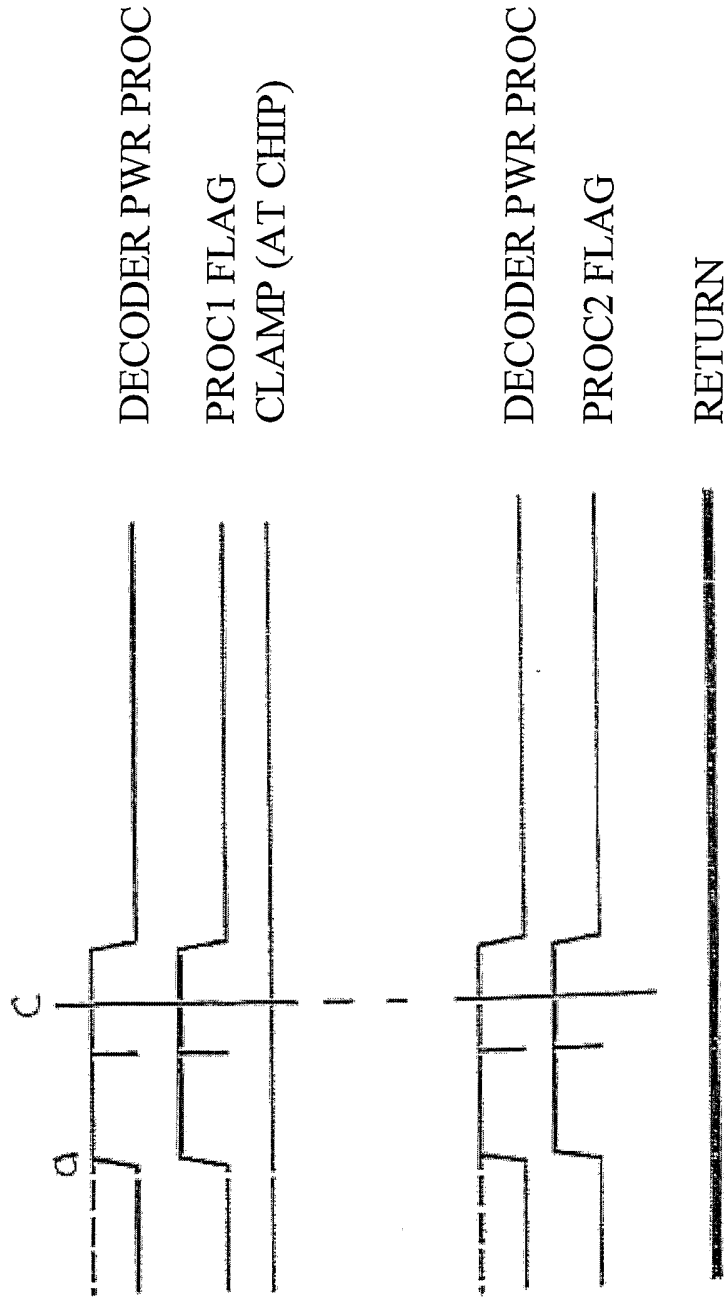


FIG. 18

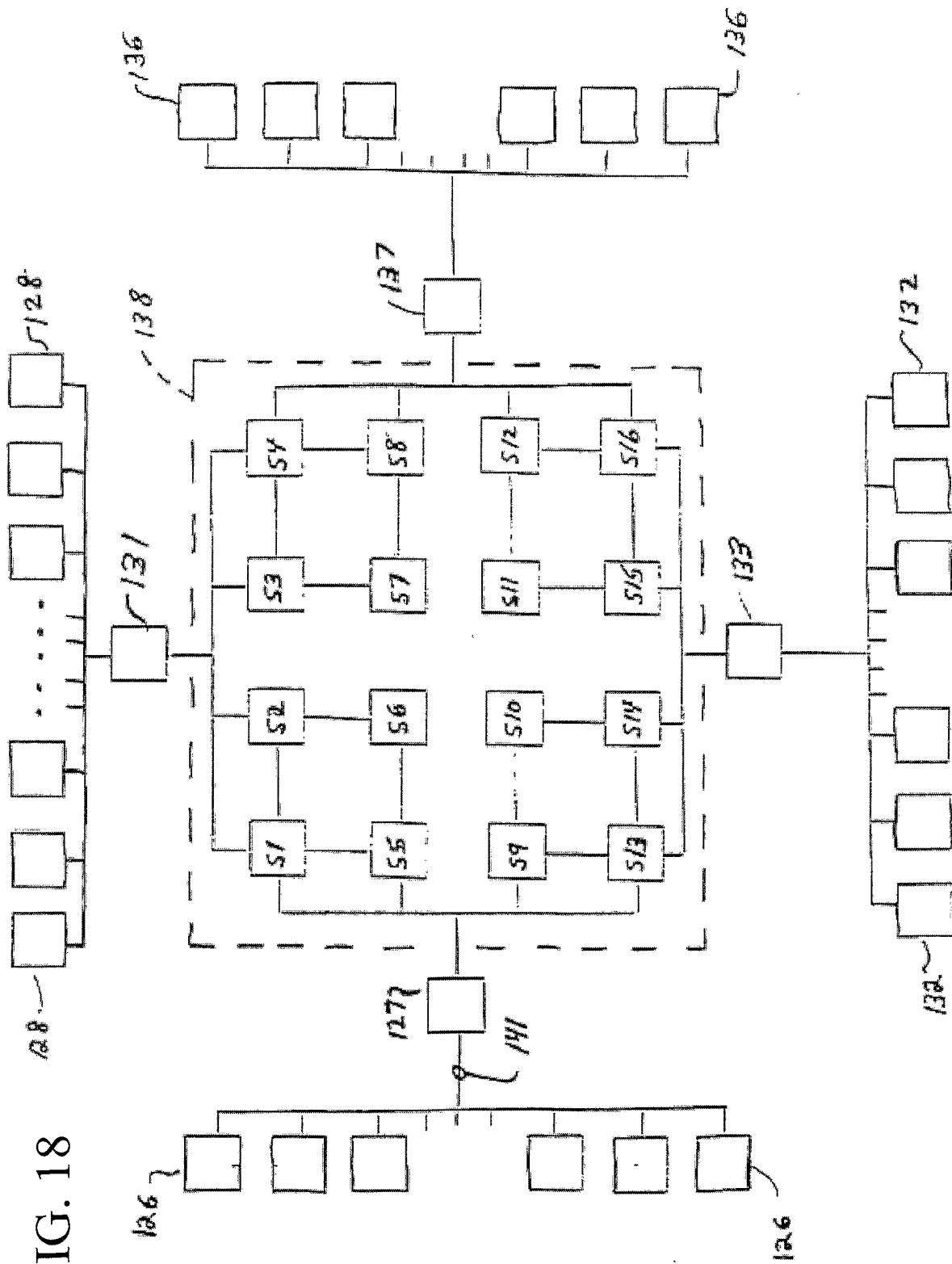


FIG. 19

