A method and apparatus are provided for using a strip socket in testing or burn-in of semiconductor devices in a strip. In one example of the method, processing of semiconductor devices involves assembling the semiconductor devices into a strip, isolating a portion of each of the semiconductor devices of the strip, and performing operations on the strip using a strip socket, wherein the strip socket is designed to make electrical contact substantially simultaneously with each semiconductor device in the strip.
TESTING AND BURN-IN USING A STRIP SOCKET

FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices. More particularly, the present invention relates to parallel testing and burn-in of semiconductor devices in a strip socket.

BACKGROUND OF THE INVENTION

[0002] A semiconductor wafer is a thin, round slice of semiconductor material, typically silicon, on which microchips are made. Manufacturers process silicon into large cylindrical masses of metal, slice the masses into wafers and then form transistors and other elements on the wafer before cutting the wafers into smaller semiconductor chips. A higher density of these semiconductor chips on the wafers is desirable for cost savings and productivity improvement. Chip manufacturers have made steady improvements in shrinking die size (i.e., chip size) and expanding wafer size. Manufacturers have also given more rows and columns to the lead frame matrix in assembly processes.

[0003] As is known, a number of semiconductor chips will fail after a relatively short period of operation. Such a failure is termed in the field as infant mortality. Semiconductor chips are subjected to heat and electric signals to cause infant mortality failures. The remaining semiconductor chips will exhibit improved reliability. Semiconductor devices must undergo a process commonly known as final testing. Final testing is the final process of an electrical testing of a semiconductor device. The final process involves using an automatic test handler, test contact and tester. The semiconductor chips are inverted to strip out lead frames. This provides easier handling and handling of multiple semiconductor chips with a single touch. However, the strip format or strip base package cannot perform other testing, such as burn-in or signal cycling (e.g., read/write endurance testing).

[0004] FIG. 1A (Prior Art) is a conventional test/burn-in socket for a singulated semiconductor package. A singulated package is a unit semiconductor device which was assembled into a strip leadframe and then singulated out of lead frame into a single semiconductor chip. The test/burn-in socket includes a cover 102 and a base 104. The socket can also be used without a cover 102. A conventional test typically involves a test method used in conjunction with an automated handler which handles the semiconductor package. The test/burn-in socket typically includes and singulated. Appropriate electronic signals are coupled to the semiconductor device to determine whether it is operational with predetermined specifications.

[0005] FIG. 1B (Prior Art) is a cross-sectional view of the conventional test/burn-in socket of FIG. 1A (Prior Art). The socket contains a socket body designed to accommodate a singulated semiconductor package 108. Electrical contacts of the package 108 are in electrical contact with corresponding electrical contacts of the socket body. The package 108 is under test in the test/burn-in socket.

[0006] In this singulated package 108, the lead 107 is formed into an appropriate shape. The base 104 of the socket is secured to the printed circuit board (PCB) 106 with contact pins 110. Numerous contact pins 110 contact the lead 107 or terminal of the package 108 for establishing an electrical connection between the PCB 106 and the package 108. Examples of a contact pin include a stamped pin 112 and a pogo pin 114.

[0007] FIG. 1C (Prior Art) is a conventional test/burn-in board, including multiple test or burn-in sockets. The test/burn-in board includes multiple sockets mounted on a PCB 106. A card edge connector 116 is integrally formed with the PCB 106. The card edge connector 116 is integrally for connecting the test/burn-in board to a test/burn-in system.

[0008] FIG. 7A (Prior Art) is a flowchart of an exemplary conventional testing/burn-in process. The process flow begins in operation 702 which includes assembly of semiconductor chips into packages. Assembly includes die attachment, wire bonding, plating and molding. The process flow proceeds to the operation 704 which includes forming the lead frame and singulation of the packages. Next, test/burn-in of singulated sockets is performed in operation 706. In the operation 708, final testing is performed. Then, in operation 710, the devices which pass final testing are packed for shipping. As shown in FIG. 7A, only the operations 702 and 704 involve handling the packages as lead frames or strips. Operations 706, 708 and 710 involve handling the devices as singulated units.

[0009] Unfortunately, a conventional test/burn-in socket for a singulated package has inherent physical limitations that cause problems in a testing/burn-in process. The method of testing and burn-in of packages 108 is time consuming because numerous packages 108 must be individually loaded and unloaded. The method of testing and burn-in can also potentially create contact terminal defects, such as bending and causing coplanarity problems to the leads 107.

SUMMARY OF THE INVENTION

[0010] What is needed is a method of testing packages that overcomes the inherent limitations of a conventional test/burn-in socket. Broadly speaking, the present invention fills these needs by providing a method of using a strip socket for testing and burn-in of strip base packages. It should be appreciated that the present invention can be implemented in numerous ways, including as a method, a process, an apparatus, a system or a device. Inventive embodiments of the present invention are summarized below.

[0011] In one embodiment, a method of processing semiconductor devices using a strip socket is provided. The method includes the steps of assembling the semiconductor devices into a strip, isolating a portion of each of the semiconductor devices in the strip, and performing operations on the semiconductor devices in the strip using a strip socket. The strip socket is designed to make electrical contact substantially simultaneously with each semiconductor device in the strip.

[0012] In another embodiment, a strip socket is provided. The strip socket is designed to make electrical contact with semiconductors devices in a strip. The electrical contact is made substantially simultaneously with each of the semiconductor devices in the strip. A user can load each of semiconductor devices of the strip into the strip socket at substantially the same time. A user can also unload each of semiconductor devices of the strip from the strip socket at substantially the same time.

[0013] In yet another embodiment, a strip of semiconductor devices is provided. The strip of semiconductor devices is designed to make electrical contact with a strip socket,
wherein electrical contact of each of the semiconductors devices is designed to be made at substantially a same time with the strip socket.

0014 The invention encompasses other embodiments as set forth above and with other features and alternatives.

BRIEF DESCRIPTION OF THE DRAWINGS

0015 The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings. To facilitate this description, like reference numerals designate like structural elements.

0016 FIG. 1A (Prior Art) is a conventional test/burn-in socket for a singulated semiconductor package;

0017 FIG. 1B (Prior Art) is a cross-sectional view of the conventional test/burn-in socket of FIG. 1A (Prior Art);

0018 FIG. 1C (Prior Art) is a conventional test/burn-in board, including multiple test or burn-in sockets;

0019 FIG. 2A is a schematic diagram showing lead/terminal isolation for a leaded package before a lead length cut, in accordance with an embodiment of the present invention;

0020 FIG. 2B is a schematic diagram showing lead/terminal isolation for a leaded package after the lead length cut, in accordance with an embodiment of the present invention;

0021 FIG. 3A is a schematic diagram of terminal isolation before isolation for a leadless package, in accordance with an embodiment of the present invention;

0022 FIG. 3B is a schematic diagram of terminal isolation after isolation for a leadless package, in accordance with an embodiment of the present invention;

0023 FIG. 4 is a diagram of a strip of ball grid arrays (BGA) or chip scale packages (CSP), in accordance with an embodiment of the present invention;

0024 FIG. 5 is a diagram of strip sockets on a testing/burn-in board, in accordance with an embodiment of the present invention;

0025 FIG. 6A is a diagram of a testing/burn-in strip socket of a leaded package, in accordance with an embodiment of the present invention;

0026 FIG. 6B is a diagram of a testing/burn-in strip socket of a leadless package, in accordance with an embodiment of the present invention;

0027 FIG. 7A (Prior Art) is a flowchart of a process involving conventional testing/burn-in; and

0028 FIG. 7B is flowchart of a process involving testing/burn-in utilizing a strip socket, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

0029 An invention for a method of using a strip socket for testing and burn-in of strip base packages is disclosed. Numerous specific details are set forth to provide a thorough understanding of the present invention. However, it will be understood, to one skilled in the art, that the present invention can be practiced with other specific details.

0030 An important purpose of the present invention is to enable a testing/burn-in method that utilizes a strip socket. A strip socket is a socket that allows substantially simultaneous electrical contact to multiple packages in strip format. The method involves performing electrical isolation of the lead or terminal of each device in the same strip.

0031 FIG. 2A is a schematic diagram showing lead/terminal isolation for a leaded package before a lead length cut, in accordance with an embodiment of the present invention. Examples of a leaded package include a surface mount device and a through-hole package. FIG. 2A shows a portion of a semiconductor lead frame strip 214. The lead frame strip 214 is a matrix of semiconductor units. The lead frame strip 214 is tied together with tie bars 204 and lead tie bars 208. The lead frame strip 214 can also include any substrate appropriate for manufacturing the matrix. The lead frame strip 214 holds each package body 206. For a surface mount or through-hole package, a mechanical punching or trimming can be applied to electrically isolate the package 206 while the package 206 is held in the same strip with a tie bar or an extrusion of molded compound. A portion of a cutting punch 210 is in position to cut the lead frame and cause electrical isolation of the packages 206. This technique is called lead length cut.

0032 FIG. 2B is a schematic diagram showing lead/terminal isolation for a leaded package after the lead length cut, in accordance with an embodiment of the present invention. The lead tips 212 have been cut and electrically isolated from an adjacent package 206 by the cutting punch 210.

0033 FIG. 3A is a schematic diagram of terminal isolation before isolation for a leadless package, in accordance with an embodiment of the present invention. Before isolation, the terminals 304 of each package are connected to their respective tie bar 306. For a leadless semiconductor package, such as a quad flat non-lead (QFN) package, its leads or terminals are normally connected to the tie bar and are thus shorted together in the same package and on adjacent packages. Accordingly, an electrical function or electrical function test can not be performed. The isolation described above can be caused by using a mechanical rounder, a sawing blade, a laser, a water jet, a chemical etchant or by using another technique designed to disconnect the lead or terminal out of a common tie bar while each device is held in the strip.

0034 FIG. 3B is a schematic diagram of terminal isolation after isolation for a leadless package, in accordance with an embodiment of the present invention. After isolation, terminals of each package are isolated and ready for electrical testing in the strip socket. A saw path 308 is shown. Preferably, the saw path 308 does not fully sever the package material to allow the electrically isolated packages to remain in a strip. A removed tie bar 310 is shown where a half cut or partial cut removed a tie bar 306.

0035 FIG. 4 is a diagram of a strip 402 of ball grid arrays (BGA) or chip scale packages (CSP), in accordance with an embodiment of the present invention. A top view 404 and a cross-sectional view 405 are shown for the BGA/CSP package 406. The BGA/CSP package 406 has leads or terminals that are already electrically isolated by design or by assembly processing. Thus, neither a BGA nor a CSP require further isolation processing.

0036 FIG. 5 is a diagram of strip sockets on a testing/burn-in board, in accordance with an embodiment of the present invention. Each strip socket 508 accommodates a whole strip 506 of packages. In other words, one whole strip 506 of packages can be placed into each strip socket 508. The strip sockets 508 are mounted to a testing/burn-in board 502. A card edge connector 504 integrally formed in an edge is mounted to the testing/burn-in board 502 for electrically coupling the testing/burn-in board to a test or burn-in system. The strip socket 508 minimizes the number of devices that need to be handled by handling multiple devices as a strip. All units or packages in the strip socket 508 are loaded and unloaded at substantially the same time.
FIG. 6A is a diagram of a testing/burn-in strip socket of a leaded package (e.g., a surface mount device or through-hole package), in accordance with an embodiment of the present invention. The strip socket of leaded packages 206 includes a cover 604 and a base 608 mounted to a PCB 502. Another name for the base 608 is cavity. Multiple leaded packages 206 or leaded devices are shown undergoing testing and/or burn in at once. Each leaded package 206 has a plurality of leads 214, which are electrically coupled with the contact pins 606. A lock 610 fixes the cover 604 to the base 608. The lead 214 is preferably not formed into a certain shape here. Rather, the leads 214 preferably remain substantially flat. Further, preferably only the tip of the lead 214 is cut and isolated. The forming of the lead 214 are preferably processed after a test or burn-in. Thus, loading or unloading of the package strip into the strip socket does not affect the shape of the lead 214.

FIG. 6B is a diagram of a testing/burn-in strip socket of a leadless package, in accordance with an embodiment of the present invention. The strip socket of a leadless package includes a cover 612 and a base 622 mounted to a PCB 620. Multiple leadless packages 614 or leadless devices are shown undergoing testing at once. As is known, each leadless package 614 has no leads. The leadless packages 614 have terminals 616, which are isolated from other semiconductor devices in the strip. Contact pins 618 electrically connect the terminals 616 to the PCB 620. A lock 624 fixes the cover 612 to the base 622.

Note that a strip socket for a BGA package 406 is not displayed. A similar method and apparatus used for leaded packages and leadless packages can be applied to BGA packages 406.

FIG. 7B is a flowchart of a process involving testing/burn-in utilizing a strip socket, in accordance with an embodiment of the present invention. The purpose is to reduce the number of separate devices that must be handled to simplify the process of assembly, testing and packing of the semiconductor devices. By reducing handling requirements, the time for manufacturing will be reduced. The process involves handling semiconductor packages from assembly to final testing utilizing strip sockets 508. The process flow begins in the operation 716, which involves assembly of semiconductor chips into packages. Assembly includes die attachment, wire bonding, plating and molding, among other things. The process flow proceeds to the operation 718 which includes lead or terminal isolation. Next, the strip of semiconductor devices is loaded into the strip socket. The physical nature of the strip and the strip socket allow a manufacturer to load each of the semiconductor devices of the strip into the strip socket at substantially a same time. Test/burn-in using a strip socket is then performed on all the devices in the strips in the operation 720. In the operation 722, final testing by an automatic base test handler is performed. The strip of semiconductor devices can then be unloaded from the strip socket. The physical nature of the strip and the strip socket allow a manufacturer to unload all of the semiconductor devices of the strip from the strip socket at substantially a same time. Then, in the operation 724, the packages undergo forming and singulating. Next, packing is performed in the operation 726. As shown in FIG. 7B, the operations 716, 718, 720 and 722 involve handling the packages as lead frames or strips. Only the operations 724 and 726 involve handling the packages as singulated units. The process of FIG. 7B is preferably handled in a temperature range of ~65°C. to 185°C.

Advantageously, the strip socket of the present invention significantly reduces mechanical lead defects in test/burn-in processing. Time is dramatically saved during loading and unloading of the packages on the testing/burn-in board. Further, processing is substantially simplified by handling the packages in a strip format from assembly to final testing.

In the foregoing specification, the invention has been described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

1.-17. (canceled)

18. A leadframe strip of semiconductor devices, configured for making electrical contact with a strip socket, wherein electrical contact of each of the semiconductor devices is made at substantially a same time with the strip socket.

19. The leadframe strip of semiconductor devices claim 18, wherein each of the semiconductor devices of the leadframe strip of semiconductor devices is designed to be loaded into the strip socket at substantially a same time.

20. The leadframe strip of semiconductor devices of claim 18, wherein each of the semiconductor devices of the leadframe strip of semiconductor devices is designed to be unloaded from the strip socket at substantially a same time.

21. The leadframe strip of semiconductor devices claim 18, wherein the leadframe strip of semiconductor devices is designed to facilitate testing of the semiconductor devices in the leadframe strip of semiconductor devices.

22. The leadframe strip of semiconductor devices of claim 18, wherein the leadframe strip of semiconductor devices is designed to facilitate burn-in of the semiconductor devices in the leadframe strip of semiconductor devices.