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POWER TRANSISTOR GATE-CHARGE HARVESTER FOR INTERNAL SUPPLY GENERATION

[0001] This relates generally to the field of power control circuits. More particularly, and not by way of any limitation, the description is directed to a power transistor gate-charge harvester for internal supply generation.

SUMMARY

[0002] Some embodiments provide circuitry to recover parts of the power transistor gate-charge during the gate discharge period in order to generate a recycled logic supply voltage. This recycled logic supply voltage replaces portions of an input logic supply voltage, which is generated from input voltage V_{in} ; the recycled logic supply voltage may increase the overall efficiency of the power circuit.

[0003] In one aspect, an embodiment of a gate-charge harvester is described. The gate-charge harvester includes a harvest capacitor having a first plate and a second plate, the second plate being coupled to a lower rail; and a low-side harvest transistor having a first terminal coupled to a gate of a low-side power transistor and a second terminal coupled to the first plate, wherein the first plate is further coupled to send a voltage towards a regulator.

[0004] In another aspect, an embodiment of an integrated power circuit is described. The integrated power circuit includes a low-side power transistor and a high-side power transistor coupled in series between a first pin and a second pin; a gate driver coupled to provide a low-side gate control signal to a gate of the low-side power transistor and to provide a high-side gate control signal to a gate of the high-side power transistor; and a gate-charge harvester comprising: a harvest capacitor having a first plate and a second plate, the second plate being coupled to a lower rail; a first N-type metal oxide silicon (NMOS) harvest transistor having a first terminal coupled to the gate of the high-side power transistor and a second terminal coupled to the first plate; and a second NMOS harvest transistor having a first terminal coupled to a gate of the low-side power transistor and a second terminal coupled to the first plate, wherein the first plate is further coupled to provide a harvested voltage.

[0005] In yet another aspect, an embodiment of an integrated power circuit is described. The integrated power circuit includes a power transistor coupled between a first pin and a second pin;

a gate driver coupled to provide a gate control signal to a gate of the power transistor; and a gate-charge harvester comprising: a harvest capacitor having a first plate and a second plate, the second plate being coupled to a lower rail; and an N-type metal oxide silicon (NMOS) harvest transistor having a first terminal coupled to the gate of the power transistor and a second terminal coupled to the first plate; wherein the first plate is further coupled to provide a harvested voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Embodiments of the description are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like references indicate similar elements. Different references to "an" or "one" embodiment in this description are not necessarily to the same embodiment, and such references may mean at least one. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, the description encompasses such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described. The term "couple" or "couples" means either an indirect or direct electrical connection unless qualified, as in "communicably coupled" which may include wireless connections. Thus, if a first device couples to a second device, that connection may be through a direct electrical connection, or through an indirect electrical connection via other devices and connections.

[0007] The accompanying drawings are incorporated into and form a part of the specification to illustrate one or more exemplary embodiments of the description. Various advantages and features are described in the following Detailed Description taken in connection with the appended claims and with reference to the attached drawing figures in which:

[0008] FIG. 1A depicts an example of a DC/DC boost converter containing a gate-charge harvester according to an embodiment;

[0009] FIG. 1B depicts an example of a DC/DC boost converter containing a gate-charge harvester according to an embodiment;

[0010] FIG. 1C depicts an example of a DC/DC boost converter containing a gate-charge harvester according to an embodiment;

[0011] FIG. 1D depicts an example of a DC/DC buck converter containing a gate-charge harvester according to an embodiment;

[0012] FIG. 2 depicts various voltage levels during operation of the circuit of FIG. 1A according to an embodiment;

[0013] FIG. 3 depicts a block diagram of various circuits within a DC/DC boost converter according to an embodiment;

[0014] FIG. 4A is directed to simulations comparing the efficiency of AVDD supply current generation across increasing logic-level current loads in a circuit containing the gate-charge harvester versus a prior art circuit with no gate-charge harvester;

[0015] FIG. 4B depicts an efficiency calculation of the both the prior art circuit of FIG. 5 and the circuit of FIG. 1A over a range of the output current I_{out} ;

[0016] FIG. 4C depicts the increase in efficiency provided by the gate-charge harvester;

[0017] FIG. 5 depicts a block diagram of various circuits within a DC/DC boost converter according to the prior art;

[0018] FIG. 6 depicts an example of a DC/DC boost converter according to the prior art; and

[0019] FIG. 7 depicts various voltage levels during operation of the circuit of FIG. 6.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0020] Specific embodiments of the invention will now be described in detail with reference to the accompanying figures. Numerous specific details are set forth in order to provide a more thorough understanding of the invention. However, the invention may be practiced without these specific details. In other instances, well-known features have not been described in detail to avoid unnecessarily complicating the description.

[0021] FIG. 5 depicts a high-level block diagram of a DC/DC boost converter 500 according to the prior art. DC/DC boost converter 500 depicts an input voltage V_{in} , which is coupled to switch-node SW through an inductor L. Low-side power transistor M1 is coupled in series with high-side power transistor M2 between the lower rail, which can be a ground plane, and an output voltage V_{out} , which is shown coupled to an output capacitor C_{out} and a load represented by output resistor R_{out} . In the embodiment shown, low-side power transistor M1 is an N-type metal oxide silicon (NMOS) power transistor and high-side power transistor M2 is a P-type metal oxide silicon (PMOS) power transistor, although these are not limitations. The gate of low-side power transistor M1 is coupled to receive low-side gate control signal LS_GATE and high-side power transistor M2 is coupled to receive high-side gate control signal HS_GATE, both of which control signals are provided by boost gate driver 502. Boost gate driver 502 receives control signals from boost control circuit 505. Power to operate boost control circuit 505 and boost gate driver 502 is provided by internal low dropout (LDO) regulator 508, which is

responsible for generating both a gate driver supply voltage V_{max} (not specifically shown in this figure) and a logic supply voltage $AVDD$ from the input voltage. Internal LDO regulator 508 can also supply logic supply voltage $AVDD$ to other control circuits and to any additional circuit, such as monitoring circuits (not specifically shown). Gate driver supply voltage V_{max} is the greater of input voltage V_{in} and output voltage V_{out} . Internal LDO regulator 508 can sometimes draw large currents in order to operate DC/DC boost converter 500, so it is desirable to improve the system efficiency. The description is directed to reducing this problem by harvesting a portion of the gate charge on low-side power transistor M1 and high-side power transistor M2 to provide a portion of the logic supply voltage $AVDD$. The gate charge is otherwise routed to the ground plane and lost each time the gate is discharged. In order to better understand how this gate charge is harvested, we first look more closely at boost gate driver 502.

[0022] FIG. 6 depicts a somewhat more detailed example of a DC/DC boost converter 600 according to the prior art. DC/DC boost converter 600 again includes low-side power transistor M1 and high-side power transistor M2 that are coupled in series between the lower rail and an output node that provides output voltage V_{out} . A switch-node SW between low-side power transistor M1 and high-side power transistor M2 is coupled to an input voltage V_{in} through an inductor L. Output transistor Cout is coupled between the output voltage V_{out} and the lower rail; output resistor Rout represents the load on the output.

[0023] Gate driver 602 is an example embodiment of boost gate driver 502. Gate driver 602 is coupled to the gate of low-side power transistor M1 and to the gate of high-side power transistor M2 and includes four gate control transistors. A first P-type gate control transistor M3 is coupled in series with a first N-type gate control transistor M4 between gate driver supply voltage V_{max} and the lower rail, with a node between first P-type gate control transistor M3 and first N-type gate control transistor M4 providing a low-side gate control signal LS_GATE. Similarly, a second P-type gate control transistor M5 is coupled in series with a second N-type gate control transistor M6 between gate driver supply voltage V_{max} and the lower rail, with a node between second P-type gate control transistor M5 and second N-type gate control transistor M6 providing a high-side gate control signal HS_GATE. A logic circuit 604 receives one or more boost control signals, which are provided by the previously mentioned voltage control and/or current control. Logic circuit 604 provides four intermediate control signals: low-side-P control signal LS_P, low-side-N control signal LS_N, high-side-P control signal HS_P and high-

side-N control signal HS_N respectively to the gates of gate control transistors M3, M4, M5, M6.

[0024] FIG. 7 depicts the timing related to driving one of low-side power transistor M1 and high-side power transistor M2. FIG. 7 contains two graphs 700A, 700B. Graph 700A depicts the voltage on the gate of a power transistor. Although low-side power transistor M1, which is NMOS, is turned on by the gate going high and high-side power transistor M2, which is PMOS, is turned off by the gate going high, the gates of these two power transistors are driven in the same manner. Because of the similar gate-drive approach, only one example waveform is given, where the designations LS_GATE and HS_GATE are replaced by power gate control signal xx_GATE to indicate that the voltage illustrated can refer to either high-side gate control signal HS_GATE or low-side gate control signal LS_GATE. Graph 700B depicts the voltages on the respective gate control transistors of gate driver 602 that drive the power gate control signal xx_GATE shown in graph 700A. Similarly to the upper graph, the designations LS_P and HS_P are replaced by intermediate-P control signal xx_P to indicate that the voltage can refer to either the voltage on low-side-P control signal LS_P or high-side-P control signal HS_P and the designations LS_N and HS_N are replaced by intermediate-N control signal xx_N to indicate that the voltage can refer to either the voltage on low-side-N control signal LS_N or high-side-N control signal HS_N.

[0025] A gate driver non-overlap between intermediate-P control signal xx_P and intermediate-N control signal xx_N is necessary to avoid cross-conduction. This non-overlap is shown and labelled as P-dead time T_{dead,p} and N-dead time T_{dead,n}, which are well controlled. During both P-dead time T_{dead,p} and N-dead time T_{dead,n}, power gate control signal xx_GATE is high-impedant. The transition of intermediate-P control signal xx_P and intermediate-N control signal xx_N in the region surrounding P-dead time T_{dead,p} is divided into six time periods, indicated by the circled numbers 1-6. For ease in distinguishing the time periods, P-dead time T_{dead,p} and N-dead time T_{dead,n} are delineated by long dotted lines, while the other time periods are delineated by shorter dotted lines.

[0026] During time period (1), both of intermediate-N control signal xx_N and intermediate-P control signal xx_P are coupled to ground. Intermediate-P control signal xx_P causes a corresponding P-type gate control transistor, either first P-type gate control transistor M3 or second P-type gate control transistor M5 to conduct current and intermediate-N control signal

xx_N causes a corresponding N-type gate control transistor, either first N-type gate control transistor M4 or second N-type gate control transistor M6 to be turned off. This results in the corresponding power gate control signal xx_GATE being high potential, which in FIG. 6 is the value of gate driver supply voltage Vmax. During time period (2), the intermediate-N control signal xx_N remains off and the intermediate-P control signal xx_P rises. During P-dead time Tdead,p, which is also time period (3), both of the gate control transistors associated with intermediate-N control signal xx_N and intermediate-P control signal xx_P are in the off state and the power gate control signal xx_GATE is high-impedant. This P-dead time Tdead,p, which occurs after the rise of intermediate-P control signal xx_P and before the rise of intermediate-N control signal xx_N, is used to avoid a potential cross-current between gate driver supply voltage Vmax and the ground plane and also to increase the efficiency. During time period (4), the P-dead time Tdead,p has ended and the voltage on intermediate-N control signal xx_N rises to gate driver supply voltage Vmax. The increasing voltage on intermediate-N control signal xx_N begins to pull the voltage on power gate control signal xx_GATE to ground. During time period (5), the dynamic transition of power gate control signal xx_GATE ends with power gate control signal xx_GATE at low potential. During time period (6), which extends until intermediate-P control signal xx_P is at ground, a reverse operation turns off intermediate-N control signal xx_N and intermediate-P control signal xx_P, which will cause the power gate control signal xx_GATE to charge to high potential again.

[0027] FIG. 1A depicts an example of a DC/DC boost converter 100A embodied in an integrated circuit chip 101A and containing a gate-charge harvester 106A according to an embodiment. DC/DC boost converter 100A contains low-side power transistor M1 and high-side power transistor M2 coupled in series between a first pin P1 and a second pin P2, with switch-node SW coupled to a third pin. During operation of DC/DC boost converter 100A, first pin P1 is coupled to a ground plane, second pin P2 is coupled to an output capacitor Cout and to a load represented by resistor Rout, and third pin P3 is coupled to inductor L and through inductor L to input voltage Vin. For simplicity and without loss of generality, the gates of low-side power transistor M1 and high-side power transistor M2 are assumed to withstand both gate driver supply voltage Vmax in case of low-side power transistor M1 and the ground plane in case of high-side power transistor M2, so that the maximum allowed gate/source or gate/bulk potentials are not violated. In other embodiments (not specifically shown), the high potential of

low-side gate control signal LS_GATE and the low potential of high-side gate control signal HS_GATE are clamped to a safe potential, such that the gates of low-side power transistor M1 and high-side power transistor M2 are safe.

[0028] Low-side power transistor M1 and high-side power transistor M2 are enabled anti-phased, such that DC/DC boost converter 100A operates in a continuous operation to charge and discharge the inductor L for energy transfer towards the output capacitor C_{out}. The turn on and off of the gates of low-side power transistor M1 and high-side power transistor M2 show a characteristic non-overlap behavior to avoid cross-conduction. This non-overlap is ensured by a proper gate drive topology provided by logic circuit 104 to control low-side gate control signal LS_GATE and high-side gate control signal HS_GATE through gate driver 102. A similar gate-drive non-overlap between the low-side-P control signal LS_P and low-side-N control signal LS_N, as well as between high-side-P control signal HS_P and high-side-N control signal HS_N may be used avoid gate-driver cross-conduction. This method may be especially important in high-power and/or high efficiency systems, where low-side power transistor M1 and high-side power transistor M2 are huge and also require a non-negligible gate-drive circuitry, or in systems where the peak efficiency and/or light-load efficiency are critical.

[0029] Gate driver 102 contains first P-type gate control transistor M3 and first N-type gate control transistor M4, which are coupled in series between gate driver supply voltage V_{max} and the lower rail to provide low-side gate control signal LS_GATE, and second P-type gate control transistor M5 and second N-type gate control transistor M6, which are coupled in series between gate driver supply voltage V_{max} and the lower rail to provide high-side gate control signal HS_GATE. Gate driver 102 receives low-side-P control signal LS_P, low-side-N control signal LS_N, high-side-P control signal HS_P and high-side-N control signal HS_N from logic circuit 104, which itself receives boost control signals as input.

[0030] Gate-charge harvester 106A contains two transistors that control the harvest of the gate charge and a capacitor on which the harvested gate charge can be temporarily stored. Low-side harvest transistor M_{harvLS} is coupled between low-side gate control signal LS_GATE and a first plate of harvest capacitor C_{harv} and high-side harvest transistor M_{harvHS} is coupled between high-side gate control signal HS_GATE and the first plate of harvest capacitor C_{harv}. In each of the examples given in this application, low-side harvest transistor M_{harvLS} and high-side harvest transistor M_{harvHS} are shown as NMOS transistors for simplicity, although any

type of transistor can be utilized. A harvest gate control signal G_{harv} controls the timing of low-side harvest transistor M_{harvLS} and high-side harvest transistor M_{harvHS} . A second plate of harvest capacitor C_{harv} is coupled to the lower rail. As will be shown below, the harvested voltage V_{pre} is an unregulated voltage that is less than gate driver supply voltage V_{max} and greater than logic supply voltage $AVDD$. Harvested voltage V_{pre} can also vary considerably over time and is not appropriate to be utilized as a supply voltage. Therefore, harvested voltage V_{pre} is provided to a harvest regulator 108 that can regulate the harvested voltage V_{pre} to generate recycled logic supply voltage $AVDD_{recyl}$ on $AVDD$ capacitor C_{avdd} to supply resistor load R_{avdd} . Harvest regulator 108 can be a simple LDO regulator or any other circuit that generates a recycled logic supply voltage $AVDD_{recyl}$ having a controlled voltage from uncontrolled harvested voltage V_{pre} . How the operation of gate-charge harvester 106A fits in with the operation of gate driver 102 is described with reference to FIG. 2.

[0031] FIG. 2 is similar to FIG. 7, but depicts the differences brought about by gate-charge harvester 106A. Graph 200A again depicts the charge on power gate control signal xx_GATE , with power gate control signal 202 depicting the loss of charge when there is no harvest of the charge and power gate control signal 204 depicting the loss of charge when there is a harvest of the charge. Also shown are the harvested voltage V_{pre} 206 and the recycled logic supply voltage $AVDD_{recyl}$. Graph 200B again depicts the intermediate-N control signal xx_N and intermediate-P control signal xx_P and also depicts the harvest gate control signal G_{harv} .

[0032] The transition of intermediate-P control signal xx_P and intermediate-N control signal xx_N during time period $T_{dead,P}$ is again divided into six parts, which are again indicated by the circled numbers 1-6. During time period (1), both intermediate-N control signal xx_N and intermediate-P control signal xx_P are connected to the ground plane. The low value on intermediate-P control signal xx_P causes a corresponding one of first P-type gate control transistor M3 and second P-type gate control transistor M5 to conduct current. The low value on intermediate-N control signal xx_N causes a corresponding one of first N-type gate control transistor M4 and second N-type gate control transistor M6 to be off. The power gate control signal xx_GATE is high potential, which has a value equal to gate driver supply voltage V_{max} in this example. At time period (2), the intermediate-N control signal xx_N remains low and intermediate-P control signal xx_P rises to a high potential. At the beginning of P-dead time $T_{dead,P}$, which is also time period (3), intermediate-N control signal xx_N is holding a

respective one of N-type gate control transistors M4, M6 in the off state and intermediate-P control signal xx_P is holding a respective one of P-type gate control transistors M3, M5 in the off state.

[0033] As soon as both intermediate control transistors xx_N and xx_P are holding their respective gate control transistors off in time period (3), harvest gate control signal G_{harv} is pulled to high potential, such that the corresponding gate/source voltage $V_{gs,harv}$ is now greater than the harvested voltage V_{pre} plus the threshold voltage V_{th} of the harvest transistors and low-side harvest transistor M_{harvLS} and high-side harvest transistor M_{harvHS} are enabled. Instead of power gate control signal xx_GATE having a floating potential, as indicated by the old waveform in power gate control signal 202, the power gate control signal 204 now decreases by the harvest current as indicated by the waveform. The harvested voltage V_{pre} 206 then increases to near the value of power gate control signal xx_GATE 204 and follows the gate potential until the end of the P-dead time $T_{dead,P}$.

[0034] During time period (4), the intermediate-N control signal xx_N rises to a high potential and starts pulling power gate control signal xx_GATE to a low potential. At the same time, harvest gate control signal G_{harv} is pulled to low potential to stop the harvest. The power gate control signal 204 is now further discharged to a low potential and harvested voltage V_{pre} on harvest capacitor C_{harv} is at a high value due to the sampling of power gate control signal 204. During time periods (5) and (6), the gate-switching is not changed from older switching patterns. From the uncontrolled harvested voltage V_{pre} 206, a post-regulator such as harvest regulator 108 further down-converts the charge stored on harvest capacitor C_{harv} to logic supply voltage $AVDD_{recyl}$, which can be stored on logic-level capacitor C_{avdd} and supplied to the resistor load R_{avdd} .

[0035] Given the need to also provide a dead time between low-side power transistor M1 and high-side power transistor M2, although FIG. 1A depicts a single harvest gate control signal G_{harv} for simplicity, a low-side harvest gate control signal G_{harvLS} and a high-side harvest gate control signal G_{harvHS} can be utilized to separately control the timing of the gate harvest from the power transistors, as will be shown in other examples.

[0036] FIG. 3 depicts a high-level block diagram of DC/DC boost converter 300 according to an embodiment. A distinction is made in this figure between an input logic supply voltage $AVDD_{in}$, a recycled logic supply voltage $AVDD_{recyl}$ and a multiplexed logic supply voltage

AVDDmux that includes both AVDDin and AVDDrecl. The previously seen internal LDO regulator 308, which supplies power rails to boost control circuit 305 and boost gate driver 302, is now supported in providing the power rails by gate-charge harvester 306 and decision circuit 310. Gate-charge harvester 306 is coupled to harvest a portion of the gate charge on low-side power transistor M1 and high-side power transistor M2 any time there is switching activity on low-side power transistor M1 and high-side power transistor M2. After regulation of the harvested voltage V_{pre} , the results are provided to decision circuit 310 as recycled logic supply voltage AVDDrecyl. Decision circuit 310 multiplexes the input logic supply voltage AVDDin from internal LDO regulator 308 and the recycled logic supply voltage AVDDrecyl from gate-charge harvester 306 to provide multiplexed logic supply voltage AVDDmux. Because there can be time periods during the operation of DC/DC boost converter 300 when low-side power transistor M1 and high-side power transistor M2 are not switching, decision circuit 310 must guarantee that the use of recycled logic supply voltage AVDDrecyl does not interfere with critical switching operations. In one embodiment, decision circuit 310 utilizes the recycled logic supply voltage AVDDrecyl to supply only portions of the boost converter that are not switching-critical. In one embodiment, decision circuit 310 ensures appropriate multiplexing of input logic supply voltage AVDDin and recycled logic supply voltage AVDDrecyl as soon as the switching of low-side power transistor M1 and high-side power transistor M2 starts or stops and the recycled logic supply voltage AVDDrecyl is built-up or collapses.

[0037] FIG. 4A is directed to simulations comparing the efficiency of AVDD supply current generation across increasing logic-level current loads in a circuit containing the gate-charge harvester versus a prior art circuit with no gate-charge harvester. Current consumption over increasing levels of current load I_{AVDD} was first simulated, with Table 1 showing results for the prior art circuit and Table 2 providing results for the circuit with a gate-charge harvester.

Table 1 Without gate-charge harvester

I_AVDD	I_SUM	I_VMAX	I_VIN	I_HARV
0	1.334mA	1.33mA	4.5uA	0
20uA	1.354mA	1.33mA	24.5uA	0
40uA	1.374mA	1.33mA	44.4uA	0
60uA	1.393mA	1.33mA	64.3uA	0
80uA	1.413mA	1.33mA	84.2uA	0

100uA	1.433mA	1.33mA	104uA	0
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[0038] In these tables, I_{AVDD} is the current load, I_{VMAX} is the current generated to provide the gate driver supply voltage, I_{VIN} is the current generated to supply the logic supply voltage, I_{SUM} is the sum of the generated currents ($I_{VMAX}+I_{VIN}$) and I_{HARV} is the current harvested by the gate-charge harvester. In Table 1, no gate-charge was harvested and harvested current I_{HARV} is zero for all values of current load I_{AVDD} . As the value of current load I_{AVDD} increases, the gate current drawn as I_{MAX} remains the same but the current I_{VIN} generated to supply the logic supply voltage increases, so that I_{SUM} also increases as current load I_{AVDD} increases.

Table 2 With gate-charge harvester

I_{AVDD}	I_{SUM}	I_{VMAX}	I_{VIN}	I_{HARV}
0	1.33mA	1.33mA	0	0
20uA	1.33mA	1.33mA	0	24.5uA
40uA	1.33mA	1.33mA	0	44.4uA
60uA	1.33mA	1.33mA	0	64.3uA
80uA	1.33mA	1.33mA	0	84.2uA
100uA	1.33mA	1.33mA	0	104uA

[0039] In Table 2, a gate-charge harvester is providing the logic supply voltage, so that there is no need to generate current I_{VIN} for this purpose. Since the current generated to supply the gate driver supply voltage I_{VMAX} is constant, the value of I_{SUM} is also constant. Based on the values of the sum of generated current I_{SUM} shown in the above two tables, an efficiency calculation was made with input voltage V_{in} equal to 3.8 V, output voltage V_{out} equal to 4.6 V and output current I_{out} equal to 10 mA. The results are shown in Table 3 below and in FIG. 4A, which depicts the efficiency of the prior art circuit as decreasing linearly as current load I_{AVDD} increases, while the efficiency of the circuit remains constant across values of current load I_{AVDD} .

Table 3 Efficiency improvement

I_{AVDD}	Efficiency Without harvest	Efficiency With harvest	Efficiency Improvement
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0	88.236	88.261	0.026
20u	88.107	88.261	0.154
40u	87.979	88.261	0.282
60u	87.858	88.261	0.404
80u	87.730	88.261	0.531
100u	87.603	88.261	0.658

[0040] FIG. 4B depicts the efficiency calculation of the both the prior art circuit of FIG. 5 and the circuit of FIG. 1A over a range of the output current I_{out} . In FIG. 4B, the efficiency of both circuits increases as the output current I_{out} increases. At the lowest output current I_{out} having a value of $1.00E-03$, the use of the gate-charge harvester provides a small but clear improvement, while at the highest output current I_{out} having a value of $1.00E-01$, the efficiency is virtually identical. The efficiency improvement over the prior art is more clearly quantified in FIG. 4C. In this curve, it can be seen that the gate-charge harvester provides about 1.44 percent increase in efficiency at the lowest output current I_{out} of $1.00E-3$ and about 0.08 percent increase in efficiency at the highest output current I_{out} of $1.00E-1$.

[0041] Simulations were also performed to determine the ramp times of harvested voltage V_{pre} and recycled logic supply voltage $AVDD_{recyl}$. The rate at which harvested voltage V_{pre} ramps up is dependent on the size of harvest transistors M_{harvLS} and M_{harvHS} , while the rate at which recycled logic supply voltage $AVDD_{recyl}$ ramps up is dependent on the bandwidth of regulator 108. The simulations were performed with an input voltage V_{in} 3.8 V and an output voltage V_{out} of 4.6 V. In one embodiment, harvested voltage V_{pre} ramped to an average voltage of about 4.5 V in about 10 μs and recycled logic supply voltage $AVDD_{recyl}$ ramped to a value of about 1.8 V in approximately 60 μs .

[0042] While gate-charge harvester 106A has been described as part of a DC/DC boost converter 100A having a PMOS power transistor for high-side power transistor M2, the gate-charge harvester may be utilized in other circuits. FIG. 1B depicts a DC/DC boost converter 100B implemented on an IC chip 101B and containing a gate-charge harvester 106B according to an embodiment. DC/DC boost converter 100B is similar to DC/DC boost converter 100A in most respects, but differs in several important ways. To avoid repetition, the similarities are not repeated and only the differences are noted. In DC/DC boost converter 100B, rather than having a PMOS power transistor for the high-side power transistor M2, an NMOS power transistor is

utilized instead. As is known, a bootstrapped gate-driver (not specifically shown) provides a bootstrap voltage V_{boot} to the high-side driver circuit. Also, while a single harvest gate control signal G_{harv} was shown in gate-charge harvester 106A, gate-charge harvester 106B contains two separate gate control signals. High-side harvest gate control signal G_{harvHS} is provided to high-side harvest transistor M_{harvHS} and low-side harvest gate control signal G_{harvLS} is provided to low-side harvest transistor M_{harvLS} . In at least one embodiment, the low-side harvest gate control signal G_{harvLS} is coupled to be high during a first dead time for both first P-type gate control transistor $M3$ and first N-type gate control transistor $M4$, the first dead time occurring when first P-type gate control transistor $M3$ has been turned off and N-type gate control transistor $M4$ has not yet been turned on. Similarly, the high-side harvest gate control signal G_{harvHS} is coupled to be high during a second dead time for both second P-type gate control transistor $M5$ and second N-type gate control transistor $M6$, the second dead time occurring when second P-type gate control transistor $M5$ has been turned off and second N-type gate control transistor $M6$ has not yet been turned on.

[0043] FIG. 1C depicts DC/DC boost converter 100C implemented on an IC chip 101C and containing a low-side power transistor $M1$ coupled in series with a diode $D1$ between first pin $P1$ and second pin $P2$. Switch node SW lies between low-side power transistor $M1$ and diode $D1$. During operation of DC/DC boost converter 100C, first pin $P1$ is coupled to the ground plane, pin $P2$ is coupled to an output capacitor C_{out} to provide an output voltage V_{out} to a load represented by resistor R_{out} . Because only a single power transistor is utilized in this application, gate driver 102C contains only first P-type gate control transistor coupled in series with first N-type gate control transistor between gate driver supply voltage V_{max} and the lower rail and receives low-side-P control signal LS_P and high-side-N control signal LS_N from logic circuit 104. Gate-charge harvester 106C includes low-side harvest transistor M_{harvLS} , which is coupled between the gate of low-side power transistor $M1$ and the first plate of harvest capacitor C_{harv} .

[0044] FIG. 1D depicts a high-level block diagram of a DC/DC buck converter 100D implemented on an IC chip 101D and containing a gate-charge harvester 106D according to an embodiment. For DC/DC buck converter 100D, low-side power transistor $M1$ is coupled in series with high-side power transistor $M2$ between first pin $P1$ and second pin $P2$. A node between low-side power transistor $M1$ and high-side power transistor $M2$ is coupled to a third

pin P3. During operation of DC/DC buck converter 100D, pin P1 is coupled to the ground plane, pin P2 is coupled to an input voltage V_{in} and pin P3 is coupled to provide an output voltage V_{out} . Gate driver 102 is again coupled to provide low-side gate control signal LS_GATE to the gate of low-side power transistor M1 and to provide high-side gate control signal HS_GATE to the gate of high-side power transistor M2. Gate-charge harvester 106D operates in a manner similar to gate-charge harvesters 106A, 106B as previously described. In the embodiment shown, high-side power transistor M2 is a PMOS power transistor and low-side power transistor M1 is an NMOS power transistor. However, both high-side power transistor M2 and low-side power transistor M1 can be NMOS power transistors. In one embodiment, high-side power transistor M2 can be replaced by a diode, as was shown in FIG. 1C.

[0045] A gate-charge harvester harvests a portion of the gate charge from one or more power transistors that is currently wasted when the gate of the power transistors are discharged. The gate-charge harvester requires only a corresponding harvest transistor for each power transistor, with a harvest control signal providing appropriate timing of the charge harvesting and a harvest capacitor on which to store the harvested charge. The harvesting process provides an uncontrolled harvested charge, which can then be sent to a regulator that down-converts the harvested charge into a logic supply voltage that has a constant voltage. The gate charge used to turn the power transistors on and off is initially drawn from either input voltage V_{in} or output voltage V_{out} , which in some embodiments can be itself derived from input voltage V_{in} by up-conversion. Gate charge harvesting can allow some of this charge to be recycled and down-converted to provide a logic-level voltage that is lower than the power gate voltage. By taking over part of the internal logic supply generation, an increase of the overall efficiency of the IC chip is provided.

[0046] The claims are not limited to any particular embodiment or example, and no particular component, element, step, act, or function is essential such that it must be included in the scope of the claims. Reference to an element in the singular does not mean "one and only one" unless explicitly so stated, but rather "one or more." The description encompasses all structural and functional equivalents to the above elements and such equivalents are encompassed by the claims. Accordingly, the exemplary embodiments described herein can be practiced with various modifications and alterations within the spirit and scope of the claims appended below.

CLAIMS

What is claimed is:

1. A gate-charge harvester comprising:
 - a harvest capacitor having a first plate and a second plate, the second plate being coupled to a lower rail; and
 - a low-side harvest transistor having a first terminal coupled to a gate of a low-side power transistor and a second terminal coupled to the first plate;wherein the first plate is further coupled to send a voltage towards a regulator.
2. The gate-charge harvester as recited in claim 1 further comprising a low-side harvest gate control signal coupled to a gate of the low-side harvest transistor, the low-side harvest gate control signal being coupled to be high during a first dead time for both a first P-type gate control transistor and a first N-type gate control transistor that drive a gate of the low-side power transistor, the first dead time occurring when the first P-type gate control transistor has been turned off and the first N-type gate control transistor has not yet been turned on.
3. The gate-charge harvester as recited in claim 2 further comprising:
 - a high-side harvest transistor having a first terminal coupled to a gate of a high-side power transistor and a second terminal coupled to the first plate; and
 - a high-side harvest gate control signal coupled to a gate of the high-side harvest transistor, the high-side harvest gate control signal being coupled to be high during a second dead time for both a second P-type gate control transistor and a second N-type gate control transistor that drive the gate of the high-side power transistor, the second dead time occurring when the second P-type gate control transistor has been turned off and the second N-type gate control transistor has not yet been turned on.
4. The gate-charge harvester as recited in claim 2 wherein the low-side harvest transistor is an N-type metal oxide silicon (NMOS) transistor.
5. The gate-charge harvester as recited in claim 3 wherein the low-side harvest transistor and the high-side harvest transistor are N-type metal oxide silicon (NMOS) transistors.
6. An integrated power circuit comprising:
 - a low-side power transistor and a high-side power transistor coupled in series between a first pin and a second pin;
 - a gate driver coupled to provide a low-side gate control signal to a gate of the low-side

power transistor and to provide a high-side gate control signal to a gate of the high-side power transistor; and

a gate-charge harvester comprising:

a harvest capacitor having a first plate and a second plate, the second plate being coupled to a lower rail;

a first N-type metal oxide silicon (NMOS) harvest transistor having a first terminal coupled to the gate of the high-side power transistor and a second terminal coupled to the first plate; and

a second NMOS harvest transistor having a first terminal coupled to a gate of the low-side power transistor and a second terminal coupled to the first plate,

wherein the first plate is further coupled to provide a harvested voltage.

7. The circuit as recited in claim 6 wherein the gate-charge harvester further comprises:

a low-side harvest gate control signal coupled to a gate of the low-side harvest transistor, the low-side harvest gate control signal being coupled to be high during a first dead time for both a first P-type gate control transistor and a first N-type gate control transistor that drive a gate of the low-side power transistor, the first dead time occurring when the first P-type gate control transistor has been turned off and the first N-type gate control transistor has not yet been turned on; and

a high-side harvest gate control signal coupled to a gate of the high-side harvest transistor, the high-side harvest gate control signal being coupled to be high during a second dead time for both a second P-type gate control transistor and a second N-type gate control transistor that drive the gate of the high-side power transistor, the second dead time occurring when the second P-type gate control transistor has been turned off and the second N-type gate control transistor has not yet been turned on.

8. The circuit as recited in claim 7 further comprising:

a harvest regulator coupled to receive the harvested voltage and to provide a recycled logic supply voltage; and

a harvest capacitor having a first terminal coupled to the output of the harvest regulator and a second terminal coupled to a lower supply rail.

9. The circuit as recited in claim 8 further comprising:

a low-dropout regulator coupled to receive an input voltage and to provide an input logic supply voltage;

a decision circuit coupled to multiplex the input logic supply voltage and the recycled logic supply voltage and to provide a multiplexed logic supply voltage.

10. The circuit as recited in claim 9 further comprising a logic circuit coupled to receive the multiplexed logic supply voltage and a lower rail.

11. The circuit as recited in claim 10 wherein the logic circuit provides signals to respective gates of the first P-type gate control transistor, the first N-type gate control transistor, the second P-type gate control transistor and the second N-type gate control transistor.

12. The circuit as recited in claim 10 wherein the logic circuit comprises a monitoring circuit.

13. The circuit as recited in claim 6 wherein the integrated power circuit is a DC/DC boost converter.

14. The circuit as recited in claim 6 wherein the integrated power circuit is a DC/DC buck converter.

15. The circuit as recited in claim 6 wherein the high-side power transistor and the low-side power transistor are NMOS transistors.

16. The circuit as recited in claim 6 wherein the high-side power transistor is a PMOS transistor and the low-side power transistor is an NMOS transistor.

17. The circuit as recited in claim 6 wherein the gate driver comprises a PMOS transistor coupled in series with an NMOS transistor between a gate driver supply voltage and a lower rail, the gate driver supply voltage chosen to have the higher voltage from a group consisting of an input voltage and an output voltage to the circuit.

18. A DC/DC boost converter comprising:

a low-side power transistor coupled in series with a diode between a first pin and a second pin, a switch node located between the low-side power transistor and the diode being coupled to a third pin;

a gate driver coupled to provide a gate control signal to a gate of the low-side power transistor; and

a gate-charge harvester comprising:

a harvest capacitor having a first plate and a second plate, the second plate being

coupled to a lower rail; and

a low-side harvest transistor having a first terminal coupled to the gate of the low-side power transistor and a second terminal coupled to the first plate;

wherein the first plate is further coupled to provide a harvested voltage.

19. The DC/DC boost converter as recited in claim 18 wherein the gate-charge harvester further comprises:

a low-side harvest gate control signal coupled to a gate of the low-side harvest transistor, the low-side harvest gate control signal being coupled to be high during a dead time for both a P-type gate control transistor and an N-type gate control transistor that drive a gate of the low-side power transistor, the dead time occurring when the P-type gate control transistor has been turned off and the N-type gate control transistor has not yet been turned on.

20. The DC/DC boost converter as recited in claim 19 further comprising:

a harvest regulator coupled to receive the harvested voltage and to provide a recycled logic supply voltage; and

a harvest capacitor having a first terminal coupled to the output of the harvest regulator and a second terminal coupled to a lower supply rail.

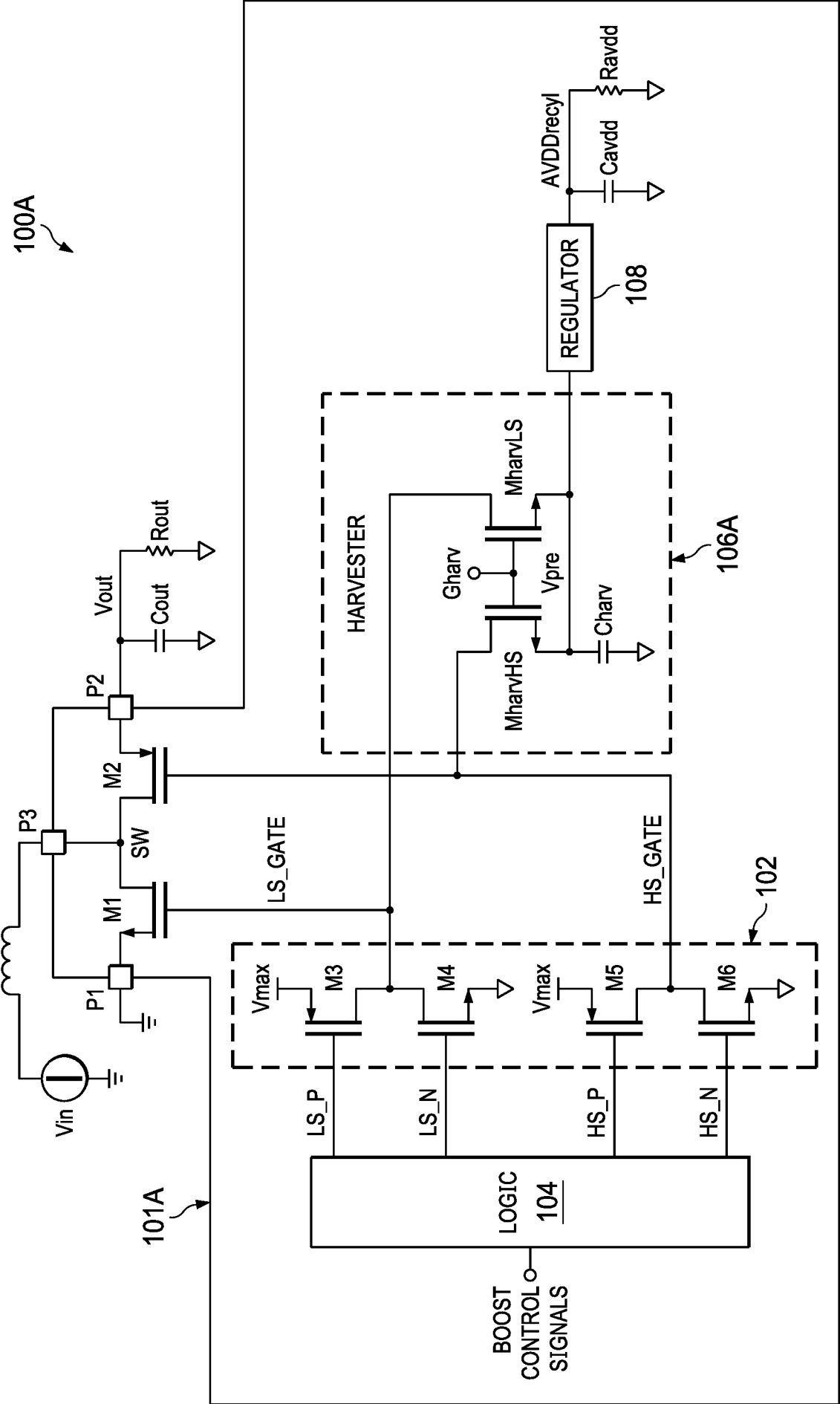


FIG. 1A

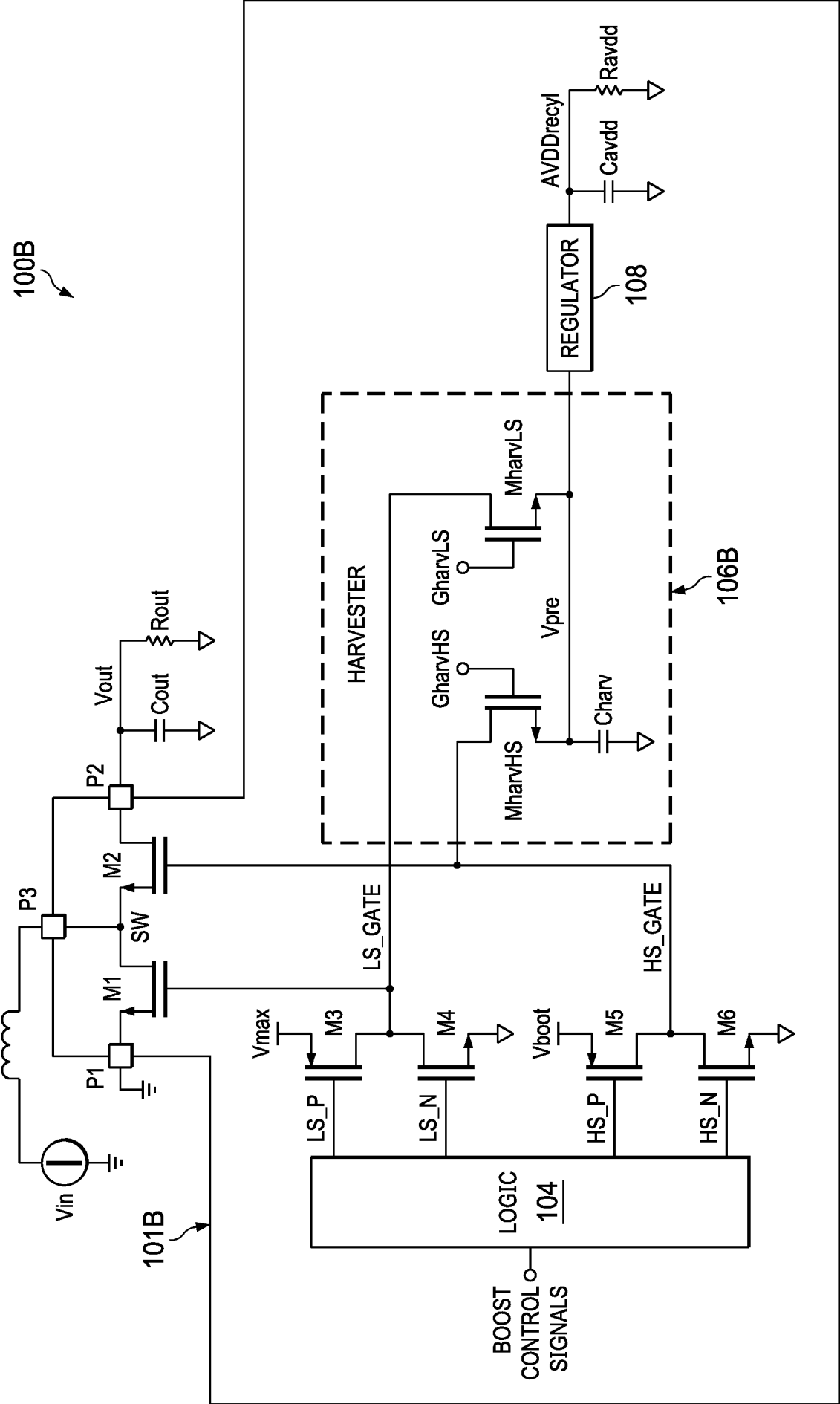


FIG. 1B

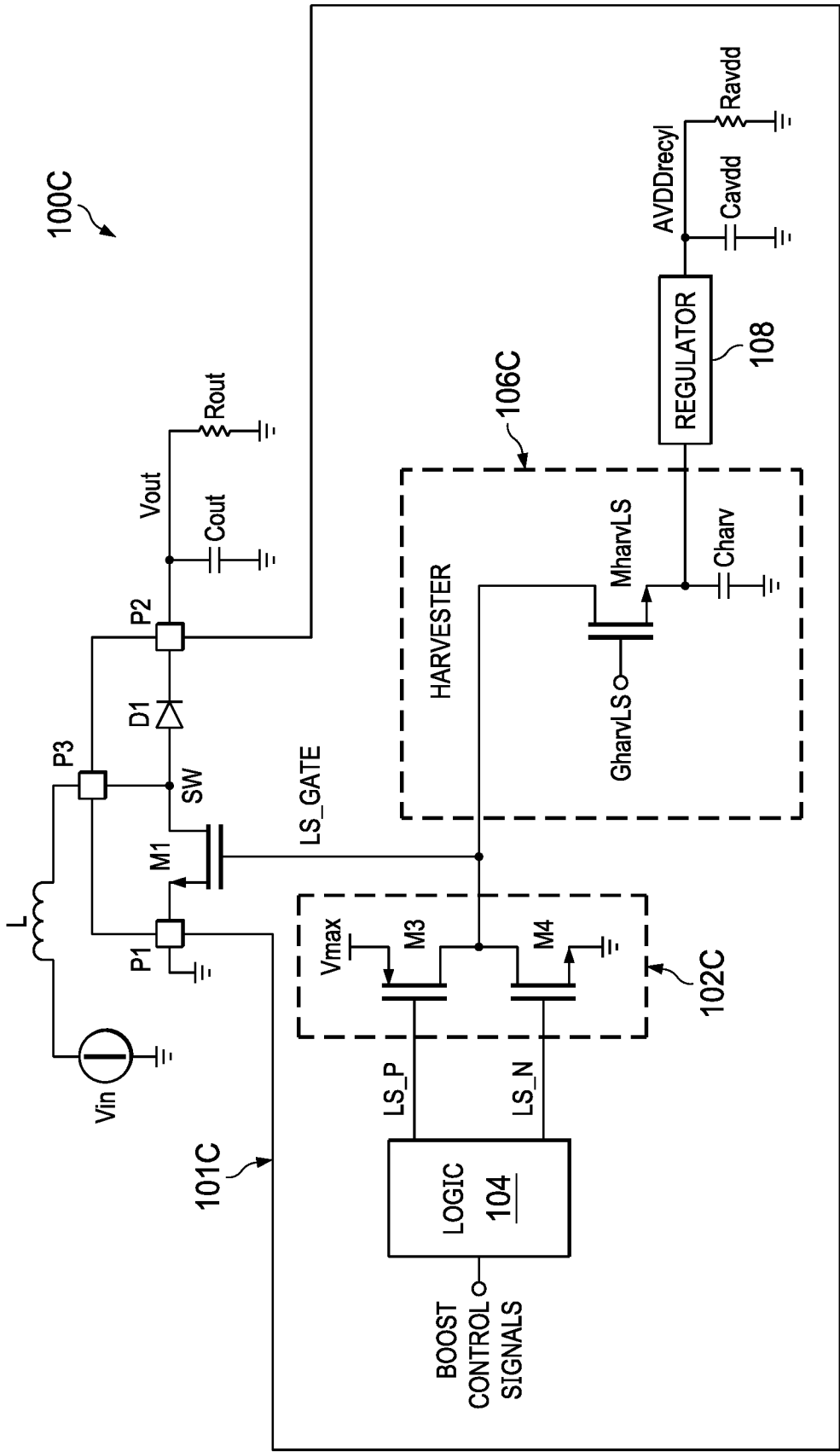


FIG. 1C

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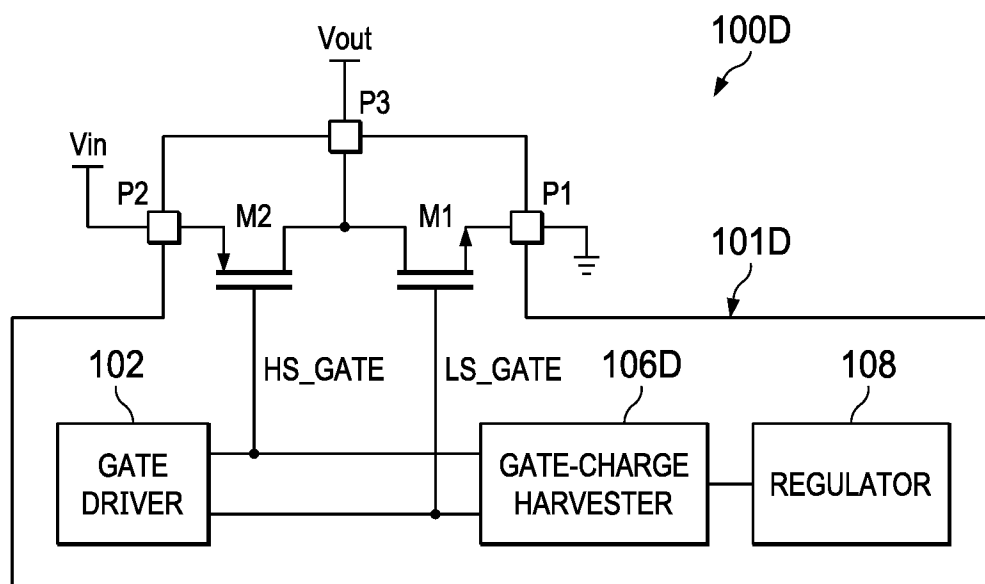


FIG. 1D

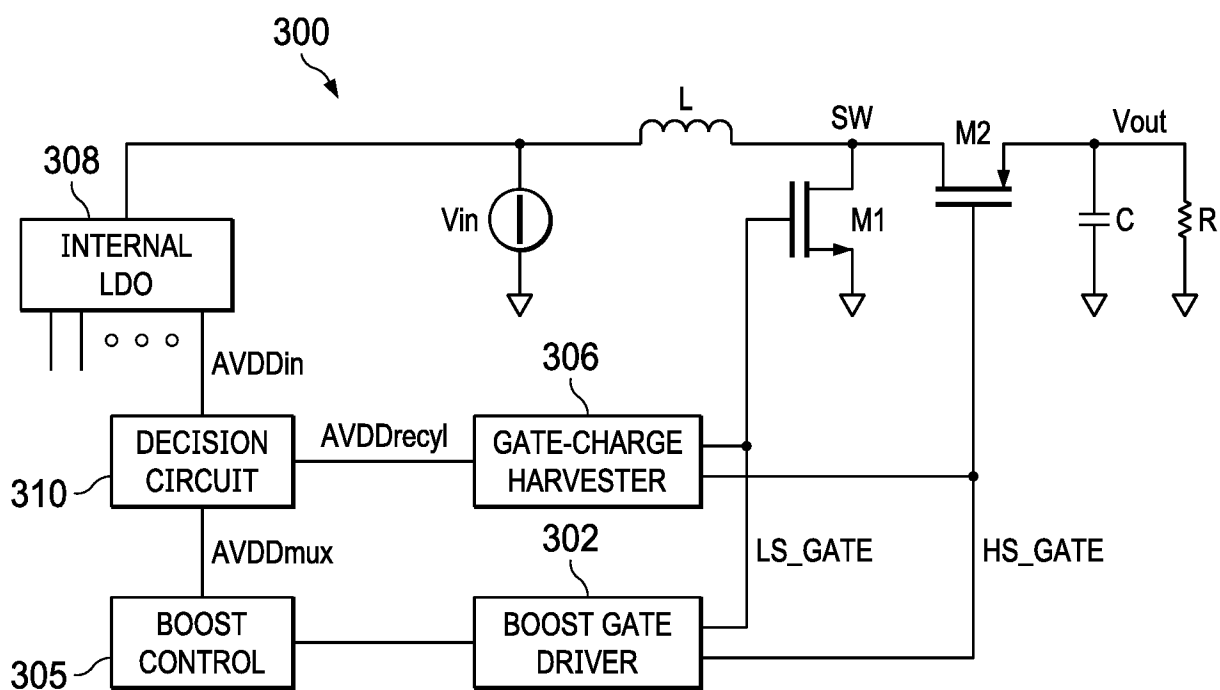


FIG. 3

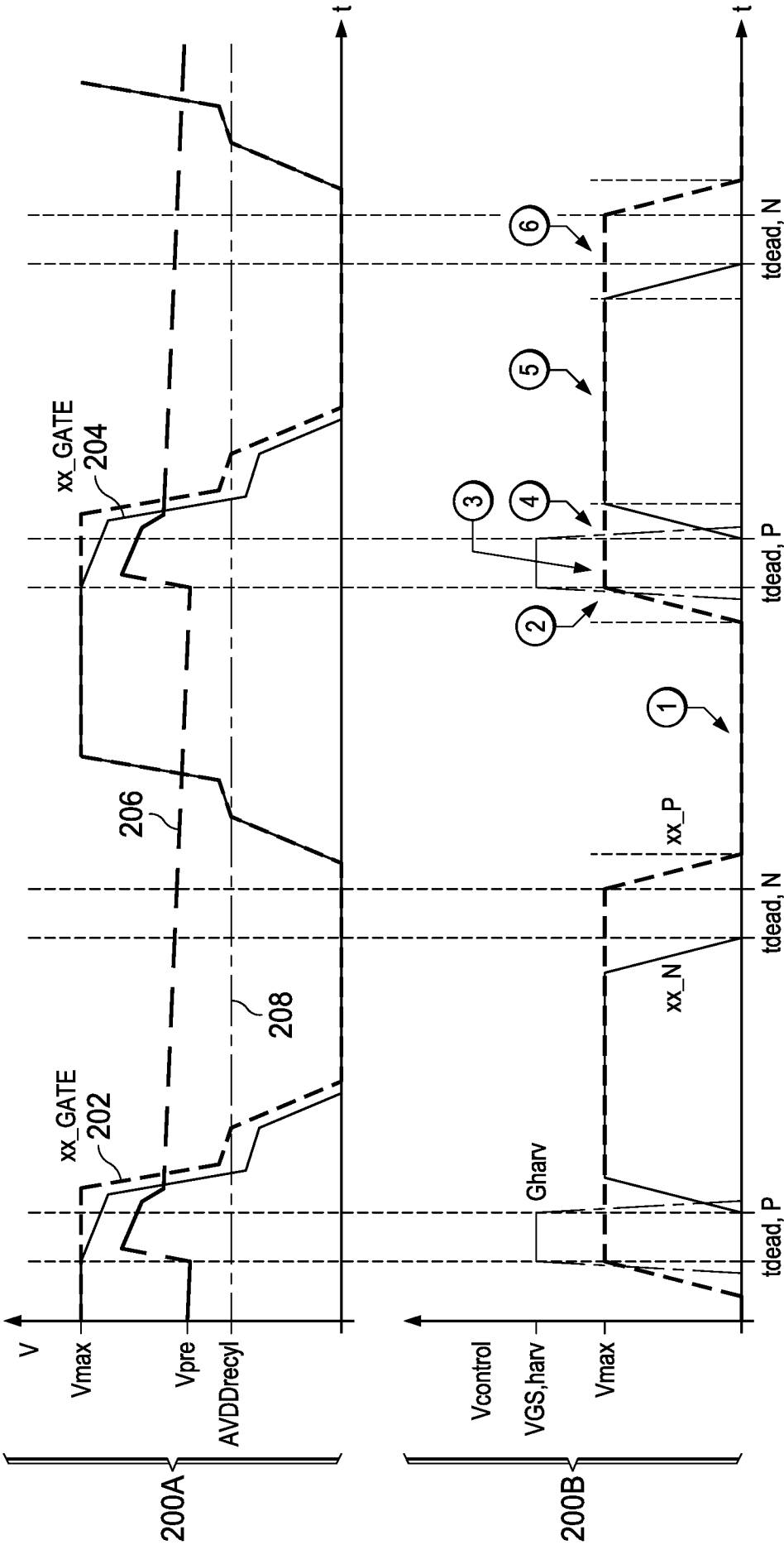
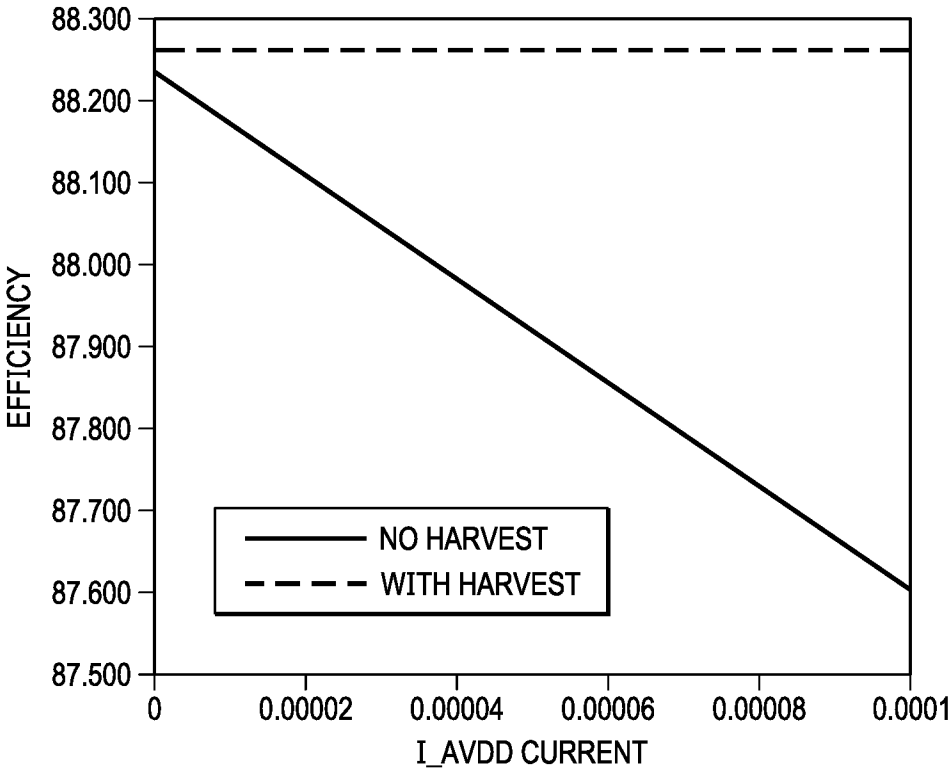


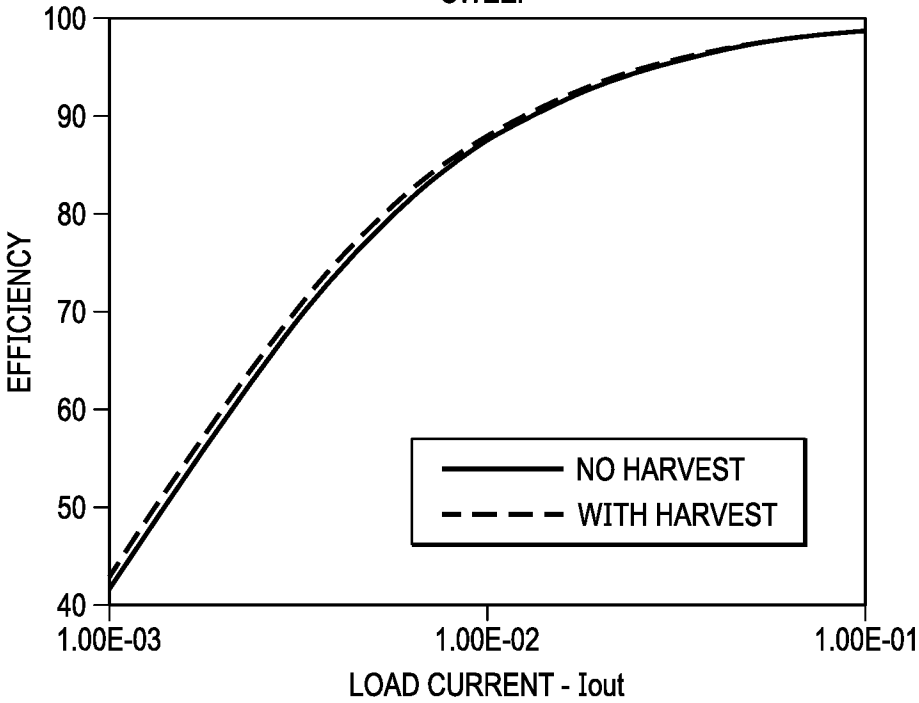
FIG. 2

FIG. 4A



EFFICIENCY SWEEP

FIG. 4B



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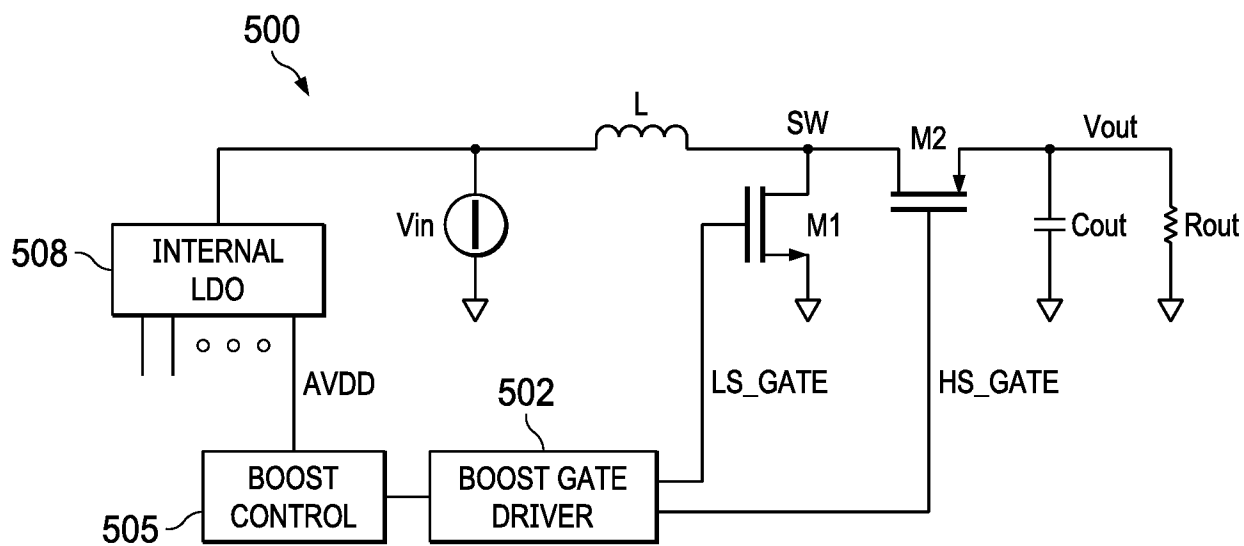
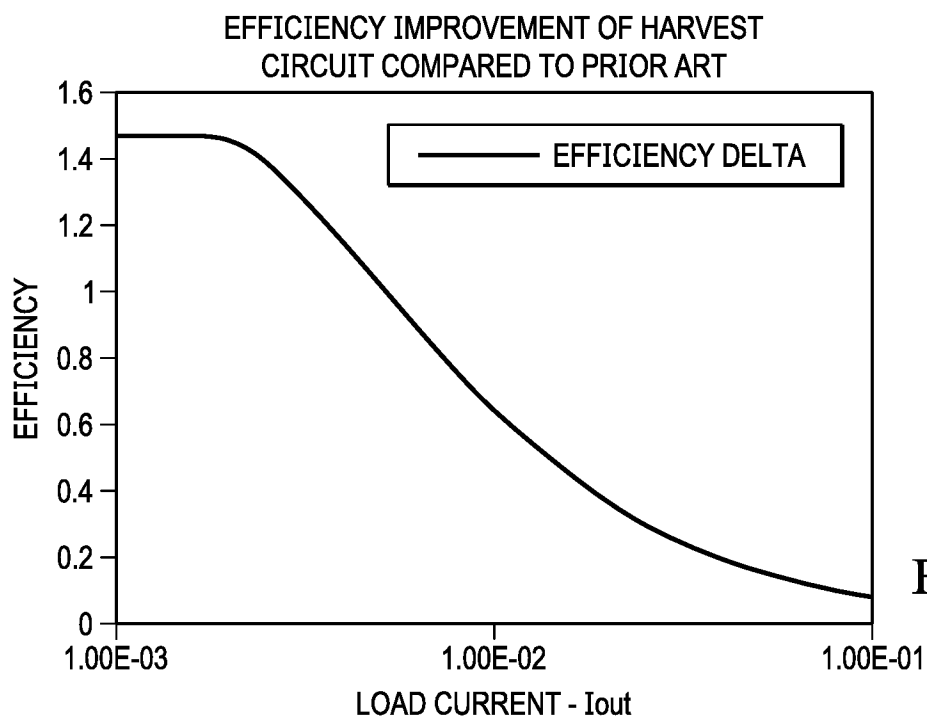


FIG. 5
(PRIOR ART)

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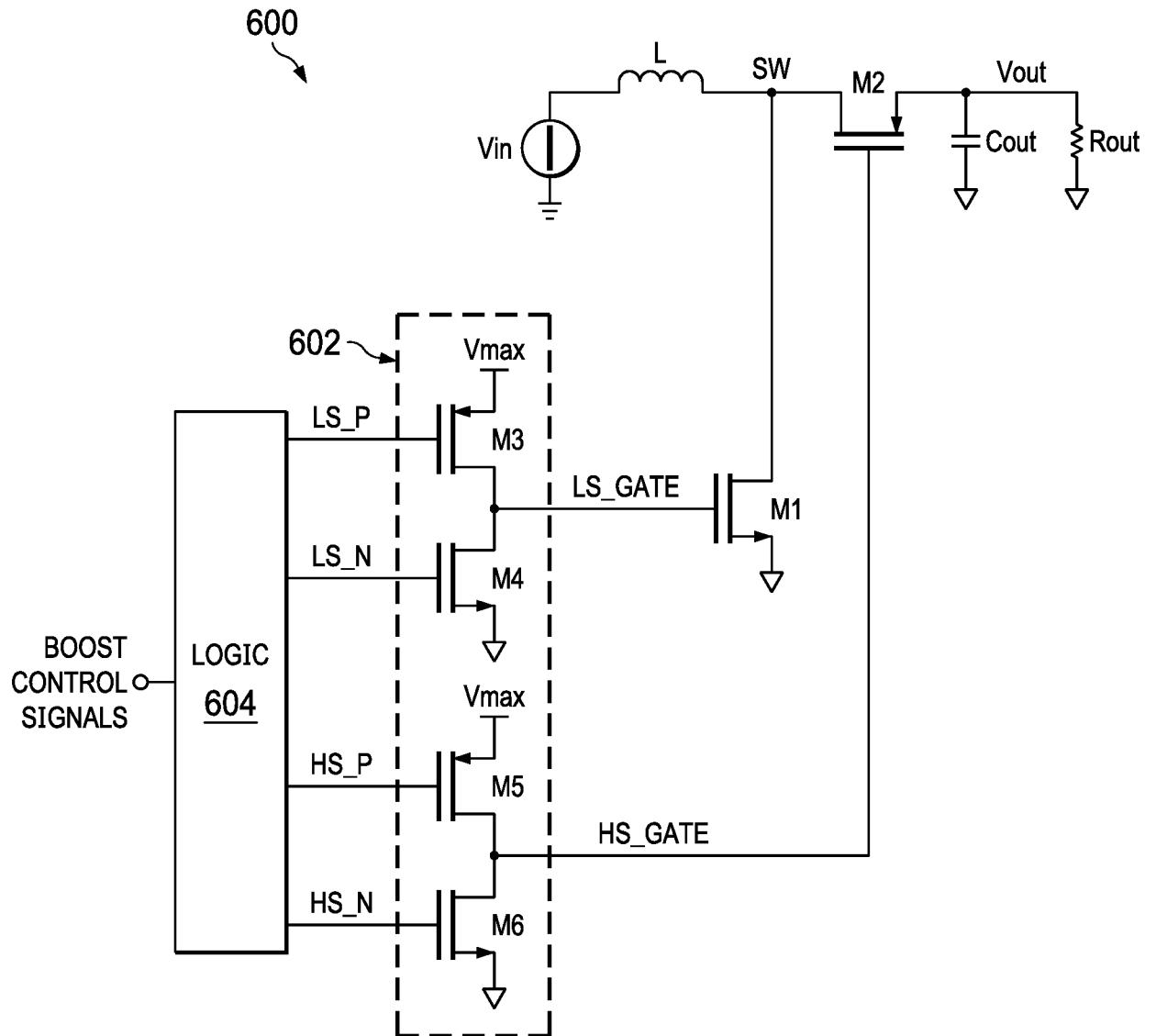


FIG. 6
(PRIOR ART)

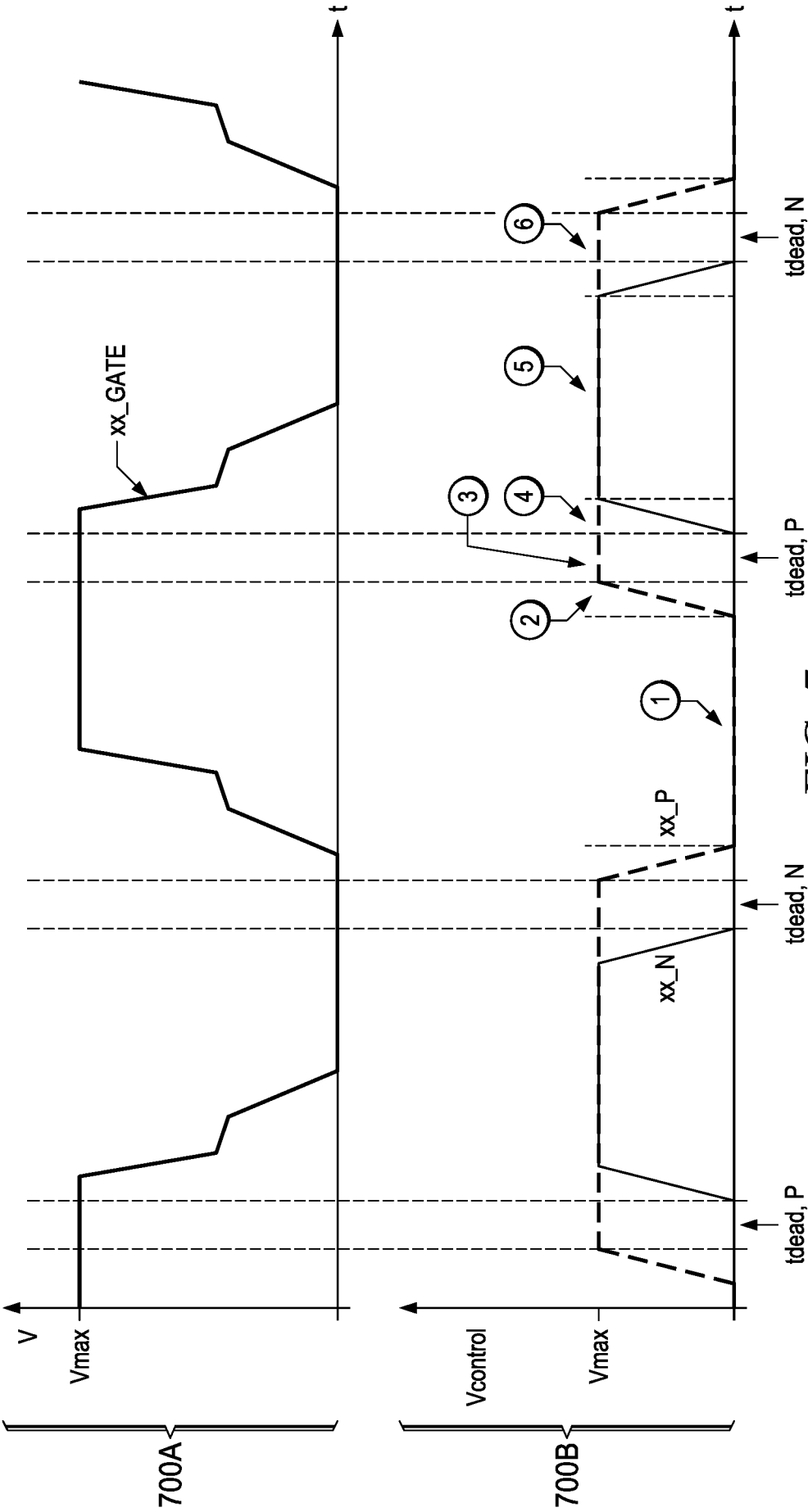


FIG. 7
(PRIOR ART)

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 2020/020732

A. CLASSIFICATION OF SUBJECT MATTER		
<i>H02M 3/158 (2006.01)</i>		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H02M 3/158, 3/18		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
PAJ, Esp@cenet, PCT online, USPTO, RUPTO, PatSearch		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2017/0133945 A1 (STMICROELECTRONICS S.R.L.) 11.05.2017	1-20
A	US 2011/0204860 A1 (TEXAS INSTRUMENTS DEUTSCHLAND GMBH) 25.08.2011	1-20
A	US 2014/0239917 A1 (STMICROELECTRONICS S.R.L.) 28.08.2014	1-20
A	US 2013/0162236 A1 (YANG ERIC) 27.06.2013	1-20
☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.		
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"O" document referring to an oral disclosure, use, exhibition or other means		
"P" document published prior to the international filing date but later than the priority date claimed		
Date of the actual completion of the international search	Date of mailing of the international search report	
04 June 2020 (04.06.2020)	04 June 2020 (04.06.2020)	
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer N. Listvina Telephone No. 499-240-60-15	