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(54) **INCREMENTING SUBTRACTIVE CIRCUITS.**

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Proceedings of the Annual International Phoenix Conference on Computers and Communications, vol. conf. 8, March 22-24, 1989, Scottsdale 1989, IEEE Computer Society Press, Washington, US, pages 49-53, Lu et al.: "A Bit-Level Pipelined Implementation of a CMOS Multiplier-Accumulator Using a New Pipelined Full-Adder Cell Design"

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Description

Field of the Invention

The present invention relates generally to digital signal processing and more particularly to incrementing subtractive circuits which are primarily intended for use in high performance integer arithmetic logic circuits such as those incorporated in digital signal processors, particularly as implemented in very large scale integrated circuits though the invention in its broadest aspects is not limited for use in such a context.

Background to the Invention

For reasons which are well established in the practice of digital signal processing, it is usually desirable to perform arithmetic computations on numbers which are represented in 2's - complement form. In such a form positive numbers are represented by a sign bit (0) and bits representing the magnitude of the number whereas a negative number has a sign bit of unity (1) and bits representing the 2's complement of the magnitude. As is well known, the 2's complement form of a number is formed by taking the 1's complement of the number, by changing each zero to a 1 and vice versa, and adding unity at the least significant bit position. The 2's complement system is very convenient for the representation of negative numbers because the operation of subtraction may be performed implicitly by the actual performance of addition.

In networks composed of 2's complement integer arithmetic operators which share a common data transmission format, there is often a requirement to maximize the use of available numerical resources. Additive operators can cause a single bit word growth, which must be counteracted by single bit arithmetic downshifting if overflow is to be avoided. Arithmetic downshifting introduces an error which can be minimized and made zero-mean by the operation of 'rounding'. Rounding is essentially the action of adding one bit (i.e. incrementing) at the significance of the discarded bit before that bit is discarded. While this is trivial to achieve in the case of an adder, with no penalty in relation to the area occupied by the circuits or time delay, it is more difficult to achieve in relation to a subtracter.

As is well known, subtraction of a number may be performed by 1's complementing the number, adding the number and then adding an incrementing bit at the least significant bit position. This requires only one carry propagation but its achievement requires the operation of incrementing. In a serial data system, the corresponding bits of two numbers which are to be added (or subtracted) are fed synchronously to an adder (or subtracter), normally starting with the least significant bit, and the incrementing is performed in response to a LSB control signal.

The present invention however concerns incrementing subtraction. Whereas simple subtraction may be represented as the formation of the quantity (A - B), incrementing subtraction may be represented as the formation of the quantity (A - B + 1) or the quantity -(A + B). The former requires an incrementing operation additional to that required for two's complementing (-B). The latter (usually termed 'negating addition') also requires an additional incrementing operation. There is therefore the considerable problem of how to provide an incrementing subtractive circuit, e.g. an incrementing subtracter or negating adder, which requires a incrementing operation additional to that necessary for simple subtraction. The difficulty arises from the existence of, apparently, only one opportunity, namely the time of the least significant bit, for incrementing.

Summary of the Invention

It is therefore one object of the invention to provide an incrementing subtractive circuit.

The invention provides an incrementing subtractive circuit for two input bit-serial signals each having a least significant bit and corresponding more significant bits, comprising a full adder; a carry recirculation loop which extends from a carry signal output of the full adder and includes a clocked delay and a means for coupling a recirculated carry signal to a carry signal input at times other than the time of the least significant bits; and means for providing a control signal at the time of the least significant bits; characterised by means coupled to the loop and responsive alternatively to said control signal and the recirculated carry signal for providing to said carry signal input of the full adder an incrementing signal by way of a clocked delay, whereby the value of the said recirculated carry signal is augmented by integer two.

In a preferred form of the invention a half-adder is included in a carry path from the carry output to the carry input of an implicit subtractor, the half adder having a recirculating carry path into which an incrementing bit is injected under least-significant bit control. As will be further explained hereinafter, the effect is to add integer two, by incrementing before the upshift operation performed by the main adder, to the carry value of the main adder.

Brief Description of the Drawings

Figure 1 illustrates a bit-serial adder by way of explanation.

Figure 2 illustrates by way of explanation an implicit subtracter comprising a modification to the adder of Figure 1.

Figure 3 illustrates one embodiment of an incre-

menting subtracter, developed from the subtracter of Figure 2.

Figure 4 illustrates a negating adder according to the invention.

Detailed Description of Preferred Embodiments

In order to explain the operation and significance of the preferred embodiments of the invention, reference will first be made to Figures 1 and 2.

Figure 1 illustrates a serial adder arranged to receive at successive clock times the corresponding bits of two digital signals at inputs A, B respectively. The adder comprises a full adder U1 having a sum output S, a carry output C and a carry input to which is connected an AND gate U2 which receives a least-significant bit control signal, which is active-low, and the recirculated carry signal. The sum and carry outputs of the adder are latched, in this embodiment by means of clocked D-flip-flops U7 and U8 respectively. For simplicity the clock inputs are omitted.

A bit serial adder assimilates two equally weighted input signals and produces their sum as an output. For each bit the sum function is not closed because the output may take the numerical value outside the binary set of values associated with its input. This requires the provision of a second output, the carry, which has to have twice the (binary) weight of the sum signal.

In a bit-parallel adding, the carry is doubled in weight by connection to the spatially successive full adder. In bit-serial operation, the doubling of the weight is achieved by coupling the carry signal to the temporally successive adder, i.e. by recirculation of the carry signal by way of a clocked delay.

The function of the AND-gate U2 is to insert a zero in the carry loop at LSB time, clearing the loop. The LSBN signal is active-low. In fact this gate U2 acts as a one bit upshifter (or 2 times multiply). The upshifting has the effect of removing the most significant bit of a carry word, replacing it with logical zero. The operation has a functional latency of -1 bit, which cancels the actual delay of the latch U8 in the carry path, thereby maintaining signal consistency. For a further explanation of the operation and significance of up-shifting, reference may be made to Smith and Denyer, 'Serial Data Computation', Kluwer Academic Press, 1988, pages 59 to 67.

From the adder circuit shown in Figure 1 one may construct a simple subtracter by including the inverter U5, inverting the control signal (LSBN) by means of, for example, an inverter U12, and changing the AND-gate U2 to an OR-gate U2', as shown in Figure 2. The inverter U5 will effect a 1's complement of the input B whereas the inversion of the control signal and the change of the AND-gate U2 to an OR-gate effectively insert a logical '1' instead of '0' at the time of the least significant bit so as to provide the incrementing bit necessary for the correct 2's complementing of the input B. This is possible because the upshifting is effectively a multiply by two operation; this provides a bottom zero which can be incremented by unity without the propagation of a carry bit.

However, such an incrementing operation can be performed only once and the same prescription cannot be used for an incrementing subtracter.

The present invention solves the problem by the addition of, effectively, integer two to the recirculated, upshifted carry signal. This addition may be achieved by an incrementation before the upshift operation.

To derive one embodiment of the invention, instead of converting the adder shown in Figure 1 to a simple subtracter, the AND-gate U2 is retained because no increment will be performed in the main adder. In order to provide the incrementation of the carry before the upshifting, the implicit subtracter is modified by the inclusion in the carry path of a half adder constituted by an exclusive OR-gate U6 and an AND-gate U3, providing a sum output and a carry output respectively. The half adder receives its own carry signal and the carry signal from the main adder and an incrementing bit is injected into the carry path of the half adder under LSB control.

In particular, the inputs to the half adder are the recirculated carry from the latch U8 and the recirculated carry from the half adder. The carry output from the gate U3 is applied to one input of an OR gate U4 which is latched by means of a clocked D-type flip-flop U9. The other input of the OR-gate U4 is an active-high LSB control signal, obtained by way of an inverter U10 from the active-low LSB control signal.

In this circuit, the incrementing bit at LSB-time is derived from the inverted LSB control signal using the OR-gate U4.

The difference in operation from that of the subtracter is that the incrementing bit is inserted before the latch U9.

Thus the extra circuitry effectively adds integer two to the carry value.

Although this circuit introduces an extra gate delay (the exclusive-OR gate U6) in the carry path, there is minimal increase in delay through the subtracter, as measured between a data or control input and the data output.

Whereas the carry path is local, in general data and control inputs originate more remotely and, owing to propagation delays, can be expected to arrive later than the carry signal. Because the logic evaluation of the extra exclusive-OR gate proceeds concurrently with the propagation of remotely generated data and control signals, its effect on overall delay is minimal. Moreover, in most realizations one of the three inputs to a full adder 'sees' a shorter path to the outputs than do the other inputs. That one input is usually the carry-input and so even if the XOR gate U6 is in the critical path (as regards full-adder inputs) there is

more slack time available while the A and B inputs are being evaluated.

The embodiment shown in Figure 4 operates in a manner similar to that shown in Figure 3. However it includes an inverter U11 for the A input of the adder, which now is configured to compute, bit-serially, the negated sum -(A + B). The incrementing bit is inserted in the same way as described in relation to Figure 3.

A negated sum can be computed using known circuits which perform two distinct carry-propagate delays, viz. adding and then negating. The present invention enables the computation of a negated sum with effectively only one carry-propagate delay. This is particulary important in high-performance digital signal processing wherein it is important to maximize the usage of the available hardware and achieve reduction in delay.

Those skilled in the art will understand that various changes and modifications may be made. In particular the various gates may be replaced by their respective logic equivalents.

Claims

1. An incrementing subtractive circuit for two input bit-serial signals each having a least significant bit and corresponding more significant bits, comprising a full adder (U1); a carry recirculation loop which extends from a carry signal output of the full adder and includes a clocked delay (U8) and a means (U2) for coupling a recirculated carry signal to a carry signal input at times other than the time of the least significant bits; and means for providing a control signal (LSBN) at the time of the least significant bits; characterised by means (U3,U6,U4,U9,U10) coupled to the loop and responsive alternatively to said control signal and the recirculated carry signal for providing to said carry signal input of the full adder an incrementing signal by way of a clocked delay (U9), whereby the value of the said recirculated carry signal is augmented by integer two.

2. A circuit according to claim 1 wherein the said carry recirculation loop includes a logic circuit (U3,U6) for providing both a sum output and a carry output in response to the recirculated carry signal of the full adder and a signal recirculated around a recirculation path (U4,U9) including said clocked delay (U9) from the said carry output, the said sum output being coupled to said carry signal input of the full adder.

3. A circuit according to claim 2 wherein the said recirculation path comprises an OR-function gate (U4) having inputs for receiving the said carry output and the said control signal.

4. A circuit according to claim 2 or 3 wherein an exclusive-OR gate (U6) provides the said sum output and an AND gate (U3) provides the said carry output.

Patentansprüche

1. Inkrementierende Subtrahierschaltung für zwei bit-serielle Eingangssignale mit jeweils einem niedrigst-wertigen Bit und entsprechend höherwertigen Bits mit einem Volladdierer (U1), einer ÜbertragsRezirkulationsschleife, die sich von einem Übertragssignalausgang des Volladdierers erstreckt und eine getaktete Verzögerungseinrichtung (U8) und ein Mittel (U2) aufweist zum Koppeln eines rezirkulierten Übertragssignals an einen Übertragssignaleingang zu anderen Zeiten als dem Zeitpunkt des niedrigstwertigen Bits, und Mittel zum Liefern eines Steuersignals (LSBN) zum Zeitpunkt des niedrigstwertigen Bits,
gekennzeichnet durch Mittel (U3, U6, U4, U9, U10), die mit der Schleife verbunden sind und abwechselnd auf das Steuersignal und das rezirkulierte Übertragssignal ansprechen, zum Lieferen eines inkrementierten Signals mittels einer getakteten Verzögerungseinrichtung (U9) an den Übertragssignaleingang des Volladdierers, wodurch der Wert des rezirkulierten Übertragssignals um die ganze Zahl zwei erweitert wird.

2. Schaltung nach Anspruch 1, wobei die Übertrags-Rezirkulationsschleife eine Logikschaltung (U3, U6) aufweist, um sowohl eine Summenausgabe als auch eine Übertragausgabe in Abhängigkeit von dem rezirkulierten Übertragssignal des Volladdierers und eines Signals zu liefern, das um einen Rezirkulationsweg (U4, U9) einschließlich der getakteten Verzögerungseinrichtung (U9) von dem Übertragausgang rezirkuliert wurde, wobei die Summenausgabe mit dem Übertragssignaleingang des Volladdierers verbunden ist.

3. Schaltung nach Anspruch 2, wobei der Rezirkulationsweg ein ODER-Funktiontor (U4) aufweist mit Eingängen zum Empfangen der Übertragausgabe und des Steuersignals.

4. Schaltung nach Anspruch 2 oder 3, wobei ein Exklusiv-ODER-Tor (U6) die Summenausgabe liefert und ein UND-Tor (U3) die Übertragausgabe liefert.

Revendications

1. Circuit soustracteur d'incrémentation pour des signaux série à deux entrées, comportant chacun un bit moins significatif et des bits plus significatifs correspondants, comprenant : un additionneur (U1) ; une boucle à circulation de report qui s'étend depuis une sortie de signal de report de l'additionneur et comprend un retardateur cadencé (U8) et un moyen (U2) pour délivrer, à une entrée de signal de report, un signal de report ayant circulé, à des instants autres que l'instant des bits les moins significatifs ; et un moyen pour fournir un signal de commande (LSBN) à l'instant des bits les moins significatifs ; caractérisé par un moyen (U3, U6, U4, U9 U10) relié à la boucle et sensible alternativement audit signal de commande et audit signal de report ayant circulé pour délivrer, à ladite entrée de signal de report de l'additionneur, un signal d'incrémentation, au moyen d'un retardateur cadencé (U9), ce par quoi la valeur dudit signal de report ayant circulé est augmentée de deux nombres entiers.

2. Circuit selon la revendication 1, dans lequel ladite boucle à circulation de report comprend un circuit logique (U3, U6) pour délivrer à la fois une sortie de somme et une sortie de report en réponse au signal de report ayant circulé de l'additionneur et un signal ayant circulé suivant un trajet de circulation (U4, U9) incluant ledit retardateur cadencé (U9) provenant de ladite sortie de report, ladite sortie de somme étant délivrée à ladite entrée de signal de report de l'additionneur.

3. Circuit selon la revendication 2, dans lequel ledit trajet de circulation comprend une porte OU (U4) ayant des entrées pour recevoir ladite sortie de report et ledit signal de commande.

4. Circuit selon la revendication 2 ou 3, dans lequel une porte OU-EXCLUSIF (U6) délivre ladite sortie somme et une porte ET (U3) délivre ladite sortie de report.

FIG. 1

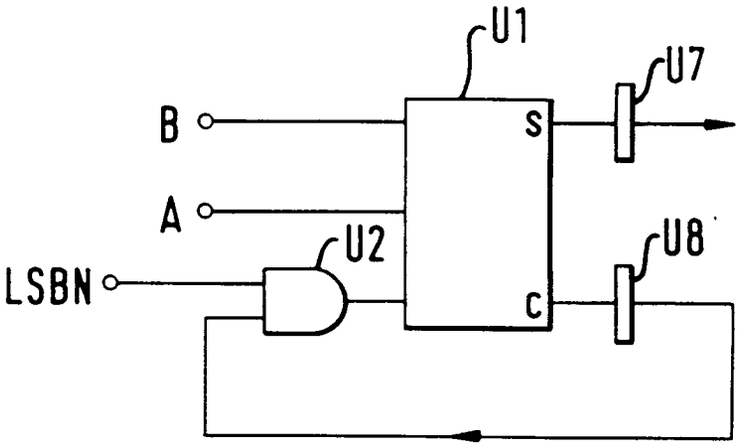
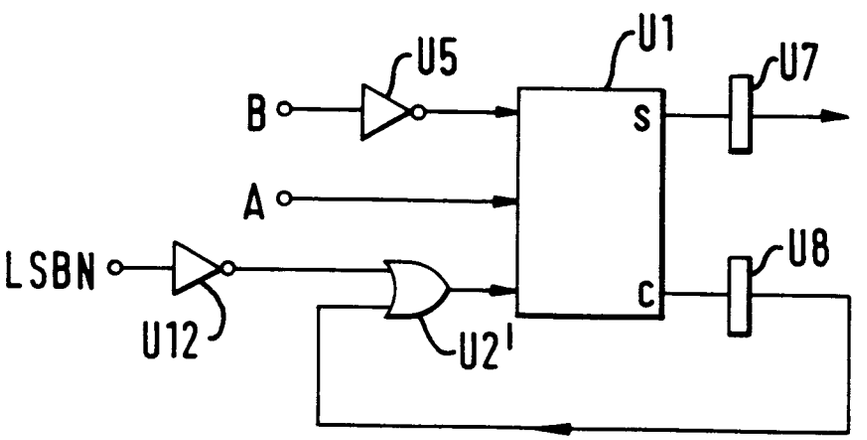


FIG. 2



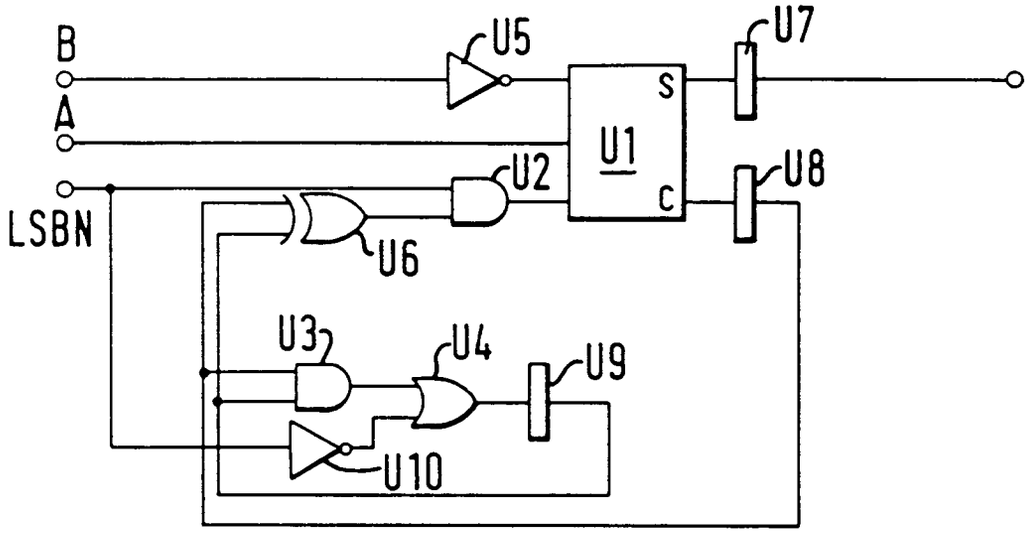

B
A
LSBN
U5
U7
U1
S
C
U2
U8
U6
U3
U4
U9
U10

FIG.3

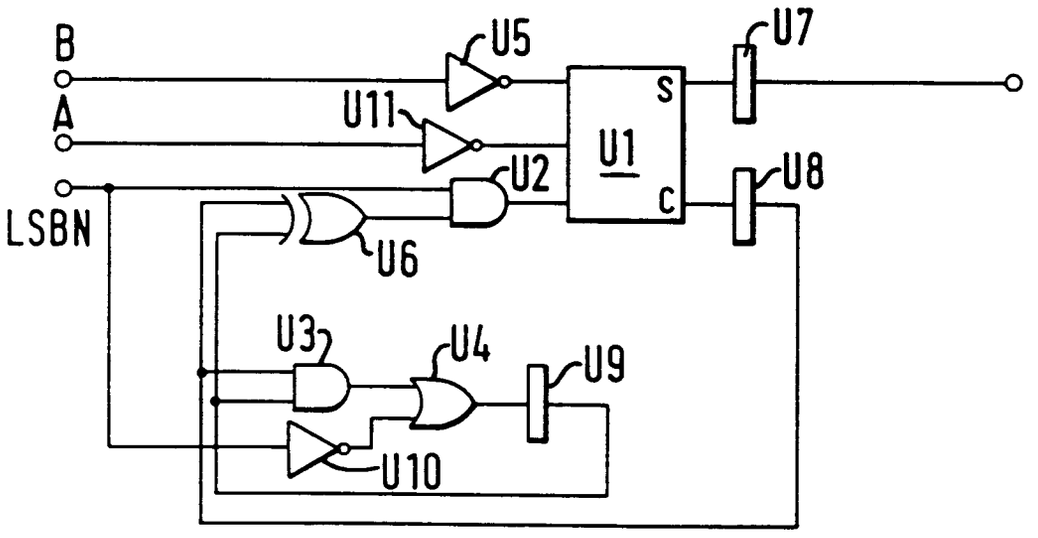

B
A
LSBN
U5
U11
U7
U1
S
C
U2
U8
U6
U3
U4
U9
U10

FIG.4