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by mesne assignments to

[54] SOLID STATE ANALOG COMPUTER-TYPE
CALIBRATOR FOR A RADIO INTERFEROMETER
6 Claims, 6 Drawing Figs.

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235/194, 235/186
[51] Int. Cl. G06g 7/22,
G06g 7/16
[50] Field of Search 235/186,
189, 190, 191, 192, 194, 195, 196, 197, 150.26,
150.27

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ABSTRACT: A solid state multiplier for an analogue computer which permits the unique determination of the bearing and elevation angles of arrival of a signal ray. The multiplier provides solutions to a set of interferometer descriptive equations corresponding to data supplied by three two-element interferometers and a central-crossed Adcock array.

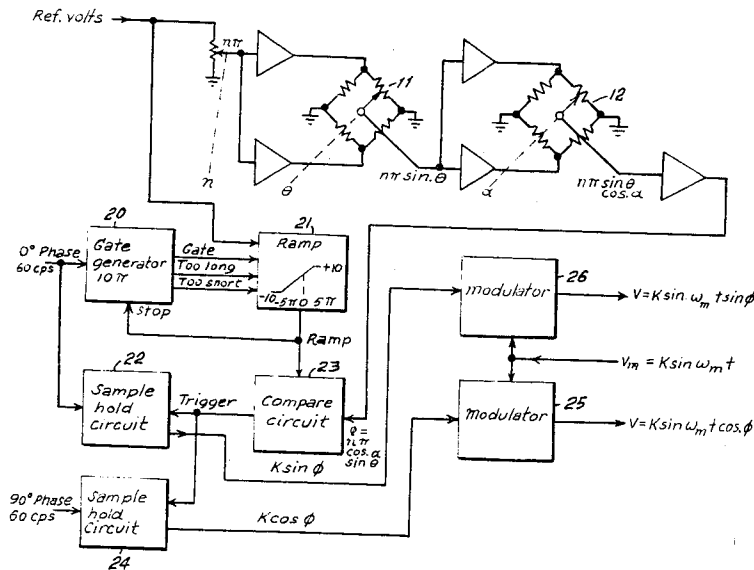


Fig. 1.

PRIOR ART

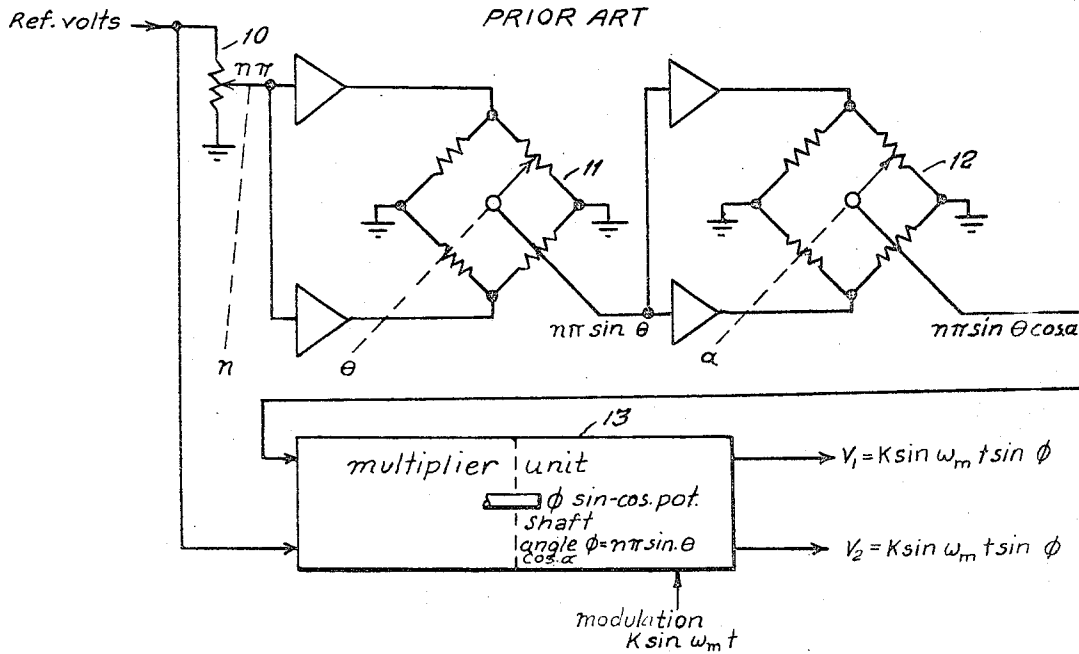
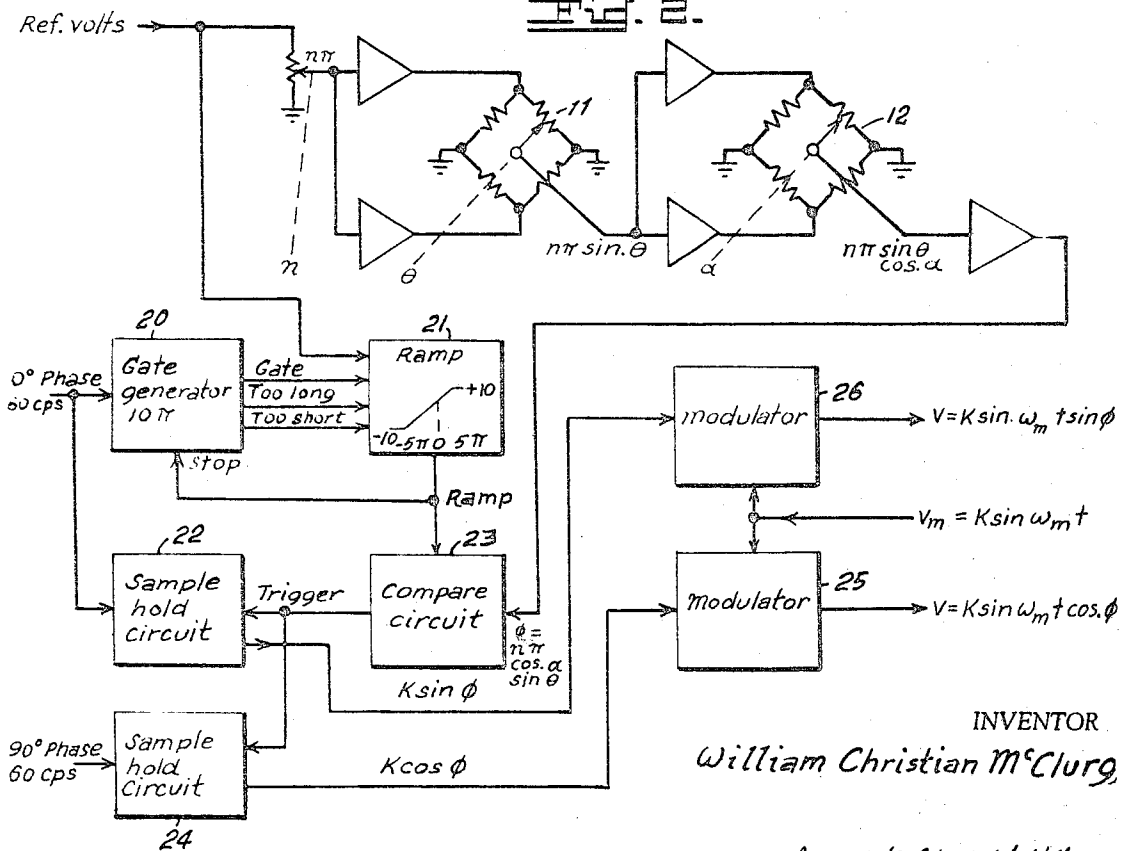


Fig. 2.

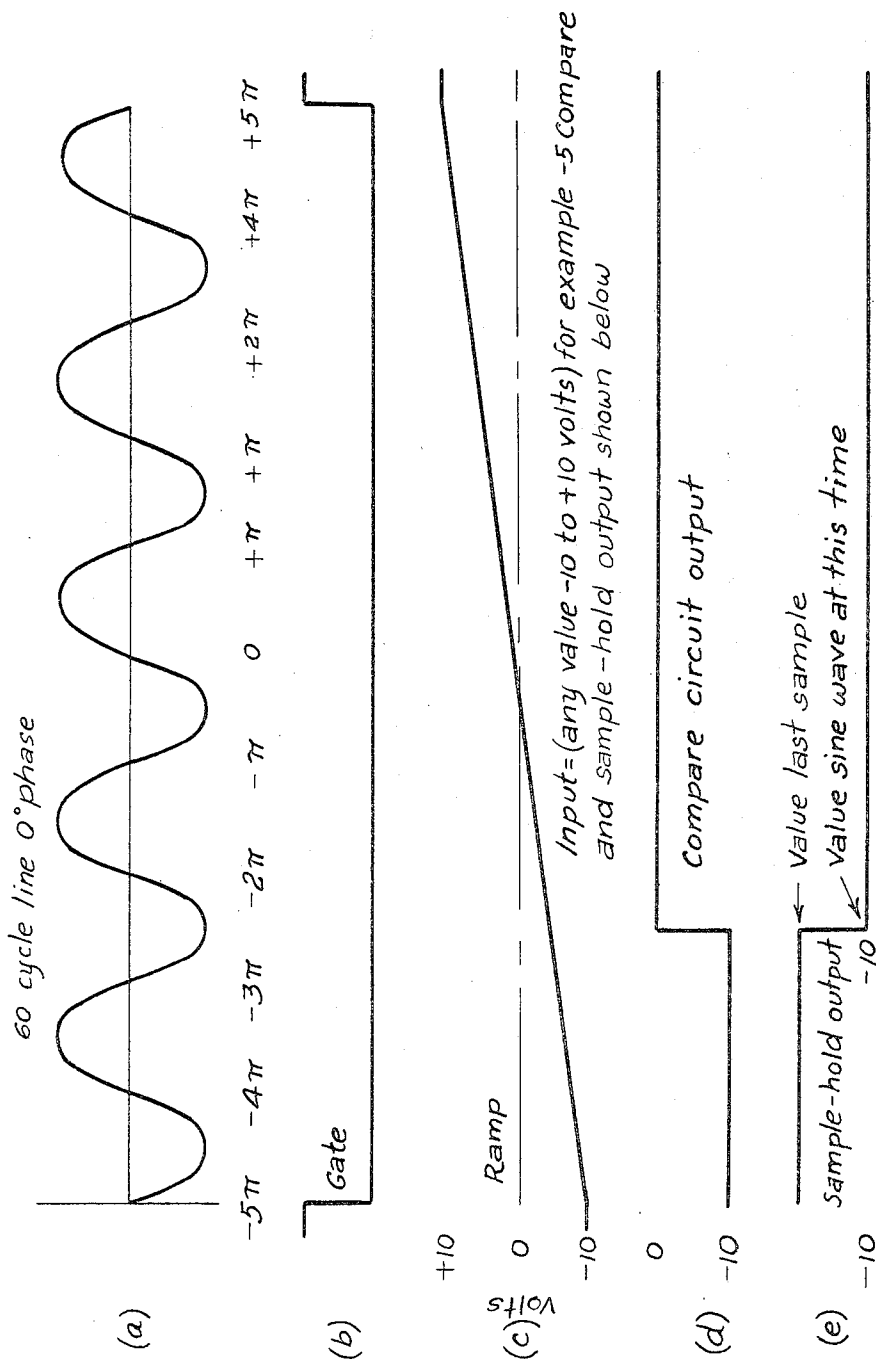


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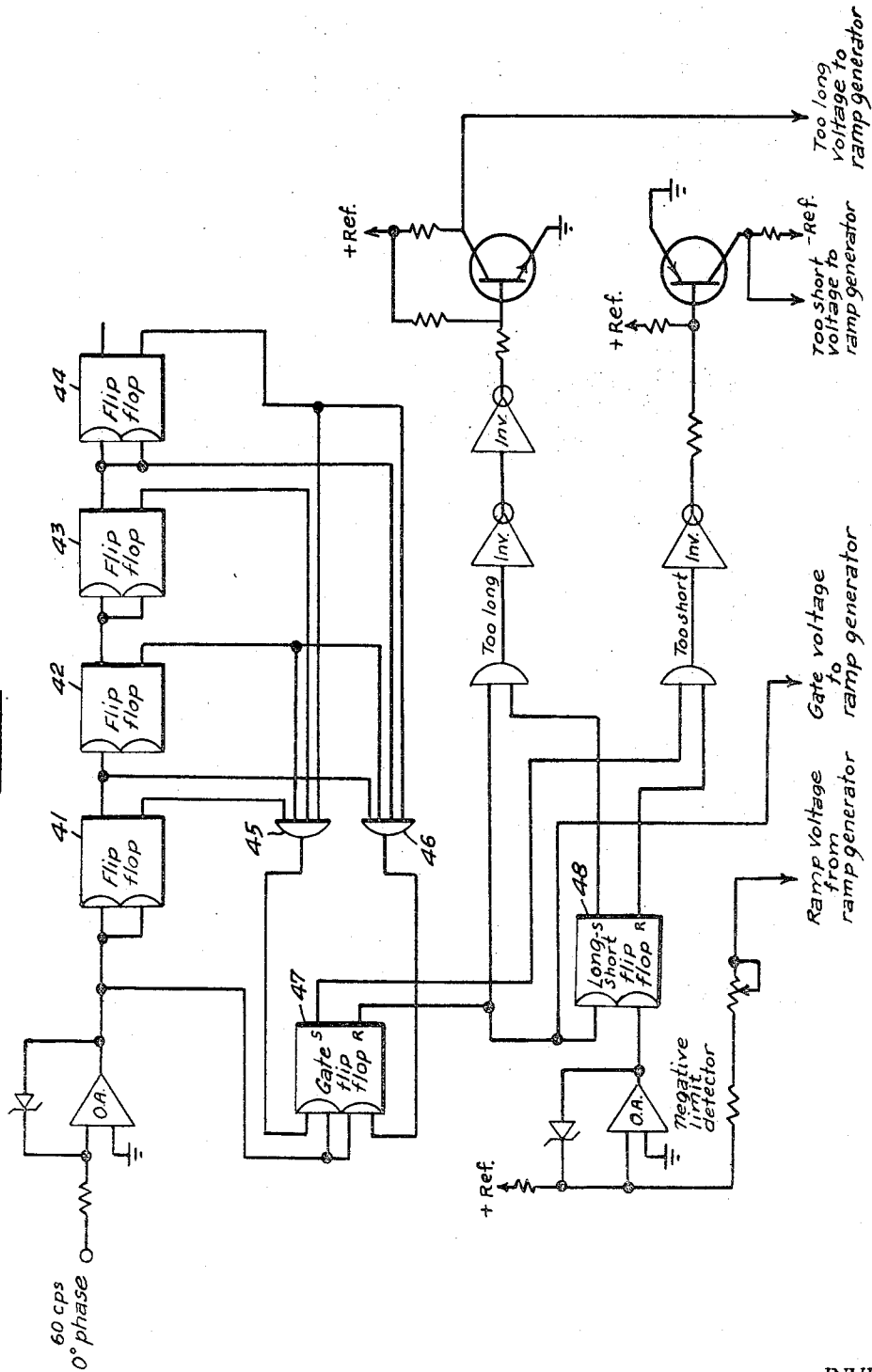
Fig. 3.



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Fig. 4.



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Fig. 5.

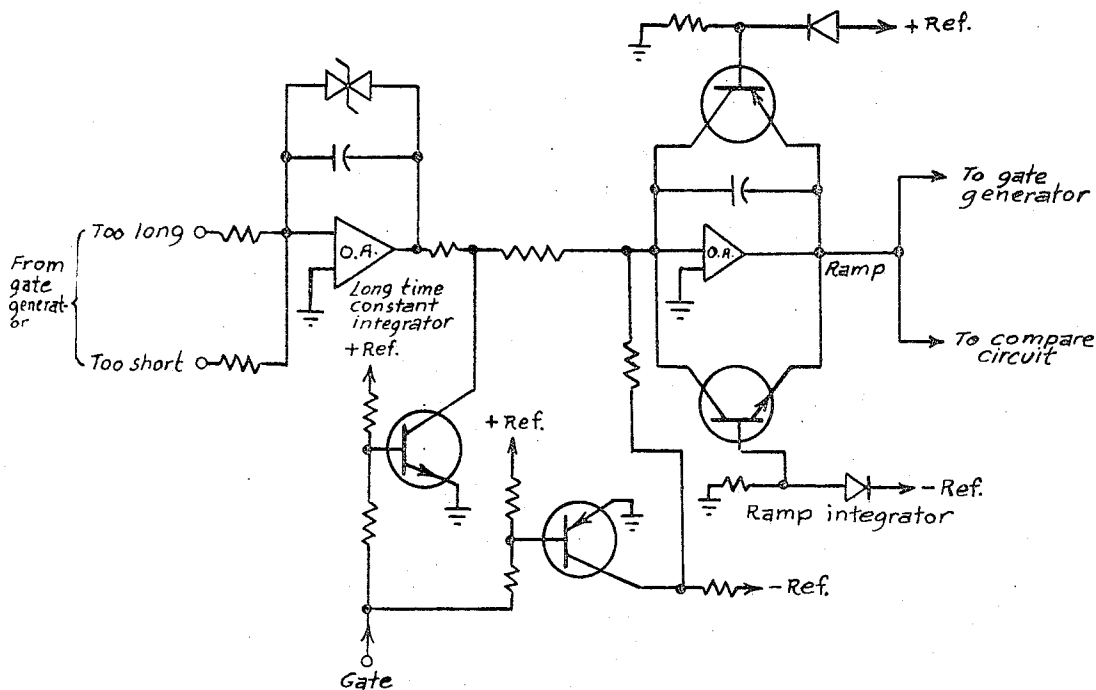
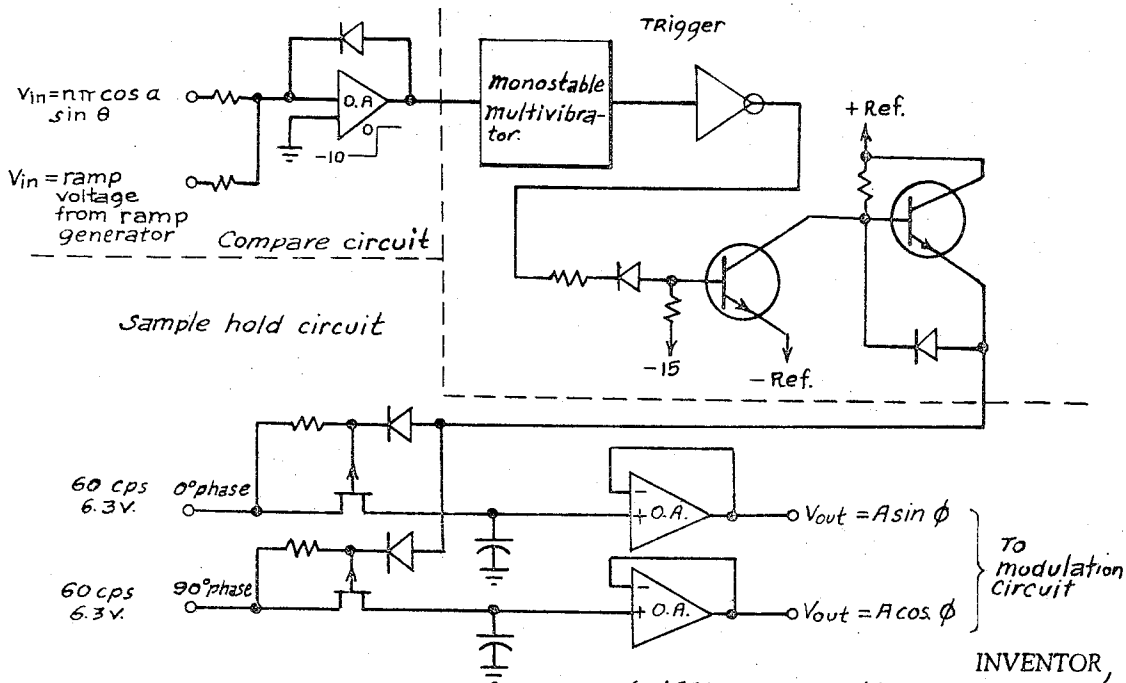


Fig. 6.



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SOLID STATE ANALOG COMPUTER-TYPE CALBRATOR FOR A RADIO INTERFEROMETER

BACKGROUND OF THE INVENTION

This invention pertains to multipliers as used in an analogue computer network and, more particularly, to an electronic multiplier for providing solutions to a corresponding set of interferometer descriptive equations.

The use of trigonometric multipliers and electronic resolvers, in the prior art, has in general presented numerous problems. In the case of electromechanical devices such as servomechanisms for driving mechanical or electrical cams and potentiometers, limitations arise due to the requirement for large, bulky, and heavy regulated high voltage power supplies. In mechanical systems, poor resolution, low reliability, and wear of moving parts become very evident limitations. Prior art devices have also included induction resolvers which utilize a driving servo, but, in this case also, limitations exist in the form of limited response of the driving servomotor.

SUMMARY OF INVENTION

It is the general purpose of this invention to provide a solid state multiplier which embraces all the advantages of the prior art electromechanical multipliers and resolvers but is considerably smaller in size, all electronic, more reliable, lighter in weight, and requires much less power to operate than its electromechanical counterparts. To attain this, the instant invention contemplates a unique circuit arrangement for integrating a gating signal to produce a linear ramp voltage. A reference input signal is compared to the ramp signal and upon coincidence of the two signals a sample and hold circuit is triggered for sampling and holding the instantaneous value of the input signal. A subsequent modulation of the sampled signal produces an output analogous to the output of the equivalent electromechanical device.

BRIEF DESCRIPTION OF THE DRAWINGS

The exact nature of this invention will be readily apparent from consideration of the following specification relating to the annexed drawings in which:

FIG. 1 shows a typical prior art electromechanical resolver as used in a mechanical analogue computer;

FIG. 2 shows the equivalent of FIG. 1 as visualized by the instant invention;

FIG. 3s a waveform diagram illustrating typical waveforms at various points in the circuit during normal operation;

FIG. 4 shows circuitry for the gate generator of FIG. 2;

FIG. 5 shows circuitry for the ramp generator of FIG. 2; and

FIG. 6 shows circuitry for the compare and sample-and-hold arrangement of FIG. 2.

DESCRIPTION OF THE INVENTION

The present invention is an electronic analogue of a wide-band high frequency radio direction finder system of the interferometer type. The system permits measurement of both the azimuthal and elevation angles of arrival of a signal ray and is a true direction finder.

The electrical output from a given two-element radio interferometer consisting of isotropic elements may be converted to an angle Φ which is a function of wavelength, angle of incidence, and angle of azimuth of the arriving ray. The value of Φ is not necessarily unique; ambiguities may be present and these need to be resolved to obtain a unique answer.

The $\Phi(n, \theta, \alpha)$ function is of a form that can be closely approximated by a product of functions in the analogue computer of FIG. 2. The philosophy that is adopted here is a system approach using electronic components that are combined in a novel way. Specifically, one knows the law of the interferometer. Hence the analogue computer of FIG. 2 can be programmed to generate the same kind of output voltage function as the radio interferometer. Two sets of outputs, one from the interferometer and another from the computer can

be displayed on the same cathode-ray oscillograph for alignment purposes. The input control dials of the computer, shown as n , θ and α in FIG. 2, can be manually adjusted so that the two displays are made to coincide. No other combination of θ and α values can produce this set of coincidences.

FIG. 2 shows a functional block diagram of an assembly of analogue computer type components which will permit the generation of the $\Phi(n, \theta, \alpha)$ functions by appropriate hand settings of the three dials labeled n , θ and α respectively. A well regulated reference voltage proportional to $n\pi$ which represents the number of radians that the interferometer base covers, is supplied to a linear potentiometer 10. Unity-gain operational amplifiers are used to interconnect in cascade the linear potentiometer 10, sine potentiometer 11, cosine potentiometer 12, and the solid state multiplier. The input to the multiplier is proportional to $n\pi \sin \frac{1}{4} \cos \alpha$, i.e. angle Φ .

As seen in FIG. 2, a balanced supply voltage is applied through operational amplifiers to a pair of diametrically opposed taps on potentiometer 11. The other pair of taps of the potentiometer is grounded. Each quadrant of the resistive element is tapered to give a sinusoidal output when a specified load is connected between the slider and ground. The output of potentiometer 11 takes the form on $n\pi \sin \theta$ and is fed to potentiometer 12 for producing a product $n\pi \sin \theta \cos \alpha$. This signal is applied to a comparator 23, shown in detail in FIG. 6, where it is amplitude compared to a ramp signal emanating from ramp generator 21. Comparator 23 functions in such a rapid manner that the input $n\pi \sin \theta \cos \alpha$ appears to be a constant DC voltage at any particular time.

The ramp signal of FIG. 3 (c), produced by ramp generator 21 and shown in detail in FIG. 5, represents the number of radians over which the interferometer base extends and covers 10π radians in the illustration shown in FIG. 3.

As shown in FIG. 2, a 60 cycle line voltage at 0° phase angle is applied simultaneously to a gate generator 20 (shown in FIG. 4) and a sample-and-hold circuit 22 (shown in FIG. 6). The gate generator 20 functions in the dual capacity of gating the ramp generator 21 for the entire desired period of the ramp signal, and should the period of the ramp signal vary either greater or less than the desired base period, appropriate corrections are initiated by the feedback circuit from the output of ramp generator 21 to gate generator 20. Detailed circuitry for this correction network is shown in FIG. 4.

The gate generator circuit 20 controls both the length and slope of the ramp. A binary divider shown in FIG. 4 comprising flip-flops 41, 42, 43 and 44 and logic gates 45 and 46 generates a gate signal 10π radians long in this particular example. The binary divider sets the gate flip-flop 47 on some arbitrary first pulse from the 60 cycle line and six pulses later resets the gate flip-flop. The long-short flip-flop 48 is set at the beginning of the gate and reset when the ramp exceeds the negative reference voltage by a small amount. The long-short flip-flop 48 is compared with the gate flip-flop 47 to generate a positive voltage of fixed value for the length of time the ramp is longer than the gate signal. Also, the same long-short Flip-flop 48 is compared with gate flip-flop to generate a negative voltage of constant value for the length of time the ramp is shorter than the gate signal. In the ramp generator of FIG. 2, a long time-constant integrator shown in FIG. 5 develops the correct output voltage such that the ramp slope is controlled to the correct value. The long-time constant integrator has a pair of inputs representing the control signal as being either too long or too short. The ramp integrator has transistors in parallel with the integration capacitor to set the ramp beginning and end point voltages to equal the reference voltage.

In the comparator of FIG. 2, the ramp signal is compared with the input voltage. When the ramp is equal to the input voltage and of opposite sign, the compare circuit output changes level. This triggers a one-shot multivibrator shown in FIG. 6 which generates a sample pulse for two field effect transistors. When the FET gate-to-source voltage is zero, the FET equivalent circuit is a simple resistance.

The modulation circuits 25 and 26 chop the sample-hold outputs and then integrate the chopped signal to form the final output voltages.

Various modifications and variations of the present invention are possible in light of the above teachings. It is therefore to be understood, that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

I claim:

1. A solid state multiplier comprising:
 - a gate generator responsive to any suitable source of alternating current, said generator effective for producing a gating signal corresponding to a predetermined number of cycles of the input AC source;
 - a ramp generator electrically connected to said gate generator, whereby a linear voltage ramp is provided at the output terminal of said ramp generator in response to and for the duration of each gating signal;
 - an analogue input signal source for providing a trigonometric representation of the bearing and elevation angles of arrival of an input signal ray;
 - a sample and hold circuit connected to the same input alternating current source as said gate generator;
 - comparator means for comparing said input analogue signal with said ramp signal and, upon detection of both signals being of equal value, for providing a trigger signal to said sample and hold circuit;
 - said sample and hold circuit activated by said trigger pulse from said comparator means for providing an output signal indicative of the phase and amplitude of said alternating current input signal at the instant the ramp signal and the analogue signal are of equal amplitude.
2. The multiplier as set forth in claim 1, further including a feedback circuit from the output of the ramp generator to the gate generator whereby the period of the ramp signal is con-

trolled both as to length and slope,

3The multiplier as set forth in claim 1, further including at least two sample and hold circuits, wherein both of said circuits are connected to be simultaneously activated upon the receipt of a trigger pulse from said comparator with each of said sample and hold circuits being connected to said source of alternating current, one circuit connected for zero degree phase angle reception and the other circuit connected for 90° phase angle reception thus providing sine and cosine functions respectively as output signals.

4. The multiplier as set forth in claim 2, further including at least two sample and hold circuits, wherein both of said circuits are connected to be simultaneously activated upon the receipt of a trigger pulse from said comparator with each of said sample and hold circuits being connected to said source of alternating current, one circuit connected for zero degree phase angle reception and the other circuit connected for 90° phase angle reception thus providing sine and cosine functions respectively as output signals.

5. The apparatus as set forth in claim 3, wherein the gating signal produced by the gate generator is of rectangular form, said analogue input signal takes the form of $n\pi \cos \alpha \sin \theta$ where $n\pi$ represents the wavelength or number of radians over which the interferometer base covers and the angles α and θ represent respectively, the angle of incidence and angle of azimuth of an input ray to the interferometer.

6. The apparatus as set forth in claim 4, wherein the gating signal produced by the gate generator is of rectangular form, said analogue input signal takes the form of $n\pi \sin \theta \cos \alpha$ where $n\pi$ represents the wavelength or number of radians over which the interferometer base covers and the angles α and θ represent respectively, the angle of incidence and angle of azimuth of an input ray to the interferometer.

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