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[Continued on next page]

(54) **Title:** ADJUSTABLE-RESISTOR ARRAY TYPE CIRCUIT OF A SEMI-DIGITAL RATIOMETRIC FINITE IMPULSE RESPONSE DIGITAL-TO-ANALOG CONVERTER (FIRDAC)

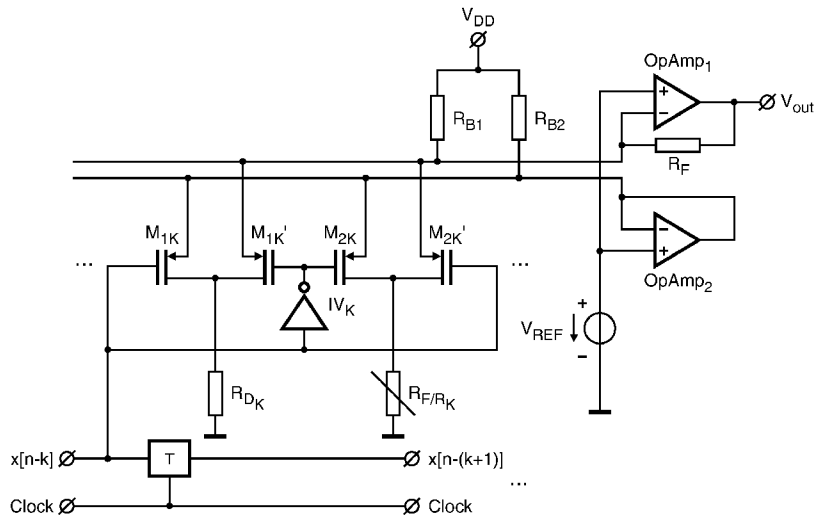

FIG. 7

(57) **Abstract:** The present invention refers to an adjustable-resistor arraytype circuitof asemi-digitalratiometric finite impulse response digital-to-analog converter (FIRDAC). The proposed FIRDAC provides an output voltage (V out) having an accurate and linear 5 relation to the circuit s supply voltage (V DD). This is accomplished by using a linear adaptive finite impulse response (FIR) filter whose weighting coefficients (a 1, a 2,, a k,, a N) are implemented by means of an array of adjustable ohmic resistors (R FIR 1, R FIR 2,, R FIR k,, R FIR N). The accuracyofconversion can easily be enhanced by additionally applying dynamic element matching techniques. This is less sophisticated than in con-10 ventionalFIRDACs known from the prior art, which are based on a weighted current approach. Furthermore, the present invention proposes a semi-digital circuit implemen- tation which enables the use of low-voltage transistors in an adjustable-resistor array type FIRDAC whose supply voltage (V DD) is allowed to exceed the breakdown voltage ofintegrated low-voltage transistors which are used for switching said ohmic resistors (R FIR 1, R FIR 2,, R FIR k,, R FIR N), which will result in a smaller chip size. Another aspect ofthe present invention is directed to the circuit design of aFIRDAC which employs an arrayofdummy resistors (R D 1, R D 2,, R D k,, R D N) whose resistance values are chosen such that the FIRDAC circuit s supply current is independent of the digital data stream (x[n]) to be converted to the analog domain. In this way, the analog output voltage (V out) ofthe FIRDAC circuit is less sensitive to a varying series impedance in its supply leads.

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Adjustable-Resistor Array Type Circuit of a Semi-Digital Ratiometric Finite Impulse Response Digital-to-Analog Converter (FIRDAC)

FIELD OF THE INVENTION

The present invention refers to an adjustable-resistor array type circuit of a semi-digital ratiometric finite impulse response digital-to-analog converter (FIRDAC). The proposed FIRDAC provides an output voltage having an accurate and linear relation to the circuit's supply voltage. This is accomplished by using a linear adaptive finite impulse response (FIR) filter whose weighting coefficients are implemented by means of an array of adjustable ohmic resistors. The accuracy of conversion can easily be enhanced by additionally applying dynamic element matching techniques. This is less complicated than in conventional FIRDACs known from the prior art, which are based on a weighted current approach. Furthermore, the present invention proposes a semi-digital circuit implementation which enables the use of low-voltage transistors in an adjustable-resistor array type FIRDAC whose supply voltage is allowed to exceed the breakdown voltage of integrated low-voltage transistors which are used for switching said ohmic resistors, which will result in a smaller chip size. Another aspect of the present invention is directed to the circuit design of a FIRDAC which employs an array of dummy resistors whose resistance values are chosen such that the FIRDAC circuit's supply current is independent of the digital data stream to be converted to the analog domain. In this way, the analog output voltage of the FIRDAC circuit is less sensitive to a varying series impedance in its supply leads.

BACKGROUND OF THE INVENTION

Converting digital signals to analog signals and vice versa is an important task in electronic signal processing. Digital-to-analog conversion thereby stands for a process in which digital words are applied to the input port of a digital-to-analog converter (DAC), the latter being required for scaling a given reference voltage V_{REF} in such a way that the obtained result yields an analog output voltage V_{out} which constitutes an analog representation of the respective digital word. To be more precise, an M-bit digital word D is mapped to an analog output voltage V_{out}, where V_{out} is given by a

real-valued proper fraction κ of a reference voltage V_{REF} as indicated by the equation $V_{out} = \kappa \cdot V_{REF}$ [V] (with $0 \leq \kappa \leq 1$) and κ is defined by the input word D. The number of input combinations represented by the input word D is thus given by 2^M. From equation (1a) it follows that the maximum value of a DAC's output voltage V_{out} is limited by the value of reference voltage V_{REF}. For an M-bit input word D, fraction κ can be determined by calculating

$$\kappa = \frac{D}{2^M}. \quad (1a)$$

For a given reference voltage V_{REF} and said M-bit word D, wherein D can be written as

$$D = \sum_{m=0}^{M-1} b_m \cdot 2^m \quad (1b)$$

with M being the total number of bits of this digital word D and b_m (with $b_m \in \{0, 1\}$) being its m-th binary coefficient of digital word D, analog output voltage V_{out} can be expressed as

$$V_{out} = \underbrace{K \cdot D}_{=\kappa} \cdot V_{REF} \text{ [V] with } K := \frac{1}{2^M}. \quad (1c, d)$$

By combining equations (1b) and (1c), analog output voltage V_{out} is thus given as

$$V_{out} \propto V_{REF} \cdot \sum_{m=0}^{M-1} b_m \cdot 2^m . \quad (1e)$$

D/A converters typically operate by a resistor, capacitor divider, or current steering method to convert digital-to-analog signals or, operate using a sigma-delta conversion method. The basic architecture of a DAC comprises a voltage reference, which can be

supplied externally, binary switches, a scaling network, and an output amplifier. The voltage reference, binary switches, and scaling network convert the digital word as either a voltage or current signal, and the output amplifier converts this signal to a voltage signal that can be sampled without affecting the value of conversion. Sigma-delta D/A converters are often preferred because of their inherent feasibility to be manufactured as integrated circuits in standard digital integrated circuit processes.

Many D/A converters utilize oversampled digital data output from an interpolation circuit, which is then converted by DAC circuitry into an analog output. Sigma-delta D/A converters inherently introduce noise outside the passband of the D/A converter circuit. To alleviate this out-of-band noise, various filtering techniques are employed.

Oversampled D/A converters generally include the following signal processing blocks: (1) an interpolator filter, or series of filters, which raises the sample rate of the incoming digital signal to a higher sample rate, (2) a digital sigma-delta processor (or noise shaper) which lowers the number of bits representing the signal by shaping the quantization noise in a way that places most of it at higher frequencies, (3) a D/A converter which converts the output of the noise shaper into an analog signal, and (4) an analog low pass filter which removes, or substantially lowers, the noise that was placed at higher frequencies by the noise shaper.

In all sigma-delta D/A converters, there exists a need to filter the high frequency noise inherent to this method of conversion. Digital noise shaper typically provide a one-bit digital output signal which is converted to an analog signal by using switched capacitor techniques or switched current source techniques. Once this conversion is made, filtering of the high frequency noise is then accomplished through a variety of means. Over the past two decades, sigma-delta analog-to-digital converters (ADC) and digital-to-analog converters (DAC) have become widely available, such as e.g. for low-frequency applications such as high-fidelity audio.

For implementing such a filtering procedure as a non-recursive filter (which means as a finite impulse response filter, FIR), said filter being post-connected

to a sigma-delta D/A converter as described above and realized by a semi-digital circuit implementation, a tapped delay line or shift register as described in US 5,995,030 may be used. Thereby, weighted and time-delayed versions of a digital input stream are summed together, thus yielding an analog output voltage which represents said digital input stream. Thereby, an array of current sources may be employed for providing a number of output currents that represent the filter coefficients of the FIR filter which are to be multiplied with the time-delayed versions of the digital input stream at the taps of shift register. As disclosed in US 5,995,030, the output currents of each current source may be adjustable such that a desired FIR filter response can be achieved. These output currents are then provided, or steered, to a current summing node or to an alternative current summing node, depending on the logic state of the control bit at the delay line tap associated with each current source. The currents at one or both of the current summing nodes are then converted to a voltage by using standard current-to-voltage conversion techniques. Additional filtering may then be employed to remove high-frequency noise.

Alternatively, FIR coefficients may be represented as charges which are stored on a plurality of capacitors. The charge on each capacitor can then be summed by employing a switched capacitor summing amplifier. Once again, additional filtering may be employed to remove any extremely high frequency noise.

In another semi-digital filtering scheme known from the prior art, the FIR coefficients may be represented as currents flowing through an array of ohmic resistors. Thereby, each resistor is selectively connected to a voltage reference depending on the state of the individual control bit from the delay line tap associated with each individual resistor. The current is then summed and converted to a voltage by means of a feedback resistor in the feedback line of a negative-feedback operational amplifier. As discussed in the previous sections, additional filtering may be employed to remove high-frequency noise.

Current steering semi-digital FIR filters utilize current paths having linear resistors, or resistive elements such as FETs or CMOS transmission gates biased in the linear region. This results in relatively low output impedance of a FIR filter's resis-

tive elements. Any offset on inputs to an operational amplifier connected to the current paths in the prior filter circuits may cause an error term. Since the current through each path depends on the resistance of the resistive element in each path, the state of the switches and the operational amplifier offset, the filter coefficients of the FIR filter, as determined by the current in each path, may be given by a function of the operational amplifier offset.

In US 5,323,157 A, a sigma-delta digital-to-analog converter is described that receives oversampled input data representative of an analog signal, wherein said data may optionally be interpolated to a higher rate by means of an interpolator. A noise-shaping sigma-delta modulator connected to the output port of the interpolator provides an output signal which is fed to a linear adaptive finite impulse response (FIR) filter having a frequency response characteristic that reduces shaped noise having a tendency to inter-modulate back into the DAC's passband as well as aliased components. The filter thereby uses a series of flip-flops functioning as delay elements with well-controlled timing edges. The time-delayed output signals of these concatenated flip-flops are used for controlling a set of current sources whose DC output currents are weighted corresponding to the linear adaptive finite impulse response filter's coefficients. The weighted DC currents supplied by these current sources are then summed and transformed into an analog output voltage.

SUMMARY OF THE INVENTION

Aside from depending on the FIRDAC's digital input stream $x[n]$, in some applications it is also required that the analog output voltage V_{out} of a FIRDAC is given by a linear ratio of its supply voltage V_{DD}. This property is often described as the output voltage V_{out} being ratiometric to the supply voltage. In a switched current source type FIRDAC implementation as known from the prior art where the filter coefficients $\{a_k \mid k \in \{0, 1, 2, \ldots, N\}$ of the FIRDAC's integrated finite impulse response filter are generated by adjustable DC output currents of a set of switchable current sources, wherein said output currents are summed at the inverting input of an output-sided inverting operational amplifier circuit and converted to an analog output voltage V_{out}

through a conversion resistor R_F (see Fig. 4), this requirement could be fulfilled if the sum of output currents I_{P1}, I_{P2}, ..., I_{PN} and I_{N1}, I_{N2}, ..., I_{NN} of all current sources is made proportional to the FIRDAC's supply voltage V_{DD}. This could be achieved by using an additional voltage-to-current converter, which converts supply voltage V_{DD} into a reference current I_{REF}. The current sources in the filter taps then should become scaled copies of the reference current. A disadvantage of this approach is that the accuracy of the supply-voltage-to-output-voltage conversion is limited by the matching of the current sources and by the matching of the voltage-to-reference-current converter and the currents-to-voltage converter at the output. To overcome these matching limits, dynamic element matching techniques are often applied. In a FIRDAC implementation which is based on using switchable current sources, however, it is not trivial to implement such a dynamic element matching strategy.

An exemplary embodiment of the present invention is therefore directed to a semi-digital FIRDAC implementation where the filter coefficients are implemented by adjustable ohmic resistors instead of switchable current sources with adjustable output currents. The FIRDAC's output voltage can thus be made ratiometric to its supply voltage. When using ohmic resistors as filter coefficients, the accuracy of conversion from supply voltage to output voltage depends on less variables than in a switched current source type FIRDAC. Moreover, in a FIRDAC with adjustable ohmic resistors realizing said filter coefficients it is easier to apply dynamic element matching techniques to increase accuracy.

To be less susceptible to a varying series impedance in the supply leads, it is desired to have a signal-independent supply current. This may be realized by implementing an array of dummy resistors, whose resistance values are respectively equal to the resistance value of a corresponding one of filter resistors, and by driving these resistors by the bit-inverse signal. This leads to the advantage that the circuit is less susceptible to a varying series impedance in its supply leads.

In modern CMOS processes, transistors with different voltage handling capability can be distinguished. Typically, low-voltage transistors consume less chip area than their high-voltage counterparts. A problem of the ratiometric DAC according to the above-described embodiment is the fact that the FIRDAC's supply voltage is often much higher than the voltage tolerated by low-voltage transistors. This would imply that an inverter stage, which has to be used at every tap of the FIR filter, would have to be realized by means of high-voltage transistors, which consequently results in a large IC size.

Using adjustable ohmic resistors whose resistance values constitute the filter coefficients of the FIRDAC also leads to the advantage that is possible to avoid using high-voltage transistors in the numerous taps of the FIR filter, which hence results in a FIRDAC with a reduced chip area size.

To be more precise, the present invention is thus dedicated to a semi-digital finite impulse response digital-to-analog converter (FIRDAC) circuit which comprises a linear adaptive finite impulse response (FIR) filter including a shift register, said shift register being realized as a tapped delay line with an input port and a plurality of output taps, wherein said input port is supplied with a one-bit digital input stream and each output tap provides a time-delayed version of the one-bit digital input stream, and an output-sided operational amplifier stage comprising at least one operational amplifier in a negative-feedback configuration which provides at its output port an analog voltage representing the digital input stream. In addition to that, said semi-digital finite impulse response digital-to-analog converter circuit further comprises an array of selectively adjustable ohmic filter resistors, each filter resistor being respectively connected to a distinct output tap of the finite impulse response filter's shift register, wherein the resistance values of these ohmic filter resistors constitute and are being used as a set of filter coefficients for weighting a corresponding one of the digital input stream stream's time-delayed versions at the shift register's output taps having the same tap index.

The resistance values of the adjustable ohmic filter resistors may adaptively be set such that the resulting analog output voltage representing an analog equivalent of the digital input stream is made ratiometric to the FIRDAC circuit's supply voltage.

A further exemplary embodiment of the present invention is directed to a semi-digital FIRDAC implementation where the complete finite impulse response filter is modeled by just one switchable ohmic resistor whose resistance value can be adjusted. To be more precise, the FIRDAC's linear adaptive finite impulse response filter may be realized as a single adjustable ohmic resistor serially connected to a switch which is pulsed with the clock signal of the digital input stream, wherein said switch is closed for bits of the one-bit digital input stream carrying a logical one and open for bits of the one-bit digital input stream carrying a logical zero, or vice versa.

The herewith proposed FIRDAC circuit may also comprise an array of ohmic dummy resistors, wherein each dummy resistor is serially connected to a distinct one of the shift register's output taps and to the output-sided operational amplifier stage. The dummy resistor at each tap may thereby have a similar or the same resistance value as the corresponding filter resistor having the same tap index. Moreover, the dummy resistor at each tap may be driven by the bit-inverse of the corresponding one-bit digital input stream's time-delayed version which is weighted by the resistance value of the filter resistor having the same tap index.

According to a further exemplary embodiment of the present invention, said one-bit digital input stream may be output from an oversampled sigma-delta converter circuit.

The output-sided operational amplifier stage of the proposed FIRDAC circuit may be realized by a differential current-to-voltage conversion circuit, wherein the latter may e.g. comprise a first operational amplifier circuit with a first operational amplifier a negative feedback configuration having an input port connected to a non-

inverted current output path beginning from a first current summing node to which the filter resistors of each shift register tap are connected and a second operational amplifier circuit with a second operational amplifier in a negative feedback configuration having an input port connected to an inverted current path beginning from a second current summing node to which the dummy resistors of each shift register tap are connected. The voltage output of said first and said second operational amplifier circuits may thereby be given by a differential analog output voltage. Furthermore, a conversion means for converting said differential analog output voltage to a single-ended voltage may be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Advantageous features, aspects, and advantages of the invention will become evident from the following description, the appended claims and the accompanying drawings. Thereby,

Fig. 1a shows the block diagrams of a conventional first-order sigma-delta modulator (SDM) supplied with an analog input signal $x(t)$ which provides a digital output signal $y[n]$ in form of a sequence of impulses,

Fig. 1b shows the digital counterpart of this circuit,

Fig. 2 illustrates in a partial block diagram and a partial logic diagram form a conventional finite impulse response digital-to-analog converter (FIRDAC) circuit as known from the prior art,

Fig. 3 illustrates in a partial block diagram and a partial logic diagram form an implementation of the finite impulse response filter from the FIRDAC circuit as depicted in Fig. 2,

Fig. 4 shows a semi-digital finite impulse response digital-to-analog converter circuit whose filter coefficients are provided by switchable current sources with ad-

justable DC output currents,

Fig. 5 shows a FIRDAC with filter coefficients provided by adjustable ohmic resistors according to an exemplary embodiment of the present invention, and

Fig. 6 shows an inverting operational amplifier stage with an input-sided voltage divider which, according to another exemplary embodiment of the present invention, comprises a switchable resistor for modeling the FIRDAC circuit's finite impulse response filter, which enables the use of low-voltage transistors at every tap of the FIRDAC's integrated finite impulse response filter, and

Fig. 7 a finite impulse response digital-to-analog converter (FIRDAC) circuit according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

In the following, the above-described semi-digital finite impulse response digital-to-analog converter circuit will be explained in more detail with respect to special refinements and referring to the accompanying drawings and in comparison the prior art. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but, on the contrary, the intention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

Fig. 1a shows a block diagram of a first-order sigma-delta modulator (SDM) as known from the prior art which is supplied with an analog input signal $x(t)$ and provides a digital output signal $y[n]$ in form of a sequence of impulses. The SDM circuit comprises an analog integrator 2 and a one-bit quantizer 3 in a feed-forward line and a one-bit digital-to-analog converter 4 (DAC) in a feedback line as well as a summation element 1 for additively combining analog input signal $x(t)$ with a digital-to-analog converted and inverted version of digital output signal $y[n]$. Fig. 1b shows the

digital counterpart of this circuit, wherein analog integrator 2 is realized by a digital representation whose transfer function is given by the numerator z^{-1} in the transfer function of loop filter 6 and one-bit quantizer 3 is modeled as an additive white Gaussian noise source providing a noise signal $e[n]$ which is additively combined with the output of said loop filter at summation element 7. An impulse is generated, in time with the clock, whenever the integrated difference between the input and the output is positive. This way the circuit regulates the rate at which impulses occur attempting to keep the average output equal to the average input. Zero input corresponds to no output impulses while maximum input corresponds to impulses generated at the clock rate. The output of the SDM is restricted to only two levels, thus forming a serial binary output code (a one-bit quantizer has two output levels, $\Delta/2$and $\tilde{}\Delta/2$, with $\Delta = 2^{-M}$ being the quantizer's step size and M (with $M = 1$) being the number of binary digits used to represent two quantized amplitude levels).

By using negative feedback, the converter outputs a binary 1 if the input waveform accumulated over one sampling period T rises above the value accumulated in the negative feedback loop during previous input samples. If the waveform falls below the accumulated value, the converter outputs a binary zero, and otherwise a binary one. Sigma-delta modulators use oversampling and noise shaping (quantization) techniques. Oversampling offers two important advantages: the specification of an anti-aliasing filter is reduced from the Nyquist specification, and the M bits resolution obtained from the ADC can be increased to M+1 bits by oversampling the signal by a factor of four. Noise shaping is a technique in which the feedback architecture of a sigma-delta converter allows the analog input signal of interest to pass unfiltered through the converter, while the quantization noise power is shifted to higher frequencies. Hence, if the quantization noise is high-pass filtered, the baseband signal of interest can be extracted by digital low-pass filtering. Consequently, sigma-delta modulation demands a considerable increase in digital processing compared to traditional methods such as pulse code modulation. However, in many applications, the advantages for sigma-delta modulation over other methods far outweigh the disadvantages. One significant advantage of sigma-delta modulation is that analog signals are converted using only a one-bit

analog-to-digital converter and analog signal processing circuits having a precision that is usually much less than the resolution of the overall converter. Furthermore, the circuitry of a sigma-delta analog-to-digital converter only requires analog components of a comparator and an integrating component, making digital signal processor chip devices less costly. For analysis, the one-bit quantizer of the sigma-delta modulator is replaced by an additive white Gaussian noise source as shown in Fig. 1b, although, in practice, the quantizer may be nonlinear and quantization noise $e[n]$ may be not white. Following the model of Fig. 1b, the modulator output $y[n]$ is given by:

$$y[n] = x[n-1] + e[n] - e[n-1] \quad [\sqrt{W}] \quad \forall\, n \in \mathbb{N}. \quad (2)$$

Using the z-transform, its equivalent frequency domain representation is given by:

$$Y(z) = Z\{y[n]\} = \sum_{n=0}^{+\infty} y[n] \cdot z^{-n}$$

$$= X(z) \cdot z^{-1} + E(z) \cdot (1 - z^{-1}) \quad [\sqrt{W}] \quad \forall\, |z| \in]r, R[\quad (3)$$

with

$$X(z) = Z\{x[n]\} = \sum_{n=0}^{+\infty} x[n] \cdot z^{-n} \quad [\sqrt{W}] \quad \forall\, |z| \in]r, R[\quad \text{and} \quad (4a)$$

$$E(z) = Z\{e[n]\} = \sum_{n=0}^{+\infty} e[n] \cdot z^{-n} \quad [\sqrt{W}] \quad \forall\, |z| \in]r, R[\quad (4b)$$

being the frequency-domain representations of $x[n]$ and $e[n]$, respectively, and r and R being the inner and outer convergence radius of a ring-shaped convergence area $r < |z| < R$, respectively. As can be taken from equation (3) and the transfer function of loop filter 6 in Fig. 1b, the signal transfer function (STF) and noise transfer function (NTF) are respectively given by

$$H_x(z) = z^{-1} \text{ and} \quad (5a)$$

$$H_e(z) = 1 - z^{-1}. \quad (5b)$$

From equations (2) and (3), it can easily be seen that the output of sigma-delta modulator 1b (which may also be referred to as "noise shaper") is a delayed input signal plus a high-pass shaped quantization noise. Since noise transfer function $H_e(z)$ contains a zero at $z = 1$ and thus at DC frequency, $H_e(z)$ provides zero gain or infinite attenuation at DC frequency.

The finite impulse response principle for a digital-to-analog converter is known per se, and described for instance in US 5,323,157 as well as in the article „A CMOS Oversampling D/A Converter with a Current Mode Semidigital Reconstruction Filter" (IEEE J. Solid-State Circuits, Vol. 28, pp. 1224-1233, Dec. 1993) by D. Su and B. Wooley. Generally speaking, a FIRDAC is a one-bit digital-to-analog converter which is implemented together with a reconstruction filter in one combination, the latter being required to filter out quantization noise. Such a FIRDAC thereby comprises a shift register (realized as a tapped delay line) with a large number of stages, typically more than hundred stages and receives a bitstream input signal of one bit (i.e. a serial data stream with one-bit amplitude resolution). Each of the shift register stages switches a dedicated current source on or off. The DC currents thus generated by all of the shift register stages are added to generate a DC output current of the FIRDAC. Usually, the DC output current is applied to a current-to-voltage converter to generate an analog FIRDAC output voltage. Each stage of the FIRDAC hence produces a DC output current contributing to the overall output current of the FIRDAC. However, the stages of the FIRDAC do not all contribute in the same extent. In order to obtain a desired filter characteristic, each stage of the FIRDAC has an associated weighting coefficient, which is constituted by the magnitude of the DC output current of the current source.

In such a FIRDAC, a digital input stream $x[n]$ is fed to a shift register and traverses through this shift register at each clock cycle. In a semi-digital FIRDAC

implementation, the shift register is typically implemented as a digital tapped delay line, while the filter coefficients are analog. Each intermediate node of the shift register is supplied with a filter coefficient a_k (with $k \in \{0, 1, 2, \ldots, N\}$) whose value can be set by adjusting the DC output current of the corresponding current source at the respective intermediate node. By these filter coefficients, the transfer function $H(z)$ of the FIR-DAC's finite impulse response filter is realized. Using Dirac's delta function

$$\delta(t) := \begin{cases} 0 & \text{for} \quad t \neq 0 \\ \infty & \text{for} \quad t = 0 \end{cases} \quad \text{with} \quad \text{(6a)}$$

$$\int_{-\infty}^{+\infty} \delta(t)\, dt := 1 \quad \text{(6b)}$$

and the two z correspondences

$$Z\{\delta[n]\} = 1 \quad \text{and} \quad \text{(7a)}$$

$$Z\{\delta[n-k]\} = z^{-k} \quad \forall\, k \in \mathbb{N}, \quad \text{(7b)}$$

this transfer function can be obtained by applying a one-sided z transform to the output signal's impulse response

$$\begin{aligned} y[n] &= x[n] * h[n] \\ &= x[n] * \sum_{k=0}^{N} a_k \cdot \delta[n-k] = \sum_{k=0}^{N} a_k \cdot x[n-k] \quad [\sqrt{W}] \quad (n \in \mathbb{N}_0) \quad \text{(8)} \end{aligned}$$

which is obtained at the summing node of the FIR filter's output port, where operator "*" denotes the convolution operation, and solving the hereby obtained z-domain equation, given in the form $Y(z) = H(z) \cdot X(z)$, for transfer function $H(z)$:

$$H(z) := \frac{Y(z)}{X(z)} = \sum_{k=0}^{N} a_k \cdot z^{-k} = a_0 + \frac{\sum_{k=1}^{N} a_k \cdot z^{N-k}}{z^N} = a_0 + a_1 \cdot \frac{\prod_{k=1}^{N-1} (z - z_{c,k})}{\prod_{k=1}^{N} (z - z_{p,k})}. \quad (9)$$

Thereby, $H(z)$ is defined for $|z| \in]r, R[$ with r and R again being the inner and outer convergence radius of a ring-shaped convergence area $r < |z| < R$, respectively. In equation (9),

$$X(z) = Z\{x[n]\} = \sum_{n=0}^{+\infty} x[n] \cdot z^{-n} \quad [\sqrt{W}] \quad \forall |z| \in]r, R[\text{ and} \quad (10a)$$

$$Y(z) = Z\{y[n]\} = \sum_{n=0}^{+\infty} y[n] \cdot z^{-n} \quad [\sqrt{W}] \quad \forall |z| \in]r, R[, \quad (10b)$$

denote the z transforms of digital input stream $x[n]$ and obtained output signal $y[n]$, respectively, $\{z_{c,k}\}_{k=1,\ldots,N-1}$ (with each $z_{c,k}$ having an order $O_{c,k}$ in a range between 1 and N-1) are the N-1 zeros of transfer function $H(z)$, and $\{z_{c,k}\}_{k=1,\ldots,N}$ (with $z_{c,N} = z_{c,N-1} = \ldots = z_{c,1}$) represent an N-fold pole at position $z = 0$ of said transfer function $H(z)$.

In a typical application situation, the FIRDAC is used in a signal-processing path of a mobile telephone for providing an analog audio signal to a speaker or earphone. The FIRDAC typically receives its input bitstream signal from a noise shaper, which increases the signal-to-noise ratio of the FIRDAC by shifting quantisation noise from the voice band to higher frequencies. Due to spurious influences, noise shapers have a tendency of repeating certain patterns, leading to small audible tones, called „idle tones“. In order to prevent said idle tones from being audible, it is known per se to digitally offset the noise shaper with a fixed amount, called „DC dither“, resulting in the idle tones being pushed to a high frequency above an audible level.

Fig. 2 illustrates in partial block diagram and partial logic diagram of a digital-to-analog converter 10 (DAC) as known from US 5,323,157 A, which is herewith incorporated by reference. DAC 10 is based on CMOS technology and comprises an interpolator 11, a sigma-delta modulator 12, and a digital finite impulse response (FIR) filter 13. Interpolator 11 has an input terminal for receiving digital input data, a first clock input terminal for receiving a clock signal labelled „DCLK“, a second clock input terminal for receiving a clock signal labelled „MCLK“, and an output terminal for providing an *N*-bit output signal. Interpolator 11 receives digital input data at a first sampling rate (the frequency of DCLK), and provides the *N*-bit output code at the output thereof at a second, higher sampling rate (the frequency of MCLK) by performing an interpolation between the samples. Thereby, said digital input data may be provided in an oversampled form.

Sigma-delta modulator 12 has an input terminal connected to the output terminal of interpolator 11, a clock input terminal for receiving signal MCLK, and an output terminal for providing output signal AOUT. Sigma-delta modulator 12 shapes the quantization noise in AOUT out-of-band, and thus AOUT is a substantially linear analog representation of the digital input data within the passband.

FIR filter 13 has an input terminal connected to the output terminal of sigma-delta modulator 12, and an output terminal for providing an analog output voltage V_{OUT}. FIR filter 13 is single-bit, *N*-stage digital filter which eliminates the need for a complex analog smoothing filter at the output of sigma-delta modulator 12. In addition, FIR filter 13 reduces the requirements placed on interpolator 11 compared to interpolator 23. The filter function and number of tap lengths can be chosen in a way that is optimal for the particular application.

As shown functionally in Fig. 2, FIR filter 13 includes *N* delay elements each with corresponding amplifier weightings, of which representative delay elements 16-1, 16-2, and 16-N, and representative weighting amplifiers 14-1, 14-2, ..., 14-N are illustrated in Fig. 2. Each delay element has an input terminal connected to a previous

delay element, if any, and an output terminal. Amplifiers 14-1, 14-2, .., 14-N have inputs connected to outputs of corresponding delay elements 16-1, 16-2, ..., 16-N, outputs connected to corresponding positive inputs of a summing device 15, and multiply the inputs thereof to implement FIR filter coefficients a_1, a_2, ..., a_N, respectively, associated therewith. Summing device 15 sums the outputs of all the amplifiers and has an output terminal for providing output signal V_{OUT} thereon.

The actual implementation of filter 13 is better understood with reference to Fig. 3, which illustrates in partial block diagram and partial logic diagram form an implementation 20 of FIR filter 13 of Fig. 2. FIR filter 20 implements an N-tap FIR filter using N D-type flip-flops (corresponding to the delay elements) and N controlled current sources (corresponding to coefficient weightings). The outputs of the current sources are connected together and to the input of a summing device 30. Fig. 3 illustrates representative portions of FIR filter 20 including D-type flip-flops 21-1, 21-2, and 21-N, and controlled current sources 22-1, 22-2, and 22-N. Flip-flop 21-1 has a D input connected to the output of sigma-delta modulator 12, a clock input for receiving a signal labelled „2MCLK“, a Q output for providing a true output signal, and a $\overline{Q}$ output for providing a complementary output signal. 2MCLK is a digital clock signal having frequency twice that of modulator clock MCLK. Flip-flop 21-2 has a D input connected to the Q output of flip-flop 21-1, a CLK input for receiving 2MCLK, a Q output provided to a subsequent flip-flop (not shown), and a Q output for providing a complementary output signal. Flip-flop 21-N has a D input connected to the Q output of a preceding flip-flop (not shown), a CLK input for receiving 2MCLK, an unused Q output, and a $\overline{Q}$ output.

Controlled current source 22-1 has a first terminal connected to a common node 23, a second terminal connected to a power supply voltage terminal labelled „V_{SS}“, and an active-low control terminal connected to the $\overline{Q}$ output terminal of flip-flop 21-1. V_{SS} is a negative power supply voltage terminal having a nominal value of approximately zero volts. Controlled current source 22-2 has a first terminal connected to node 23, a second terminal connected to V_{SS}, and an active-low control terminal con-

nected to the $\overline{Q}$ output terminal of flip-flop 21-2. Controlled current source 22-N has a first terminal connected to node 23, a second terminal connected to V_{SS}, and an active-low control terminal connected to the $\overline{Q}$ output terminal of flip-flop 21-N.

Each controlled current source implements a coefficient weighting by conducting a current equal to the associated coefficient times a reference current, which is conducted in response to the $\overline{Q}$ output of the corresponding flip-flop. Representative weightings $a_1 \cdot I_{REF}$, $a_2 \cdot I_{REF}$, ..., $a_N \cdot I_{REF}$ corresponding to current sources 22-1, 22-2, and 22-N, respectively, are illustrated in Fig. 2. Since the FIR filter function is performed only on a single-bit binary data stream, the controlled current sources are able to multiply the data value and the coefficient by either conducting the weighted current (Q = 1) or conducting no current (Q = 0). FIR filter 20 uses a symmetrical, raised cosine (Hamming window) weighting because such a weighting gives better alias protection and requires a smaller range for the coefficients compared to other weightings. However, other filter responses may be desirable for particular applications. Negative coefficients are also possible by utilizing the true (Q) flip-flop outputs instead of the complementary ($\overline{Q}$) outputs to switch the current sources. For a minimum effect of processing variations on current size, it is preferred when using symmetrical coefficient weightings (such as a Hamming window) to lay out current sources having the same size coefficients adjacent to one another. It should be noted that in other embodiments resistor or capacitor coefficient weightings may be used.

Summing device 30 includes an operational amplifier 31, a capacitor 32, and ohmic resistors 33, 34 and 35. Operational amplifier 31 has a positive input terminal connected to the first terminals of each current source, a negative input terminal, and an output terminal for providing signal V_{out}. Capacitor 32 has a first terminal connected to the output terminal of operational amplifier 31, and a second terminal connected to the positive input terminal of operational amplifier 31. Thereby, capacitor 32 is used to provide additional filtering. Ohmic resistor 33 has a first terminal connected to the output terminal of operational amplifier 31, and a second terminal connected to the positive

input terminal of operational amplifier 31. Resistor 34 along with IREF set the gain of summing device 30. Ohmic resistor 34 has a first terminal connected to a power supply voltage terminal labelled „V_{DD}", and a second terminal connected to the negative input terminal of operational amplifier 31. V_{DD} is a more-positive power supply voltage terminal having a nominal voltage of approximately 5.0 volts. Ohmic resistor 35 has a first terminal connected to the second terminal of resistor 34, and a second terminal connected to V_{SS}. Resistors 34 and 35 are preferably equal-valued to set the voltage at the positive input terminal at mid-supply. In this embodiment, summing device 30 is a conventional operational amplifier integrator, but may be implemented in other conventional forms in other embodiments.

For low distortion applications, it is preferred that input signal AOUT be chopped with a pattern of alternating zeros and ones, as taught by US 07/860,510. A chop circuit (not shown) is placed between the output of sigma-delta modulator 12 of Fig. 2 and the input of FIR filter 20 which alternates the data with ones or zeros. With the chop circuit, the D flip-flops in FIR filter 20 are clocked by 2MCLK, at twice the modulator clock rate, to allow half of an MCLK cycle to be AOUT and the other half to be chopped to an alternating pattern of ones and zeros. In addition to preventing even-order distortion in VOUT by ensuring that a transition always occurs for each flip-flop during any given clock cycle, chopping data in this fashion prevents large current spikes by ensuring that there are approximately as many flip-flops switching to a logic high as to a logic low at any clock transition. By reducing current spikes, the chop circuit maintains the integrity of the output pulses, thereby preventing the introduction of additional distortion due to the current spikes. Note that other chop techniques are possible, such as return-to-one and return-to-zero. In addition, the hardware of FIR filter 20 may be used to implement a N-tap FIR filter on unchopped data at the MCLK rate.

Fig. 4 shows a further block diagram of a typical FIRDAC implementation as known from the prior art. Here, filter coefficients $\{a_k \mid k \in \{0, 1, 2, \ldots, N\}$ are generated by adjustable DC output currents I_{P1}, I_{P2}, …, I_{PN} and I_{N1}, I_{N2}, …, I_{NN} of a set of switchable current sources, wherein said output currents are summed at the inverting

input ports of two inverting operational amplifier circuits and converted to an analog output voltage V_{out} through a conversion resistor R_F.

Fig. 5 shows a semi-digital FIRDAC implementation where the filter coefficients are implemented by adjustable ohmic resistors R_{FIR_1}, R_{FIR_2}, ..., R_{FIR_N} instead of switchable current sources. The supply-voltage-to-output-voltage relation now only depends on a resistor matching. If required, the accuracy of conversion could easily be further enhanced by dynamic element matching.

To be less susceptible to series impedance in the supply leads, it is desired to have a signal-independent supply current. This is realized by implementing an array of dummy resistors R_{D_1}, R_{D_2}, ..., R_{D_N}, which are respectively equal to a corresponding one of filter resistors R_{FIR_1}, R_{FIR_2}, ..., R_{FIR_N}, and by driving these resistors by the bit-inverse signal. The currents generated by these dummy resistors R_{D_1}, R_{D_2}, ..., R_{D_N} could be dumped in a reference buffer as indicated by voltage source providing reference voltage V_{REF}, said voltage source being connected between the non-inverting input ports of operational amplifiers $OpAmp_1$ and $OpAmp_2$ and the ground node of the FIRDAC circuit depicted in Fig. 5.

As shown in Fig. 5, said semi-digital finite impulse response digital-to-analog converter circuit has an output-sided operational amplifier stage which realizes a differential current-to-voltage conversion circuit. The latter thereby comprises a first operational amplifier circuit with a first operational amplifier ($OpAmp_1$) in a negative feedback configuration having an input port connected to a non-inverted current output path beginning from a first current summing node to which the filter resistors (R_{FIR_1}, R_{FIR_2}, ..., R_{FIR_k}, ..., R_{FIR_N}) of each shift register tap k are connected and a second operational amplifier circuit with a second operational amplifier ($OpAmp_2$) in a negative feedback configuration having an input port connected to an inverted current path beginning from a second current summing node to which the dummy resistors (R_{D_1}, R_{D_2}, ..., R_{D_k}, ..., R_{D_N}) of each shift register tap k are connected. As can be seen, the voltage

output of said first and said second operational amplifier circuits is given by a differential analog output voltage V_{out}. A further refinement of this embodiment may therefore comprise a conversion means for converting said differential analog output voltage V_{out} to a single-ended voltage.

When implementing the FIRDAC as depicted in Fig. 6, which shows an inverting operational amplifier stage with an input-sided voltage divider which comprises an adjustable resistor R_{FIR} for modeling the filter coefficients of the FIRDAC circuit's finite impulse response filter, low-voltage transistors can be used at every tap of the FIRDAC's integrated finite impulse response filter while a higher supply voltage is applied. For simplicity, the complete FIR filter is modeled by just one ohmic resistor (R_{FIR}) and a single clock-controlled switch (S), wherein said switch is closed for the FIRDAC's one-bit digital input stream $x[n]$ carrying a logical one and open for said digital input data signal $x[n]$ carrying a logical zero, or vice versa.

Let reference voltage V_{REF} be equal to V_{DD}/χ and real-valued factor χ be given such that V_{REF} is well below the breakdown voltage of the FIRDAC's low-voltage transistors. Since voltage $V_{R_{FIR}}$ at the inverting input port of the operational amplifier (OpAmp) will follow V_{REF}, said low-voltage transistors can be used for the numerous switches in the FIR filter. This will result in a FIR filter with reduced chip area. Using equations

$$V_{R_{FIR}} = \frac{R_{FIR}}{R_{FIR} + R_B} \cdot V_{DD} = \frac{V_{DD}}{\chi} \approx V_{REF} \text{ [V] with} \quad (11a)$$

$$\chi := \frac{R_{FIR} + R_B}{R_{FIR}} = 1 + \frac{R_B}{R_{FIR}}, \quad (11b)$$

$$V_{out} = V_{R_{FIR}} - R_F \cdot I \text{ [V] and} \quad (11c)$$

$$I = \frac{V_{DD} - V_{R_{FIR}}}{R_B} - \frac{V_{R_{FIR}}}{R_{FIR}} \text{ [A]}, \quad (11d)$$

which are valid for switch S being closed, it can be shown that operational amplifier input current I is equal to zero and that output voltage V_{out} is given as follows:

$$V_{out} = V_{R_{FIR}} = \frac{V_{DD}}{\chi} \quad [\mathrm{V}]. \quad (12)$$

Thereby, R_F denotes the resistance value of an ohmic resistor in the feedback line of the depicted FIRDAC's output-sided operational amplifier stage, said stage comprises an operational amplifier in a negative-feedback configuration, R_B and R_{FIR} denote the resistance values of two serially connected adjustable ohmic resistors constituting the aforementioned voltage divider, V_{DD} denotes the FIRDAC's supply voltage, V_{REF} denotes a DC voltage supplied by a DC voltage source connected to the non-inverting input port of the output-sided operational amplifier, $V_{R_{FIR}}$ denotes the voltage drop at the adjustable voltage divider resistor R_{FIR}, voltage V_{out} denotes the resulting analog output voltage representing an analog equivalent of the FIRDAC's one-bit digital input stream, and I denotes the voltage divider's output current. When additionally demanding that the resistance value of feedback resistor R_F has to obey the condition

$$R_F \stackrel{!}{=} R_B + R_{FIR} \quad [\Omega], \quad (13)$$

filter resistor

$$R_{FIR} = R_{FIR,1} \,||\, R_{FIR,2} \,||\, \ldots \,||\, R_{FIR,k} \,||\, \ldots \,||\, R_{FIR,N} = \frac{\prod_{k=1}^{N} R_{FIR,k}}{\sum_{k=1}^{N} \prod_{\substack{l=1 \\ (l \neq k)}}^{N} R_{FIR,l}} \quad [\Omega], \quad (14a)$$

whose resistance value represents the total resistance which is obtained when connecting the all tap resistors $R_{FIR,k}$ (with $k = 1, 2, \ldots, N$) of the FIR filter in parallel, has to be set equal to

$$R_{FIR} := \frac{R_F}{\chi} \ [\Omega] \quad (14b)$$

and voltage divider resistor R_B has to be set to a resistance value as prescribed by the equation

$$R_B = R_{FIR} \cdot (\chi - 1) = R_F \cdot \left(1 - \frac{1}{\chi}\right) [\Omega]. \quad (15)$$

When switch S is open, the following equations have to be used for completely describing the functionality of the circuit depicted in Fig. 6:

$$V_{REF} \approx \frac{V_{DD}}{\chi} \ [\text{V}] \ \text{with} \quad (16a)$$

$$\chi := \frac{R_{FIR} + R_B}{R_{FIR}} = 1 + \frac{R_B}{R_{FIR}}, \quad (16b)$$

$$V_{out} = V_{DD} - (R_F + R_B) \cdot I \ [\text{V}] \ \text{and} \quad (16c)$$

$$V_{out} = V_{REF} - R_F \cdot I \ [\text{V}] \ \text{and} \quad (16d)$$

$$I = \frac{V_{DD} - V_{REF}}{R_B} \ [\text{A}], \quad (16e)$$

It can then be shown that operational amplifier input current I is independent of factor χ and can be written as

$$I = \frac{V_{DD}}{R_F} = const. \ [\text{A}], \quad (17)$$

that output voltage V_{out} as a function of real-valued factor χ is given by

$$V_{out} = -V_{DD} \cdot \left(1 - \frac{1}{\chi} \right) \text{ [V]} \quad (18)$$

and, when additionally using the condition as prescribed by equation (13), that the resistance values of filter resistor R_{FIR} and voltage divider resistor R_B have to be set as prescribed by equations (14b) and (15), respectively.

Fig. 7 shows a further exemplary embodiment of the present invention for the k-th tap (with $k \in \{1, 2, \ldots, N\}$) of the proposed ratiometric FIRDAC. Thereby, V_{REF} should scale with the supply voltage V_{DD}, which is achieved by means of a resistive voltage divider constituted by ohmic resistor R_{B1} (or R_{B2}, respectively) and ohmic resistor R_{FIR_k}, the latter providing filter coefficient a_k for this tap. Furthermore, V_{REF} has to be smaller than the breakdown voltage of the low-voltage transistors which are applied in the given IC process. In this case, switches M_{1k}, M_{2k}, M_{1k}' and M_{2k}' in the two single-balanced mixer configurations of the depicted FIR filter implementation can be realized as low-voltage bipolar transistors, low-voltage metal oxide semiconductor field effect transistors (MOSFETs) or low-voltage junction field effect transistors (JFETs), which thus results in a smaller chip size. Switching of dummy resistors $\{R_{D_k} \mid k = 1, 2, \ldots, N\}$ guarantees a signal-independent supply current which makes the FIRDAC circuit design less susceptible to variations of the series impedance in the FIRDAC's supply leads.

APPLICATIONS OF THE PRESENT INVENTION

The proposed FIRDAC circuit can advantageously be applied in high-accuracy ($M > 12$ bits) low-frequency ($f_s < 30$ kHz) digital-to-analog interfaces, e.g. in the scope of sigma-delta modulators for class-D power amplifiers in high-fidelity audio equipment or sensor equipment. The present invention may also be used in automotive angular sensors (such as e.g. the KMA200 and the KMA199 by Business Line General Applications). In this application, it is required to have an output which is ratiometric to

the supply voltage, which is due to the fact that the angular sensor has to replace a potentiometer.

While the present invention has been illustrated and described in detail in the drawings and in the foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive, which means that the invention is not limited to the disclosed embodiments. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure and the appended claims. In the claims, the word „comprising“ does not exclude other elements or steps, and the indefinite article „a“ or „an“ does not exclude a plurality. A single processor or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures can not be used to advantage. Any reference signs in the claims should not be construed as limiting the scope of the invention.

CLAIMS

1. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit, comprising

a linear adaptive finite impulse response (FIR) filter including a shift register, said shift register being realized as a tapped delay line with an input port and a plurality of output taps (k = 1, 2, …, N), wherein said input port is supplied with a one-bit digital input stream ($x[n]$) and each output tap provides a time-delayed version ($x[n-1]$, $x[n-2]$, …, $x[n-k]$, …, $x[n-N]$) of the one-bit digital input stream, and

an output-sided operational amplifier stage comprising at least one operational amplifier ($OpAmp_1$, $OpAmp_2$) in a negative-feedback configuration which provides at its output port an analog voltage (V_{out}) representing the digital input stream ($x[n]$),

wherein

the semi-digital finite impulse response digital-to-analog converter circuit further comprises an array of selectively adjustable ohmic filter resistors (R_{FIR_1}, R_{FIR_2}, …, R_{FIR_k}, …, R_{FIR_N}), each filter resistor being respectively connected to a distinct output tap of the finite impulse response filter's shift register, wherein the resistance values of these ohmic filter resistors (R_{FIR_1}, R_{FIR_2}, …, R_{FIR_k}, …, R_{FIR_N}) constitute and are being used as a set of filter coefficients (a_1, a_2, …, a_k, …, a_N) for weighting a corresponding one of the digital input stream stream's time-delayed versions ($x[n-1]$, $x[n-2]$, …, $x[n-k]$, …, $x[n-N]$) at the shift register's output taps having the same tap index (k).

2. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to claim 1,

wherein

the resistance values of the adjustable ohmic filter resistors (R_{FIR_1}, R_{FIR_2}, …, R_{FIR_k}, …, R_{FIR_N}) are adaptively set such that the resulting analog output voltage (V_{out}) representing an analog equivalent of the digital input stream ($x[n]$) is made ratiometric to the FIRDAC circuit's supply voltage (V_{DD}).

3. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to anyone of the preceding claims,
wherein
the linear adaptive finite impulse response (FIR) filter is realized as a single adjustable ohmic resistor (R_{FIR}) serially connected to a switch (S) which is pulsed with the clock signal (Clock) of the digital input stream ($x[n]$), wherein said switch (S) is closed for bits of the one-bit digital input stream carrying a logical one and open for bits of the one-bit digital input stream carrying a logical zero, or vice versa.

4. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to anyone of the preceding claims,
comprising an array of ohmic dummy resistors (R_{D_1}, R_{D_2}, ..., R_{D_k}, ..., R_{D_N}), each dummy resistor being serially connected to a distinct one of the shift register's output taps and to the output-sided operational amplifier stage.

5. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to claim 4,
wherein
the dummy resistor (R_{D_k}) at each tap (k) has a similar or the same resistance value as the corresponding filter resistor (R_{FIR_k}) having the same tap index (k).

6. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to claim 5,
wherein
the dummy resistor (R_{D_k}) at each tap (k) is driven by the bit-inverse ($\bar{x}[n-k]$) of the corresponding one-bit digital input stream's time-delayed version ($x[n-k]$) which is weighted by the resistance value of the filter resistor (R_{FIR_k}) having the same tap index (k).

7. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to anyone of the preceding claims, wherein said one-bit digital input stream is output from an oversampled sigma-delta converter circuit.

8. 8. A semi-digital finite impulse response digital-to-analog converter (FIRDAC) circuit according to anyone of the preceding claims, wherein said output-sided operational amplifier stage realizes a differential current-to-voltage conversion circuit comprising

a first operational amplifier circuit with a first operational amplifier ($OpAmp_1$) in a negative feedback configuration having an input port connected to a non-inverted current output path beginning from a first current summing node to which the filter resistors (R_{FIR_1}, R_{FIR_2}, ..., R_{FIR_k}, ..., R_{FIR_N}) of each shift register tap (k) are connected, and

a second operational amplifier circuit with a second operational amplifier ($OpAmp_2$) in a negative feedback configuration having an input port connected to an inverted current path beginning from a second current summing node to which the dummy resistors (R_{D_1}, R_{D_2}, ..., R_{D_k}, ..., R_{D_N}) of each shift register tap (k) are connected; wherein

the voltage output of said first and said second operational amplifier circuits is given by a differential analog output voltage (V_{out}).

9. A semi-digital finite impulse response digital-to-analog converter (FIR-DAC) circuit according to claim 8, further comprising a conversion means for converting said differential analog output voltage (V_{out}) to a single-ended voltage.

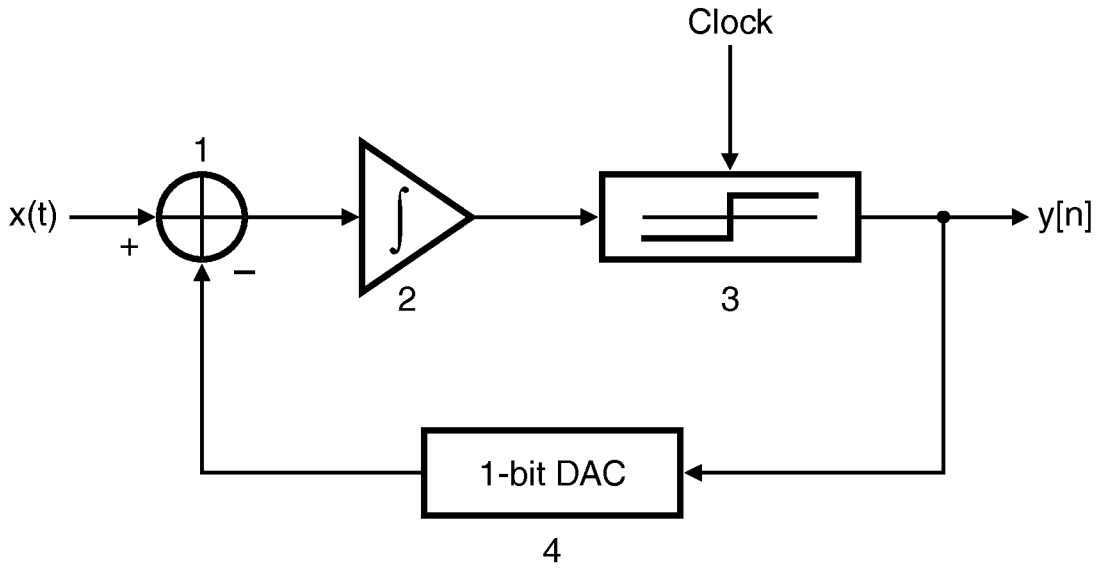

FIG. 1a

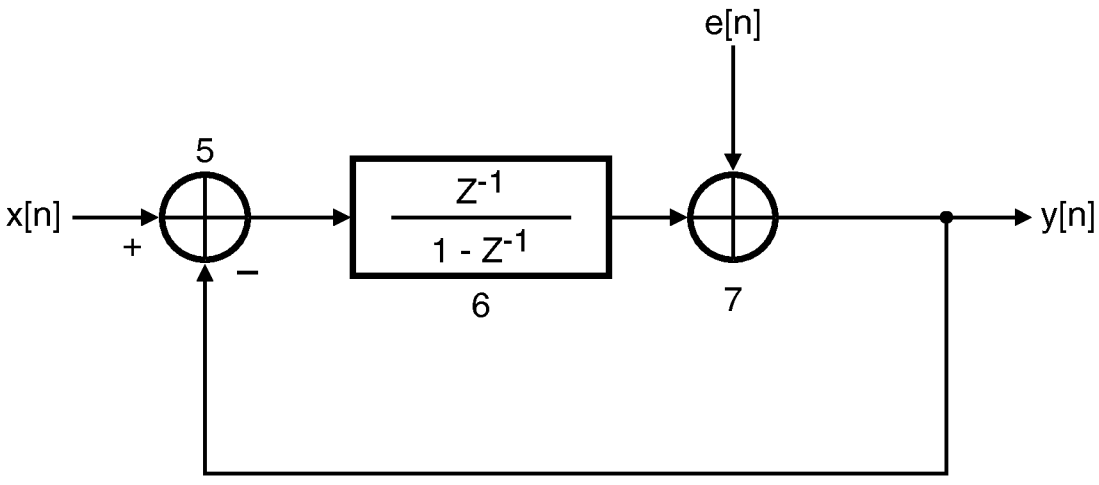

FIG. 1b

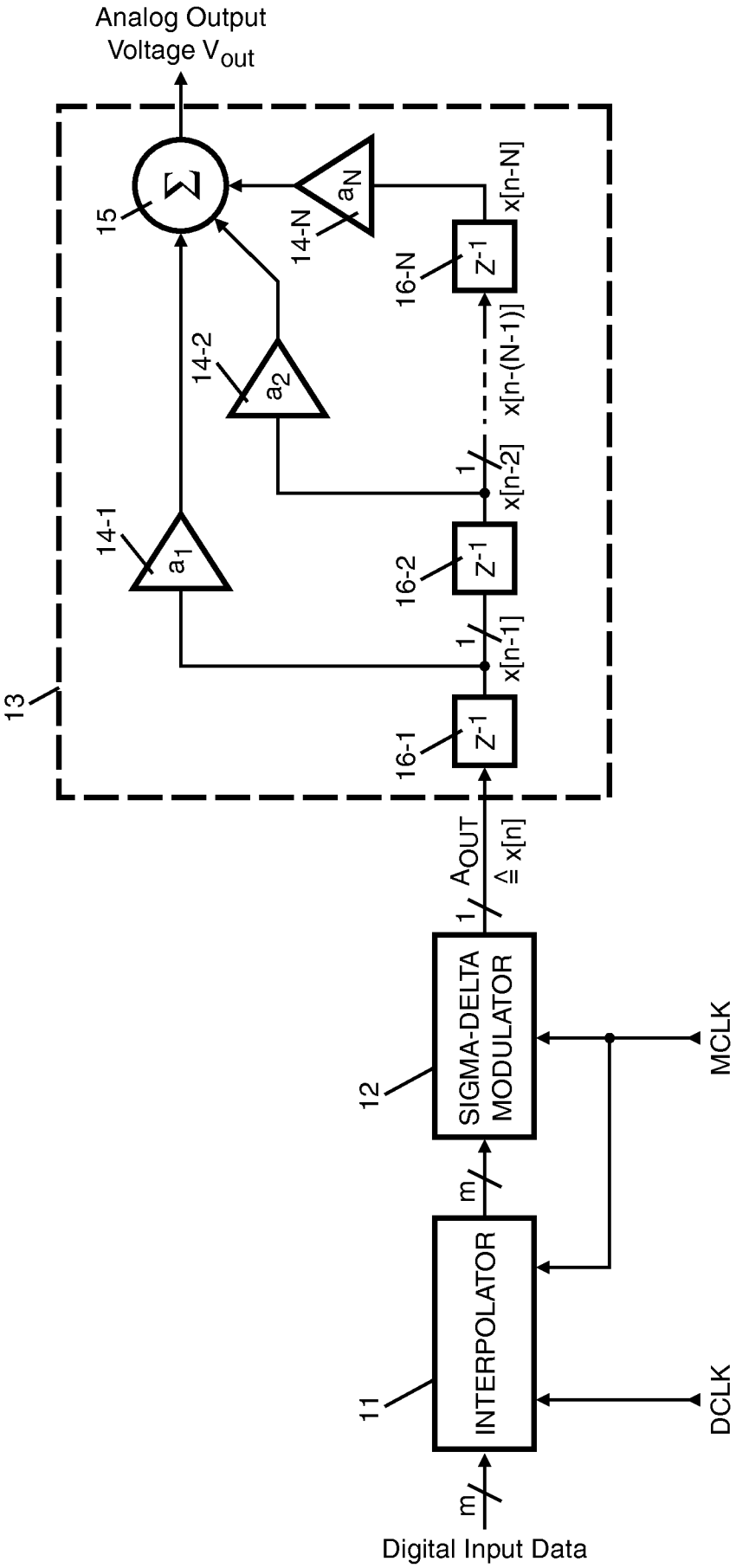
Analog Output
Voltage V_{out}
13
15
Σ
a_N
14-N
a_2
14-2
a_1
14-1
16-N
Z^{-1}
16-2
16-1
x[n-N]
x[n-(N-1)]
x[n-2]
x[n-1]
1
A_{OUT}
≙ x[n]
SIGMA-DELTA MODULATOR
12
INTERPOLATOR
11
m
MCLK
DCLK
Digital Input Data

FIG. 2

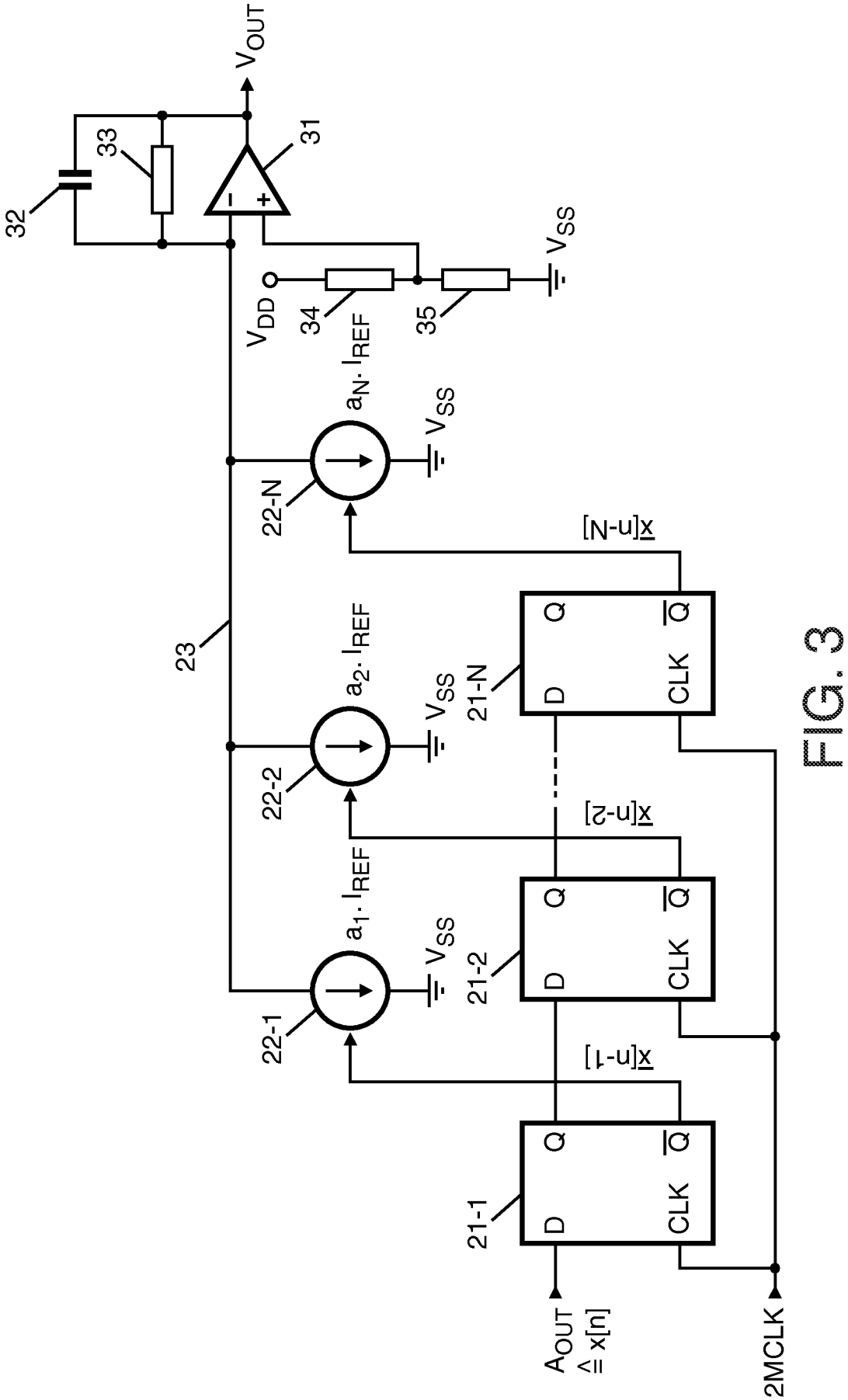
V_OUT
33
31
32
V_SS
V_DD
34
35
a_N · I_REF
V_SS
22-N
x̄[n-N]
23
a_2 · I_REF
V_SS
21-N
Q
Q̄
D
CLK
22-2
x̄[n-2]
a_1 · I_REF
V_SS
21-2
22-1
x̄[n-1]
21-1
A_OUT ≙ x[n]
2MCLK

FIG. 3

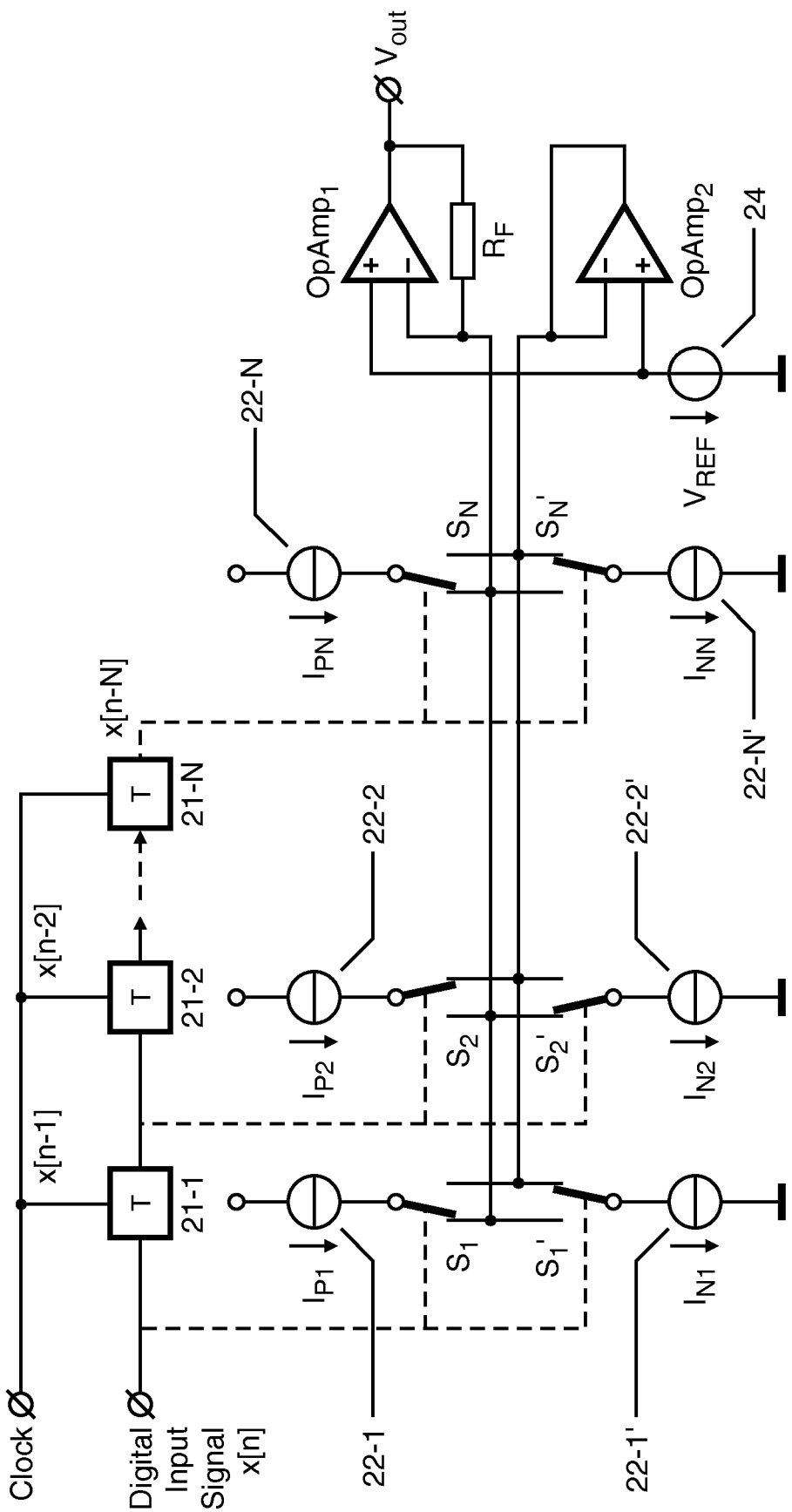
Clock
Digital Input Signal x[n]
T
21-1
21-2
21-N
x[n-1]
x[n-2]
x[n-N]
22-1
22-1'
22-2
22-2'
22-N
22-N'
24
I_{P1}
I_{P2}
I_{PN}
I_{N1}
I_{N2}
I_{NN}
S_1
S_1'
S_2
S_2'
S_N
S_N'
R_F
$OpAmp_1$
$OpAmp_2$
V_{out}
V_{REF}

FIG. 4

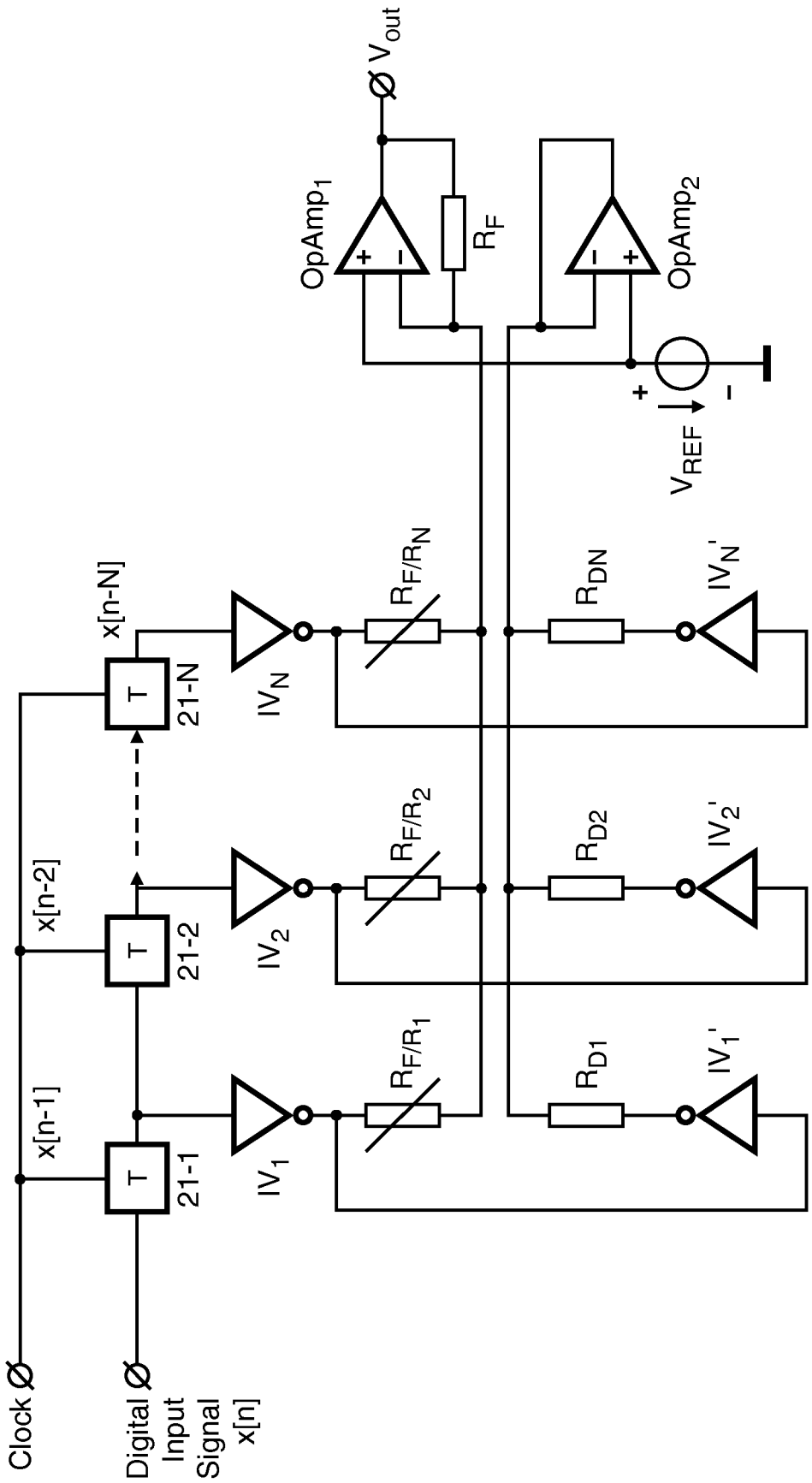
Clock
Digital Input Signal x[n]
x[n-1]
x[n-2]
x[n-N]
T
21-1
21-2
21-N
IV1
IV2
IVN
RF/R1
RF/R2
RF/RN
RD1
RD2
RDN
IV1'
IV2'
IVN'
OpAmp1
OpAmp2
RF
Vout
VREF
+
-

FIG. 5

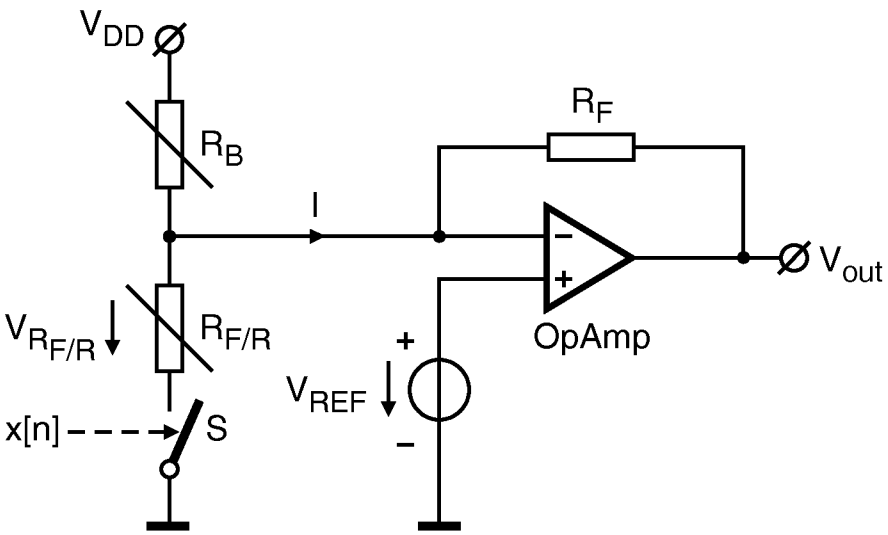

FIG. 6

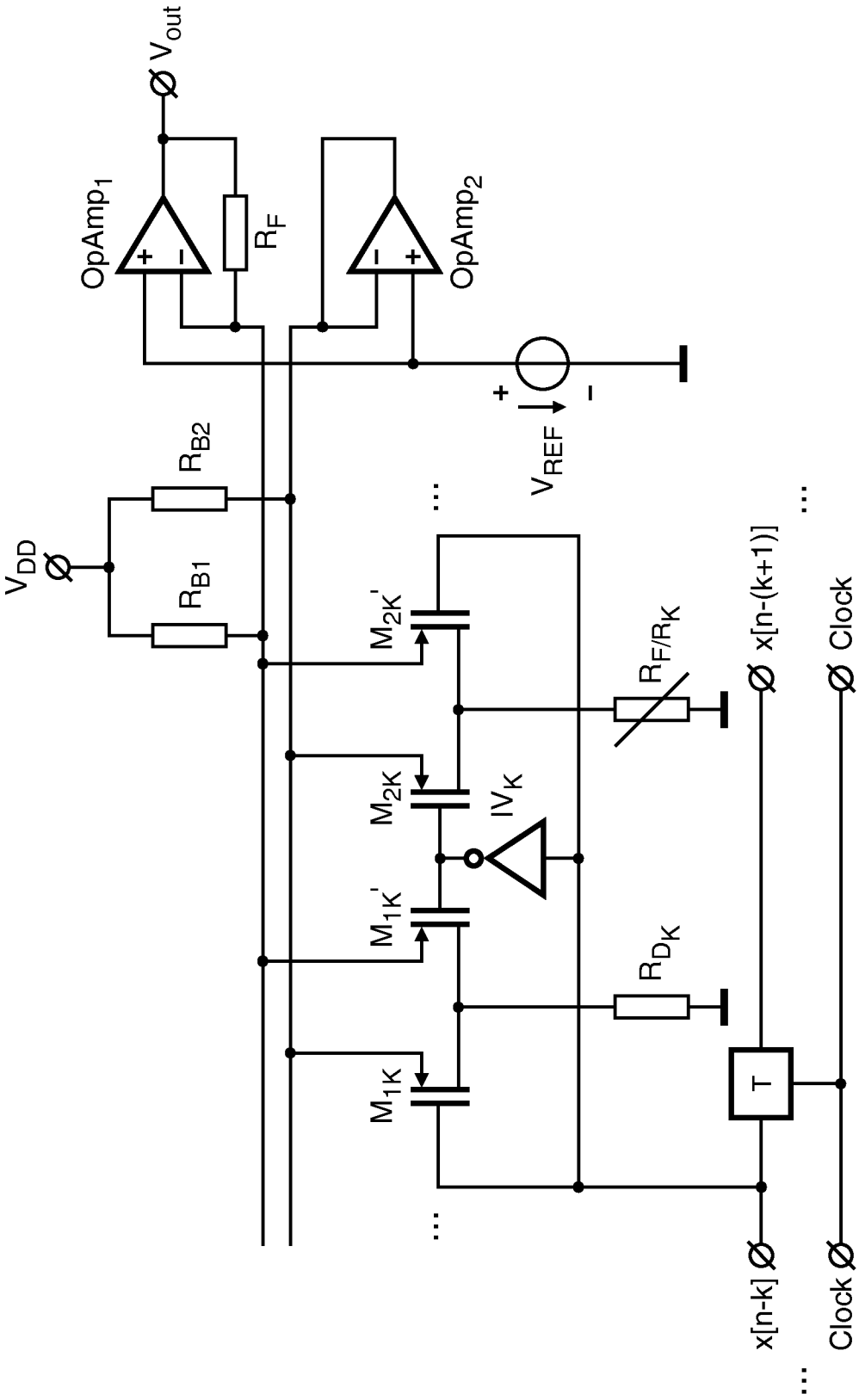
V_out
OpAmp_1
R_F
OpAmp_2
V_REF
R_B2
R_B1
V_DD
M_2K'
M_2K
IV_K
M_1K'
M_1K
R_F/R_K
R_DK
x[n-(k+1)]
Clock
T
x[n-k]
Clock

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/053425

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M H03H

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, COMPENDEX, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	SHIBATA M ET AL: "A cascaded Delta-Sigma DAC with an analog FIR filter reducing mismatch-effects" CIRCUITS AND SYSTEMS, 2005. 48TH MIDWEST SYMPOSIUM ON CINICINNATI, OHIO AUGUST 7-10, 2005, PISCATAWAY, NJ, USA,IEEE, 7 August 2005 (2005-08-07), pages 1263-1266, XP010895374 ISBN: 978-0-7803-9197-0 page 1263, right-hand column, last paragraph - page 1264, right-hand column, paragraph 2; figures 4-6 ----- -/--	1-3,7,9

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
18 November 2008	07/01/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Brosa, Anna-Maria

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2008/053425

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	PETER HOLLOWAY: "A Trimless 16b Digital Potentiometer" 1984 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE. DIGEST OF TECHNICAL PAPERS, 22 February 1984 (1984-02-22), - 24 February 1984 (1984-02-24) pages 66, 67, 320-321, XP002504434 San Francisco page 66, left-hand column - page 67, right-hand column; figures 1,2	1-3,7,9
Y	WO 96/25793 A (ADVANCED MICRO DEVICES INC [US]) 22 August 1996 (1996-08-22) page 9, lines 12-21; figure 4	9
A	WO 2007/029130 A (KONINKL PHILIPS ELECTRONICS NV [NL]; BRUIN PAUL P F M [NL]) 15 March 2007 (2007-03-15) page 10, line 3 - page 11, line 12; figure 3	4-6
A	US 5 323 157 A (LEDZIUS ROBERT C [US] ET AL) 21 June 1994 (1994-06-21) cited in the application figure 3	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2008/053425

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9625793 A	22-08-1996	DE 69510471 D1	29-07-1999
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US 5323157 A	21-06-1994	NONE	