(19)日本国特許庁(JP)　(12)公表特許公報(A)　(11)特許出願公表番号
特表2004-505433
(P2004-505433A)
(43)公表日　平成16年2月19日(2004.2.19)

(51)Int.Cl.[7]	F I		テーマコード（参考）
H01L 21/00	H01L	21/00	
H01L 21/02	H01L	21/02	Z

審査請求 未請求　予備審査請求 有　（全 160 頁）

(21)出願番号	特願2001-537527(P2001-537527)
(86)(22)出願日	平成12年11月17日(2000.11.17)
(85)翻訳文提出日	平成14年5月20日(2002.5.20)
(86)国際出願番号	PCT/US2000/031665
(87)国際公開番号	WO2001/035718
(87)国際公開日	平成13年5月25日(2001.5.25)
(31)優先権主張番号	09/442,699
(32)優先日	平成11年11月18日(1999.11.18)
(33)優先権主張国	米国(US)

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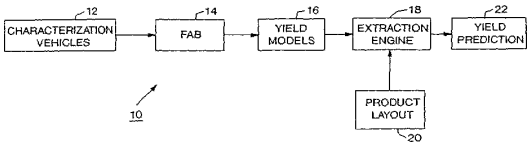
最終頁に続く

(54)【発明の名称】製品歩留まり予測用のシステムおよび方法

(57)【要約】
集積回路の歩留まりを予測するためのシステムおよび方法は、最終的な集積回路製品に組み込むべき少なくとも１つのタイプのフィーチャを表す少なくとも１つのフィーチャを組み込む、少なくとも１つのタイプの特徴付けビヒクルを含む。この特徴付けビヒクルは、歩留まりモデルを生成するために、集積回路製品を製造する際に使用すべき製造サイクルを構成するプロセス・オペレーションのうちの少なくとも１つを受ける。この歩留まりモデルは、特徴付けビヒクルによって定義されるレイアウトを実施し、好ましくは、動作速度での電気的テスト・データの収集およびプロトタイプ・セクションのテストを容易にするフィーチャを含む。抽出エンジンは、提案される製品レイアウトから所定のレイアウト属性を抽出する。歩留まりモデルに対して操作して、この抽出エンジンは、レイアウト属性と、層または製造プロセスのステップごとの破壊に応じて歩留まり予測を生成する。次いでこれらの歩留まり予測を使用して、製造プロセス中のどのエリアを最も改良する必要があるかを判定する。



【特許請求の範囲】
【請求項１】
ａ）最終的な集積回路製品に組み込むべき少なくとも１つのタイプのフィーチャを表す少なくとも１つのフィーチャを含む、少なくとも１つのタイプの特徴付けビヒクルと、
ｂ）特徴付けビヒクルによって定義されるレイアウトを実施する歩留まりモデルであって、集積回路製品を製造する際に使用すべき製造サイクルを構成する、少なくとも１つのプロセス・オペレーションを受けた歩留まりモデルと、
ｃ）製品レイアウトと、
ｄ）製品レイアウトから所定のレイアウト特性を抽出するための抽出エンジンであって、その特性が歩留まりモデルと共に使用されて、歩留まり予測が生成される抽出エンジンとを備える、
集積回路の歩留まりを予測するためのシステム。
【請求項２】
特徴付けビヒクル・レイアウトが、製品レイアウト上に現れる各フィーチャの変動の範囲と同じ範囲を含む、請求項１に記載のシステム。
【請求項３】
特徴付けビヒクルがショート・フロー・テスト・ビヒクルを備える、請求項２に記載のシステム。
【請求項４】
特徴付けビヒクルが、提案される製品レイアウトを表すフィーチャを含む部分レイアウトを有するショート・フロー・テスト・ビヒクルを備える、請求項３に記載のシステム。
【請求項５】
特徴付けビヒクルが、少なくとも１つの能動領域と、提案される製品レイアウトを表す少なくとも１つの事前選択した隣接フィーチャとを定義する、請求項４に記載のシステム。
【請求項６】
特徴付けビヒクルが金属ショート・フロー・テスト・ビヒクルを備える、請求項３に記載のシステム。
【請求項７】
金属ショート・フロー・テスト・ビヒクルが少なくとも１つの基本構造を含む、請求項６に記載のシステム。
【請求項８】
前記少なくとも１つの基本構造が、
ａ）ケルビン金属臨界寸法構造と、
ｂ）スネーク構造と、
ｃ）コーム構造と、
ｄ）スネークおよびコーム構造と、
ｅ）ネスト欠陥サイズ分布構造と、
ｆ）ファン・デル・ポー構造と、
ｇ）光近接補正構造と、
ｈ）走査電子顕微鏡構造とからなるグループから選択される、請求項７に記載のシステム。
【請求項９】
金属ショート・フロー・テスト・ビヒクルが、単一金属層中に少なくとも１つの基本構造を含む、請求項８に記載のシステム。
【請求項１０】
金属ショート・フロー・テスト・ビヒクルが、複数の金属層中に少なくとも１つの基本構造を含む、請求項８に記載のシステム。
【請求項１１】
提案される製品レイアウトを表すフィーチャが少なくとも１つのバイアまたは接点を含む、請求項４に記載のシステム。

【請求項１２】
提案される製品レイアウトを表すフィーチャが少なくとも１つの能動デバイスを含む、請求項４に記載のシステム。
【請求項１３】
提案される製品レイアウトを表すフィーチャが少なくとも１つのケイ化物領域を含む、請求項４に記載のシステム。
【請求項１４】
提案される製品レイアウトを表すフィーチャが少なくとも１つのポリシリサイド領域またはポリシリコン領域を含む、請求項４に記載のシステム。
【請求項１５】
抽出エンジンが、特徴付けビヒクルを設計するときに使用するためのレイアウト・フィーチャ・レベルの範囲を決定するためにも使用される、請求項１に記載のシステム。
【請求項１６】
レベルのレイアウト・フィーチャ範囲が、線幅、線スペース、および線密度を含む、請求項１５に記載のシステム。
【請求項１７】
ａ）最終的な集積回路製品に組み込むべき少なくとも１つのタイプのフィーチャを表す少なくとも１つのフィーチャを有する、少なくとも１つのタイプの特徴付けビヒクルを製造するための情報を提供すること、
ｂ）集積回路製品を製造する際に使用すべき製造サイクルを構成する少なくとも１つのプロセス・オペレーションを利用して、歩留まりモデルと、製品を表すレイアウト・フィーチャとを実施する特徴付けビヒクルを製造すること、
ｃ）製品レイアウトを提供すること、
ｄ）製品レイアウトから所定のレイアウト特性を抽出すること、
ｅ）抽出したレイアウト特性を歩留まりモデルとモデルと共に使用して、歩留まり予測を生成することを含む
集積回路に関する歩留まりを予測するための方法。
【請求項１８】
特徴付けビヒクル・レイアウトが、製品レイアウト上に現れる各フィーチャの変動の範囲と同じ範囲を含む、請求項１７に記載の方法。
【請求項１９】
特徴付けビヒクルがショート・フロー・テスト・ビヒクルを備える、請求項１８に記載の方法。
【請求項２０】
特徴付けビヒクルが、提案される製品レイアウトを表すフィーチャを含む部分レイアウトを有するショート・フロー・テスト・ビヒクルを備える、請求項１９に記載の方法。
【請求項２１】
特徴付けビヒクルが、少なくとも１つの能動領域と、提案される製品レイアウトを表す少なくとも１つの事前選択した隣接フィーチャとを定義する、請求項２０に記載の方法。
【請求項２２】
特徴付けビヒクルが金属ショート・フロー・テスト・ビヒクルを備える、請求項１９に記載の方法。
【請求項２３】
金属ショート・フロー・テスト・ビヒクルが少なくとも１つの基本構造を含む、請求項２２に記載の方法。
【請求項２４】
前記少なくとも１つの基本構造が、
ａ）ケルビン金属臨界寸法構造と、
ｂ）スネーク構造と、
ｃ）コーム構造と、

ｄ）スネークおよびコーム構造と、
ｅ）ネスト欠陥サイズ分布構造と、
ｆ）ファン・デル・ポー構造と、
ｇ）光近接補正構造と、
ｈ）走査電子顕微鏡構造とからなるグループから選択される、請求項２３に記載の方法。
【請求項２５】
金属ショート・フロー・テスト・ビヒクルが、単一金属層中に少なくとも１つの基本構造を含む、請求項２４に記載の方法。
【請求項２６】
金属ショート・フロー・テスト・ビヒクルが、複数の金属層中に少なくとも１つの基本構造を含む、請求項２４に記載の方法。
【請求項２７】
提案される製品レイアウトを表すフィーチャが少なくとも１つのバイアまたは接点を含む、請求項２０に記載の方法。
【請求項２８】
提案される製品レイアウトを表すフィーチャが少なくとも１つの能動デバイスを含む、請求項２０に記載の方法。
【請求項２９】
提案される製品レイアウトを表すフィーチャが少なくとも１つのケイ化物領域を含む、請求項２０に記載の方法。
【請求項３０】
提案される製品レイアウトを表すフィーチャが少なくとも１つのポリシリサイド領域またはポリシリコン領域を含む、請求項２０に記載の方法。
【請求項３１】
抽出エンジンが、特徴付けビヒクルを設計するときに使用するためのレベルの範囲を決定するためにも使用される、請求項１７に記載の方法。
【請求項３２】
レベルの範囲が、線幅、線スペース、および線密度を含む、請求項３１に記載の方法。
【請求項３３】
所定のレイアウト特性が、
ａ）特徴付けビヒクル中のすべての構造をリストするステップと、
ｂ）各構造をファミリに分類し、それによって各ファミリ中のすべての構造が特定の属性にわたる実験を形成するステップと、
ｃ）各ファミリについて、どの属性を製品レイアウトに関して抽出すべきかを決定するステップとを含むプロセスを使用して、製品レイアウトから抽出される、請求項１７に記載の方法。
【請求項３４】
ファミリが、選択した数の線幅およびスペースにわたって基本的欠陥を調査するためのネスト構造を有するファミリを含む、請求項３３に記載の方法。
【請求項３５】
ファミリが、特定の幅の線幅およびスペースにわたって歩留まりを調査するためのスネークおよびコーム構造を有するファミリを含む、請求項３３に記載の方法。
【請求項３６】
所定の範囲の線幅およびスペースが、比較的小さいスペースに並ぶ比較的広い線幅と、比較的狭い線幅に並ぶ比較的大きい線間スペースとを含む、請求項３５に記載の方法。
【請求項３７】
ファミリが、線密度、線幅、および間隔にわたる臨界寸法変動を調査するためのケルビン臨界寸法構造およびファン・デル・ポー構造を有するファミリを含む、請求項３３に記載の方法。
【請求項３８】

ファミリが、歩留まりに対する様々な光近接補正方式の効果を調査するためのボーダ構造を有するファミリを含む、請求項３３に記載の方法。
【請求項３９】
特徴付けビヒクル・データおよび抽出したレイアウト属性が与えられた場合に、歩留まり損失機構を決定し、配置するためのシステム。
【発明の詳細な説明】
【０００１】
（発明の背景）
本発明は、集積回路の製造に関し、より詳細には、製造歩留まりを改善するためのシステムおよび方法に関する。
【０００２】
集積回路の製造は、何百もの個別の作業を含むことがある非常に複雑な工程である。基本的には、この工程は、精密にあらかじめ定めた量のドーパント材料を、精密にあらかじめ定めたシリコン・ウェハのエリアに拡散し、トランジスタなどの能動デバイスを生成することを含む。これは一般に、ウェハ上に二酸化シリコンの層を形成し、次いで二酸化シリコン・マスクを通じて拡散を行うべきエリアのパターンを画定するために、フォトマスクおよびフォトレジストを利用する。次いで、二酸化シリコン層を貫いて開口がエッチングされ、大きさに合わせて精密に作られ、位置付けられた、拡散がそれを通じて行われる開口のパターンが画定される。所定の数のこのような拡散操作を実施してウェハ中に所望の数のトランジスタを生成した後、これらのトランジスタは、必要に応じて相互接続線によって相互接続される。これらの相互接続線、または相互接続としても知られるものは一般に、フォトマスク、フォトレジスト、およびエッチング工程によって所望の相互接続パターンに画定される導電性材料の付着によって形成される。典型的な完成後の集積回路は、０．１インチ×０．１インチ（２．５４ｍｍ×２．５４ｍｍ）のシリコン・チップに含まれる数百万のトランジスタと、サブミクロン寸法の相互接続とを有することができる。
【０００３】
今日の集積回路で必要とされるデバイスおよび相互接続の密度を考えると、製造工程を最大の精度で、かつ欠陥を最小にするように実施することが不可欠である。動作を信頼性あるものとするために、回路の電気的特性を、注意深く制御される限度内に保たなければならない。このことは、無数の作業および製造工程にわたって高度な制御を行うことを意味する。例えば、フォトレジスト作業およびフォトマスク作業では、塵などの異物の存在、微細なスクラッチ、およびフォトマスク上のパターン中の他の欠陥により、半導体ウェハ上に欠陥パターンが生成され、欠陥集積回路が生成される可能性がある。さらに、拡散操作自体の間に、欠陥が回路中に導入される可能性がある。欠陥のある回路は、高倍率の下での外観検査と、電気的テストの両方によって識別することができる。欠陥のある集積回路を識別した後に、その製造工程で製造された欠陥のある集積回路の数を削減するための措置を講じ、それによって仕様に適合する集積回路の歩留まりを向上することが望ましい。
【０００４】
過去においては、集積回路の芳しくない歩留まりを引き起こす欠陥の多くは、微粒子の異物または他の不定の源泉によって引き起こされた。以前にも増して、現代の集積回路工程に見られる欠陥の多くは、プロセス開発またはイールド・ランピング（ｙｉｅｌｄ　ｒａｍｐｉｎｇ）の初期段階では特に、微粒子または不定の異物を源泉とするのではなく、非常に系統的な源泉に由来している。これらの系統的な欠陥の源泉の例には、積極的なリソグラフィ・ツールを使用することによる転写問題、不十分に形成されたケイ化物によるポリ・ストリンガ、駆動される密度によるゲート長の変動、および光近接効果が含まれる。
【０００５】
製造工程で生成される欠陥のある集積回路の数を削減し、したがって歩留まりを向上するように試みるときに、場合によっては数百もの処理ステップのうちの任意の１つまたは複数の処理ステップが、特定の回路の欠陥を引き起こした可能性があるという現実に直面す

る。このような多数の変数を扱う場合、特定の回路内の欠陥の正確な原因を判定することは非常に難しいことがあり、それによって、歩留まりを低下させるプロセス・オペレーションを識別し、補正することが非常に難しくなる。完成した集積回路の詳細な検査により、どのプロセス・オペレーションが回路の欠陥を引き起こした可能性があるかについてある徴候が得られることがある。しかし、検査装置はしばしば系統的な欠陥の源泉の多くを捕捉せず、かつ／またはツールは、効果的かつ確実に同調し、最適化し、または使用することが難しいことがある。さらに、特に最近の技術における検査装置は、しばしば多くの偽りの警報または妨害欠陥を受け、周知であるように、それらにより本当の欠陥または欠陥の源泉を確実に観測するためのどんな試行も妨害される。

【０００６】

特定の問題を製造サイクルの完了後の最終テストで識別した後に、特定のプロセス・オペレーションでの問題が、数週間または数カ月早いこともある、オペレーションが実施された時間に存在したということが確認される可能性があることが一般に分かっている。したがって、問題がずっと後になって補正される可能性がある。この時点では、異なるプロセス・オペレーションにより、問題が引き起こされる可能性がある。したがって、その後では、欠陥のある集積回路の事実分析、およびこれらの欠陥のある製品を引き起こすプロセス・オペレーションの識別は、集積回路の全体的歩留まりを改善するための手段としては非常に限られたものとなる。

【０００７】

事実分析の後に不具合をもたらさずに歩留まりを予測するためのいくつかの試行が行われているが、それらの成功の程度は様々である。したがって、集積回路製品の歩留まり予測のための改良型のシステムおよび方法が求められている。

【０００８】

（発明の概要）

集積回路の歩留まりを予測するためのシステムおよび方法は、最終的な集積回路製品に組み込むべき少なくとも１つのタイプのフィーチャ（特徴：ｆｅａｔｕｒｅ）を表す少なくとも１つのフィーチャを組み込む、少なくとも１つのタイプの特徴付けビヒクル（ｖｅｈｉｃｌｅ）を含む。この特徴付けビヒクルは、歩留まりモデルを生成するために、集積回路製品を製造する際に使用すべき製造サイクルを構成するプロセス・オペレーションのうちの少なくとも１つを受ける。この歩留まりモデルは、特徴付けビヒクルによって定義されるレイアウトを実施し、好ましくは、動作速度での電気的テスト・データの収集およびプロトタイプ・セクションのテストを容易にするフィーチャを含む。抽出エンジン（抽出装置：ｅｘｔｒａｃｔｉｏｎ　ｅｎｇｉｎｅ）は、提案される製品レイアウトから所定のレイアウト属性を抽出する。歩留まりモデルに対して操作して、この抽出エンジンは、レイアウト属性と、層または製造工程のステップごとの破壊に応じて歩留まり予測を生成する。次いでこれらの歩留まり予測を使用して、製造工程中のどのエリアを最も改良する必要があるかを判定する。

【０００９】

（詳細な説明）

次に図１を参照すると、本発明に従って集積回路歩留まりを予測するために、システム１０と総称するシステムによって実行されるステップを示すブロック図が示されている。システム１０は、少なくとも１つのタイプの特徴付けビヒクル１２を利用する。特徴付けビヒクル１２は、最終的製品に組み込むべき少なくとも１つのタイプのフィーチャを表す、少なくとも１つの特定のフィーチャを組み込む集積回路構造を構築するのに必要な情報を含むソフトウェアの形態であることが好ましい。例えば、特徴付けビヒクル１２は、考慮中のプロセス・フロー（ｐｒｏｃｅｓｓ　ｆｌｏｗ）の金属相互接続モジュールのヘルスおよび製造性を検出するための単一リソグラフィック層のショート・フロー（ｓｈｏｒｔ　ｆｌｏｗ）・テスト・ビヒクルを定義することができる。この構造は、製造中に製品に影響を与える可能性の高い様々な欠陥の取込みまたはフィンガープリント（ｆｉｎｇｅｒｐｒｉｎｔ）の信頼性を高めることが可能となるように十分大きくする必要があり、かつ

製造工程で動作する実際の製品または製品のタイプと同じくらいである必要がある。ショート・フローおよびショート・フローで実施される構造のより具体的な例および説明を以下で説明する。

【００１０】

ショート・フローは、集積回路製造サイクル中のプロセス・ステップの合計数の特定のサブセットを包含するものとして定義される。例えば、合計製造サイクルは４５０またはそれ以上のプロセス・ステップを含むことができるが、単一相互接続層の製造性を調査するために設計されるような特徴付けビヒクルは、少ない数、例えば１０～２５プロセス・ステップだけが含まれることになる。能動デバイスおよび複数の相互接続層は、歩留まりモデルを得るため、またはプロセス・フロー中の単一相互接続層に関連するこれらのステップに影響を与える欠陥の正確な診断を可能にするためには必要ではないからである。

【００１１】

特徴付けビヒクル１２は、提案される製品レイアウトの１つまたは複数の属性に一致するフィーチャを定義する。例えば、特徴付けビヒクル１２は、この特定の設計タイプに影響を与え、歩留まり損失を引き起こす可能性が高い欠陥を判定するために、提案される製品レイアウトを表すフィーチャ（例えば、線サイズ、間隔、および周期性、ライン・ベンドおよびランなど）を含む部分レイアウトを有するショート・フロー・テスト・ビヒクルを定義することができる。

【００１２】

特徴付けビヒクル１２は、デバイス性能およびプロセス・パラメータに関するレイアウト近隣のインパクトを調査するために、提案される設計の１つまたは複数の能動領域および隣接フィーチャを定義し、レイアウト属性に応じてデバイス・パラメータをモデル化し、製品性能と最良に相関するデバイスを決定することもできる。さらに、プロセス全体のすべてのモジュラ構成要素のすべての可能なサブセットまたは主要なサブセットの範囲が働くように、十分な数のショート・フロー・ビヒクルを構築し、解析することによって、製造される特定の製品に影響を与えることになる歩留まり問題のすべてではないとしても、その多くの完全な評価を明らかにし、モデル化し、および／または診断することができる。

【００１３】

製造中の製品に見られる可能性の高い歩留まり問題を評価し、診断するための情報を提供することに加えて、特徴付けビヒクルは、正確な歩留まり予測のために使用できる歩留まりモデル１６を生成するように設計される。これらの歩留まりモデルは、限定はしないが、製品計画と、プロセス全体にわたる歩留まり改善作業の優先順位付けと、製品自体の元の設計を変更してより良く製造できるようにすることを含む目的のために使用することができる。

【００１４】

本発明で企図される特徴付けビヒクル１２におけるテスト構造の大部分は、電気的テスト用に設計される。この目的で、各特徴付けビヒクルによって評価される、モジュール内の故障および欠陥を検出する信頼性は非常に高い。検査装置は、この高度な信頼性を達成し、または保証することができない。さらに、電気的テストが高速かつ安価であるので、データ収集の速度および量は、それぞれ非常に高速であり、大きい。このようにして、統計的に有意な診断および／または歩留まりモデルを実現することができる。

【００１５】

好ましくは、特徴付けビヒクル１２は、テープまたはディスク上のＧＤＳ２レイアウトの形態であり、次いでそれを使用してレチクル・セット（ｒｅｔｉｃｌｅ　ｓｅｔ）が生成される。レチクル・セットが製造サイクル１４の選択した部分の間で使用され、歩留まりモデル１６が生成される。したがって、歩留まりモデル１６は、特徴付けビヒクル１２によって定義されるレチクル・セットを使用する、選択した製造プロセス・ステップを受けたウェハの少なくとも一部から測定されるデータから構築されることが好ましい。

【００１６】

歩留まりモデル１６は、特徴付けビヒクルによって定義されるレイアウトを実施するだけでなく、製造プロセス・オペレーション自体によって導入されたアーチファクトも含む。歩留まりモデル１６は、プロトタイプ・アーキテクチャおよびレイアウト・パターン、ならびに動作速度での電気的テスト・データおよびテスト・プロトタイプ・セクション収集を容易にするフィーチャも含むことができる。これにより、歩留まり予測の正確さおよび信頼性が改善される。

【００１７】

抽出エンジン（抽出装置）１８は、提案される製品レイアウト２０からレイアウト属性を抽出し、この情報を歩留まりモデル１６に接続して製品歩留まり予測２２を得るためのツールである。このようなレイアウト属性は、例えばバイア冗長度（ｖｉａ　ｒｅｄｕｎｄａｎｃｙ）、臨界エリア、正味長さ分布、および線幅／スペース分布を含むことができる。次いで、提案される製品レイアウト２０からのレイアウト属性と、特徴付けビヒクル１２からの情報に基づいて製造された歩留まりモデル１６からのデータが与えられた場合、製品歩留まり２２が予測される。本発明のシステムおよび方法を使用して、得ることのできる予測可能な製品歩留まりは、定義された各属性、機能ブロックまたは層と関連する歩留まりとすることができ、あるいは製品レイアウト全体に関して結果として得られる歩留まり予測とすることができる。

【００１８】

次に図２を参照すると、抽出エンジン２８によって製品レイアウト２０から設計属性２６を抽出するための、フィードバック・ループ２４と総称するフィードバック・ループを追加で備える、本発明による集積回路歩留まり１０を予測するためのシステムのブロック図が示されている。本発明のこの特徴によれば、特徴付けビヒクル１２は、製品レイアウト２０の属性を使用して開発される。この場合、製品レイアウトの属性が抽出され、属性の範囲が特徴付けビヒクル１２中に確実に含まれるようにされる。例えば製品レイアウトが解析されて、線スペース分布、幅分布、密度分布、アイランド・パターンの数が決定され、実質上、製造工程の設計規則のセット全体のサブセットが開発される。このサブセットは、考慮中の特定の製品レイアウトに応用可能である。パターンに関しては、製品レイアウト分析により、最も共通するパターンが決定され、２番目に共通するパターンが決定され、以下同様である。これらは、抽出エンジン２８によって抽出され、特徴付けビヒクル１２中に含めるために、これらのパターンのすべてを包含する設計属性２６が生み出される。密度に関しては、製品レイアウトの分析により、最初の金属の密度が１０％～５０％であることが明らかとなった場合、特徴付けビヒクルは、最初の金属についての幅全体の１０％～５０％を含むことになる。

【００１９】

１つのタイプの特徴付けビヒクルは、金属ショート・フロー・特徴付けビヒクルである。金属ショート・フロー・特徴付けビヒクルの目的は、単一相互接続層の転写性および製造性を定量化することである。高い製品歩留まりのために重要である金属歩留まりは、しばしば得ることが非常に難しく、かつ、いくつかの独立な処理ステップだけからなるので、通常、金属ショート・フローはプロセスの非常に初期に実行される。金属ショート・フロー・マスクを使用するショート・フロー実験を実施することにより、迅速かつ連続的に実験および分析を実施することが可能となり、完全なフロー・ランが完了するまで待機する必要なく検出される、どんな系統的歩留まり問題または不定の欠陥歩留まり問題もなくなり、または最小となる。

【００２０】

図３を参照すると、一般的に３０で示された単一のリソグラフィック層からなる通常の金属ショート・フロー・マスクの例の画像が示されている。マスク３０はチップ上の単一の金属層を画定するために使用され、図３に示す例示のチップ３２はこの例では約２２ｍｍ×２２ｍのサイズであるステッパが収容できる大きさである。このチップは図４に示す４つの象限４２、４、４６および４８に分割され、前記各象限は以下の６つの基本構造の１つまたはそれ以上を含む。すなわち、（ｉ）ケルビン金属臨界寸法構造（Ｋｅｌｖｉｎ

ｍｅｔａｌ ｃｒｉｔｉｃａｌ ｄｉｍｅｎｓｉｏｎ ｓｔｒｕｃｔｕｒｅ）、（ｉｉ）スネークおよびコーム構造（ｓｎａｋｅ ａｎｄ ｃｏｍｂ ｓｔｒｕｃｔｕｒｅ）、（ｉｉｉ）ネスト欠陥サイズ分布構造（ｎｅｓｔ ｄｅｆｅｃｔ ｓｉｚｅ ｄｉｓｔｒｉｂｕｔｉｏｎ ｓｔｒｕｃｔｕｒｅ）、（ｉｖ）ファン・デル・ポー構造（Ｖａｎ ｄｅｒ Ｐａｕｗ ｓｔｒｕｃｔｕｒｅ）、（ｖ）ＯＰＣ評価構造（ＯＰＣ ｅｖａｌｕａｔｉｏｎ ｓｔｒｕｃｔｕｒｅ）、（ｖｉ）古典的走査型電子顕微鏡（ＳＥＭ）構造（ｃｌａｓｓｉｃａｌ ｓｃａｎｎｉｎｇ ｅｌｅｃｔｒｏｎ ｍｉｃｒｏｓｃｏｐｙ（ＳＥＭ）ｓｔｒｕｃｔｕｒｅ）である。

【００２１】

チップ・エリアの約５０％が欠陥サイズ分布の抽出のためのネスト構造に使用され、チップ・エリアの４０％が系統的な歩留まり損失機構の検出とパラメータ変動の測定に使用されている。図３はまたチップ上のパッド・フレーム３４のロケーションを示す。本明細書に記載する実施形態では、図５に示すように、チップ・カードプロセス上に１３１のパッド・フレームがあり、各パッド・フレーム３４は３２のパッドを含む。各パッド・フレーム３４内のパッドは後述する試験プログラムの必要に応じて外部試験装置が接触する電機接続点を提供する。

【００２２】

このチップで使用するファン・デル・ポー構造８２（図８参照）は構造の対称性を利用してシート抵抗を直接測定する４端子の正方形構造である。シート抵抗の高精度の判定は線幅変動の測定の要件である。ファン・デル・ポー構造８２は２つの異なるフレーム・タイプ、すなわち、混載フレーム６２（図６Ａ参照）とＶＤＰ１　６４（図６Ｂ参照）とに配置されている。図７は本明細書に記載する例示の金属ショート・フロー・チップ内のファン・デル・ポー構造を含むパッド・フレーム７２のロケーションを示す。この例示のチップ内では、ファン・デル・ポー構造はチップ面積の１％未満しか占有しない。ファン・デル・ポー構造内では、線幅（ＬＷ）とＬＷタップ（図８参照）とは変動するパラメータである。テーブル１は本明細書に記載する例示の金属ショート・フロー・チップ内のファン・デル・ポー構造の変動を示す。

【００２３】

【表１】

テーブル1（TABLE I）

LW (μm)	LW タップ (μm)
1 (DR)	1 (DR)
1.1	1.1
5	1
10	2
25	5
35	7
35	3.5
50	5

【００２４】

ネスト検出サイズ分布構造はオープンおよびショート検出と欠陥サイズ分布用に設計された入れ子式の連続的な線のアレイである。線幅と線間距離は欠陥サイズ分布の検出を容易

にするために変動するパラメータである。本明細書に記載する実施形態では、これらの構造は図９に示すロケーション９２および９４でチップ面積の５０％を占め、総計１０個のセル９６内に１４の変種を有する。これらの構造が占有できるエリアの量はウェーハあたり０．２５個以内の欠陥を高精度に検出できる大きさがなくてはならない．変種の数は通常、設計規則（ＤＲ）、ＤＲよりやや下、ＤＲよりやや上、ＤＲよりほぼ上を含む。したがって、例えば、ＤＲが線間距離で１０μｍの場合、プロットはテーブル２に示すように０．９、１．１、１．３および２．５についてである。

【００２５】

【表２】

テーブル2(TABLE II)

線幅＝線間距離

Line Width = Space (μm)	Length 長さ (cm)
0.9	39.6
1.0 (DR)	36
1.1	33
1.3	28.2
2.5	24.6

【００２６】

各セルは６つのサブセルに分割され、線抵抗を合理的なレベル（２５０ｋΩ未満）に低減し、セルあたりの多数の欠陥の発生を最小限にする。この実施形態では、セル当たり１６個のスネークがある。一般的に１００２で示す例示のネスト欠陥サイズ分布構造自体も図１０に示されている。ネスト欠陥サイズ分布構造は線幅（ＬＷ）が線間距離（Ｓ）に等しく、その後のデータ解析が容易になるように設計されている。

【００２７】

ケルビン金属臨界寸法（ＣＤ）構造は各端部で成端される連続的な直線からなる。これらの構造はファン・デル・ポー構造から決定されるシート抵抗に関連してケルビン線幅の決定が可能な高精度の線抵抗測定を可能にする。これらの構造は第１に電気的臨界寸法の変動を決定するために設計されている。一般的に１１０で示す例示のケルビン臨界寸法構造を図１１に示す。電気的臨界寸法変動可能性の光近接効果のインパクトを研究するため、ローカル近隣構造が変動する。ローカル近隣で変動するパラメータは線の番号１１２、線幅１１４、線間距離１１６である。ケルビン構造周辺の大域環境１１８も変動してまず電気的臨界寸法へのエッチング関連効果が研究される（図１１参照）。大域近隣（ｇｌｏｂａｌ　ｎｅｉｇｈｂｏｒｈｏｏｄ）で変動するパラメータは集積度とエリアである。大域近隣構造は他の電気的測定のニーズにも応えることができる。例えば、これらの構造の歩留まりを測定して環境に応じた金属臨界寸法だけでなく環境の関数としての歩留まりが得られる。図１２は本明細書に記載する金属ショート・フロー・チップ内のケルビン構造のロケーションを示す。これらのロケーションは使用可能なエリアを占有するように選択されている。テーブル３～９は本明細書に記載する金属ショート・フロー・チップ内のケルビン構造の変動を説明する。これらの値は図２２（ａ）～２２（ｂ）で識別したスペースを占有するように選択されている。例えば、パターン集積度は４５％付近に集中し、線幅と線間距離は１．０～３．３μｍの範囲内にある。これは例示の製品レイアウトの大半で集中する数字であるからである。

【００２８】

【表３】

テーブル3 (TABLE III)

Line Width (μm) (線幅)	Spacing (μm) (距離)	Number of Local Lines (ローカル線数)	Fixed Parameters (固定パラメータ)
0.75	0.75	6	Local line width = 1μm
0.9	0.9	ローカル線幅	Density = 45%
1μm (DR)	1.0 (DR)	集積度	Line width of comb = 1.3μm
1.1	1.1	コームの線幅	Dx 最大 max = 400 (μm)
1.3	1.3		Dy 最大 max = 400 (μm)
2.5	2.5		
3.3	3.0		
10	3.3		
	10		
	50		

【００２９】
【表４】

テーブル4 (TABLE IV)

Line Width (μm) (線幅)	Space ratio (距離比)	Number of Local Lines (ローカル線数)	Fixed Parameters (固定パラメータ)
0.75	2 to 1	6	Local line width = 1μm
0.9	3 to1	2	Density = 45%
1 (DR)		ローカル線幅	Line width of comb = 1.3μm
1.1		集積度	Dx 最大 max = 400 (μm)
1.3		コームの線幅	Dy 最大 max = 400 (μm)
2.5			
3.3			
10			

【００３０】
【表５】

テーブル5 (TABLE V)

Line Width (μm) 線幅	Number of Local lines ローカル線数	Local Line Width (μm) ローカル線幅	Spacing (μm) 距離	Fixed Parameters 固定パラメータ
0.75	1	1 (DR)	1 (DR)	Density = 0.45
0.9	2	1.3	1.3	Line width of comb = 1.3μm
1 (DR)	4		集積度	Dx 最大 max = 400 (μm)
1.1			コームの線幅	Dy 最大 max = 400 (μm)
1.3				
2.5				
3.3				
10				

【００３１】
【表６】

テーブル6 (TABLE VI)

Line Width (μm) 線幅	Spacing (μm) 距離	Number of local lines ローカル線数	Density 集積度	LW コーム comb (μm)	Fixed Parameters 固定パラメータ
1.0 (DR)	1.0(DR)	6	0	1.3	Dx 最大 max = 400 (μm)
1.3	1.3	2	0.2	10	Dy 最大 max = 400 (μm)
			0.40		
			0.45		
			0.50		

【００３２】
【表７】

テーブル7 (TABLE VII)

Line Width (μm) 線幅	Spacing (μm) 距離	Line width local (μm) ローカル線幅	Fixed Parameters 固定パラメータ
0.9	1.0 (DR)	10	Number of local lines 2
1.0 (DR)	1.1	30	Density 0.45
1.1	1.3	100	Line width comb 1.3
1.3	2.5	ローカル線数	Dx 最大 max = 400 (μm)
2.5	3.3	集積度	Dy 最大 max = 400 (μm)
3.3	10	コームの線幅	
10			

【００３３】
【表８】

テーブル8 (TABLE VIII)

Line Width (μm) 線幅	Spacing (μm) 距離	Fixed Parameters 固定パラメータ
1.0 (DR)	1.0 (DR)	Number of local lines 6 ローカル線数 6
1.1	1.1	Density - 0.45 密積度 - 0.45
1.3	1.3	Line width comb 1.3 コームの線幅
2.5	2.5	Dx_{max} (最大) = 400(μm)
10	3.0	Dy_{max} (最大) = 400(μm)
	5.3	Line width local 1.3 ローカル線幅 1.3

【００３４】
【表９】

テーブル9 (TABLE IX)

Line Width (μm) (線幅)	Spacing (μm) (距離)	Local density (ローカル集積度)	Dx_max (最大)	Fixed Parameters (固定パラメータ)	Comments (コメント)
0.75				Number of local lines 0 (ローカル線数) Density 0 (集積度) Line width comb 0 (コームの線幅) Line width local 0 (ローカル線幅) Dx_max = 400(μm)	Isolated Kelvins (隔離ケルビン)
0.9					
1.0 (DR)					
1.1					
1.3					
2.5			最大	Dy_max = 400 (μm) 最大	
3.3					
10					
	10	2.5		Line width = 1.0 (μm) (線幅) Local line width = 1.0 (μm) (ローカル線幅)	Local neighborhood size (ローカル近隣サイズ)
	20	3.5			
	30	4.5		Number of local lines 2 (ローカル線数) Density 0.45 (集積度) Comb line width 1.3 (コーム線幅) Dx_max = 400(μm) 最大 Dy_max = 400 (μm) 最大	
	40	5.5			
	50	6.5			
	60	7.5			
	70	8.5			
	80	9.5			
			25	Line width 1.0 (線幅) Line width local 1.0 (ローカル線幅) Space 1.0 (距離) Number of local lines 6 (ローカル線数) Density 0.45 (集積度) Line width comb 1.3 (コームの線幅) Dy_max 400 (μm)	Global neighborhood size (大域近隣サイズ)
			50		
			100		
			150		
			200		
			250		
			300		
Line Width (線幅)	Spacing (距離)	N_local (N_ローカル)	Dx_max 最大	Fixed Parameters (固定パラメータ)	Comments (コメント)
1.0 (DR)	1.0 (DR)	6	最大	D_local 5 (D_ローカル) Line width comb 1.3 (コーム線幅) 0.45	Standards (標準)
1.3	1.3	6			
1.0	40	2			
1.3	40	2			

【００３５】

スネーク、コームおよびスネーク＆コーム構造は主として各種パターンについでショートおよびオープンを検出するために設計されている。スネークは主としてオープンの検出に使用され、抵抗値の変動のモニタにも使用できる。コームはショートの検出に使用される。ショートおよびオープンは基本的な歩留まり損失機構であり、両方とも最小限にして高い製品歩留まりを得る必要がある。図１３は本明細書に記載する金属ショート・フロー・チップ内のスネークおよびコーム１３０２のロケーションを示す。象限１　１３０４も例えば図１４に示すケルビン構造内に入れ子になっているスネーク１４０２およびコーム１４０４を含む。図１４に示す線幅（ＬＷ）および線間距離（Ｓ）はショートおよびオープンに与えるインパクトを研究するためのこれらの構造上で変動するパラメータである。テーブル１０～１３は本明細書に記載する金属ショート・フロー・チップ内で使用されるスネークおよびコーム構造の変動を説明する。さらに、各パラメータは線幅、線間距離および集積度が占めるスペースが図２２（ａ）～２２（ｃ）に示す例示の製品レイアウトのそれと同様になるように選択されている。

【００３６】

【表１０】

テーブル10(TABLE X)

LW_comb (μm) (LW-コーム)	Space (μm) (距離)	LW_snake (μm) (LW-スネーク)	Fixed Parameters (固定パラメータ)
20	0.9	1.0 (DR)	Dx_max = 200 μm (最大) Dy_max = 400 μm (最大)
50	1.0 (DR)		
100	1.1		
200	1.3		
300	2.5		
	3.0		
	3.3		
	10		
20	1.3	1.3	
50	3.1		
100	3.3		
200	3.5		
300	10		

【００３７】

【表１１】

テーブル11(TABLE XI)

LW_comb (μm) (LW-コーム)	Space (μm) (距離)	Fixed Parameters (固定パラメータ)
0.75	0.75	Dx_max = 200 μm (最大) Dy_max = 400 μm (最大)
0.9	0.9	
1.0 (DR)	1.0 (DR)	
1.1	1.1	
1.3	1.2	
2.0	1.3	
3.3	2.5	
10	3.0	
	3.3	
	10	

【００３８】

【表１２】

テーブル12(TABLE XII)

Line Width (μm) (線幅)	Fixed Parameters 固定パラメータ
0.75	Dx_max = 200 μm (最大)
0.9	Dy_max = 400 μm (最大)
1.0 (DR)	10 μm
1.1	
1.3	
2.5	
3.3	
1.0	

【００３９】
【表１３】

テーブル13(TABLE XIII)

LW (μm)	Space (μm) (距離)	Fixed Parameters (固定パラメータ)
20	0.7	Dx_max = 400 μm (最大)
50	1.0 (DR)	Dy_max = 200 μm (最大)
100	1.1	
200	1.3	
500	2.5	
	2.7	
	3.0	
	3.3	
	5	
	10	

【００４０】
ボーダおよびフリンジ構造はショートに与える光近接補正（ＯＰＣ）構造のインパクトを研究するために設計されている。これらの光近接補正は普通バイア歩留まりを向上させるために追加される。ただし、これらのボーダがある、またはない金属ショート歩留まりを検査してショート歩留まりへの悪影響はないという確証が得られる。ボーダ１５０２は、図１５に示すように、両方共一般的に１５０４で示すコーム構造内のコーム線端部に配置される。図１６は本明細書に記載する金属ショート・フロー・チップ内の一般的に１６０２で示すボーダ構造のロケーションを示す。
【００４１】
走査型電子顕微鏡（ＳＥＭ）構造はトップ・ダウンまたは断面ＳＥＭによる線幅の非電気的測定に使用される。本明細書に記載する金属ショート・フロー・チップ内のＳＥＭバー

の場合、線幅は従来のＳＥＭ技法による線間距離と同じである。図１７は本明細書に記載する金属ショート・フロー・チップ内のＳＥＭ構造１７０２のロケーションを示す。これらの構造は図示の実施形態の各象限１７０４、１７０６、１７０８および１７１０の底部に配置されるが、これはこの位置でスペースが利用できるからである。

【００４２】

図３～１７と付随する説明で、金属歩留まりの向上のための例示の特徴付けビヒクルについて説明した。バイア、デバイス、ケイ化物、ポリ他のその他の特徴付けビヒクルが指定され使用されることが多い。ただし、それらを設計する手順と技法は同じである。図を見やすくするために、例示の金属特徴付けビヒクルを抽出エンジンおよび歩留まりモデル上で実現される。

【００４３】

抽出エンジン１８は２つの主要な目的を有する。すなわち、（１）特徴付けビヒクルを設計する際に使用するレベル（例えば、線幅、線間距離、集積度）の範囲を決定するのに用いる。（２）その後歩留まりモデル内で使用されて歩留まりを予測するための製品レイアウトの属性を抽出するために用いる。（１）は、特徴付けビヒクルの例でスネーク、コームおよびケルビン構造の線幅、線間距離および集積度の選択方法に関してすでに述べた。したがって、以下に主として（２）に関して説明する。

【００４４】

製品レイアウトから抽出できる属性の数はほぼ無限であるため、製品ごとにすべての属性を列挙または抽出することは不可能である。したがって、どの属性を抽出するかを案内するための手順が必要である。普通、特徴付けビヒクルはどの属性を抽出するか決定する。このプロセスは以下のステップを含む。

１．特徴付けビヒクル内のすべての構造を列挙する。

２．各構造をグループまたはファミリに分類してファミリ内のすべての構造が特定の属性についての実験を形成するようにする。例えば、上記の金属特徴付けビヒクルでは、ファミリ分類表は以下のようになる。

表

ファミリ	探索する属性
ネスト構造	２、３の線幅および線間距離での基本欠陥度
スネークおよびコーム	小さい線間距離に隣接する極めて大きい線幅と小さい線幅に隣接する極めて大きい線間距離とを含む広範囲の線幅と線間距離での歩留まり
ケルビンーＣＤ＋ファン・デル・ポー構造	集積度、線幅、および線間距離でのＣＤの変動
ボーダ構造	歩留まりに対する異なるＯＰＣスキームの影響

【００４５】

３．ファミリごとに、製品レイアウトからどの属性を抽出するか決定する。選択する属性はどの属性を探索するかという点から決定される。例えば、特定のファミリが異なる範囲の線間距離の歩留まりを探索する場合、線間距離または線間距離ごとのショート可能エリアのヒストグラムを抽出しなければならない。上記の例では、必要な属性リストは以下のようになる。

表

ファミリ	探索する属性	製品レイアウトから抽出する属性
（A）ネスト構造	2、3の線幅および線間距離での基本欠陥度	臨界エリア曲線
（B）スネークおよびコーム	．．．を含む広範囲の線幅と線間距離での歩留まり	特徴付けビヒクル内で探索した線幅および線間距離ごとのショート可能エリアおよび／またはインスタンス数
（C）ケルビンーＣＤ＋ファン・デル・ポー構造	集積度、線幅および線間距離でのＣＤの変動	パターン集積度、線幅および線間距離のヒストグラム（図２２の例と同様）
（D）ボーダ構造	歩留まりに対する異なるＯＰＣスキームの影響	製品レイアウトについて使用するため選択されたＯＰＣレイアウトごとのショート可能エリアまたはインスタンス数

【００４６】
４．前述したように、適当な歩留まりモデル内で抽出した属性を使用する。
【００４７】
その他の特徴付けビヒクルの場合、ファミリと必要な属性は明らかに異なる。ただし、手順および実施態様は上記の例と同様である。
【００４８】
前述したように、歩留まりモデル１６は好ましくは特徴付けビヒクル１２によって画定された網線セットを用いる選択された製作プロセスを経たウェーハの少なくとも一部から測定されたデータから構成される。好ましい実施形態では、歩留まりは不定および系統的な構成要素からなる製品としてモデル化される。
【数１】

$$Y = \left(\prod_{i=1}^{n} Ys_i \right) \left(\prod_{j=1}^{m} Yr_j \right)$$

【００４９】
Ys_i および Yr_j を決定する方法および技法について以下に説明する。
【００５０】
系統的歩留まりモデル化
極めて多くのタイプの系統的歩留まり損失機構があり、それらはメーカごとに異なるので、可能な系統的歩留まりモデルをすべて列挙することは実際的でない。以下に２つの極めて一般的な技法を説明し、特に本明細書に記載する特徴付けビヒクルと方法に限ってその技法の用例を示す。
【００５１】
エリア・ベースのモデル
エリア・ベース・モデルは次のように書かれる。
【数２】

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)}\right]^{A(q)/A_o(q)}$$

【００５２】
上式で、ｑは線幅、線間距離、長さ、線幅／線間距離の比、集積度などの特徴付けビヒクル内で探索する設計係数である。Ｙ。（ｑ）は特徴付けビヒクルからの設計係数ｑを備えた構造の歩留まりである。Ａ。（ｑ）はこの構造のショート可能エリア、Ａ（ｑ）は製品レイアウト上のタイプｑのすべてのインスタンスのショート可能エリアである。Ｙｒ（ｑ）は不定欠陥が歩留まり損失機構のみであろうと仮定した場合のこの構造の予測歩留まりである。この量を計算する手順を不定歩留まりモデル化に関連して以下に説明する。
【００５３】
ショート可能エリアの画定は図１８の例で最もよく示されている。このタイプの試験構造はメーカがｓの線間距離を備えた曲げを有する広い線を製造できるか否かを決定するために使用できる。例示の試験構造では、ショートは端子（１）と（２）の間に電圧を印加して端子（１）から（２）に流れる電流を測定することで測定される。この電流が指定のしきい値（普通１～１００ｎＡ）より大きい場合、ショートが検出される。ショート可能エリアは、ブリッジングが発生するとショートが測定されるエリアとして画定される。図１８の例では、ショート可能エリアはほぼｘ＊ｓ）である。Ａ（ｑ）項は製品レイアウト内の図１８に示すすべての出現する厳密なまたはほぼ厳密なパターン（すなわち、線間距離がｓで４５度に曲がった広い線）のショート可能エリアである。Ｙｒ（ｑ）項は下記の臨界エリア方法を用いるこの構造の不定歩留まり限界を予測することで抽出される。
【００５４】
このモデルの有効性は特徴付けビヒクル上に配置された構造の数と構造のサイズと同じ程度でしかないということを認識することが重要である。例えば、図１８に示す角度が付いた曲がり試験構造が特徴付けビヒクル上に配置されないかまたは意味がある歩留まり数を得るほどの回数配置されなかった場合、この製品レイアウト上で幅広い線の曲がりの歩留まり損失をモデル化する望みはないであろう。どれ位大きい試験構造をいくつ特徴付けビヒクル上に配置するかを厳密に定義するのは困難であるが、実際の経験から特徴付けビヒクル上の各試験構造の全ショート可能エリアは理想的にはＡ（ｑ）／Ａｏ（ｑ）＜１０を満たすべきである。
【００５５】
ショートは一般に複数のオープン歩留まり損失機構に広がっている傾向があるので上記の説明はショートについてであった。ただし、ショート可能エリアをオープン原因エリアと交換する限り、オープン歩留まり損失機構もこの歩留まりモデルで同様にモデル化できる。
【００５６】
インスタンス・ベースの歩留まりモデル
インスタンス・ベースの歩留まりモデルの一般的な形式は、
【数３】

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)}\right]^{N_i(q)/N_o(q)}$$

のようになる。
【００５７】
上式で、Ｙｏ（ｑ）およびＹｒ（ｑ）はエリア・ベースの歩留まりモデルと厳密に同じである。Ｎｉ（ｑ）は単位格子・パターンまたは特徴付けビヒクル上の試験パターンに酷似した単位格子・パターが製品レイアウト上に出現する回数である。Ｎｏ（ｑ）は単位格子・パターンが特徴付けビヒクル上に出現する回数である。

【００５８】
例えば、図１９は線間距離ｓ付近の線の端部のＴ型末端の歩留まりを検証する簡単な試験パターンを示す。この試験パターンは端子（１）と（２）の間に電圧を印加してショート電流を測定することで測定される。このパターンが特徴付けビヒクルのどこかで２５回繰り返されると、Ｎｏ（ｑ）は２５×５＝１２５となる。試験構造あたり５つの単位格子があるからである。
【００５９】
この単位格子が線間距離ｓで出現する回数が製品レイアウトから抽出されると、このタイプの構造の系統的な歩留まりを予測できる。例えば、各々の構造に５００の単位格子を備えた５つの構造がある場合、Ｎｏ（ｑ）＝２５００である。同じ製品のＮｉ（ｑ）が１０、０００の場合、９８．２０％の特徴付けビヒクル上の試験構造の歩留まりが測定された。下記の技法を用いて、Ｙｒ（ｑ）を９９．６７％と推定することができる。これらの数字を以下の式に代入して、
【数４】

$$Ys_i = \left[\frac{0.9820}{0.9967}\right]^{10000/2500} = 92.84\%$$

が得られる。
【００６０】
不定歩留まりモデル化
不定構成要素は、
【数５】

$$Y_r = e^{-\int_{x_0}^{\infty} CA(x)\times DSD(x)\,dx}$$

のように記述できる。
【００６１】
十分に記載されているかのようにこの詳細な説明に参照として組み込まれた「Ｍｏｄｅｌｉｎｇ ｏｆ Ｌｉｔｈｏｇｒａｐｈｙ Ｒｅｌａｔｅｄ Ｙｉｅｌｄ Ｌｏｓｓｅｓ ｆｏｒ ＣＡＤ ｏｆ ＶＳＬＩ Ｃｉｒｃｕｉｔｓ」、Ｗ．ｍａｌｙ、ＩＥＥＥ Ｔｒａｎｓ．ｏｎ ＣＡＤ、１９８５年７月、ｐｐ１６１～１７７にも記載されているように、上式で、ＣＡ（ｘ）は欠陥サイズｘの臨界エリア、ＤＳＤ（ｘ）は欠陥サイズ分布である。Ｘｏは確信を持って観察または測定できる最小欠陥サイズである。これは普通最小線間距離設計規則に設定される。臨界エリアはサイズｘの欠陥が存在する場合、ショートが発生するエリアである。極めて小さいＸの場合、臨界エリアは０付近であるが、極めて大きい欠陥サイズはチップの全エリアに近づく臨界エリアを有する。臨界エリアと抽出技法の別の説明は、すべて十分に記載されているかのようにこの詳細な説明に参照として組み込まれている、Ｐ．Ｋ．ＮａｇおよびＷ．Ｍａｌｙの「Ｙｉｅｌｄ Ｅｓｔｉｍａｔｉｏｎ ｏｆ ＶＬＳＩ Ｃｉｒｃｕｉｔｓ，」Ｔｅｃｈｃｏｎ９０、１９９０年１０月１６～１８日、Ｓａｎ Ｊｏｓｅ、Ｐ．Ｋ．ＮａｇおよびＷ．Ｍａｌｙの「Ｈｉｅｒａｃｈｉｃａｌ Ｅｘｔｒａｃｔｉｏｎ ｏｆ Ｃｒｉｔｉｃａｌ Ａｒｅａ ｆｏｒ Ｓｈｏｒｔｓ ｉｎ Ｖｅｒｙ Ｌａｒｇｅ ＩＣｓ」Ｐｒｏｃｅｅｄｉｎｇｓ ｏｆ ｔｈｅ ＩＥＥＥ Ｉｎｔｅｒｎａｔｉｏｎａｌ Ｗｏｒｋｓｈｏｐ ｏｎ Ｄｅｔｅｃｔ ａｎｄ Ｆａｕｌｔ Ｔｏｌｅｒａｎｃｅ ｉｎ ＶＬＳＩ Ｓｙｓｔｅｍｓ所収，ＩＥＥＥ Ｃｏｍｐｕｔｅｒ Ｓｏｃｉｅｔｙ Ｐｒｅｓｓ １９９５年、ｐｐ．１０～１８、Ｉ．Ｂｕｂｅｌ，Ｗ．Ｍａｌｙ，Ｔ．Ｗａａｓ，Ｐ．Ｋ．Ｎａｇ，Ｈ．ＭＨａｒｔｍａｎｎ，Ｄ．Ｓｃｈｍｉｔｔ－ＬａｎｄｓｉｅｄｅｌおよびＳ．Ｇｒｉｅｐの「ＡＦＦＣＣＡ：

A tool for Critical Area Analysis with Circular Defects and Lithography Deformed Layout」Proceedings of the IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems所収，IEEE Computer Society Press 1995年、pp．19～27、C．Ouyang およびW．Malyの「Efficient Extraction of Critical Area in Large VISI ICs」Proc．IEEE International Symposium on Semiconductor manufacturing、1996年、pp．301～304、C．Ouyang，W．Pleskaz、およびW．Malyの「Extraction of Critical Area for opens in Large VLSI Circuits」Proc．IEEE International Workshop on Detect and Fault Tolerance of VLSI Systems、1996年、pp．21～29に記載されている。

【0062】

欠陥サイズ分布はサイズがｘの欠陥の欠陥密度を表す。欠陥サイズ分布のための提案されているモデルは多数ある（例えば、共に十分に記載されているかのようにこの詳細な説明に参照として組み込まれているW．Malyの「Yield Models － Comparative Study」、Defect and Fault Tolerance in VLSI Systems，Ed．by C．Stapper他、Plenum Press，New York，1990年およびC．H．Stapperの「Modeling of Integrated Circuit Defect Sensitivities」、IBM J．Res．Develop．，Vol．27，No．6、1983年11月）。ただし、図を見やすくするために、最も一般的な分布式

【数６】

$$DSD(x) = \frac{D_o \times k}{x^p}$$

が使用される。上式で、Ｄｏは観察されたｘｏより大きい欠陥総数／ｃｍ^2 を表す。Ｐは欠陥のサイズが減衰する速度を表す単位がない値である。通常、ｐは２～４の間の数である。Ｋは正規化係数である。したがって、

【数７】

$$\int_{x_o}^{\infty} \frac{k}{x^p} dx = 1$$

となる。

【0063】

以下の２つの節で特徴付けビヒクルから欠陥サイズ分布を抽出する技法を説明する。

【0064】

ネスト構造技法

ネスト構造技法は欠陥サイズ分布を抽出するために設計されている。図２０に示すように、ネスト構造は線幅がｗ、線間距離がｓのＮ本の線で構成されている。この構造は線１と２、２と３、３と４、．．．、およびＮ－１、Ｎの間のショート電流を測定することで測定される。所与の仕様書の制限値を超える電流はすべてショートと見なされる。さらに、オープンは線１、２、３、の抵抗値を測定することで試験できる。一定の仕様書の制限値を超える抵抗はすべてオープン線と見なされる。いくつの線をショートさせるかを検証することで、欠陥サイズ分布を決定できる。

【００６５】
２本の線のみがショートされる場合、欠陥サイズはｓより大きく３ｗ＋２ｓを超えないことが必要である。欠陥がｓより小さければショートは発生しないが、３ｗ＋２ｓより大きい欠陥は少なくとも３本の線のショートを引き起こすことが保証される。ショートされる線の数ごとにサイズの間隔を作成できる。
【００６６】
【表１４】

Number Lines Shorted	Size Interval
2	s to 3w+2s
3	2s+w to 3s+4w
4	3s+2w to 4s+5w
...	...
N	(N-1)s+(N-2)w to (N)s+(N+1)w

【００６７】
前記間隔は重なることに留意すべきである。したがって、欠陥サイズ分布は直接計算できない。この制約はｐの抽出を制限するのみである。したがって、ｐを推定するために、すべての偶数番号の線、次にすべての奇数番号の線についてＰの予想値が計算される。最後に、２つの値を平均してｐを推定する。ｐを抽出すため、ｌｎ（ショートしたｘ本の線での欠陥数）対ｌｏｇ（［ｘ－１］ｓ＋［ｘ－２］ｗ）がプロットされる。この線の勾配は－ｐであることが分かる。Ｄｏ項は線の各グループで欠陥数をカウントし構造のエリアで割ることで抽出される。ただし、極めて大きいＤｏの場合、この推定は楽観的すぎる。試験構造と同様の構造から欠陥サイズ分布を抽出する手順に関する別の情報が例えば、十分に記載されているかのようにこの詳細な説明に参照として組み込まれたＪ．Ｋｈａｒｅ，Ｗ．ＭａｌｙおよびＭ．Ｅ．Ｔｈｏｍａｓの「Ｅｘｔｒａｃｔｉｏｎ ｏｆ Ｄｅｆｅｃｔ Ｓｉｚｅ Ｄｉｓｔｒｉｂｕｔｉｏｎ ｉｎ ａｎ ＩＣ ｌａｙｅｒ Ｕｓｉｎｇ Ｔｅｓｔ Ｓｔｒｕｃｔｕｒｅ Ｄａｔａ」、ＩＥＥＥ Ｔｒａｎｓａｃｔｉｏｎｓ ｏｎ Ｓｅｍｉｃｏｎｄｕｃｔｏｒｓ Ｍａｎｕｆａｃｔｕｒｉｎｇ」、ｐｐ．３５４～３６８、Ｖｏｌ．７、Ｎｏ．３、１９９４年８月に記載されている。
【００６８】
例として、１００のダイの１枚のウェーハからとった以下のデータを考える。
【００６９】
【表１５】

Number Lines Shorted	Number of Failures
2	98
3	11
4	4
5	2
6	1
7	0
8	0

【００７０】
構造サイズが１ｃｍ^{2}の場合、Ｄｏは９８＋１１＋４＋２＋１＝１３３／（１００＊１）＝１．３３欠陥／ｃｍ^{2}である。また、ログのプロット（欠陥数）対ｌｏｇ（［ｘ－１］ｓ＋［ｘ－２］ｗ）（図２１を参照）によってＰ＝２．０５が分かる。
【００７１】
コーム構造技法
線幅＝線間距離＝ｓのコームを仮定すると、この構造の歩留まりは、
【数８】

$$\ln[|\ln(Y)|] = \ln[-\int_{x_0}^{\infty} DSD(x)\times CA(x)dx] \propto (1-p)\times\ln(s)$$

として記述できることが分かる。
【００７２】
したがって、Ｉｎ［｜Ｉｎ（ｎ）｜］対Ｉｎ（ｓ）のプロットの勾配から、ｐを推定することができる。Ｄｏ抽出技法は上記と同じである。
【００７３】
歩留まりインパクトおよび評価
十分な数の特徴付けビヒクルが実行され、各特徴付けビヒクルについて歩留まり推定が行われると、その結果がスプレッドシートに表示されて歩留まり活動の優先順位付けが可能になる。テーブル１４～１６はそのようなスプレッドシートに含まれる情報の例である。スプレッドシートは金属歩留まり、ポリおよびアクティブ・エリア（ＡＡ）歩留まり（テーブル１４）、コンタクトおよびバイア歩留まり（テーブル１５）、およびデバイス歩留まり（テーブル１６）に分割されている。左側のカラムは系統的な歩留まり損失機構を示し、右側のカラムは不定歩留まり損失機構を示す。系統的欠陥機構の正確なタイプは製品や技術によって異なるが、例を表ＸＩＶ～ＸＶＩに示す。
【００７４】
普通、目標はスプレッドシートに列挙した各モジュールに対応する。モジュール歩留まりが目標から離れれば離れるほど、問題解決のためにより多くの強調とリソースとが向けられる。例えば、テーブル１４～１６に示す例の各モジュールについて目標が人為的に９５パーセントに設定されると、明らかに（$M_2 \rightarrow M_3$）バイア（７５．２％）とそれに続く同様のバイア（$M_1 \rightarrow M_2$）（８１．９２％）、M_1ショート（８２．２５％）、およびポリへのコンタクト（８７．２２％）が目標を下回り、バイア（$M_1 \rightarrow M_3$）が最大量の作業を必要とし、ポリが最小量の作業を必要とする。

【００７５】
各モジュール内で、最大歩留まり損失がどこにあるかを判定できる。すなわち、歩留まりを下げているのはある特定の系統的な機構なのか、単に不定の欠陥問題なのか、または２つの組み合わせなのか。例えば、テーブル１５に示すように、バイア（$M_2 \rightarrow M_3$）歩留まり損失はＭ３レベルのロング・メタル・ランナ（ｌｏｎｇ　ｍｅｔａｌ　ｒｕｎｎｅｒ）に接続されたバイアに関する系統的な問題（７７．４０％）によって支配される。（$M_1 \rightarrow M_2$）のバイアは不定欠陥問題（９２．４９％）に加えて同じ問題（９１．５２％）を抱えている。バイア（$M_1 \rightarrow M_2$）の歩留まり問題を解決するにはこれらの問題の両方を解決する必要がある。
【００７６】
テーブル１４に示すように、M_1 歩留まり損失は小さい線間距離に近い大きい線幅に影響を与える系統的な問題（９６．６６％）に加えて不定欠陥問題（８５．２３％）によっても支配される。金属１を改良するにはこれらの問題の両方を解決する必要がある。スプレッドシートの他のモジュールについても同様の結論を出すことができる。
【００７７】
最悪の歩留まりモジュールの場合、このモジュールの別の特徴付けビヒクルを頻繁に実行する必要がある。普通、モジュール歩留まりのこれらの改良を試行、改善、確認するためにこれらの特徴付けビヒクルを分割する。目標内のモジュールの場合、モジュール歩留まりの下降などの動きが現在までないことを確認するためにショート・フロー・特徴付けビヒクルの定期的なモニタがまだ必要である。ただし、知られている問題を抱えたモジュールと比較してこれらの特徴付けビヒクルは実行頻度を減らすことができる。
【００７８】
【表１６】

テーブル14（TABLE XIV）

オープンおよびショート（金属層） Opens and Shorts (Metal Layers)

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Do	P	Estimated Yield	
金属 Metal-1	Random Yield		重畳数	推定歩留	0.7 defects/cm^2	2.3	85.23%	
	Wide lines near small space	0.034		96.66%	欠陥			
	Wide space near small lines ①	0.00014		99.99%				
	Yield for OPC structures		72,341	99.86%				
	Bent lines		492	100.00%				
	Total for M1 M1総計						82.25%	
金属 Metal-2	Random Yield				0.35 defects/cm^:	1.92	97.45%	
	Wide lines near small space	0.00079		99.92%	欠陥			
	Wide space near small lines ①	0.000042		100.00%				
	Yield for OPC structures		1040372	97.94%				
	Bent lines		103	100.00%				
	Total for M2 M2総計						95.36%	
金属 Metal-3	Random Yield				0.25 defects/cm^:	2.02	96.92%	
	Wide lines near small space	0.0000034		100.00%	欠陥			
	Wide space near small lines ①	0		100.00%				
	Yield for OPC structures		352	100.00%				
	Bent lines		7942	99.92%				
	Total for M3 M3総計						96.84%	

オープンおよびショート（ポリおよびAA層） Open and Shorts (Poly and AA Layer)

ポリ Poly	Random Yield (without silicide)				0.17 defects/cm^:	2.03	99.81%	
	Random Yield (with silicide)				4.34defects/cm^:	4.56	89.54%	89.71% from silicide ケイ化物から
	Wide lines near small space	0		100.00%	欠陥			
	Wide space near small lines ②	0.01203		98.80%				
	Yield for OPC structures		0	100.00%				
	Bent lines 曲った線		786541	92.44%				
	Over wide AA 広いAA対象	0.034		96.66%				
	Over narrow AA 狭いAA対象	0.101		99.00%				
	Total for Poly ポリ総計						87.22%	
AA	Random Yield (without silicide)				1.3	3.45	99.12%	
	Random Yield (with silicide)				1.7	3.02	98.72%	99.60% from silicide ケイ化物から
	Wide lines near small space		10952	99.96%				
	Wide space near small lines ②		0	100.00%				
	Total for AA AA総計						98.70	

① 不定歩留（ランダムな歩留）
小さい距離に近い大きい線幅
小さい線幅に近い大きい距離
OPC構造の歩留

② 不定歩留（ケイ化物なし）
不定歩留（ケイ化物あり）
小さい距離に近い広い線幅
小さい線幅に近い大きい距離
OPC構造の歩留

【００７９】
【表１７】

テーブル15 (TABLE XV)

コンタクトおよびバイア Contacts and Vias

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield	
Contact to Poly	Random Yield (without silicide)				2.20E-09	3270432	99.28%	
	Random Yield (with silicide) ①				3.10E-09	3270432	98.99%	99.71%
	Yield for Long Runners (on M1)		11,921	100.00%				
	Yield for Long Runners (on Poly) ②		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts ③		7200	96.46%				
	Total for Contact to Poly ④						94.80%	
Contact to n+AA	Random Yield (without silicide)				2.20E-09	5270432	98.85%	
	Random Yield (with silicide) ①				3.10E-09	5270532	98.38%	99.53%
	Yield for Long Runners (on M1)		75,324	99.99%				
	Yield for Long Runners (on n+AA) ⑤		0	100.00%				
	Yield for Redundant Vias		4032007	99.60%				
	Yield for very isolated contacts ③		7200	99.93%				
	Total for Contact to AA (n+) ⑥						96.78%	
Contact to p+AA	Random Yield (without silicide)				2.20E-09	6093450	98.67%	
	Random Yield (with silicide) ①				3.10E-09	6093450	98.13%	
	Yield for Long Runners (on M1)		96,732	99.99%				
	Yield for Long Runners (on p+AA) ⑦		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts ③		7200	99.93%				
	Total for Contact to AA (p+) ⑧						96.74%	
Vias M1->M2	Random Yield (single vias) ⑨				1.10E-08	7093210	92.49%	
	Yield for Long Runners (M2) ⑩		88640	91.52%				
	Yield for Long Runners (M1) ⑪		97645	99.03%				
	Yield for Redundant Vias ⑫		11003456	96.91%				
	Yield for Isolated Vias ⑬		119582	96.81%				
	Total for Via M1-M2 ⑭						81.92%	
Vias M2->M3	Random Yield (single vias) ⑨				3.10E-09	4002063	98.77%	
	Yield for Long Runners (M3) ⑮		256128	77.40%				
	Yield for Long Runners (M2) ⑩		103432	96.97%				
	Yield for Redundant Vias ⑫		7096230	99.29%				
	Yield for Isolated Vias ⑬		1024	99.99%				
	Total for Via M2-M3 ⑯						75.12%	

① 不定歩留(ケイ化物なし)
不定歩留(ケイ化物あり)
ロング・ランナの歩留(M1上)
② ロング・ランナの歩留(ポリ上)
③ 冗長バイアの歩留
超隔離バイアの歩留
④ ポリへのコンタクト総数
⑤ ロング・ランナの歩留(n+AA上)
⑥ AAへのコンタクト総数(n+)
⑦ ロング・ランナの歩留(P+AA上)
⑧ AAへのコンタクト総数(P+)
⑨ 不定歩留(単一バイア)
⑩ ロング・ランナの歩留(M2)
⑪ ロング・ランナの歩留(M1)
⑫ 冗長バイアの歩留
⑬ 隔離バイアの歩留
⑭ バイアM1-M2総計
⑮ ロング・ランナの歩留(M3)
⑯ バイアM2-M3の歩留

【００８０】
【表１８】

テーブル16(TABLE XVI) 系統的な歩留損失メカニズム

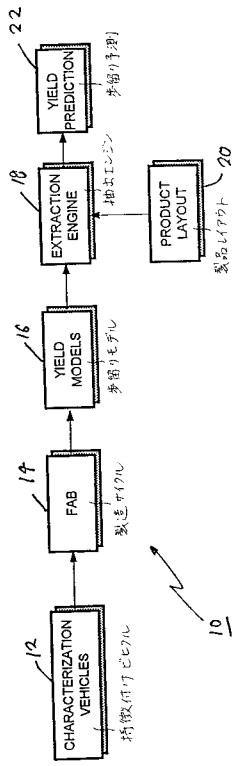
		デバイス Devices						
		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	欠陥率 Fault Rate	数 Number	Estimated Yield	
NMOS	Random Yield (Logic Xtor)				2.90E-09	1395228	99.60%	
	Random Yield (SRAM Xtor)				2.80E-09	2226720	99.38%	
	S/D Shorts				1.00E-09	3621948	99.64%	
	Bent Transistors		1113360	99.89%				
	Near Large AA		754000	99.92%				
	Near Small AA		1023452	99.90%				
	Total for NMOS Transistors						98.33%	
PMOS	Random Yield (Logic Xtor)				1.80E-09	1491003	99.73%	
	Random Yield (SRAM Xtor)				3.10E-09	1113360	99.66%	
	S/D Shorts				9.00E.10	2604363	99.77%	
	Bent Transistors		556680	99.94%				
	Near Large AA		789092	99.92%				
	Near Small AA		1309970	99.87%				
	Total for PMOS Transistors						98.89%	

① 不定歩留(論理Xtor) ② NMOSトランジスタ総計
不定歩留(SRAM Xtor) ③ PMOSトランジスタ総計
S/Dショート
曲ったトランジスタ
大きいAA付近
小さいAA付近

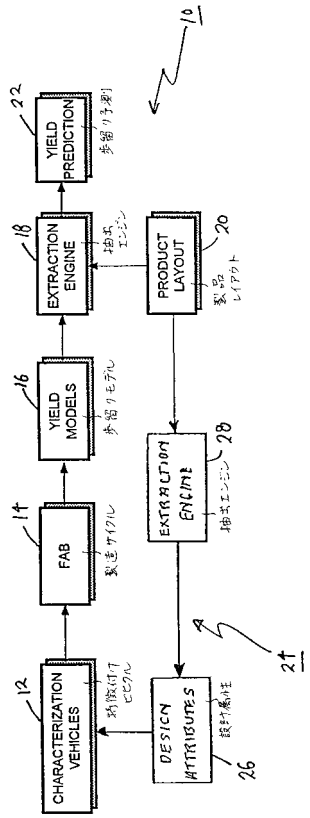
【図面の簡単な説明】
【図１】
本発明のシステムの好ましい実施形態によって実行されるステップを示すブロック図である。
【図２】
フィードバック・ループを実施するために、本発明のシステムによって実行される追加のステップを示すブロック図である。
【図３】
単一リソグラフィック層を備える例示的ショート・フロー・マスクのイメージである。
【図４】
例示的金属ショート・フロー・チップ上のパッド・フレームを示す図である。
【図５】
図４に示す各パッド・フレーム内のパッドを示す図である。
【図６】
２つのタイプの、ファン・デル・ポー構造を含むパッド・フレーム構造を示す図である。
【図７】
ファン・デル・ポー構造を含むパッド・フレームの、例示的チップ上の位置を示す図である。
【図８】
例示的ファン・デル・ポー構造を示す図である。
【図９】
例示的金属ショート・フロー・チップ上のネスト欠陥サイズ分布構造の例示的位置を示す図である。
【図１０】
例示的ネスト欠陥サイズ分布構造を示す図である。
【図１１】
例示的ケルビン臨界寸法構造を示す図である。
【図１２】

例示的金属ショート・フロー・チップ上のケルビン構造の例示的位置を示す図である。
【図１３】
例示的金属ショート・フロー・チップ上のおよびスネークおよびコームの例示的位置を示す図である。
【図１４】
例示的金属ショート・フロー・チップで使用される例示的スネークおよびコーム構造を示す図である。
【図１５】
例示的金属ショート・フロー・チップで使用されるボーダ構造の変形形態の例を示す図である。
【図１６】
例示的金属ショート・フロー・チップ上のボーダ構造の例示的位置を示す図である。
【図１７】
例示的金属ショート・フロー・チップ上の走査電子顕微鏡構造の例示的位置を示す図である。
【図１８】
ショート可能エリアを示す例示的テスト構造を示す図である。
【図１９】
線の端部のＴ字形末端の歩留まりを検査するための例示的テスト・パターンを示す図である。
【図２０】
欠陥サイズ分布を抽出するための例示的ネスト構造を示す図である。
【図２１】
サイズの変化に対する、欠陥の減少率を判定するためのプロットを示す図である。
【図２２】
図２２（ａ）、２２（ｂ）、２２（ｃ）は、サンプル製品レイアウトのメタル１層に関する線幅、線スペース、およびパターン密度分布をそれぞれ示す図である。

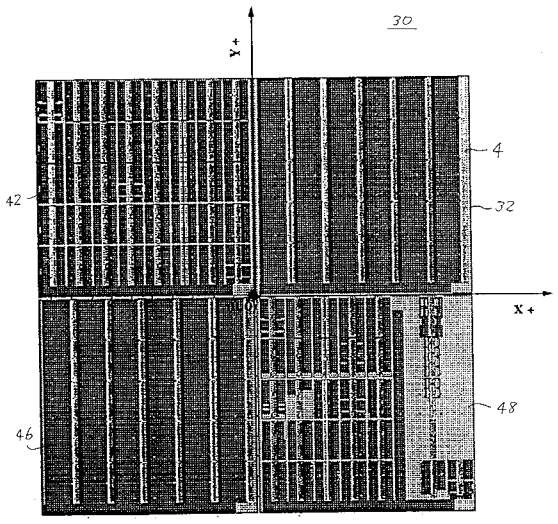
【図１】


22
YIELD PREDICTION
歩留り予測
18
EXTRACTION ENGINE
抽出エンジン
PRODUCT LAYOUT
20
製品レイアウト
16
YIELD MODELS
歩留りモデル
14
FAB
製造サイクル
12
CHARACTERIZATION VEHICLES
特徴付けビヒクル
10

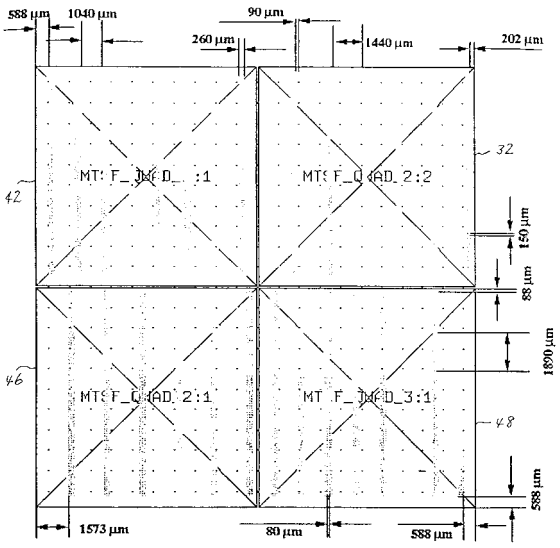
【図２】


10
22
YIELD PREDICTION
歩留り予測
18
EXTRACTION ENGINE
抽出エンジン
PRODUCT LAYOUT
20
製品レイアウト
16
YIELD MODELS
歩留りモデル
14
FAB
製造サイクル
28
EXTRACTION ENGINE
抽出エンジン
12
CHARACTERIZATION VEHICLES
特徴付けビヒクル
DESIGN ATTRIBUTES
設計属性
26
24

【図３】


30
Y+
X+
4
32
42
46
48

【図４】


588 μm
1040 μm
90 μm
260 μm
1440 μm
202 μm
42
32
MTS F_QUAD_2:2
MTS F_QUAD_2:1
MTS F_QUAD_3:1
46
48
150 μm
88 μm
1890 μm
588 μm
1573 μm
80 μm
588 μm

【図５】

【図６】

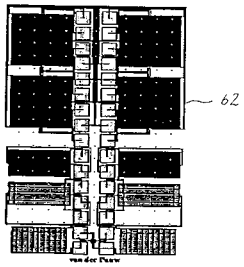
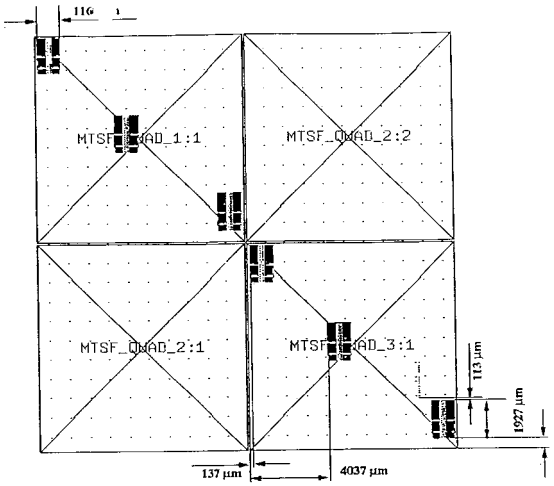


図６Ａ

図６Ｂ

【図７】



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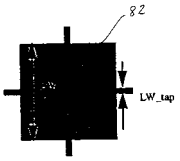

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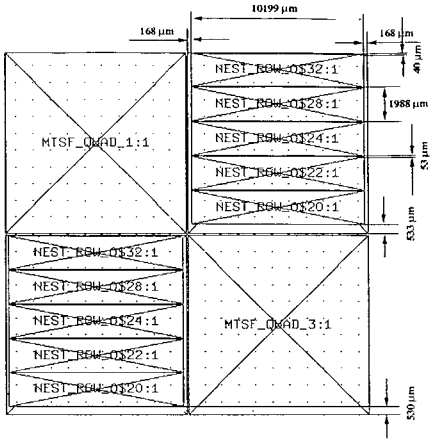

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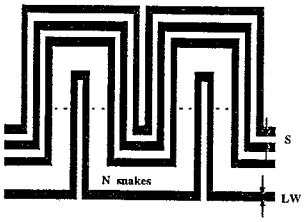

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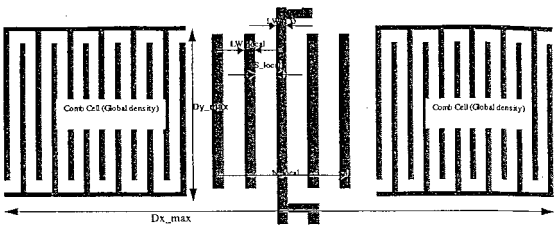

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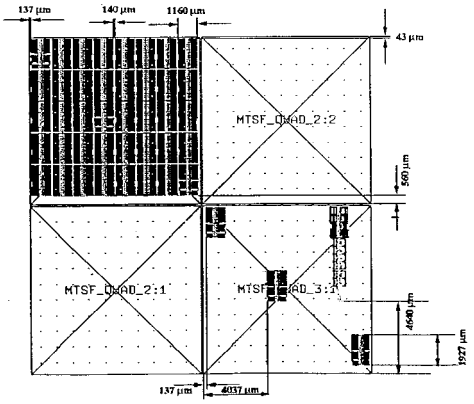

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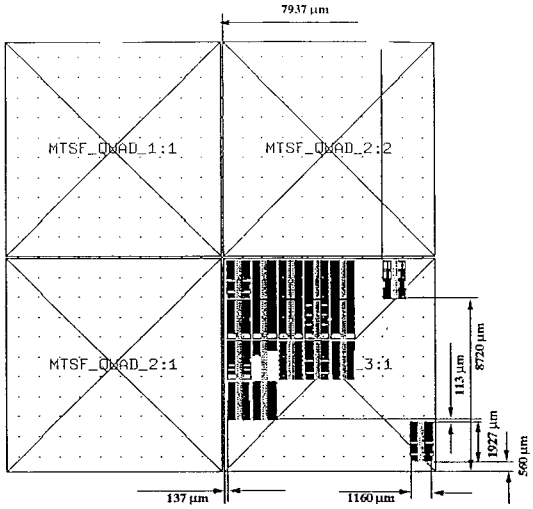

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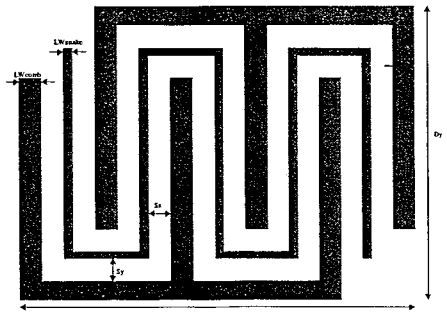

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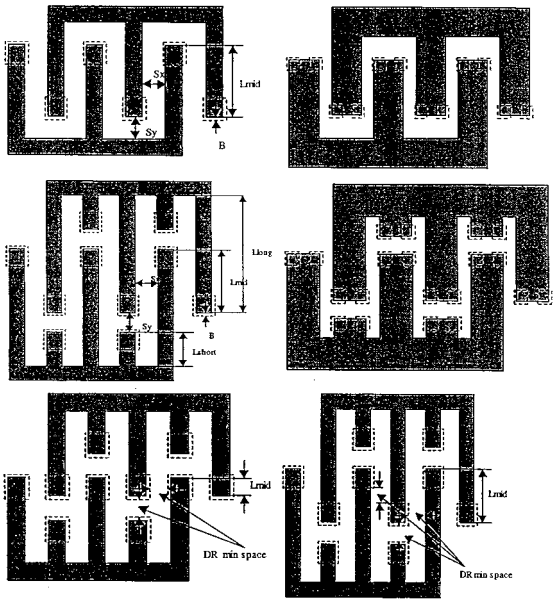

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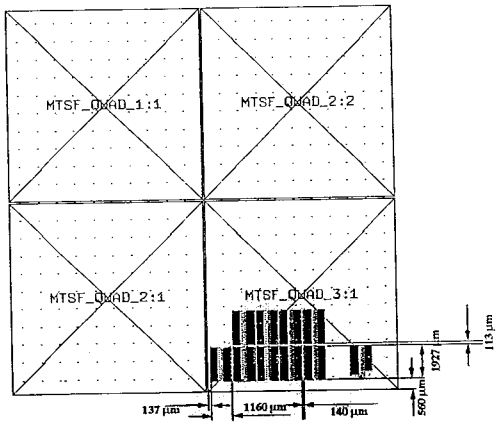

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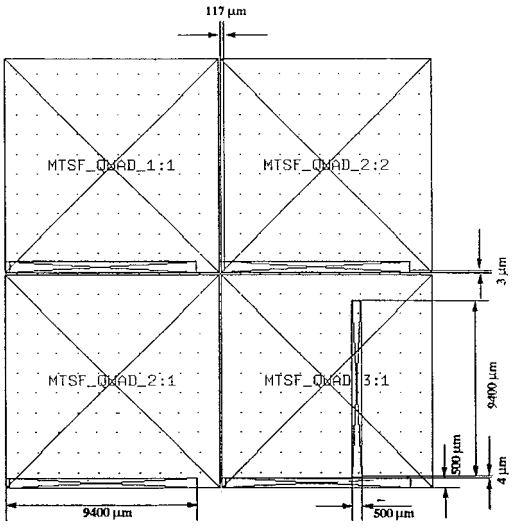
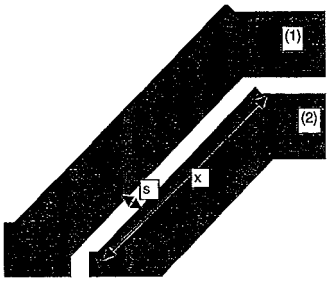


【図１８】



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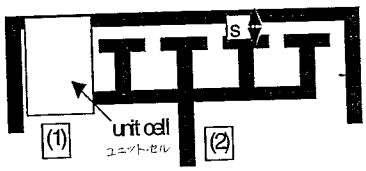
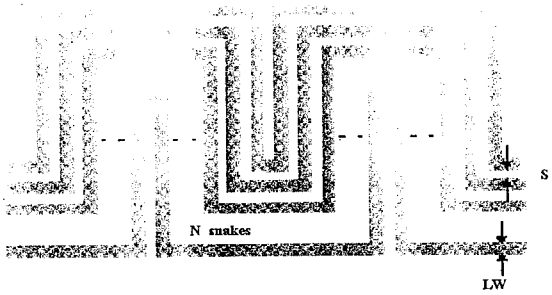
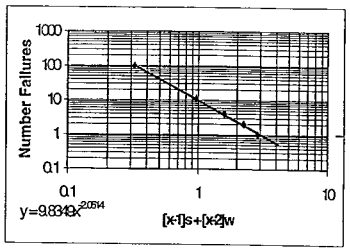


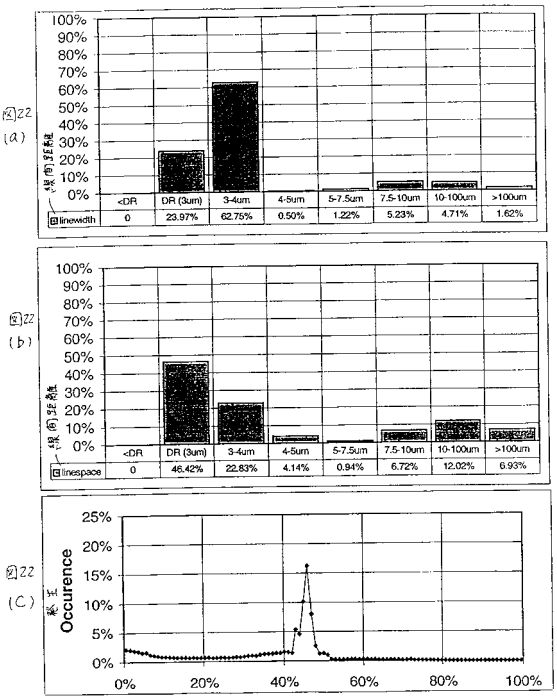
【図２０】



【図２１】



【図２２】



【国際公開パンフレット】

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 May 2001 (25.05.2001)

PCT

(10) International Publication Number
WO 01/35718 A2

(51) International Patent Classification: Not classified

(21) International Application Number: PCT/US00/31665

(22) International Filing Date:
17 November 2000 (17.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/442,699 18 November 1999 (18.11.1999) US

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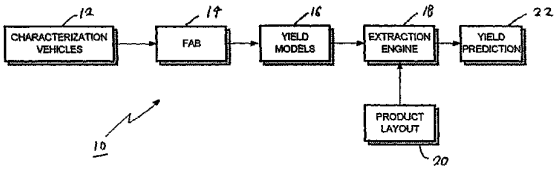
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *Without international search report and to be republished upon receipt of that report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION



(57) Abstract: A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the caracterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype section at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

WO 01/35718 A2

SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION

Background of the Invention

The present invention pertains to fabrication of integrated circuits and more particularly to systems and methods for improving fabrication yields.

The fabrication of integrated circuits is an extremely complex process that may involve hundreds of individual operations. Basically, the process includes the diffusion of precisely predetermined amounts of dopant material into precisely predetermined areas of a silicon wafer to produce active devices such as transistors. This is typically done by forming a layer of silicon dioxide on the wafer, then utilizing a photomask and photoresist to define a pattern of areas into which diffusion is to occur through a silicon dioxide mask. Openings are then etched through the silicon dioxide layer to define the pattern of precisely sized and located openings through which diffusion will take place. After a predetermined number of such diffusion operations have been carried out to produce the desired number of transistors in the wafer, they are interconnected as required by interconnection lines. These interconnection lines, or interconnects as they are also known, are typically formed by deposition of an electrically conductive material which is defined into the desired interconnect pattern by a photomask, photoresist and etching process. A typical completed integrated circuit may have millions of transistors contained with a 0.1 inch by 0.1 inch silicon chip and interconnects of submicron dimensions.

In view of the device and interconnect densities required in present day integrated circuits, it is imperative that the manufacturing processes be carried out with utmost precision and in a way that minimizes defects. For reliable operation, the electrical characteristics of the circuits must be kept within carefully controlled limits, which implies a high degree of control over the myriad of operations and fabrication processes. For example, in the photoresist and photomask operations, the presence of contaminants such as dust, minute scratches and other imperfections in the patterns on the photomasks can produce defective patterns on the semiconductor wafers, resulting in defective integrated circuits. Further, defects can be introduced in the circuits during the diffusion operations themselves. Defective circuits may be identified both by visual inspection under high magnification and by electrical tests. Once defective integrated circuits have been identified, it is desired to take steps to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield of the integrated circuits meeting specifications.

In the past, many of the defects which caused poor yield in integrated circuits were caused by particulate contaminants or other random sources. Increasingly, many of the defects seen in modern integrated circuit processes are not sourced from particulates or random contaminants, especially in the earlier stages of process development or yield ramping, but rather stem from very systematic sources. Examples of these systematic defect sources include printability problems from using aggressive lithography tools, poly stringers from poorly formed silicides, gate length variation from density driven and optical proximity effects.

In attempting to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield, one is faced with the fact that any one or more of possibly several hundred processing steps may have caused a particular circuit to be defective. With such a large number of variables to work with, it can be extremely difficult to determine the exact cause or causes of the defect or defects in a particular circuit thereby making it extraordinarily difficult to identify and correct the yield detracting process operations. Detailed inspection of the completed integrated circuits may provide some indication of which process operation may have caused the circuits to be defective. However, inspection equipment often does not capture many of the systematic defect sources and/or the tools can be difficult to tune, optimize, or use effectively and reliably. Furthermore, inspection equipment, especially in recent technologies is often plagued with many false alarms or nuisance defects, as they are known, which serve to frustrate any attempts to reliably observe true defects or sources of defects.

It is typically discovered that, once a particular problem has been identified at final test after completion of the fabrication cycle, it can be confirmed that a problem in a particular process operation did exist at the time that operation was carried out, which could have been weeks or even months earlier. Thus the problem might be corrected well after the fact. At this time, different process operations may be causing problems. Thus, after the fact analysis of defective integrated circuits and identification of process operations causing these defective products is severely limited as a means for improving the overall yield of integrated circuits.

A number of attempts to predict yields instead of conducting unsatisfactory after the fact analysis have been made with varying degrees of success. Thus, there is a need for an improved system and method for integrated circuit product yield prediction.

SUMMARY OF THE INVENTION

A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the characterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype sections at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram depicting the steps performed by a preferred embodiment of the system of the present invention.

FIGURE 2 is a block diagram depicting additional steps performed by the system of the present invention to effect a feedback loop.

FIGURE 3 is an image of an illustrative short flow mask comprising a single lithographic layer.

FIGURE 4 depicts pad frames on an exemplary metal short flow chip.

FIGURE 5 depicts pads within each pad frame depicted in FIGURE 4.

FIGURE 6 depicts two types of pad frame structures which contain van der Pauw structures.

FIGURE 7 depicts locations, on the exemplary chip, of the pad frames containing the van der Pauw structures.

FIGURE 8 depicts an exemplary van der Pauw structure.

FIGURE 9 depicts exemplary locations of nest defect size distribution structures on an exemplary metal short flow chip.

FIGURE 10 depicts an exemplary nest defect size distribution structure.

FIGURE 11 depicts an exemplary Kelvin critical dimension structure.

FIGURE 12 depicts exemplary locations of Kelvin structures on an exemplary metal short flow chip.

FIGURE 13 depicts exemplary locations of snakes and combs on an exemplary metal short flow chip.

FIGURE 14 depicts exemplary snake and comb structures used in an exemplary metal short flow chip.

FIGURE 15 depicts examples of variations of border structures used in an exemplary metal short flow chip.

FIGURE 16 depicts exemplary locations of border structures on an exemplary metal short flow chip.

FIGURE 17 depicts exemplary locations of scanning electron microscope structures on an exemplary metal short flow chip.

FIGURE 18 depicts an exemplary test structure illustrating a shortable area.

FIGURE 19 depicts an exemplary test pattern for examining the yield of T-shaped endings at the ends of lines.

FIGURE 20 depicts an exemplary nest structure for extracting defect size distributions.

FIGURE 21 depicts a plot for determining the rate at which defects decay over size.

FIGURE 22(a), 22(b) and 22(c) depict, respectively, linewidth, linespace and pattern density distributions for a metal-1 layer of a sample product layout.

DETAILED DESCRIPTION

Referring now to Figure 1, there is shown a block diagram depicting the steps performed by a system, generally designated 10, for predicting integrated circuit yields in accordance with the present invention. The system 10 utilizes at least one type of characterization vehicle 12. The characterization vehicle 12 preferably is in the form of software containing information required to build an integrated circuit structure which incorporates at least one specific feature

representative of at least one type of feature to be incorporated into the final product. For example, the characterization vehicle 12 might define a short flow test vehicle of a single lithographic layer for probing the health and manufacturability of the metal interconnection module of the process flow under consideration. The structures need to be large enough and similar enough to the actual product or type of products running in the fabrication process to enable a reliable capture or fingerprint of the various maladies that are likely to affect the product during the manufacturing. More specific examples and descriptions of short flows and the structures embodied in them are described below.

Short flow is defined as encompassing only a specific subset of the total number of process steps in the integrated circuit fabrication cycle. For example, while the total fabrication cycle might contain up to 450 or more process steps, a characterization vehicle such as one designed to investigate manufacturability of a single interconnection layer would only need to include a small number, for example 10 to 25 process steps, since active devices and multiple interconnection layers are not required to obtain a yield model or allow accurate diagnosis of the maladies afflicting these steps associated with a single interconnection layer in the process flows.

The characterization vehicle 12 defines features which match one or more attributes of the proposed product layout. For example, the characterization vehicle 12 might define a short flow test vehicle having a partial layout which includes features which are representative of the proposed product layout (e.g. examples of line size, spacing and periodicity; line bends and runs;

etc.) in order to determine the maladies likely afflicting those specific design types and causing yield loss.

The characterization vehicle 12 might also define one or more active regions and neighboring features of the proposed design in order to explore impact of layout neighborhood on device performance and process parameters; model device parameters as a function of layout attributes; and determine which device correlate best with product performance. Furthermore, by constructing and analyzing a sufficient number of short flow vehicles such that the range of all possible or a major subset of all the modular components of the entire process is exercised, a full evaluation of many if not all of the yield problems which will afflict the specific product manufactured can be uncovered, modeled, and/or diagnosed.

In addition to providing information for assessing and diagnosing yield problems likely to be seen by the product(s) under manufacture, the characterization vehicle is designed to produce yield models 16 which can be used for accurate yield prediction. These yield models 16 can be used for purposes including, but not limited to, product planning, prioritizing yield improvement activities across the entire process, and modifying the original design of the product itself to make it more manufacturable.

The majority of the test structures in the characterization vehicle 12 contemplated in the invention are designed for electrical testing. To this end, the reliability of detecting faults and defects in the modules evaluated by each characterization vehicle is very high. Inspection

equipment cannot deliver or promise this high degree of reliability. Furthermore, the speed and volume of data collection is very fast and large respectively since electrical testing is fast and cheap. In this way, statistically valid diagnosis and/or yield models can be realized.

The characterization vehicle 12 is preferably in the form of a GDS 2 layout on a tape or disc which is then used to produce a reticle set. The reticle set is used during the selected portions of the fabrication cycle 14 to produce the yield model 16. Thus the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12.

The yield model 16 not only embodies the layout as defined by the characterization vehicle, it also includes artifacts introduced by the fabrication process operations themselves. The yield model 16 may also include prototype architecture and layout patterns as well as features which facilitate the gathering of electrical test data and testing prototype sections at operating speeds which enhances the accuracy and reliability of yield predictions.

An extraction engine 18 is a tool for extracting layout attributes from a proposed product layout 20 and plugging this information into the yield model 16 to obtain a product yield prediction 22. Such layout attributes might include, for example, via redundancy, critical area, net length distribution, and line width/space distribution. Then, given layout attributes from the proposed product layout 20 and data from yield models 16 which have been fabricated based

upon information from the characterization vehicles 12, product yield 22 is predicted. Using the system and method of the present invention, the predictable product yield obtainable can be that associated with each defined attribute, functional block, or layer, or the resultant yield prediction for the entire product layout.

Referring now to Figure 2, there is shown a block diagram of the system for predicting integrated circuit yields 10 in accordance with the present invention additionally comprising a feedback loop, generally designated 24, for extracting design attributes 26 from product layout 20 by means of extraction engine 28. In accordance with this feature of the present invention, the characterization vehicle 12 is developed using attributes of the product layout 20. In this case, attributes of the product layout are extracted, making sure that the range of attributes are spanned in the characterization vehicle 12. For example, the product layout is analyzed to determine line space distribution, width distribution, density distribution, the number of island patterns, in effect developing a subset of the entire set of design rules of the fabrication process, which subset is applicable to the particular product layout under consideration. With respect to patterns, the product layout analysis would determine the most common pattern, the second most common pattern, and so forth. These would be extracted by the extraction engine 28 yielding design attributes 26 encompassing all of these patterns for inclusion into the characterization vehicle 12. With respect to densities, if the analysis of the product layout reveals that the density of a first metal is from 10% to 50%, then the characterization vehicle would include the entire range of 10% to 50% for the first metal.

One type of characterization vehicle is a metal short flow characterization vehicle. The purpose of the metal short flow characterization vehicle is to quantify the printability and manufacturability of a single interconnect layer. Usually a metal short flow is run very early in the process since metal yield is crucial for high product yield, is often very difficult to obtain, and consists of only a few independent processing steps. Conducting short flow experiments using a metal short flow mask, enables experiments and analysis to be carried out in rapid succession to eliminate or minimize any systematic yield or random defect yield issue that is detected without having to wait for complete flow runs to finish.

Referring to Figure 3, there is shown an image of a typical and illustrative metal short flow mask, generally designated 30, which consists of a single lithographic layer. The mask 30 is used to define a single metal layer on a chip, and the exemplary chip 32 depicted in Figure 3 is as large as the stepper can accomodate which is, in this example, approximately 22 mm x 22 mm in size. It is divided into four quadrants, 42, 4, 46 and 48 as shown in Figure 4, each containing one or more of six basic structures: (i) Kelvin metal critical dimension structures; (ii) snake and comb structures; (iii) nest defect size distribution structures; (iv) van der Pauw structures; (v) OPC evaluation structures; and (vi) classical scanning electron microscopy (SEM) structures.

Approximately 50% of the chip area is devoted to nest structures for extraction of defect size distribution while 40% of the chip area is devoted to detecting systematic yield loss mechanisms and measuring parametric variation. Figure 3 also depicts the location of pad frames 34 on the chip. In the embodiment described herein, there are 131 pad frames on the chip, with

each pad frame 34 comprising thirty-two pads as shown in Figure 5. The pads within each pad frame 34 provide electrical connection points which are contacted by external test equipment as required by a test program to be described later.

The van der Pauw test structures 82 used in this chip (see Figure 8) are four terminal square structures which take advantage of the symmetry of the structure for direct determination of the sheet resistance. Accurate determination of sheet resistance is a requirement for measurement of linewidth variation. The van der Pauw structures 82 are arranged in two different frame types: mixed 62 (see Figure 6A) and VDP 1 64 (see Figure 6 B). Figure 7 depicts the location of the pad frames 72 containing the van der Pauw structures in the exemplary metal short flow chip described herein. In this exemplary chip, the van der Pauw structures occupy less than 1% of the chip area. In the van der Pauw structures the line width (LW) and the LW tap (see Figure 8) are the parameters that are varied. Table I shows the variations in the van der Pauw structures in the exemplary metal short flow chip described herein.

TABLE I

LW (μm)	LW tap (μm)
1 (DR)	1 (DR)
1.1	1.1
5	1
10	2
25	5
35	7
35	3.5
50	5

The nest defect size distribution structures are arrays of nested continuous lines designed for opens and shorts detection and for the extraction of defect size distribution. Line width and space between the line are the parameters that are varied to facilitate the extraction of defect size distribution. In the embodiment described herein, these structures occupy 50% of the chip area at locations 92 and 94 shown in Figure 9 and have fourteen variants in a total of ten cells 96. The amount of area these structures can occupy needs to be large enough to accurately detect less than 0.25 defects/cm^2 for one wafer. The number of variants typically include the design rule (DR), slightly below DR, slightly above DR and substantially above DR. Therefore, for example, if DR is 1.0 μm for line spacing, the plots might be for 0.9, 1.1, 1.3 and 2.5 as shown in Table II.

TABLE II

Line Width = Space (μm)	Length (cm)
0.9	39.6
1.0 (DR)	36
1.1	33
1.3	28.2
2.5	24.6

Each cell is split into six sub-cells to reduce the line resistance to reasonable levels (less than 250 kΩ) and to minimize the incidence of multiple defects per cell. In this embodiment, there are sixteen snakes per cell. An exemplary nest defect size distribution structure itself, generaly designated 1002, is depicted in Figure 10. The nest defect size distribution structures are designed such that the line width (LW) is equal to the spacing (S) between the lines to simplify subsequent analysis of data.

The Kelvin metal critical dimension (CD) structures are made up of a continuous straight line with terminal connections at each end. These structures allow for precise line resistance measurements which, in conjunction with the sheet resistance determined from the van der Pauw structures, allow for the determination of Kelvin line width. These structures are designed primarily to determine the variation in the electrical critical dimension. An exemplary Kelvin critical dimension structure, generally designated 110, is depicted in Figure 11. To study the impact of optical proximity effect on the variability in the electrical critical dimension, local neighborhood structures are varied. The parameters varied for the local neighborhood are the

number 112, line width 114 and space 116 of the lines. The global environment 118 around the Kelvin structures is also varied, primarily to study etch related effects on the electrical critical dimension (see Figure 11). Parameters varied for global neighborhood are the density and area. The global neighborhood structures can also serve other electrical measurement needs. For example, the yield of these structures can be measured so that not only metal critical dimension as a function of environment is obtained, but also yield as a function of environment. Figure 12 depicts the location of Kelvin structures 122 in the metal short flow chip described herein. These locations are chosen to cover available area. Tables III through IX describe the variations in the Kelvin structures used in the metal short flow chip described herein. These values were chosen as to cover the space identified in Figure 22(a) through 22(b). For example, the pattern density is centered around 45% and the line width and spaces are in the range of 1.0 to 3.3 μm since this is where most of an exemplary product layout is centered.

TABLE III

Line Width (μm)	Spacing (μm)	Number of Local Lines	Fixed Parameters
0.75	0.75	6	Local line width = 1μm
0.9	0.9		Density = 45%
1μm (DR)	1.0 (DR)		Line width of comb = 1.3μm
1.1	1.1		Dx max = 400 (μm)
1.3	1.3		Dy max = 400 (μm)
2.5	2.5		
3.3	3.0		
10	3.3		
	10		
	50		

TABLE IV

Line Width (μm)	Space ratio	Number of Local Lines	Fixed Parameters
0.75	2 to 1	6	Local line width = 1μm
0.9	3 to1	2	Density = 45%
1 (DR)			Line width of comb = 1.3μm
1.1			Dx max = 400 (μm)
1.3			Dy max = 400 (μm)
2.5			
3.3			
10			

TABLE V

Line Width (μm)	Number of Local lines	Local Line Width (μm)	Spacing (μm)	Fixed Parameters
0.75	1	1 (DR)	1 (DR)	Density = 0.45
0.9	2	1.3	1.3	Line width of comb = 1.3μm
1 (DR)	4			Dx max = 400 (μm)
1.1				Dy max = 400 (μm)
1.3				
2.5				
3.3				
10				

TABLE VI

Line Width (μm)	Spacing (μm)	Number of local lines	Density	LW comb (μm)	Fixed Parameters
1.0 (DR)	1.0(DR)	6	0	1.3	Dx max = 400 (μm)
1.3	1.3	2	0.2	10	Dy max = 400 (μm)
			0.40		
			0.45		
			0.50		

TABLE VII

Line Width (μm)	Spacing (μm)	Line width local (μm)	Fixed Parameters
0.9	1.0 (DR)	10	Number of local lines 2
1.0 (DR)	1.1	30	Density 0.45
1.1	1.3	100	Line width comb 1.3
1.3	2.5		Dx max = 400 (μm)
2.5	3.3		Dy max = 400 (μm)
3.3	10		
10			

TABLE VIII

Line Width (μm)	Spacing (μm)	Fixed Parameters
1.0 (DR)	1.0 (DR)	Number of local lines 6
1.1	1.1	Density - 0.45
1.3	1.3	Line width comb 1.3
2.5	2.5	Dx_max = 400(μm)
10	3.0	Dy_max = 400(μm)
	5.3	Line width local 1.3

TABLE IX

Line Width (μm)	Spacing (μm)	Local density	Dx_max	Fixed Parameters	Comments
0.75				Number of local lines 0	Isolated Kelvins
0.9				Density 0	
1.0 (DR)				Line width comb 0	
1.1				Line width local 0	
1.3				Dx_max = 400(μm)	
2.5				Dy_max = 400 (μm)	
3.3					
10					
	10	2.5		Line width = 1.0 (μm)	Local
	20	3.5		Local line width = 1.0 (μm)	neighborhood
	30	4.5		Number of local lines 2	size
	40	5.5		Density 0.45	
	50	6.5		Comb line width 1.3	
	60	7.5		Dx_max = 400(μm)	
	70	8.5		Dy_max = 400 (μm)	
	80	9.5			
			25	Line width 1.0	Global
			50	Line width local 1.0	neighborhood
			100	Space 1.0	size
			150	Number of local lines 6	
			200	Density 0.45	
			250	Line width comb 1.3	
			300	Dy_max 400 (μm)	
Line Width	Spacing	N_local	Dx_max	Fixed Parameters	Comments
1.0 (DR)	1.0 (DR)	6		D_local 5	Standards
1.3	1.3	6		Line width comb 1.3	
1.0	40	2		0.45	
1.3	40	2			

The snake, comb and snake & comb structures are designed primarily for the detection of shorts and opens across a wide variety of patterns. Snakes are used primarily for the detection of

opens and can also be used for monitoring resistance variation. Combs are used for monitoring shorts. Shorts and opens are fundamental yield loss mechanisms and both need to be minimized to obtain high product yield. Figure 13 shows the location of snakes and combs 1302 in the metal short flow chip described herein. Quadrant one 1304 also contains snakes 1402 and combs 1404 nested within the Kelvin structures asshown, for example in Figure 14. Line width (LW) and space (S), see Figure 14, are the parameters varied on these structures to study their impact on shorts and opens. Tables X through XIII describe the variations of snake and comb structures used in the metal short flow chip described herein. Again, the parameters were chosen such that the space covered in line width, line space, and density is similar to that seen in the example product layout, as shown in Figure 22(a) through 22(c).

TABLE X

LW_comb (μm)	Space (μm)	LW_snake (μm)	Fixed Parameters
20	0.9	1.0 (DR)	Dx_max = 200 μm
50	1.0 (DR)		Dy_max = 400 μm
100	1.1		
200	1.3		
300	2.5		
	3.0		
	3.3		
	10		
20	1.3	1.3	
50	3.1		
100	3.3		
200	3.5		
300	10		

TABLE XI

LW_comb (μm)	Space (μm)	Fixed Parameters
0.75	0.75	Dx_max = 200 μm
0.9	0.9	Dy_max = 400 μm
1.0 (DR)	1.0 (DR)	
1.1	1.1	
1.3	1.2	
2.0	1.3	
3.3	2.5	
10	3.0	
	3.3	
	10	

TABLE XII

Line Width (μm)	Fixed Parameters
0.75	Dx_max = 200 μm
0.9	Dy_max = 400 μm
1.0 (DR)	10 μm
1.1	
1.3	
2.5	
3.3	
1.0	

TABLE XIII

LW (μm)	Space (μm)	Fixed Parameters
20	0.7	Dx_max = 400 μm
50	1.0 (DR)	Dy_max = 200 μm
100	1.1	
200	1.3	
500	2.5	
	2.7	
	3.0	
	3.3	
	5	
	10	

Border and fringe structures are designed to study the impact of optical proximity correction (OPC) structures on shorts. These optical proximity corrections are usually added to improve via yields. However, it is necessary to check metal short yield with and without these borders to ensure that there is no detrimental impact to short yield. Borders 1502 are placed both at the end of the comb lines and in the interior of comb structures, generally designated 1504, as shown in Figure 15. Figure 16 shows the location of border structures, generally designated 1602, in the metal short flow chip described herein.

Scanning electron microscopy (SEM) structures are used for non-electrical measurements of line width through top down or cross sectional SEM. For the SEM bars in the metal short flow

chip described herein the line width is the same as the spacing between the lines in accordance with traditional SEM techniques. Figure 17 depicts the location of the SEM structures 1702 in the metal short flow chip described herein. The structures are placed at the bottom of each quadrant 1704, 1706, 1708 and 1710 of the embodiment depicted since this is where space was available.

In Figures 3 through 17, and accompanying text, an example characterization vehicle for metal yield improvement has been described. Other characterization vehicles for via, device, silicides, poly, el al, are often designed and utilized. However, the procedure and techniques for designing them are the same. For purposes of illustration, the example metal characterization vehicle will be carried through on extraction engines and yield models.

The extraction engine 18 has two main purposes: (1) it is used in determining the range of levels (e.g. linewidth, linespace, density) to use when designing a characterization vehicle. (2) It is used to extract the attributes of a product layout which are then subsequently used in the yield models to predict yield. (1) has already been described above with reference to how the line width, space and density of the snake, comb and Kelvin structures were chosen in the example characterization vehicle. Thus, most of the following discussion focuses on (2).

Since there are nearly infinite numbers of attributes that can be extracted from the product layout, it is impossible to list or extract all of them for each product. Thus, a procedure is

required to guide which attributes should be extracted. Usually, the characterization vehicle drives which attributes to extract. The process consists of:

1. List all structures in the characterization vehicle
2. Classify each structure into groups or families such that all structures in the family form an experiment over a particular attribute. For example, in the metal characterization vehicle discussed above, a table of family classifications might be:

Family	Attributes Explored
Nest structures	Basic defectivity over a few linewidths and spaces
Snakes and Combs	Yield over wide range of linewidths and spaces including very large widths next to small spaces and very large spaces next to small widths.
Kelvin-CD + van der Pauws	CD variation across density, linewidth, and linespace.
Border structures	Effect of different OPC schemes on yield.

3. For each family, determine which attributes must be extracted from the product layout. The exact attributes to choose are driven from which attributes are explored. For example, if a particular family explores yield over different ranges of space, then either a

histogram of spaces or the shortable area for each space must be extracted. For the above example, the required list of attributes might be:

Family	Attributes Explored	Attributes to Extract from Product Layout
(A) Nest structures	Basic defectivity over a few linewidths and spaces.	Critical area curves.
(B) Snakes and combs	Yield over wide range of linewidths and spaces including…	Shortable area and/or instance counts for each line width and space explored in the characterization vehicle.
(C) Kelvin-CD and van der Pauws	CD variation across density, linewidth, and space	Histograms of pattern density, linewidth, and linespace (similar to example shown in Figure 22)
(D) Border structures	Effect of different OPC schemes on yield	For each OPC scheme selected to use on product layout, the shortable area or instance count.

4. Use the attributes extracted in the appropriate yield models as previously described.

For other characterization vehicles, the families and required attributes will obviously be different. However, the procedure and implementation is similar to the example described above.

As previously stated, the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12. In the preferred embodiment, the yield is modeled as a product of random and systematic components:

$$Y = \left(\prod_{i=1}^{n} Ys_i \right) \left(\prod_{j=1}^{m} Yr_j \right)$$

The methods and techniques for determining Ys_i and Yr_j are as follows.

SYSTEMATIC YIELD MODELING

Since there are so many types of systematic yield loss mechanisms and they vary from fab to fab, it is not practicable to list every possible systematic yield model. However, the following describes two very general techniques and gives an example of their use especially within the context of characterization vehicles and the methodology described herein.

AREA BASED MODELS

The area based model can be written as:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)} \right]^{A(q)/A_o(q)}$$

Where q is a design factor explored in the characterization vehicle such as line width, line space, length, ratio of width/space, density, etc. $Y_o(q)$ is the yield of a structure with design factor q from the characterization vehicle. $A_o(q)$ is the shortable area of this structure and $A(q)$ is the shortable area of all instances of type q on the product layout. $Y_r(q)$ is the predicted yield of this structure assuming random defects were the only yield loss mechanism. The procedure for calculating this quantity is described below in connection with random yield modeling.

The definition of shortable area is best illustrated with the example shown in Figure 18. This type of test structure can be used to determine if the fab is capable of yielding wide lines that have a bend with a spacing of s. In this sample test structure, a short is measured by applying a voltage between terminal (1) and (2) and measuring the current flowing from terminal (1) to (2). If this current is larger than a specified threshold (usually 1-100nA), a short is detected. The shortable area is defined to be the area where if a bridging occurs, a short will be measured. In the example of Figure 18, the shortable area is approximately x*s). The A(q) term is the shortable area of all occurrences of the exact or nearly exact patten (i.e. a large line with a spacing of s and a bend of 45 degrees) shown in Figure 18 in a product layout. The Yr(q) term is extracted by predicting the random yield limit of this particular structure using the critical area method described below.

It is important to realize that the effectiveness of this model is only as good as the number of structures and size of structures placed on the characterization vehicle. For example, if the angled bend test structure shown in Figure 18 were never put on the characterization vehicle or was not placed frequently enough to get a meaningful yield number, then there would be no hope of modeling the yield loss of wide line bends on the product layout. While it is difficult to define exactly how many of how big the test structure should be on the characterization vehicle, practical experience has shown that the total shortable area of each test structure on the characterization vehicle should ideally be such that A(q)/Ao(q)<10.

The above discussion has concentrated on shorts since they generally tend to dominate over open yield loss mechanisms. However, open yield loss mechanisms can be modeled equally well with this yield model so long as shortable area is replaced by open causing area.

INSTANCE BASED YIELD MODEL

The general form of the instance based yield model is:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)}\right]^{N_f(q)/N_a(q)}$$

Where Yo(q) and Yr(q) are exactly the same as in the area based yield model. Ni(q) is the number of times the unit cell pattern or very similar unit cell pattern to the test pattern on the characterization vehicle appears on the product layout. No(q) is the number of times the unit cell pattern appears on the characterization vehicle.

For example, Figure 19 shows a simple test pattern for examining the yield of T-shaped endings at the ends of lines near a space of s. This test pattern is measured by applying a voltage across terminals (1) and (2) and measuring the shorting current. If this pattern was repeated 25 times somewhere on the characterization vehicle, then No(q) would be 25x5=125 since there are five unit cells per each test structure.

If the number of times this unit cell occurs with a spacing of s near it is extracted from the product layout, the systematic yield of this type of structure can be predicted. For example, if there are five structures with 500 unit cells in each structure then No(q)=2500. If Ni(q) from some product was 10,000 and a yield of the test structures on the characterization vehicle of 98.20% was measured. Using the techniques described below, Yr(q) can be estimated as 99.67%. Using these numbers in the equation:

$$Ys_i = \left[\frac{0.9820}{0.9967}\right]^{10000/2500} = 92.84\%$$

RANDOM YIELD MODELING

The random component can be written as:

$$Y_r = e^{-\int_{x_0}^{\infty} CA(x) \times DSD(x)\,dx}$$

Where CA(x) is the critical area of defect size x and DSD(x) is the defective size distribution, as also described in"Modeling of Lithography Related Yield Losses for CAD of VSLI Circuits", W. Maly, IEEE Trans. on CAD, July 1985, pp161-177, which is incorporated by reference as if fully

set forth herein. Xo is the smallest defect size which can be confidently observed or measured. This is usually set at the minimum line space design rule. The critical area is the area where if a defect of size x landed, a short would occur. For very small x, the critical area is near 0 while very large defect sizes have a critical area approaching the entire area of the chip. Additional description of critical area and extraction techniques can be found in P. K. Nag and W. Maly, "Yield Estimation of VLSI Circuits," Techcon90, Oct. 16-18, 1990. San Jose; P. K. Nag and W. Maly, "Hierarchical Extraction of Critical Area for Shorts in Very Large ICs," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 10-18; I. Bubel, W. Maly, T. Waas, P. K. Nag, H. Hartmann, D. Schmitt-Landsiedel and S. Griep, "AFFCCA: A Tool for Critical Area Analysis with Circular Defects and Lithography Deformed Layout," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 19-27; C. Ouyang and W. Maly, "Efficient Extraction of Critical Area in Large VISI ICs," Proc. IEEE International Symposium on Semiconductor Manufacturing, 1996, pp. 301-304; C. Ouyang, W. Pleskacz, and W. Maly, "Extraction of Critical Area for Opens in Large VLSI Circuits," Proc. IEEE International Workshop on Defect and Fault Tolerance of VLSI Systems, 1996, pp. 21-29, all of which references are incorporated in this detailed description as if fully set forth herein.

The defect size distribution represents the defect density of defects of size x. There are many proposed models for defect size distributions (see, for example, "Yield Models - Comparative Study", W. Maly, Defect and Fault Tolerance in VLSI Systems, Ed. by C. Stapper, et al, Plenum Press, New York, 1990; and "Modeling of Integrated Circuit Defect Sensitivities", C.H. Stapper, IBM J. Res. Develop., Vol. 27, No. 6, November, 1983, both of which are incorporated by reference as if fully set forth herein), but for purposes of illustrations, the most common distribution:

$$DSD(x) = \frac{D_o \times k}{x^p}$$

will be used where Do represents the total number of defects/cm^2 greater than x_0 observed. P is a unitless value which represents the rate at which defects decay over size. Typically, p is between 2 and 4. K is a normalization factor such that

$$\int_{x_o}^{\infty} \frac{k}{x^p} dx = 1$$

The following two sections describe techniques for extracting defect size distributions from characterization vehicles.

THE NEST STRUCTURE TECHNIQUE

The nest structure is designed for extracting defect size distributions. It is composed of N lines of width w and space s as shown in Figure 20. This structure is tested by measuring the shorting current between lines 1 and 2, 2 and 3, 3 and 4, ..., and N-1 and N. Any current above a given spec limit is deemed a short. In addition, opens can be testing by measuring the resistance of lines 1, 2, 3, ..., N-1, and N. Any resistance above a certain spec limit is deemed to be an open line. By examining how many lines are shorted together the defect size distribution can be determined.

If only two lines are shorted then the defect size must be greater than s and no larger than 3w + 2s. Any defects smaller than s will not cause a short at all while defects larger than 3w+2s are guaranteed to cause a short of at least 3 lines. For each number of lines shorted, an interval of sizes can be created:

Number Lines Shorted	Size Interval
2	s to 3w+2s
3	2s+w to 3s+4w
4	3s+2w to 4s+5w
...	...
N	(N-1)s+(N-2)w to (N)s+(N+1)w

It should be noted that the intervals overlap; thus, a defect size distribution cannot be directly computed. This restriction only places a limit on p extraction. Thus, in order to estimate p, a p estimate is computed from the distribution from all the even number lines and then from all the odd number lines. Finally, the two values are averaged together to estimate p. To extract p, the ln (number of faults for x lines shorted) vs log ([x-1]s + [x-2]w) is plotted. It can be shown that the slope of this line is -p. The Do term is extracted by counting the number of failures at each grouping of lines and dividing by the area of the structure. However, for very large Do, this estimate will be too optimistic. Additional information on extracing defect size distribution from structures similar to the test structures can be found, for example, in "Extraction of Defect Size Distribution in an IC Layer Using Test Structure Data", J. Khare, W. Maly and M.E. Thomas, IEEE Transactions on Semiconductor Manufacturing, pp. 354-368, Vol. 7, No. 3, August, 1994, which is incorporated by reference as if fully set forth herein.

As an example, consider the following data taken from 1 wafer of 100 dies:

Number Lines Shorted	Number of Failures
2	98
3	11
4	4
5	2
6	1
7	0
8	0

If the structure size is lcm^2 then the Do would be 98 + 11 +4 + 2 +1 = 133 / (100 * 1) = 1.33 defects/cm^2. Also, the plot of log (number of failures) vs log ([x-1]s + [x-2]w) (see Figure 21) shows that p=2.05.

THE COMB STRUCTURE TECHNIQUE

Assuming a comb of width = space = s, it can be shown that the yield of this structure can be written as:

$$\ln[|\ln(Y)|] = \ln[-\int_{x_0}^{\infty} DSD(x) \times CA(x)dx] \propto (1-p) \times \ln(s)$$

Thus, from the slope of the plot of ln[|ln(Y)|] vs. ln(s), p can be estimated. The Do extraction technique is the same technique as mentioned above.

YIELD IMPACT AND ASSESSMENT

Once a sufficient number of characterization vehicles has been run and yield estimates are made for each characterization vehicle, the results are placed in a spread sheet to enable prioritization of yield activities. Tables XIV through XVI are examples of information contained in such a spread sheet. It has been divided into sections of metal yield, poly and active area (AA) yield (Table XIV), contact and via yield (Table XV), and device yield (Table XVI). The columns on the left indicate systematic yield loss mechanisms while the columns on the right indicate random yield loss mechanisms. Although the exact type of systematic failure mechanisms vary from product to product, and technology by technology, examples are shown in Tables XIV through XVI.

Usually, targets are ascribed to each module listed in the spread sheet. The further a module yield is away from a target, the more emphasis and resources are devoted to fixing the problem. For example, if the target was set artificially at 95 percent for each module in the example shown in Tables XIV through XVI, then clearly (M_2 -M_3) vias (75.12%) followed by similar vias (M_1 -M_2) (81.92%), M_1 shorts (82.25%), and contacts to poly (87.22%) are below target and, with vias (M_2 -M_3) needing the most amount of work and contacts to poly needing the least amount of work.

Within each module, it is also possible to tell where the greatest yield loss is situated. That is, is it one particular systematic mechanism being the yield down or is it merely a random defectivity problem, or is it some combination of the two? For example, as shown in Table XV, via (M_2 -M_3) yield loss is clearly dominated by a systematic problem affecting vias connected to

long metal runners on the M_3 level (77.40%). Vias from (M_1 to M_2) are affected by the same problems (91.52%) in addition to a random defectivity problem (92.49%). Solving vias (M_1 to M_2) yield problems would require fixing both of these problems.

As shown in Table XIV, M_1 yield loss is also dominated by a random defectivity issue (85.23%) in addition to a systematic problem affecting wide lines near small spaces (96.66%). Fixing both of these problems would be required for improving Metal 1. Similar conclusions can be made for other modules in the spread sheet.

For the worst yielding modules, frequent running of further characterization vehicles for this module would be required. Usually, splits will be done on these characterization vehicles to try and improve and validate those improvements in module yield. For the modules which are within target, routine monitoring of short flow characterization vehicles would still be required to validate that there has been no down turn or other movement in module yield. However, these characterization vehicles can be run less frequently than for those modules with known problems.

TABLE XIV

Opens and Shorts (Metal Layers)

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Do	P	Estimated Yield	
Metal-1	Random Yield				0.7 defects/cm^2	2.3	85.23%	
	Wide lines near small space	0.034		96.66%				
	Wide space near small lines	0.00014		99.99%				
	Yield for OPC structures		72,341	99.86%				
	Bent lines		492	100.00%				
	Total for M1						82.25%	
Metal-2	Random Yield				0.35 defects/cm^2	1.92	97.45%	
	Wide lines near small space	0.00079		99.92%				
	Wide space near small lines	0.000042		100.00%				
	Yield for OPC structures		1040372	97.94%				
	Bent lines		103	100.00%				
	Total for M2						95.36%	
Metal-3	Random Yield				0.25 defects/cm^2	2.02	96.92%	
	Wide lines near small space	0.0000034		100.00%				
	Wide space near small lines	0		100.00%				
	Yield for OPC structures		352	100.00%				
	Bent lines		7942	99.92%				
	Total for M3						96.84%	
	Open and Shorts (Poly and AA Layer)							
Poly	Random Yield (without silicide)				0.17 defects/cm^2	2.03	99.81%	
	Random Yield (with silicide)				4.34defects/cm^2	4.56	89.54%	89.71% from silicide
	Wide lines near small space	0		100.00%				
	Wide space near small lines	0.01203		98.80%				
	Yield for OPC structures		0	100.00%				
	Bent lines		786541	92.44%				
	Over wide AA	0.034		96.66%				
	Over narrow AA	0.101		99.00%				
	Total for Poly						87.22%	
AA	Random Yield (without silicide)				1.3	3.45	99.12%	
	Random Yield (with silicide)				1.7	3.02	98.72%	99.60% from silicide
	Wide lines near small space		10952	99.96%				
	Wide space near small lines		0	100.00%				
	Total for AA						98.70	

TABLE XV

Contacts and Vias

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield	
Contact to Poly	Random Yield (without silicide)				2.20E-09	3270432	99.28%	
	Random Yield (with silicide)				3.10E-09	3270432	98.99%	99.71%
	Yield for Long Runners (on M1)		11,921	100.00%				
	Yield for Long Runners (on Poly)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	96.46%				
	Total for Contact to Poly						94.80%	
Contact to n+AA	Random Yield (without silicide)				2.20E-09	5270432	98.85%	
	Random Yield (with silicide)				3.10E-09	5270532	98.38%	99.53%
	Yield for Long Runners (on M1)		75,324	99.99%				
	Yield for Long Runners (on n+AA)		0	100.00%				
	Yield for Redundant Vias		4032007	99.60%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (n+)						96.78%	
Contact to p+AA	Random Yield (without silicide)				2.20E-09	6093450	98.67%	
	Random Yield (with silicide)				3.10E-09	6093450	98.13%	
	Yield for Long Runners (on M1)		96,732	99.99%				
	Yield for Long Runners (on p+AA)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (p+)						96.74%	
Vias M1->M2	Random Yield (single vias)				1.10E-08	7093210	92.49%	
	Yield for Long Runners (M2)		88640	91.52%				
	Yield for Long Runners (M1)		97645	99.03%				
	Yield for Redundant Vias		11003456	96.91%				
	Yield for Isolated Vias		119582	96.81%				
	Total for Via M1-M2						81.92%	
Vias M2->M3	Random Yield (single vias)				3.10E-09	4002063	98.77%	
	Yield for Long Runners (M3)		256128	77.40%				
	Yield for Long Runners (M2)		103432	96.97%				
	Yield for Redundant Vias		7096230	99.29%				
	Yield for Isolated Vias		1024	99.99%				
	Total for Via M2-M3						75.12%	

TABLE XVI

	Devices					
		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism		
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield
NMOS	Random Yield (Logic Xtor)				2.90E-09	1395228	99.60%
	Random Yield (SRAM Xtor)				2.80E-09	2226720	99.38%
	S/D Shorts				1.00E-09	3621948	99.64%
	Bent Transistors		1113360	99.89%			
	Near Large AA		754000	99.92%			
	Near Small AA		1023452	99.90%			
	Total for NMOS Transistors						98.33%
PMOS	Random Yield (Logic Xtor)				1.80E-09	1491003	99.73%
	Random Yield (SRAM Xtor)				3.10E-09	1113360	99.66%
	S/D Shorts				9.00E-10	2604363	99.77%
	Bent Transistors		556680	99.94%			
	Near Large AA		789092	99.92%			
	Near Small AA		1309970	99.87%			
	Total for PMOS Transistors						98.89%

I claim:

I claim:

1. A system for predicting yield of integrated circuits comprising:

a) at least one type of characterization vehicle including at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) a yield model which embodies a layout as defined by the characterization vehicle, said yield model having been subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) a product layout; and

d) an extraction engine for extracting predetermined layout characteristics from the product layout, which characteristics are used in connection with the yield model to produce a yield prediction.

2. A system in accordance with claim 1 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

3. A system in accordance with claim 2 wherein the characterization vehicle comprises a short flow test vehicle.

4. A system in accordance with claim 3 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

5. A system in accordance with claim 4 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

6. A system in accordance with claim 3 wherein the characterization vehicle comprises a metal short flow test vehicle.

7. A system in accordance with claim 6 wherein the metal short flow test vehicle includes at least one basic structure.

8. A system in accordance with claim 7 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;

b) snake structure;

c) comb structure;

d) snake and comb structures;

e) nest defect size distribution structure;

f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

9. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

10. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

11. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one via or contact.

12. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one active device.

13. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one silicide region.

14. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

15. A system in accordance with claim 1 wherein the extraction engine is also used to determine a range of layout feature levels for use when designing a characterization vehicle.

16. A system in accordance with claim 15 wherein the layout feature range of levels includes line width, line space and line density.

17. A method for predicting a yield for an integrated circuits comprising:

a) providing information for fabricating at least one type of characterization vehicle having at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) fabricating a characterization vehicle which embodies a yield model and layout features representative of the product employing at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) providing a product layout;

d) extracting predetermined layout characteristics from the product layout; and

e) using the extracted layout characteristics in connection with the yield model to produce a yield prediction.

18. A method in accordance with claim 17 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

19. A method in accordance with claim 18 wherein the characterization vehicle comprises a short flow test vehicle.

20. A method in accordance with claim 19 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

21. A method in accordance with claim 20 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

22. A method in accordance with claim 19 wherein the characterization vehicle comprises a metal short flow test vehicle.

23. A method in accordance with claim 22 wherein the metal short flow test vehicle includes at least one basic structure.

24. A method in accordance with claim 23 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;

b) snake structure;

c) comb structure;

d) snake and comb structures;

e) nest defect size distribution structure;

f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

25. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

26. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

27. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one via or contact.

28. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one active device.

29. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one silicide region.

30. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

31. A method in accordance with claim 17 wherein the extraction engine is also used to determine a range of levels for use when designing a characterization vehicle.

32. A method in accordance with claim 31 wherein the range of levels includes line width, line space and line density.

33. A method in accordance with claim 17 wherein the predetermined layout characteristics are extracted from the product layout using a process which includes the steps of:

a) listing all structures in the characterization vehicle;

b) classifying each structure into families such that all structures in each family form an experiment over a particular attribute; and

c) for each family, determine which attributes are to be extracted forr the product layout.

34. A method in accordance with claim 33 wherein the families include a family comprising nest structures for exploring basic defectivity over a selected number of line widths and spaces.

35. A method in accordance with claim 33 wherein the families include a family comprising snake and comb structures for exploring yield over a predetermined range of line widths and spaces.

36. A method in accordance with claim 35 wherein the predetermined range of line widths and spaces include relatively large line widths next to relatively small spaces and relatively large interline spaces next to relatively small line widths.

37. A method in accordance with claim 33 wherein the families include a family comprising Kelvin critical dimension and van der Pauw structures for exploring critical dimension variation across line density, width and spacing.

38. A method in accordance with claim 33 wherein the families include a family comprising border structures for exploring the effect of various optical proximity correction schemes on yield.

39. A system for determining and ranking yield loss mechanisms given characterization vehicle data and extracted layout attributes.

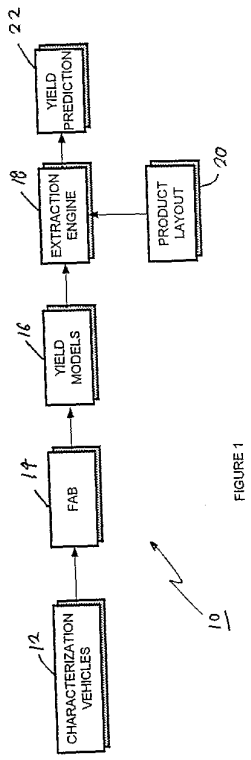
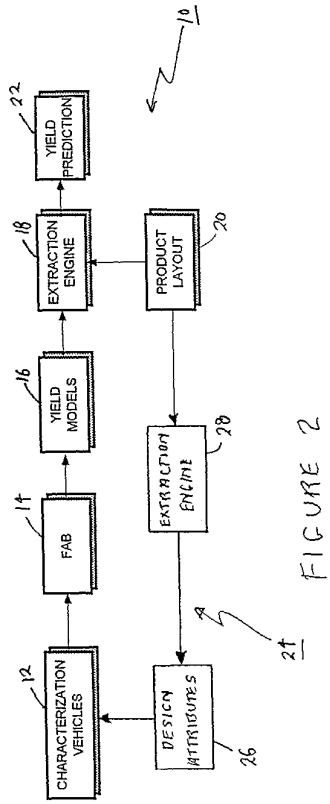

22
YIELD PREDICTION
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
16
YIELD MODELS
14
FAB
12
CHARACTERIZATION VEHICLES
10

FIGURE 1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22
YIELD PREDICTION
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
16
YIELD MODELS
28
EXTRACTION ENGINE
14
FAB
24
12
CHARACTERIZATION VEHICLES
DESIGN ATTRIBUTES
26

FIGURE 2

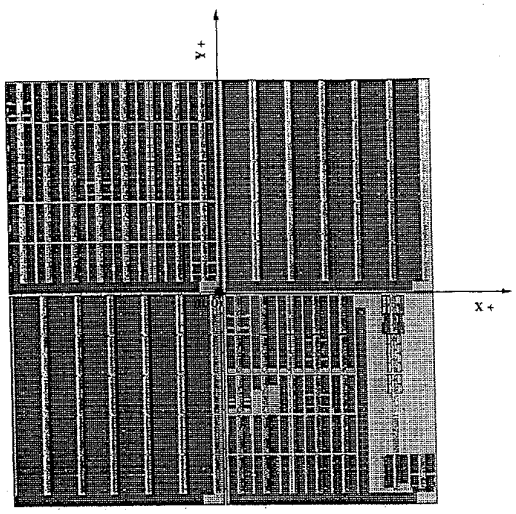


FIGURE 3

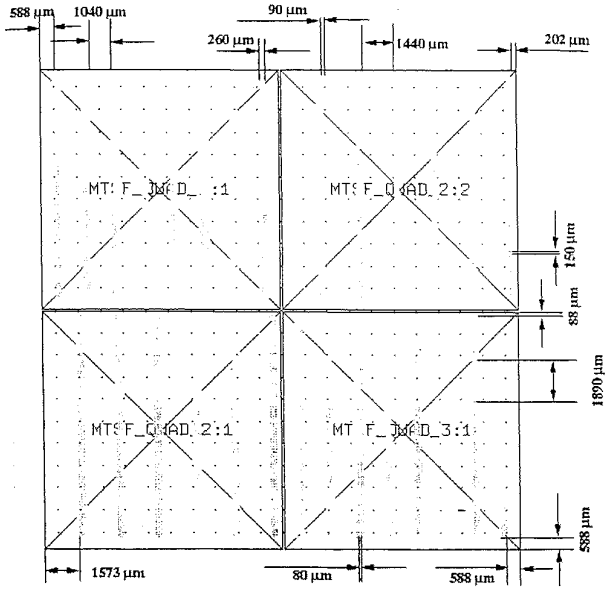
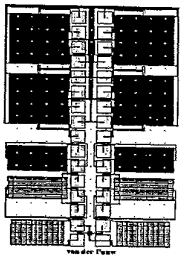

588 µm
1040 µm
90 µm
260 µm
1440 µm
202 µm
MT F_QUAD_2:2
150 µm
88 µm
1890 µm
MT F_QUAD_2:1
MT F_QUAD_3:1
588 µm
1573 µm
80 µm
588 µm

FIGURE 4

FIGURE 5



A

B

FIGURE 6

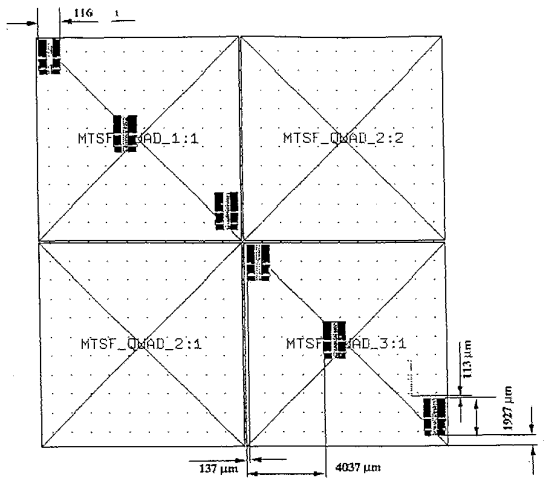


FIGURE 7

FIGURE 8

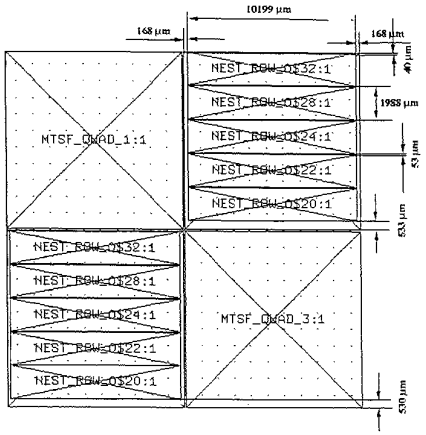


FIGURE 9

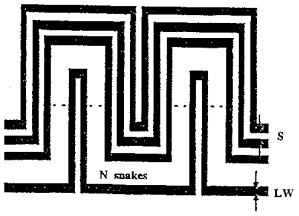


FIGURE 10

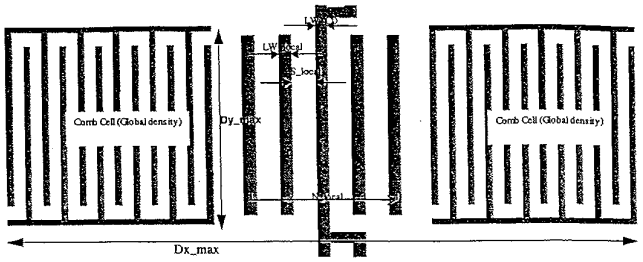


FIGURE 11

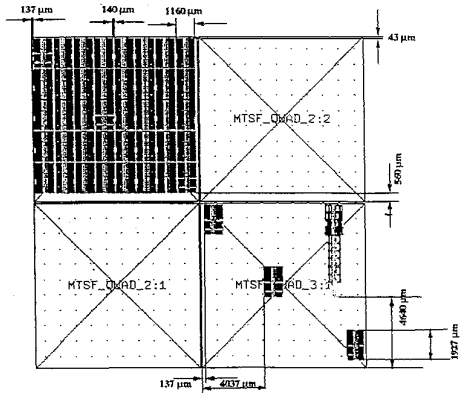


FIGURE 12

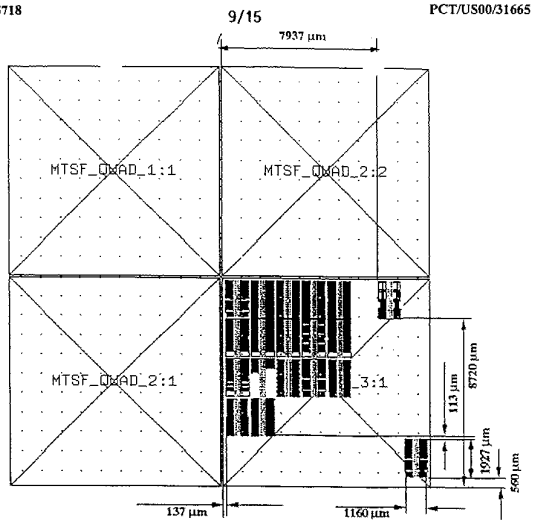


FIGURE 13

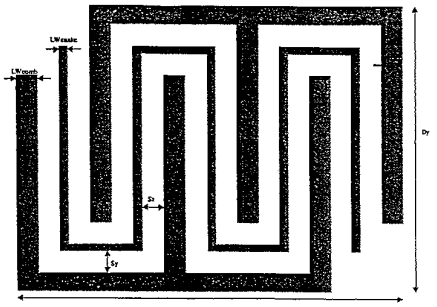


FIGURE 14

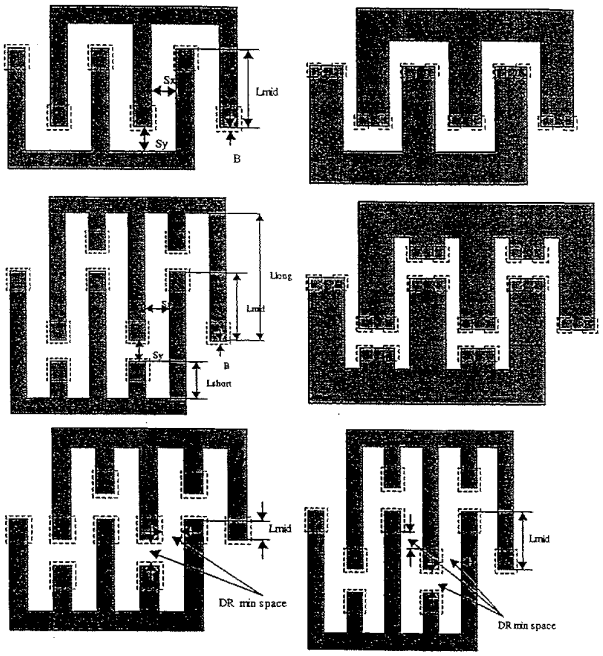

Sx
Sy
Lmid
B
Llong
Lmid
Sy
B
Lshort
Lmid
DR min space
Lmid
DR min space

FIGURE 15

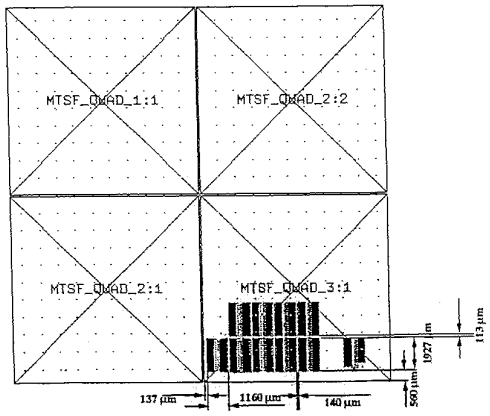

MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
113 µm
1927 µm
560 µm
137 µm
1160 µm
140 µm

FIGURE 16

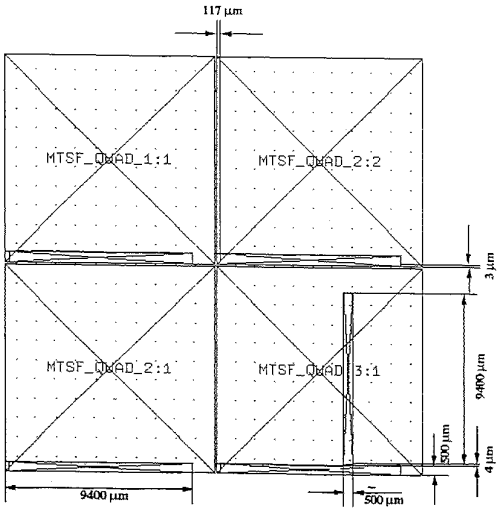

117 µm
MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
3 µm
9400 µm
500 µm
4 µm
9400 µm
500 µm

FIGURE 17

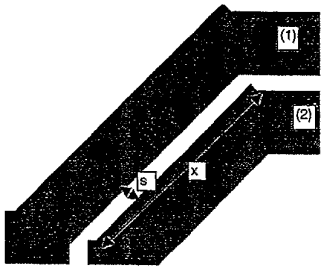


FIGURE 18

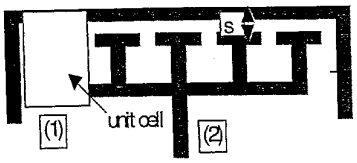


FIGURE 19

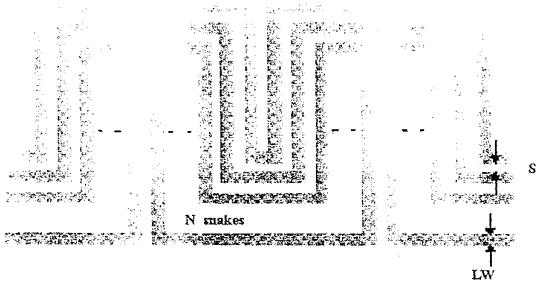


FIGURE 20

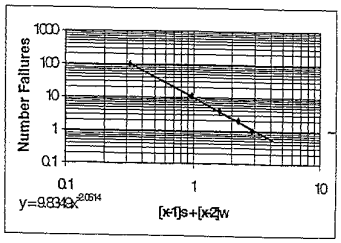


FIGURE 21

FIGURE 22(a)

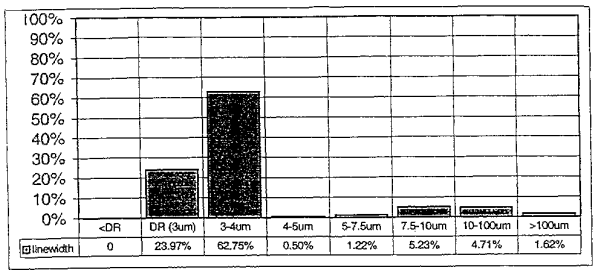


FIGURE 22(b)

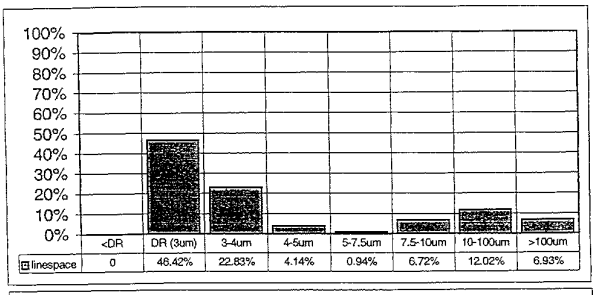
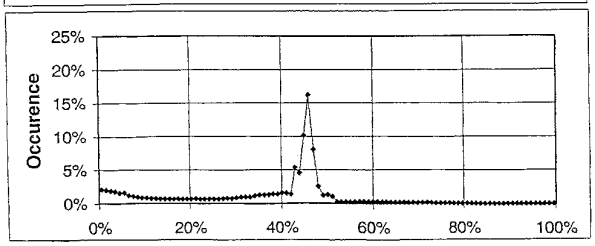


FIGURE 22(c)



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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 May 2001 (25.05.2001)

PCT

(10) International Publication Number
WO 01/35718 A2

(51) International Patent Classification: Not classified

(21) International Application Number: PCT/US00/31665

(22) International Filing Date:
17 November 2000 (17.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/442,699 18 November 1999 (18.11.1999) US

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(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

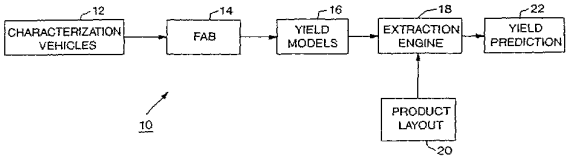
Published:
— *without international search report and to be republished upon receipt of that report*

(48) Date of publication of this corrected version:
30 May 2002

(15) Information about Correction:
see PCT Gazette No. 22/2002 of 30 May 2002, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION



(57) Abstract: A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the caracterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype section at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

WO 01/35718 A2

SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION

Background of the Invention

The present invention pertains to fabrication of integrated circuits and more particularly to systems and methods for improving fabrication yields.

The fabrication of integrated circuits is an extremely complex process that may involve hundreds of individual operations. Basically, the process includes the diffusion of precisely predetermined amounts of dopant material into precisely predetermined areas of a silicon wafer to produce active devices such as transistors. This is typically done by forming a layer of silicon dioxide on the wafer, then utilizing a photomask and photoresist to define a pattern of areas into which diffusion is to occur through a silicon dioxide mask. Openings are then etched through the silicon dioxide layer to define the pattern of precisely sized and located openings through which diffusion will take place. After a predetermined number of such diffusion operations have been carried out to produce the desired number of transistors in the wafer, they are interconnected as required by interconnection lines. These interconnection lines, or interconnects as they are also known, are typically formed by deposition of an electrically conductive material which is defined into the desired interconnect pattern by a photomask, photoresist and etching process. A typical completed integrated circuit may have millions of transistors contained with a 0.1 inch by 0.1 inch silicon chip and interconnects of submicron dimensions.

In view of the device and interconnect densities required in present day integrated circuits, it is imperative that the manufacturing processes be carried out with utmost precision and in a way that minimizes defects. For reliable operation, the electrical characteristics of the circuits must be kept within carefully controlled limits, which implies a high degree of control over the myriad of operations and fabrication processes. For example, in the photoresist and photomask operations, the presence of contaminants such as dust, minute scratches and other imperfections in the patterns on the photomasks can produce defective patterns on the semiconductor wafers, resulting in defective integrated circuits. Further, defects can be introduced in the circuits during the diffusion operations themselves. Defective circuits may be identified both by visual inspection under high magnification and by electrical tests. Once defective integrated circuits have been identified, it is desired to take steps to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield of the integrated circuits meeting specifications.

In the past, many of the defects which caused poor yield in integrated circuits were caused by particulate contaminants or other random sources. Increasingly, many of the defects seen in modern integrated circuit processes are not sourced from particulates or random contaminants, especially in the earlier stages of process development or yield ramping, but rather stem from very systematic sources. Examples of these systematic defect sources include printability problems from using aggressive lithography tools, poly stringers from poorly formed silicides, gate length variation from density driven and optical proximity effects.

In attempting to decrease the number of defective integrated circuits produced in the manufacturing process, thus increasing the yield, one is faced with the fact that any one or more of possibly several hundred processing steps may have caused a particular circuit to be defective. With such a large number of variables to work with, it can be extremely difficult to determine the exact cause or causes of the defect or defects in a particular circuit thereby making it extraordinarily difficult to identify and correct the yield detracting process operations. Detailed inspection of the completed integrated circuits may provide some indication of which process operation may have caused the circuits to be defective. However, inspection equipment often does not capture many of the systematic defect sources and/or the tools can be difficult to tune, optimize, or use effectively and reliably. Furthermore, inspection equipment, especially in recent technologies is often plagued with many false alarms or nuisance defects, as they are known, which serve to frustrate any attempts to reliably observe true defects or sources of defects.

It is typically discovered that, once a particular problem has been identified at final test after completion of the fabrication cycle, it can be confirmed that a problem in a particular process operation did exist at the time that operation was carried out, which could have been weeks or even months earlier. Thus the problem might be corrected well after the fact. At this time, different process operations may be causing problems. Thus, after the fact analysis of defective integrated circuits and identification of process operations causing these defective products is severely limited as a means for improving the overall yield of integrated circuits.

A number of attempts to predict yields instead of conducting unsatisfactory after the fact analysis have been made with varying degrees of success. Thus, there is a need for an improved system and method for integrated circuit product yield prediction.

SUMMARY OF THE INVENTION

A system and method for predicting yield of integrated circuits includes at least one type of characterization vehicle which incorporates at least one feature which is representative of at least one type of feature to be incorporated in the final integrated circuit product. The characterization vehicle is subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product in order to produce a yield model. The yield model embodies a layout as defined by the characterization vehicle and preferably includes features which facilitate the gathering of electrical test data and testing of prototype sections at operating speeds. An extraction engine extracts predetermined layout attributes from a proposed product layout. Operating on the yield model, the extraction engine produces yield predictions as a function of layout attributes and broken down by layers or steps in the fabrication process. These yield predictions are then used to determine which areas in the fabrication process require the most improvement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a block diagram depicting the steps performed by a preferred embodiment of the system of the present invention.

FIGURE 2 is a block diagram depicting additional steps performed by the system of the present invention to effect a feedback loop.

FIGURE 3 is an image of an illustrative short flow mask comprising a single lithographic layer.

FIGURE 4 depicts pad frames on an exemplary metal short flow chip.

FIGURE 5 depicts pads within each pad frame depicted in FIGURE 4.

FIGURE 6 depicts two types of pad frame structures which contain van der Pauw structures.

FIGURE 7 depicts locations, on the exemplary chip, of the pad frames containing the van der Pauw structures.

FIGURE 8 depicts an exemplary van der Pauw structure.

FIGURE 9 depicts exemplary locations of nest defect size distribution structures on an exemplary metal short flow chip.

FIGURE 10 depicts an exemplary nest defect size distribution structure.

FIGURE 11 depicts an exemplary Kelvin critical dimension structure.

FIGURE 12 depicts exemplary locations of Kelvin structures on an exemplary metal short flow chip.

FIGURE 13 depicts exemplary locations of snakes and combs on an exemplary metal short flow chip.

FIGURE 14 depicts exemplary snake and comb structures used in an exemplary metal short flow chip.

FIGURE 15 depicts examples of variations of border structures used in an exemplary metal short flow chip.

FIGURE 16 depicts exemplary locations of border structures on an exemplary metal short flow chip.

FIGURE 17 depicts exemplary locations of scanning electron microscope structures on an exemplary metal short flow chip.

FIGURE 18 depicts an exemplary test structure illustrating a shortable area.

FIGURE 19 depicts an exemplary test pattern for examining the yield of T-shaped endings at the ends of lines.

FIGURE 20 depicts an exemplary nest structure for extracting defect size distributions.

FIGURE 21 depicts a plot for determining the rate at which defects decay over size.

FIGURE 22(a), 22(b) and 22(c) depict, respectively, linewidth, linespace and pattern density distributions for a metal-1 layer of a sample product layout.

DETAILED DESCRIPTION

Referring now to Figure 1, there is shown a block diagram depicting the steps performed by a system, generally designated 10, for predicting integrated circuit yields in accordance with the present invention. The system 10 utilizes at least one type of characterization vehicle 12. The characterization vehicle 12 preferably is in the form of software containing information required to build an integrated circuit structure which incorporates at least one specific feature

representative of at least one type of feature to be incorporated into the final product. For example, the characterization vehicle 12 might define a short flow test vehicle of a single lithographic layer for probing the health and manufacturability of the metal interconnection module of the process flow under consideration. The structures need to be large enough and similar enough to the actual product or type of products running in the fabrication process to enable a reliable capture or fingerprint of the various maladies that are likely to affect the product during the manufacturing. More specific examples and descriptions of short flows and the structures embodied in them are described below.

Short flow is defined as encompassing only a specific subset of the total number of process steps in the integrated circuit fabrication cycle. For example, while the total fabrication cycle might contain up to 450 or more process steps, a characterization vehicle such as one designed to investigate manufacturability of a single interconnection layer would only need to include a small number, for example 10 to 25 process steps, since active devices and multiple interconnection layers are not required to obtain a yield model or allow accurate diagnosis of the maladies afflicting these steps associated with a single interconnection layer in the process flows.

The characterization vehicle 12 defines features which match one or more attributes of the proposed product layout. For example, the characterization vehicle 12 might define a short flow test vehicle having a partial layout which includes features which are representative of the proposed product layout (e.g. examples of line size, spacing and periodicity; line bends and runs;

etc.) in order to determine the maladies likely afflicting those specific design types and causing yield loss.

The characterization vehicle 12 might also define one or more active regions and neighboring features of the proposed design in order to explore impact of layout neighborhood on device performance and process parameters; model device parameters as a function of layout attributes; and determine which device correlate best with product performance. Furthermore, by constructing and analyzing a sufficient number of short flow vehicles such that the range of all possible or a major subset of all the modular components of the entire process is exercised, a full evaluation of many if not all of the yield problems which will afflict the specific product manufactured can be uncovered, modeled, and/or diagnosed.

In addition to providing information for assessing and diagnosing yield problems likely to be seen by the product(s) under manufacture, the characterization vehicle is designed to produce yield models 16 which can be used for accurate yield prediction. These yield models 16 can be used for purposes including, but not limited to, product planning, prioritizing yield improvement activities across the entire process, and modifying the original design of the product itself to make it more manufacturable.

The majority of the test structures in the characterization vehicle 12 contemplated in the invention are designed for electrical testing. To this end, the reliability of detecting faults and defects in the modules evaluated by each characterization vehicle is very high. Inspection

equipment cannot deliver or promise this high degree of reliability. Furthermore, the speed and volume of data collection is very fast and large respectively since electrical testing is fast and cheap. In this way, statistically valid diagnosis and/or yield models can be realized.

The characterization vehicle 12 is preferably in the form of a GDS 2 layout on a tape or disc which is then used to produce a reticle set. The reticle set is used during the selected portions of the fabrication cycle 14 to produce the yield model 16. Thus the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12.

The yield model 16 not only embodies the layout as defined by the characterization vehicle, it also includes artifacts introduced by the fabrication process operations themselves. The yield model 16 may also include prototype architecture and layout patterns as well as features which facilitate the gathering of electrical test data and testing prototype sections at operating speeds which enhances the accuracy and reliability of yield predictions.

An extraction engine 18 is a tool for extracting layout attributes from a proposed product layout 20 and plugging this information into the yield model 16 to obtain a product yield prediction 22. Such layout attributes might include, for example, via redundancy, critical area, net length distribution, and line width/space distribution. Then, given layout attributes from the proposed product layout 20 and data from yield models 16 which have been fabricated based

upon information from the characterization vehicles 12, product yield 22 is predicted. Using the system and method of the present invention, the predictable product yield obtainable can be that associated with each defined attribute, functional block, or layer, or the resultant yield prediction for the entire product layout.

Referring now to Figure 2, there is shown a block diagram of the system for predicting integrated circuit yields 10 in accordance with the present invention additionally comprising a feedback loop, generally designated 24, for extracting design attributes 26 from product layout 20 by means of extraction engine 28. In accordance with this feature of the present invention, the characterization vehicle 12 is developed using attributes of the product layout 20. In this case, attributes of the product layout are extracted, making sure that the range of attributes are spanned in the characterization vehicle 12. For example, the product layout is analyzed to determine line space distribution, width distribution, density distribution, the number of island patterns, in effect developing a subset of the entire set of design rules of the fabrication process, which subset is applicable to the particular product layout under consideration. With respect to patterns, the product layout analysis would determine the most common pattern, the second most common pattern, and so forth. These would be extracted by the extraction engine 28 yielding design attributes 26 encompassing all of these patterns for inclusion into the characterization vehicle 12. With respect to densities, if the analysis of the product layout reveals that the density of a first metal is from 10% to 50%, then the characterization vehicle would include the entire range of 10% to 50% for the first metal.

One type of characterization vehicle is a metal short flow characterization vehicle. The purpose of the metal short flow characterization vehicle is to quantify the printability and manufacturability of a single interconnect layer. Usually a metal short flow is run very early in the process since metal yield is crucial for high product yield, is often very difficult to obtain, and consists of only a few independent processing steps. Conducting short flow experiments using a metal short flow mask, enables experiments and analysis to be carried out in rapid succession to eliminate or minimize any systematic yield or random defect yield issue that is detected without having to wait for complete flow runs to finish.

Referring to Figure 3, there is shown an image of a typical and illustrative metal short flow mask, generally designated 30, which consists of a single lithographic layer. The mask 30 is used to define a single metal layer on a chip, and the exemplary chip 32 depicted in Figure 3 is as large as the stepper can accomodate which is, in this example, approximately 22 mm x 22 mm in size. It is divided into four quadrants, 42, 4, 46 and 48 as shown in Figure 4, each containing one or more of six basic structures: (i) Kelvin metal critical dimension structures; (ii) snake and comb structures; (iii) nest defect size distribution structures; (iv) van der Pauw structures; (v) OPC evaluation structures; and (vi) classical scanning electron microscopy (SEM) structures.

Approximately 50% of the chip area is devoted to nest structures for extraction of defect size distribution while 40% of the chip area is devoted to detecting systematic yield loss mechanisms and measuring parametric variation. Figure 3 also depicts the location of pad frames 34 on the chip. In the embodiment described herein, there are 131 pad frames on the chip, with

each pad frame 34 comprising thirty-two pads as shown in Figure 5. The pads within each pad frame 34 provide electrical connection points which are contacted by external test equipment as required by a test program to be described later.

The van der Pauw test structures 82 used in this chip (see Figure 8) are four terminal square structures which take advantage of the symmetry of the structure for direct determination of the sheet resistance. Accurate determination of sheet resistance is a requirement for measurement of linewidth variation. The van der Pauw structures 82 are arranged in two different frame types: mixed 62 (see Figure 6A) and VDP 1 64 (see Figure 6 B). Figure 7 depicts the location of the pad frames 72 containing the van der Pauw structures in the exemplary metal short flow chip described herein. In this exemplary chip, the van der Pauw structures occupy less than 1% of the chip area. In the van der Pauw structures the line width (LW) and the LW tap (see Figure 8) are the parameters that are varied. Table I shows the variations in the van der Pauw structures in the exemplary metal short flow chip described herein.

TABLE I

LW (μm)	LW tap (μm)
1 (DR)	1 (DR)
1.1	1.1
5	1
10	2
25	5
35	7
35	3.5
50	5

The nest defect size distribution structures are arrays of nested continuous lines designed for opens and shorts detection and for the extraction of defect size distribution. Line width and space between the line are the parameters that are varied to facilitate the extraction of defect size distribution. In the embodiment described herein, these structures occupy 50% of the chip area at locations 92 and 94 shown in Figure 9 and have fourteen variants in a total of ten cells 96. The amount of area these structures can occupy needs to be large enough to accurately detect less than 0.25 defects/cm^2 for one wafer. The number of variants typically include the design rule (DR), slightly below DR, slightly above DR and substantially above DR. Therefore, for example, if DR is 1.0 μm for line spacing, the plots might be for 0.9, 1.1, 1.3 and 2.5 as shown in Table II.

TABLE II

Line Width = Space (μm)	Length (cm)
0.9	39.6
1.0 (DR)	36
1.1	33
1.3	28.2
2.5	24.6

Each cell is split into six sub-cells to reduce the line resistance to reasonable levels (less than 250 kΩ) and to minimize the incidence of multiple defects per cell. In this embodiment, there are sixteen snakes per cell. An exemplary nest defect size distribution structure itself, generaly designated 1002, is depicted in Figure 10. The nest defect size distribution structures are designed such that the line width (LW) is equal to the spacing (S) between the lines to simplify subsequent analysis of data.

The Kelvin metal critical dimension (CD) structures are made up of a continuous straight line with terminal connections at each end. These structures allow for precise line resistance measurements which, in conjunction with the sheet resistance determined from the van der Pauw structures, allow for the determination of Kelvin line width. These structures are designed primarily to determine the variation in the electrical critical dimension. An exemplary Kelvin critical dimension structure, generally designated 110, is depicted in Figure 11. To study the impact of optical proximity effect on the variability in the electrical critical dimension, local neighborhood structures are varied. The parameters varied for the local neighborhood are the

number 112, line width 114 and space 116 of the lines. The global environment 118 around the Kelvin structures is also varied, primarily to study etch related effects on the electrical critical dimension (see Figure 11). Parameters varied for global neighborhood are the density and area. The global neighborhood structures can also serve other electrical measurement needs. For example, the yield of these structures can be measured so that not only metal critical dimension as a function of environment is obtained, but also yield as a function of environment. Figure 12 depicts the location of Kelvin structures 122 in the metal short flow chip described herein. These locations are chosen to cover available area. Tables III through IX describe the variations in the Kelvin structures used in the metal short flow chip described herein. These values were chosen as to cover the space identified in Figure 22(a) through 22(b). For example, the pattern density is centered around 45% and the line width and spaces are in the range of 1.0 to 3.3 μm since this is where most of an exemplary product layout is centered.

TABLE III

Line Width (μm)	Spacing (μm)	Number of Local Lines	Fixed Parameters
0.75	0.75	6	Local line width = 1μm
0.9	0.9		Density = 45%
1μm (DR)	1.0 (DR)		Line width of comb = 1.3μm
1.1	1.1		Dx max = 400 (μm)
1.3	1.3		Dy max = 400 (μm)
2.5	2.5		
3.3	3.0		
10	3.3		
	10		
	50		

TABLE IV

Line Width (μm)	Space ratio	Number of Local Lines	Fixed Parameters
0.75	2 to 1	6	Local line width = 1μm
0.9	3 to1	2	Density = 45%
1 (DR)			Line width of comb = 1.3μm
1.1			Dx max = 400 (μm)
1.3			Dy max = 400 (μm)
2.5			
3.3			
10			

TABLE V

Line Width (μm)	Number of Local lines	Local Line Width (μm)	Spacing (μm)	Fixed Parameters
0.75	1	1 (DR)	1 (DR)	Density = 0.45
0.9	2	1.3	1.3	Line width of comb = 1.3μm
1 (DR)	4			Dx max = 400 (μm)
1.1				Dy max = 400 (μm)
1.3				
2.5				
3.3				
10				

TABLE VI

Line Width (μm)	Spacing (μm)	Number of local lines	Density	LW comb (μm)	Fixed Parameters
1.0 (DR)	1.0(DR)	6	0	1.3	Dx max = 400 (μm)
1.3	1.3	2	0.2	10	Dy max = 400 (μm)
			0.40		
			0.45		
			0.50		

TABLE VII

Line Width (μm)	Spacing (μm)	Line width local (μm)	Fixed Parameters
0.9	1.0 (DR)	10	Number of local lines 2
1.0 (DR)	1.1	30	Density 0.45
1.1	1.3	100	Line width comb 1.3
1.3	2.5		Dx max = 400 (μm)
2.5	3.3		Dy max = 400 (μm)
3.3	10		
10			

TABLE VIII

Line Width (μm)	Spacing (μm)	Fixed Parameters
1.0 (DR)	1.0 (DR)	Number of local lines 6
1.1	1.1	Density - 0.45
1.3	1.3	Line width comb 1.3
2.5	2.5	Dx_max = 400(μm)
10	3.0	Dy_max = 400(μm)
	5.3	Line width local 1.3

TABLE IX

Line Width (μm)	Spacing (μm)	Local density	Dx_max	Fixed Parameters	Comments
0.75				Number of local lines 0	Isolated Kelvins
0.9				Density 0	
1.0 (DR)				Line width comb 0	
1.1				Line width local 0	
1.3				Dx_max = 400(μm)	
2.5				Dy_max = 400 (μm)	
3.3					
10					
	10	2.5		Line width = 1.0 (μm)	Local
	20	3.5		Local line width = 1.0 (μm)	neighborhood
	30	4.5		Number of local lines 2	size
	40	5.5		Density 0.45	
	50	6.5		Comb line width 1.3	
	60	7.5		Dx_max = 400(μm)	
	70	8.5		Dy_max = 400 (μm)	
	80	9.5			
			25	Line width 1.0	Global
			50	Line width local 1.0	neighborhood
			100	Space 1.0	size
			150	Number of local lines 6	
			200	Density 0.45	
			250	Line width comb 1.3	
			300	Dy_max 400 (μm)	
Line Width	Spacing	N_local	Dx_max	Fixed Parameters	Comments
1.0 (DR)	1.0 (DR)	6		D_local 5	Standards
1.3	1.3	6		Line width comb 1.3	
1.0	40	2		0.45	
1.3	40	2			

The snake, comb and snake & comb structures are designed primarily for the detection of shorts and opens across a wide variety of patterns. Snakes are used primarily for the detection of

opens and can also be used for monitoring resistance variation. Combs are used for monitoring shorts. Shorts and opens are fundamental yield loss mechanisms and both need to be minimized to obtain high product yield. Figure 13 shows the location of snakes and combs 1302 in the metal short flow chip described herein. Quadrant one 1304 also contains snakes 1402 and combs 1404 nested within the Kelvin structures asshown, for example in Figure 14. Line width (LW) and space (S), see Figure 14, are the parameters varied on these structures to study their impact on shorts and opens. Tables X through XIII describe the variations of snake and comb structures used in the metal short flow chip described herein. Again, the parameters were chosen such that the space covered in line width, line space, and density is similar to that seen in the example product layout, as shown in Figure 22(a) through 22(c).

TABLE X

LW_comb (μm)	Space (μm)	LW_snake (μm)	Fixed Parameters
20	0.9	1.0 (DR)	Dx_max = 200 μm
50	1.0 (DR)		Dy_max = 400 μm
100	1.1		
200	1.3		
300	2.5		
	3.0		
	3.3		
	10		
20	1.3	1.3	
50	3.1		
100	3.3		
200	3.5		
300	10		

TABLE XI

LW_comb (μm)	Space (μm)	Fixed Parameters
0.75	0.75	Dx_max = 200 μm
0.9	0.9	Dy_max = 400 μm
1.0 (DR)	1.0 (DR)	
1.1	1.1	
1.3	1.2	
2.0	1.3	
3.3	2.5	
10	3.0	
	3.3	
	10	

TABLE XII

Line Width (μm)	Fixed Parameters
0.75	Dx_max = 200 μm
0.9	Dy_max = 400 μm
1.0 (DR)	10 μm
1.1	
1.3	
2.5	
3.3	
1.0	

TABLE XIII

LW (μm)	Space (μm)	Fixed Parameters
20	0.7	Dx_max = 400 μm
50	1.0 (DR)	Dy_max = 200 μm
100	1.1	
200	1.3	
500	2.5	
	2.7	
	3.0	
	3.3	
	5	
	10	

Border and fringe structures are designed to study the impact of optical proximity correction (OPC) structures on shorts. These optical proximity corrections are usually added to improve via yields. However, it is necessary to check metal short yield with and without these borders to ensure that there is no detrimental impact to short yield. Borders 1502 are placed both at the end of the comb lines and in the interior of comb structures, generally designated 1504, as shown in Figure 15. Figure 16 shows the location of border structures, generally designated 1602, in the metal short flow chip described herein.

Scanning electron microscopy (SEM) structures are used for non-electrical measurements of line width through top down or cross sectional SEM. For the SEM bars in the metal short flow

chip described herein the line width is the same as the spacing between the lines in accordance with traditional SEM techniques. Figure 17 depicts the location of the SEM structures 1702 in the metal short flow chip described herein. The structures are placed at the bottom of each quadrant 1704, 1706, 1708 and 1710 of the embodiment depicted since this is where space was available.

In Figures 3 through 17, and accompanying text, an example characterization vehicle for metal yield improvement has been described. Other characterization vehicles for via, device, silicides, poly, el al, are often designed and utilized. However, the procedure and techniques for designing them are the same. For purposes of illustration, the example metal characterization vehicle will be carried through on extraction engines and yield models.

The extraction engine 18 has two main purposes: (1) it is used in determining the range of levels (e.g. linewidth, linespace, density) to use when designing a characterization vehicle. (2) It is used to extract the attributes of a product layout which are then subsequently used in the yield models to predict yield. (1) has already been described above with reference to how the line width, space and density of the snake, comb and Kelvin structures were chosen in the example characterization vehicle. Thus, most of the following discussion focuses on (2).

Since there are nearly infinite numbers of attributes that can be extracted from the product layout, it is impossible to list or extract all of them for each product. Thus, a procedure is

required to guide which attributes should be extracted. Usually, the characterization vehicle drives which attributes to extract. The process consists of:

1. List all structures in the characterization vehicle

2. Classify each structure into groups or families such that all structures in the family form an experiment over a particular attribute. For example, in the metal characterization vehicle discussed above, a table of family classifications might be:

Family	Attributes Explored
Nest structures	Basic defectivity over a few linewidths and spaces
Snakes and Combs	Yield over wide range of linewidths and spaces including very large widths next to small spaces and very large spaces next to small widths.
Kelvin-CD + van der Pauws	CD variation across density, linewidth, and linespace.
Border structures	Effect of different OPC schemes on yield.

3. For each family, determine which attributes must be extracted from the product layout. The exact attributes to choose are driven from which attributes are explored. For example, if a particular family explores yield over different ranges of space, then either a

histogram of spaces or the shortable area for each space must be extracted. For the above example, the required list of attributes might be:

Family	Attributes Explored	Attributes to Extract from Product Layout
(A) Nest structures	Basic defectivity over a few linewidths and spaces.	Critical area curves.
(B) Snakes and combs	Yield over wide range of linewidths and spaces including…	Shortable area and/or instance counts for each line width and space explored in the characterization vehicle.
(C) Kelvin-CD and van der Pauws	CD variation across density, linewidth, and space	Histograms of pattern density, linewidth, and linespace (similar to example shown in Figure 22)
(D) Border structures	Effect of different OPC schemes on yield	For each OPC scheme selected to use on product layout, the shortable area or instance count.

4. Use the attributes extracted in the appropriate yield models as previously described.

For other characterization vehicles, the families and required attributes will obviously be different. However, the procedure and implementation is similar to the example described above.

As previously stated, the yield model 16 is preferably constructed from data measured from at least a portion of a wafer which has undergone the selected fabrication process steps using the reticle set defined by the characterization vehicle 12. In the preferred embodiment, the yield is modeled as a product of random and systematic components:

$$Y = \left(\prod_{i=1}^{n} Ys_i \right) \left(\prod_{j=1}^{m} Yr_j \right)$$

The methods and techniques for determining Ys_i and Yr_j are as follows.

SYSTEMATIC YIELD MODELING

Since there are so many types of systematic yield loss mechanisms and they vary from fab to fab, it is not practicable to list every possible systematic yield model. However, the following describes two very general techniques and gives an example of their use especially within the context of characterization vehicles and the methodology described herein.

AREA BASED MODELS

The area based model can be written as:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)} \right]^{A(q)/A_o(q)}$$

Where q is a design factor explored in the characterization vehicle such as line width, line space, length, ratio of width/space, density, etc. $Y_o(q)$ is the yield of a structure with design factor q from the characterization vehicle. $A_o(q)$ is the shortable area of this structure and A(q) is the shortable area of all instances of type q on the product layout. $Y_r(q)$ is the predicted yield of this structure assuming random defects were the only yield loss mechanism. The procedure for calculating this quantity is described below in connection with random yield modeling.

The definition of shortable area is best illustrated with the example shown in Figure 18. This type of test structure can be used to determine if the fab is capable of yielding wide lines that have a bend with a spacing of s. In this sample test structure, a short is measured by applying a voltage between terminal (1) and (2) and measuring the current flowing from terminal (1) to (2). If this current is larger than a specified threshold (usually 1-100nA), a short is detected. The shortable area is defined to be the area where if a bridging occurs, a short will be measured. In the example of Figure 18, the shortable area is approximately x*s). The A(q) term is the shortable area of all occurrences of the exact or nearly exact patten (i.e. a large line with a spacing of s and a bend of 45 degrees) shown in Figure 18 in a product layout. The Yr(q) term is extracted by predicting the random yield limit of this particular structure using the critical area method described below.

It is important to realize that the effectiveness of this model is only as good as the number of structures and size of structures placed on the characterization vehicle. For example, if the angled bend test structure shown in Figure 18 were never put on the characterization vehicle or was not placed frequently enough to get a meaningful yield number, then there would be no hope of modeling the yield loss of wide line bends on the product layout. While it is difficult to define exactly how many of how big the test structure should be on the characterization vehicle, practical experience has shown that the total shortable area of each test structure on the characterization vehicle should ideally be such that $A(q)/Ao(q)<10$.

The above discussion has concentrated on shorts since they generally tend to dominate over open yield loss mechanisms. However, open yield loss mechanisms can be modeled equally well with this yield model so long as shortable area is replaced by open causing area.

INSTANCE BASED YIELD MODEL

The general form of the instance based yield model is:

$$Ys_i = \left[\frac{Y_o(q)}{Y_r(q)}\right]^{N_i(q)/N_o(q)}$$

Where Yo(q) and Yr(q) are exactly the same as in the area based yield model. Ni(q) is the number of times the unit cell pattern or very similar unit cell pattern to the test pattern on the characterization vehicle appears on the product layout. No(q) is the number of times the unit cell pattern appears on the characterization vehicle.

For example, Figure 19 shows a simple test pattern for examining the yield of T-shaped endings at the ends of lines near a space of s. This test pattern is measured by applying a voltage across terminals (1) and (2) and measuring the shorting current. If this pattern was repeated 25 times somewhere on the characterization vehicle, then No(q) would be 25x5=125 since there are five unit cells per each test structure.

If the number of times this unit cell occurs with a spacing of s near it is extracted from the product layout, the systematic yield of this type of structure can be predicted. For example, if there are five structures with 500 unit cells in each structure then No(q)=2500. If Ni(q) from some product was 10,000 and a yield of the test structures on the characterization vehicle of 98.20% was measured. Using the techniques described below, Yr(q) can be estimated as 99.67%. Using these numbers in the equation:

$$Ys_i = \left[\frac{0.9820}{0.9967}\right]^{10000/2500} = 92.84\%$$

RANDOM YIELD MODELING

The random component can be written as:

$$Y_r = e^{-\int_{x_0}^{\infty} CA(x) \times DSD(x)\,dx}$$

Where CA(x) is the critical area of defect size x and DSD(x) is the defective size distribution, as also described in"Modeling of Lithography Related Yield Losses for CAD of VSLI Circuits", W. Maly, IEEE Trans. on CAD, July 1985, pp161-177, which is incorporated by reference as if fully

set forth herein. Xo is the smallest defect size which can be confidently observed or measured. This is usually set at the minimum line space design rule. The critical area is the area where if a defect of size x landed, a short would occur. For very small x, the critical area is near 0 while very large defect sizes have a critical area approaching the entire area of the chip. Additional description of critical area and extraction techniques can be found in P. K. Nag and W. Maly, "Yield Estimation of VLSI Circuits," Techcon90, Oct. 16-18, 1990. San Jose; P. K. Nag and W. Maly, "Hierarchical Extraction of Critical Area for Shorts in Very Large ICs," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 10-18; I. Bubel, W. Maly, T. Waas, P. K. Nag, H. Hartmann, D. Schmitt-Landsiedel and S. Griep, "AFFCCA: A Tool for Critical Area Analysis with Circular Defects and Lithography Deformed Layout," in Proceedings of The IEEE International Workshop on Detect and Fault Tolerance in VLSI Systems, IEEE Computer Society Press 1995, pp. 19-27; C. Ouyang and W. Maly, "Efficient Extraction of Critical Area in Large VlSI ICs," Proc. IEEE International Symposium on Semiconductor Manufacturing, 1996, pp. 301-304; C. Ouyang, W. Pleskacz, and W. Maly, "Extraction of Critical Area for Opens in Large VLSI Circuits," Proc. IEEE International Workshop on Defect and Fault Tolerance of VLSI Systems, 1996, pp. 21-29, all of which references are incorporated in this detailed description as if fully set forth herein.

The defect size distribution represents the defect density of defects of size x. There are many proposed models for defect size distributions (see, for example, "Yield Models - Comparative Study", W. Maly, Defect and Fault Tolerance in VLSI Systems, Ed. by C. Stapper, et al, Plenum Press, New York, 1990; and "Modeling of Integrated Circuit Defect Sensitivities", C.H. Stapper, IBM J. Res. Develop., Vol. 27, No. 6, November, 1983, both of which are incorporated by reference as if fully set forth herein), but for purposes of illustrations, the most common distribution:

$$DSD(x) = \frac{D_o \times k}{x^p}$$

will be used where Do represents the total number of defects/cm^2 greater than x_o observed. P is a unitless value which represents the rate at which defects decay over size. Typically, p is between 2 and 4. K is a normalization factor such that

$$\int_{x_o}^{\infty} \frac{k}{x^p} dx = 1$$

The following two sections describe techniques for extracting defect size distributions from characterization vehicles.

THE NEST STRUCTURE TECHNIQUE

The nest structure is designed for extracting defect size distributions. It is composed of N lines of width w and space s as shown in Figure 20. This structure is tested by measuring the shorting current between lines 1 and 2, 2 and 3, 3 and 4, ..., and N-1 and N. Any current above a given spec limit is deemed a short. In addition, opens can be testing by measuring the resistance of lines 1, 2, 3, ..., N-1, and N. Any resistance above a certain spec limit is deemed to be an open line. By examining how many lines are shorted together the defect size distribution can be determined.

If only two lines are shorted then the defect size must be greater than s and no larger than 3w + 2s. Any defects smaller than s will not cause a short at all while defects larger than 3w+2s are guaranteed to cause a short of at least 3 lines. For each number of lines shorted, an interval of sizes can be created:

Number Lines Shorted	Size Interval
2	s to 3w+2s
3	2s+w to 3s+4w
4	3s+2w to 4s+5w
...	...
N	(N-1)s+(N-2)w to (N)s+(N+1)w

It should be noted that the intervals overlap; thus, a defect size distribution cannot be directly computed. This restriction only places a limit on p extraction. Thus, in order to estimate p, a p estimate is computed from the distribution from all the even number lines and then from all the odd number lines. Finally, the two values are averaged together to estimate p. To extract p, the ln (number of faults for x lines shorted) vs log ([x-1]s + [x-2]w) is plotted. It can be shown that the slope of this line is -p. The Do term is extracted by counting the number of failures at each grouping of lines and dividing by the area of the structure. However, for very large Do, this estimate will be too optimistic. Additional information on extracing defect size distribution from structures similar to the test structures can be found, for example, in "Extraction of Defect Size Distribution in an IC Layer Using Test Structure Data", J. Khare, W. Maly and M.E. Thomas, IEEE Transactions on Semiconductor Manufacturing, pp. 354-368, Vol. 7, No. 3, August, 1994, which is incorporated by reference as if fully set forth herein.

As an example, consider the following data taken from 1 wafer of 100 dies:

Number Lines Shorted	Number of Failures
2	98
3	11
4	4
5	2
6	1
7	0
8	0

If the structure size is lcm^2 then the Do would be 98 + 11 +4 + 2 +1 = 133 / (100 * 1) = 1.33 defects/cm^2. Also, the plot of log (number of failures) vs log ([x-1]s + [x-2]w) (see Figure 21) shows that p=2.05.

THE COMB STRUCTURE TECHNIQUE

Assuming a comb of width = space = s, it can be shown that the yield of this structure can be written as:

$$\ln[|\ln(Y)|] = \ln[-\int_{x_0}^{\infty} DSD(x) \times CA(x)dx] \propto (1-p) \times \ln(s)$$

Thus, from the slope of the plot of ln[|ln(Y)|] vs. ln(s), p can be estimated. The Do extraction technique is the same technique as mentioned above.

YIELD IMPACT AND ASSESSMENT

Once a sufficient number of characterization vehicles has been run and yield estimates are made for each characterization vehicle, the results are placed in a spread sheet to enable prioritization of yield activities. Tables XIV through XVI are examples of information contained in such a spread sheet. It has been divided into sections of metal yield, poly and active area (AA) yield (Table XIV), contact and via yield (Table XV), and device yield (Table XVI). The columns on the left indicate systematic yield loss mechanisms while the columns on the right indicate random yield loss mechanisms. Although the exact type of systematic failure mechanisms vary from product to product, and technology by technology, examples are shown in Tables XIV through XVI.

Usually, targets are ascribed to each module listed in the spread sheet. The further a module yield is away from a target, the more emphasis and resources are devoted to fixing the problem. For example, if the target was set artificially at 95 percent for each module in the example shown in Tables XIV through XVI, then clearly (M_2 -0 M_3) vias (75.12%) followed by similar vias (M_1 -0 M_2) (81.92%), M_1 shorts (82.25%), and contacts to poly (87.22%) are below target and, with vias (M_2 -0 M_3) needing the most amount of work and contacts to poly needing the least amount of work.

Within each module, it is also possible to tell where the greatest yield loss is situated. That is, is it one particular systematic mechanism being the yield down or is it merely a random defectivity problem, or is it some combination of the two? For example, as shown in Table XV, via (M_2 -0 M_3) yield loss is clearly dominated by a systematic problem affecting vias connected to

long metal runners on the M_2 level (77.40%). Vias from (M_1 -> M_2) are affected by the same problems (91.52%) in addition to a random defectivity problem (92.49%). Solving vias (M_1 -> M_2) yield problems would require fixing both of these problems.

As shown in Table XIV, M_1 yield loss is also dominated by a random defectivity issue (85.23%) in addition to a systematic problem affecting wide lines near small spaces (96.66%). Fixing both of these problems would be required for improving Metal 1. Similar conclusions can be made for other modules in the spread sheet.

For the worst yielding modules, frequent running of further characterization vehicles for this module would be required. Usually, splits will be done on these characterization vehicles to try and improve and validate those improvements in module yield. For the modules which are within target, routine monitoring of short flow characterization vehicles would still be required to validate that there has been no down turn or other movement in module yield. However, these characterization vehicles can be run less frequently than for those modules with known problems.

TABLE XIV

Opens and Shorts (Metal Layers)

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Do	P	Estimated Yield	
Metal-1	Random Yield				0.7 defects/cm^2	2.3	85.23%	
	Wide lines near small space	0.034		96.66%				
	Wide space near small lines	0.00014		99.99%				
	Yield for OPC structures		72,341	99.86%				
	Bent lines		492	100.00%				
	Total for M1						82.25%	
Metal-2	Random Yield				0.35 defects/cm^2	1.92	97.45%	
	Wide lines near small space	0.00079		99.92%				
	Wide space near small lines	0.000042		100.00%				
	Yield for OPC structures		1040372	97.94%				
	Bent lines		103	100.00%				
	Total for M2						95.36%	
Metal-3	Random Yield				0.25 defects/cm^2	2.02	96.92%	
	Wide lines near small space	0.0000034		100.00%				
	Wide space near small lines	0		100.00%				
	Yield for OPC structures		352	100.00%				
	Bent lines		7942	99.92%				
	Total for M3						96.84%	

Open and Shorts (Poly and AA Layer)

Poly	Random Yield (without silicide)				0.17 defects/cm^2	2.03	99.81%	
	Random Yield (with silicide)				4.34defects/cm^2	4.56	89.54%	89.71% from silicide
	Wide lines near small space	0		100.00%				
	Wide space near small lines	0.01203		98.80%				
	Yield for OPC structures		0	100.00%				
	Bent lines		786541	92.44%				
	Over wide AA	0.034		96.66%				
	Over narrow AA	0.101		99.00%				
	Total for Poly						87.22%	
AA	Random Yield (without silicide)				1.3	3.45	99.12%	
	Random Yield (with silicide)				1.7	3.02	98.72%	99.60% from silicide
	Wide lines near small space		10952	99.96%				
	Wide space near small lines		0	100.00%				
	Total for AA						98.70	

TABLE XV

Contacts and Vias

		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism			
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield	
Contact to Poly	Random Yield (without silicide)				2.20E-09	3270432	99.28%	
	Random Yield (with silicide)				3.10E-09	3270432	98.99%	99.71%
	Yield for Long Runners (on M1)		11,921	100.00%				
	Yield for Long Runners (on Poly)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	96.46%				
	Total for Contact to Poly						94.80%	
Contact to n+AA	Random Yield (without silicide)				2.20E-09	5270432	98.85%	
	Random Yield (with silicide)				3.10E-09	5270532	98.38%	99.53%
	Yield for Long Runners (on M1)		75,324	99.99%				
	Yield for Long Runners (on n+AA)		0	100.00%				
	Yield for Redundant Vias		4032007	99.60%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (n+)						96.78%	
Contact to p+AA	Random Yield (without silicide)				2.20E-09	6093450	98.67%	
	Random Yield (with silicide)				3.10E-09	6093450	98.13%	
	Yield for Long Runners (on M1)		96,732	99.99%				
	Yield for Long Runners (on p+AA)		0	100.00%				
	Yield for Redundant Vias		39421	100.00%				
	Yield for very isolated contacts		7200	99.93%				
	Total for Contact to AA (p+)						96.74%	
Vias M1->M2	Random Yield (single vias)				1.10E-08	7093210	92.49%	
	Yield for Long Runners (M2)		88640	91.52%				
	Yield for Long Runners (M1)		97645	99.03%				
	Yield for Redundant Vias		11003456	96.91%				
	Yield for Isolated Vias		119582	96.81%				
	Total for Via M1-M2						81.92%	
Vias M2->M3	Random Yield (single vias)				3.10E-09	4002063	98.77%	
	Yield for Long Runners (M3)		256128	77.40%				
	Yield for Long Runners (M2)		103432	96.97%				
	Yield for Redundant Vias		7096230	99.29%				
	Yield for Isolated Vias		1024	99.99%				
	Total for Via M2-M3						75.12%	

TABLE XVI

	Devices					
		Systematic Yield Loss Mechanisms			Random Yield Loss Mechanism		
		Shortable Area (cm^2)	Instant Count	Estimated Yield	Fault Rate	Number	Estimated Yield
NMOS	Random Yield (Logic Xtor)				2.90E-09	1395228	99.60%
	Random Yield (SRAM Xtor)				2.80E-09	2226720	99.38%
	S/D Shorts				1.00E-09	3621948	99.64%
	Bent Transistors		1113360	99.89%			
	Near Large AA		754000	99.92%			
	Near Small AA		1023452	99.90%			
	Total for NMOS Transistors						98.33%
PMOS	Random Yield (Logic Xtor)				1.80E-09	1491003	99.73%
	Random Yield (SRAM Xtor)				3.10E-09	1113360	99.66%
	S/D Shorts				9.00E-10	2604363	99.77%
	Bent Transistors		556680	99.94%			
	Near Large AA		789092	99.92%			
	Near Small AA		1309970	99.87%			
	Total for PMOS Transistors						98.89%

I claim:

I claim:

1. A system for predicting yield of integrated circuits comprising:

a) at least one type of characterization vehicle including at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) a yield model which embodies a layout as defined by the characterization vehicle, said yield model having been subjected to at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) a product layout; and

d) an extraction engine for extracting predetermined layout characteristics from the product layout, which characteristics are used in connection with the yield model to produce a yield prediction.

2. A system in accordance with claim 1 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

3. A system in accordance with claim 2 wherein the characterization vehicle comprises a short flow test vehicle.

4. A system in accordance with claim 3 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

5. A system in accordance with claim 4 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

6. A system in accordance with claim 3 wherein the characterization vehicle comprises a metal short flow test vehicle.

7. A system in accordance with claim 6 wherein the metal short flow test vehicle includes at least one basic structure.

8. A system in accordance with claim 7 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;
b) snake structure;
c) comb structure;
d) snake and comb structures;
e) nest defect size distribution structure;
f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

9. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

10. A system in accordance with claim 8 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

11. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one via or contact.

12. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout include at least one active device.

13. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one silicide region.

14. A system in accordance with claim 4 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

15. A system in accordance with claim 1 wherein the extraction engine is also used to determine a range of layout feature levels for use when designing a characterization vehicle.

16. A system in accordance with claim 15 wherein the layout feature range of levels includes line width, line space and line density.

17. A method for predicting a yield for an integrated circuits comprising:

a) providing information for fabricating at least one type of characterization vehicle having at least one feature which is representative of at least one type of feature to be incorporated into a final integrated circuit product;

b) fabricating a characterization vehicle which embodies a yield model and layout features representative of the product employing at least one of the process operations making up the fabrication cycle to be used in fabricating the integrated circuit product;

c) providing a product layout;

d) extracting predetermined layout characteristics from the product layout; and

e) using the extracted layout characteristics in connection with the yield model to produce a yield prediction.

18. A method in accordance with claim 17 wherein the characterization vehicle layout contains the same range of variation of each feature as appears on the product layout.

19. A method in accordance with claim 18 wherein the characterization vehicle comprises a short flow test vehicle.

20. A method in accordance with claim 19 wherein the characterization vehicle comprises a short flow test vehicle having a partial layout including features which are representative of a proposed product layout.

21. A method in accordance with claim 20 wherein the characterization vehicle defines at least one active region and at lease one preselected neighboring feature representative of a proposed product layout.

22. A method in accordance with claim 19 wherein the characterization vehicle comprises a metal short flow test vehicle.

23. A method in accordance with claim 22 wherein the metal short flow test vehicle includes at least one basic structure.

24. A method in accordance with claim 23 wherein said at least one basic structure is selected from the group consisting of:

a) Kelvin metal critical dimension structure;

b) snake structure;

c) comb structure;

d) snake and comb structures;

e) nest defect size distribution structure;

f) van der Pauw structure;

g) optical proximity correction structure; and

h) scanning electron microscopy structure.

25. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in a single metal layer.

26. A method in accordance with claim 24 wherein the metal short flow test vehicle includes at least one basic structure in multiple metal layers.

27. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one via or contact.

28. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout include at least one active device.

29. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one silicide region.

30. A method in accordance with claim 20 wherein the features which are representative of a proposed product layout includes at least one polysilicide or polysilicon region.

31. A method in accordance with claim 17 wherein the extraction engine is also used to determine a range of levels for use when designing a characterization vehicle.

32. A method in accordance with claim 31 wherein the range of levels includes line width, line space and line density.

33. A method in accordance with claim 17 wherein the predetermined layout characteristics are extracted from the product layout using a process which includes the steps of:

a) listing all structures in the characterization vehicle;

b) classifying each structure into families such that all structures in each family form an experiment over a particular attribute; and

c) for each family, determine which attributes are to be extracted forr the product layout.

34. A method in accordance with claim 33 wherein the families include a family comprising nest structures for exploring basic defectivity over a selected number of line widths and spaces.

35. A method in accordance with claim 33 wherein the families include a family comprising snake and comb structures for exploring yield over a predetermined range of line widths and spaces.

36. A method in accordance with claim 35 wherein the predetermined range of line widths and spaces include relatively large line widths next to relatively small spaces and relatively large interline spaces next to relatively small line widths.

37. A method in accordance with claim 33 wherein the families include a family comprising Kelvin critical dimension and van der Pauw structures for exploring critical dimension variation across line density, width and spacing.

38. A method in accordance with claim 33 wherein the families include a family comprising border structures for exploring the effect of various optical proximity correction schemes on yield.

39. A system for determining and ranking yield loss mechanisms given characterization vehicle data and extracted layout attributes.

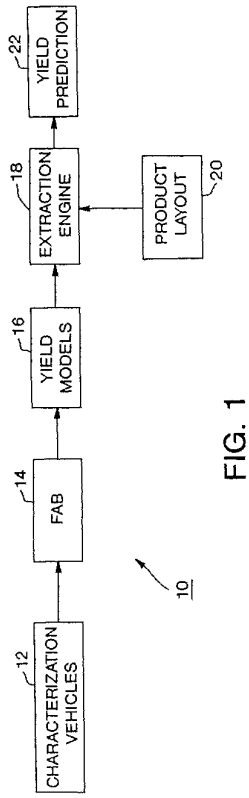

10
12
CHARACTERIZATION VEHICLES
14
FAB
16
YIELD MODELS
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
22
YIELD PREDICTION

FIG. 1

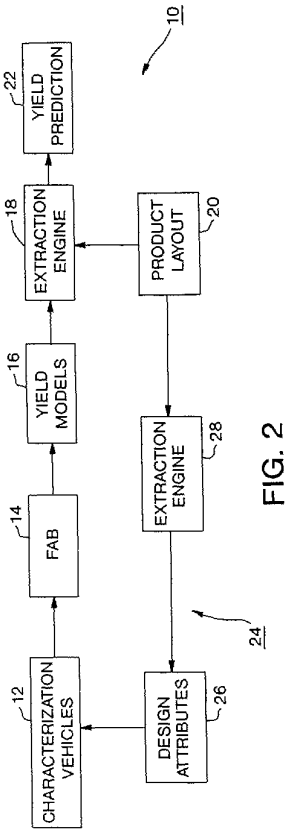

10
12
CHARACTERIZATION VEHICLES
14
FAB
16
YIELD MODELS
18
EXTRACTION ENGINE
20
PRODUCT LAYOUT
22
YIELD PREDICTION
24
26
DESIGN ATTRIBUTES
28
EXTRACTION ENGINE

FIG. 2

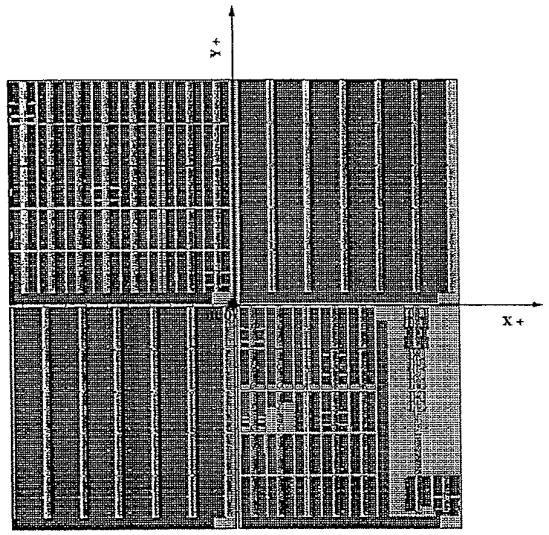


FIG. 3

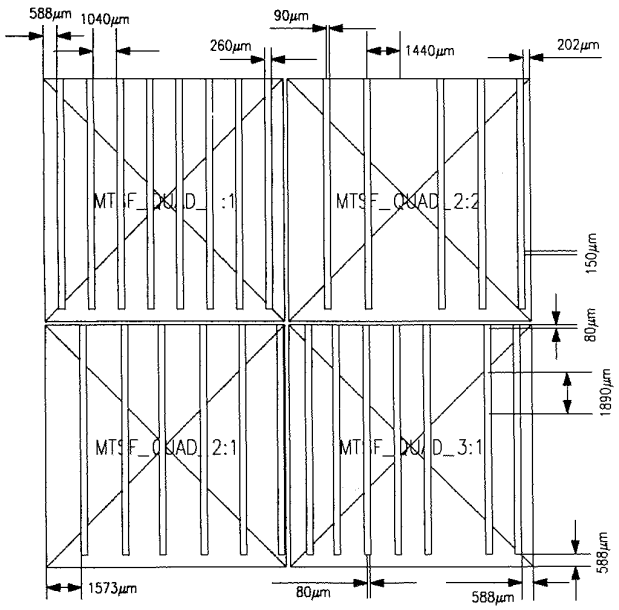

588μm
1040μm
90μm
260μm
1440μm
202μm
150μm
80μm
1890μm
588μm
1573μm
80μm
588μm

FIG. 4

FIG. 5

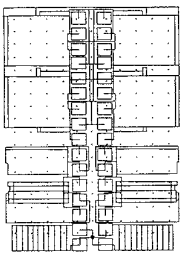


FIG. 6A

FIG. 6B

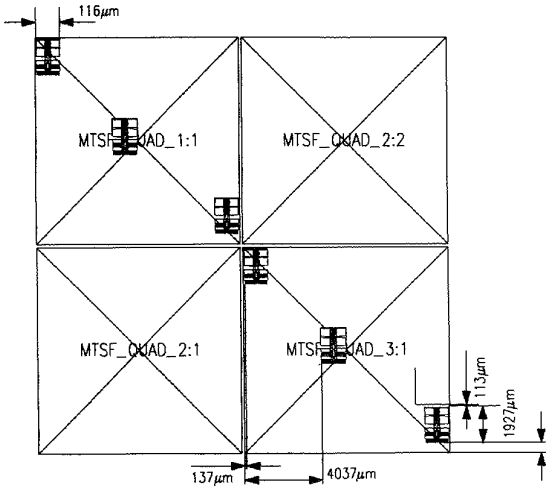

116μm
MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
113μm
1927μm
137μm
4037μm

FIG. 7

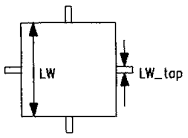

LW
LW_top

FIG. 8

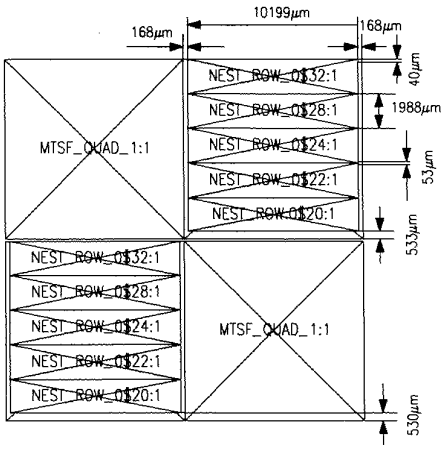

10199μm
168μm
168μm
40μm
1988μm
53μm
533μm
530μm
MTSF_QUAD_1:1
MTSF_QUAD_1:1
NEST_ROW_01$32:1
NEST_ROW_01$28:1
NEST_ROW_01$24:1
NEST_ROW_01$22:1
NEST_ROW_01$20:1
NEST_ROW_01$32:1
NEST_ROW_01$28:1
NEST_ROW_01$24:1
NEST_ROW_01$22:1
NEST_ROW_01$20:1

FIG. 9

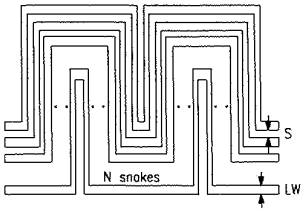

S
N snakes
LW

FIG. 10

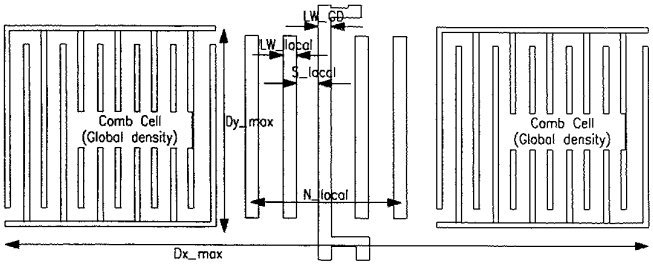

LW_GD
LW_local
S_local
Comb Cell
(Global density)
Dy_max
Comb Cell
(Global density)
N_local
Dx_max

FIG. 11

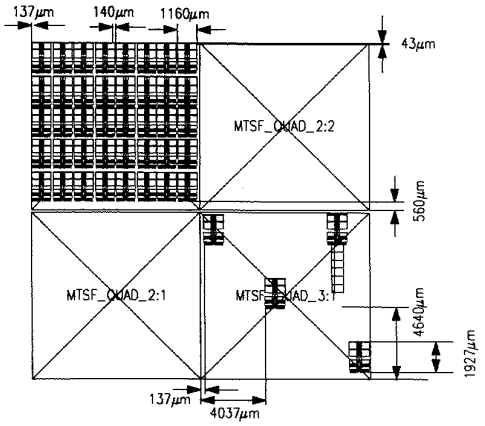

137μm
140μm
1160μm
43μm
MTSF_QUAD_2:2
560μm
MTSF_QUAD_2:1
MTSF_QUAD_3:1
4640μm
1927μm
137μm
4037μm

FIG. 12

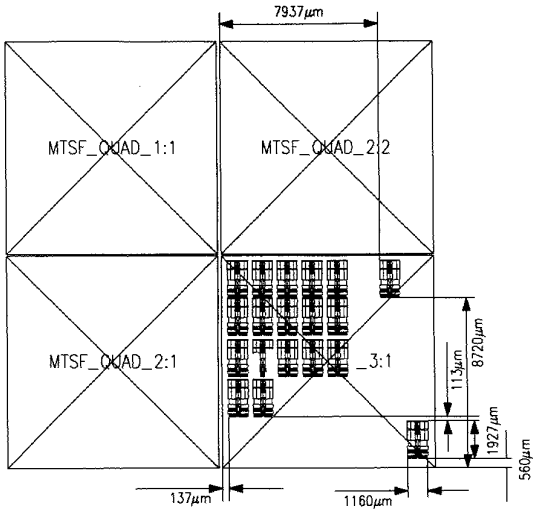

7937μm
MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
_3:1
8720μm
113μm
1927μm
560μm
137μm
1160μm

FIG. 13

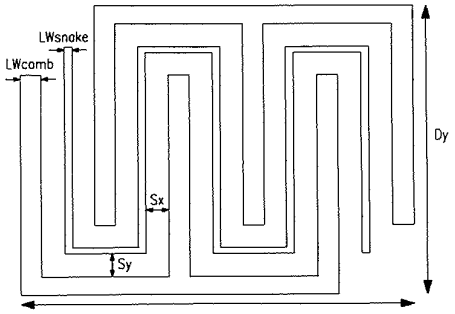

LWsnake
LWcomb
Dy
Sx
Sy

FIG. 14

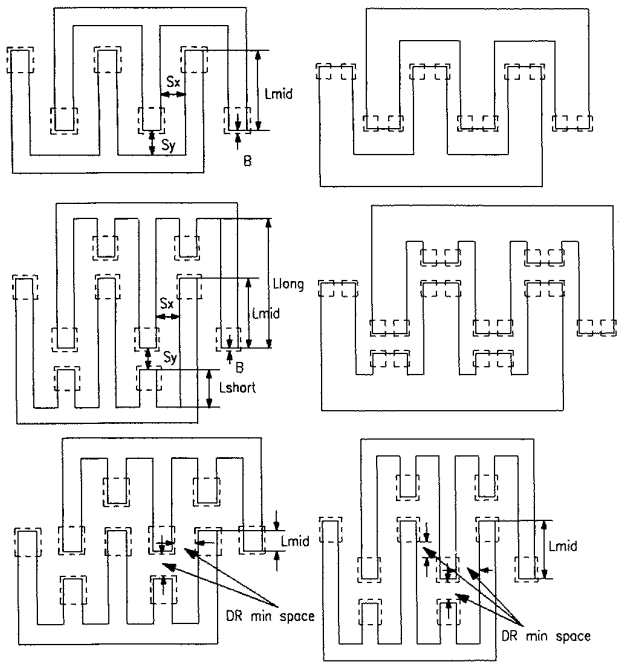

Sx
Sy
Lmid
B
Llong
Lmid
Sx
Sy
B
Lshort
Lmid
DR min space
Lmid
DR min space

FIG. 15

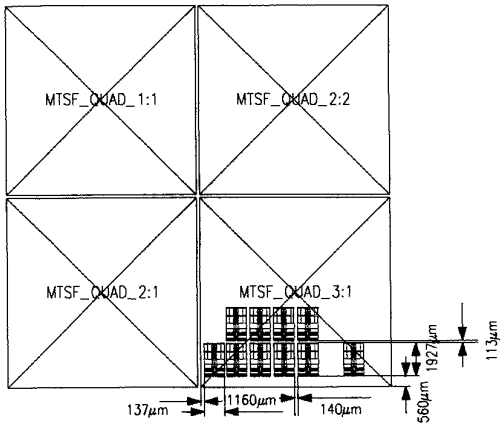

MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
113μm
192μm
560μm
137μm
1160μm
140μm

FIG. 16

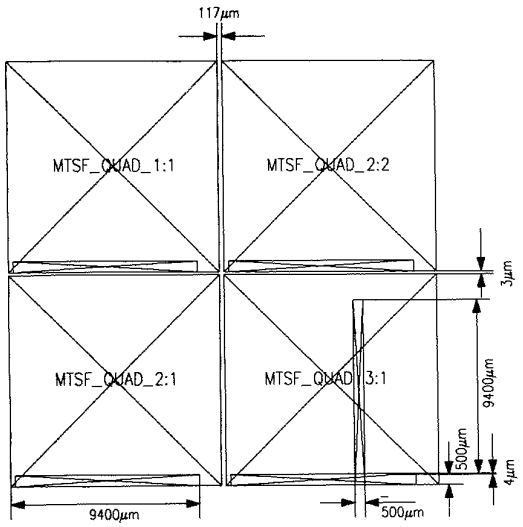

117μm
MTSF_QUAD_1:1
MTSF_QUAD_2:2
MTSF_QUAD_2:1
MTSF_QUAD_3:1
3μm
9400μm
500μm
4μm
9400μm
500μm

FIG. 17

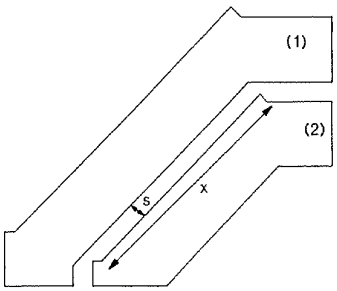


FIG. 18

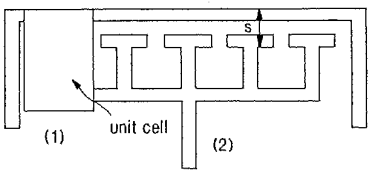


FIG. 19

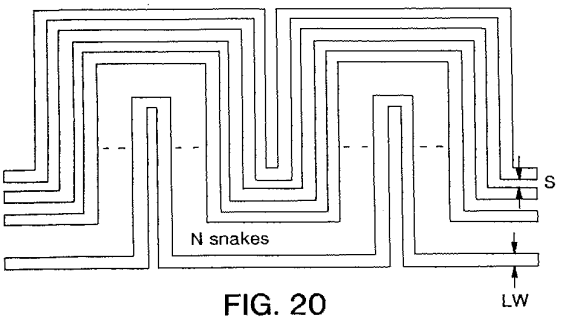

S
N snakes
LW

FIG. 20

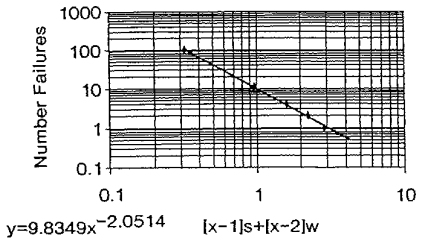

Number Failures
1000
100
10
1
0.1
0.1
1
10
y=9.8349x^-2.0514
[x-1]s+[x-2]w

FIG. 21

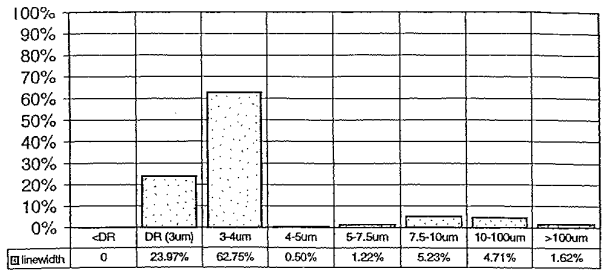


FIG. 22(a)

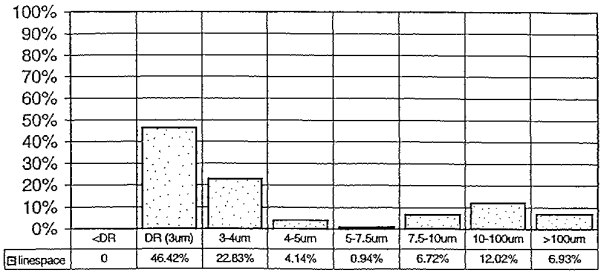


FIG. 22(b)

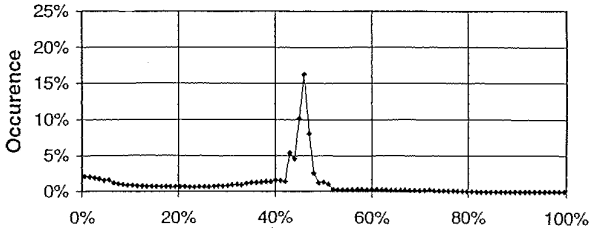


FIG. 22(c)

フロントページの続き

(81)指定国 AP(GH,GM,KE,LS,MW,MZ,SD,SL,SZ,TZ,UG,ZW),EA(AM,AZ,BY,KG,KZ,MD,RU,TJ,TM),EP(AT,BE,CH,CY,DE,DK,ES,FI,FR,GB,GR,IE,IT,LU,MC,NL,PT,SE,TR),OA(BF,BJ,CF,CG,CI,CM,GA,GN,GW,ML,MR,NE,SN,TD,TG),AE,AG,AL,AM,AT,AU,AZ,BA,BB,BG,BR,BY,BZ,CA,CH,CN,CR,CU,CZ,DE,DK,DM,DZ,EE,ES,FI,GB,GD,GE,GH,GM,HR,HU,ID,IL,IN,IS,JP,KE,KG,KP,KR,KZ,LC,LK,LR,LS,LT,LU,LV,MA,MD,MG,MK,MN,MW,MX,MZ,NO,NZ,PL,PT,RO,RU,SD,SE,SG,SI,SK,SL,TJ,TM,TR,TT,TZ,UA,UG,UZ,VN,YU,ZA,ZW

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