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(54) **SYSTEM AND METHOD FOR PROVIDING SUBSTANTIALLY UNINTERRUPTED DIGITAL VIDEO DURING A SWITCHING EVENT BETWEEN A FIRST DIGITAL VIDEO SOURCE AND A SECOND DIGITAL VIDEO SOURCE**

(71) Applicant: **Crestron Electronics, Inc.**, Rockleigh, NJ (US)

(72) Inventors: **Adolfo Velasco**, Dumont, NJ (US); **Daniel Jackson**, Norwood, NJ (US)

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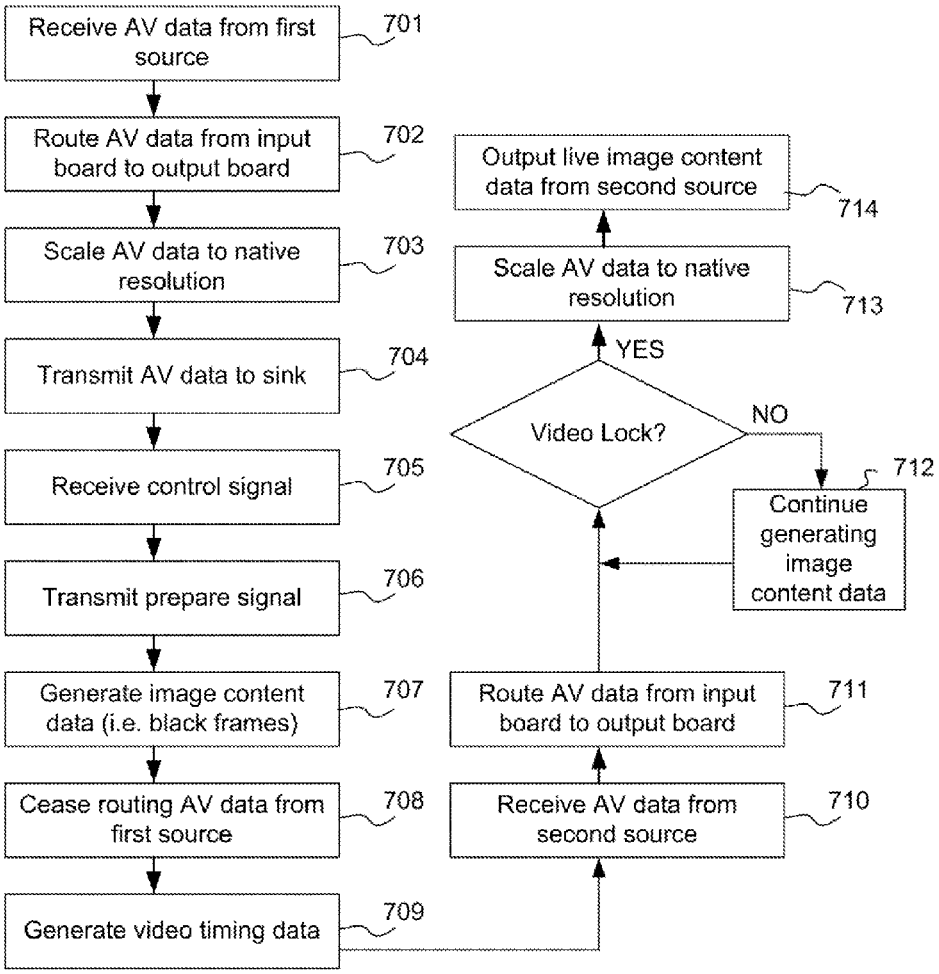
(57) **ABSTRACT**

When switching sources, resolutions or refresh rates in a video distribution network, switching times are reduced by maintaining video lock and security authentication between a video switcher and a video sink. The scaler maintains video lock and security authentication by continuing to generate video timing data during switching events. The scaler also facilitates an aesthetically pleasing transition by generating image content data prior to and after the switching event.



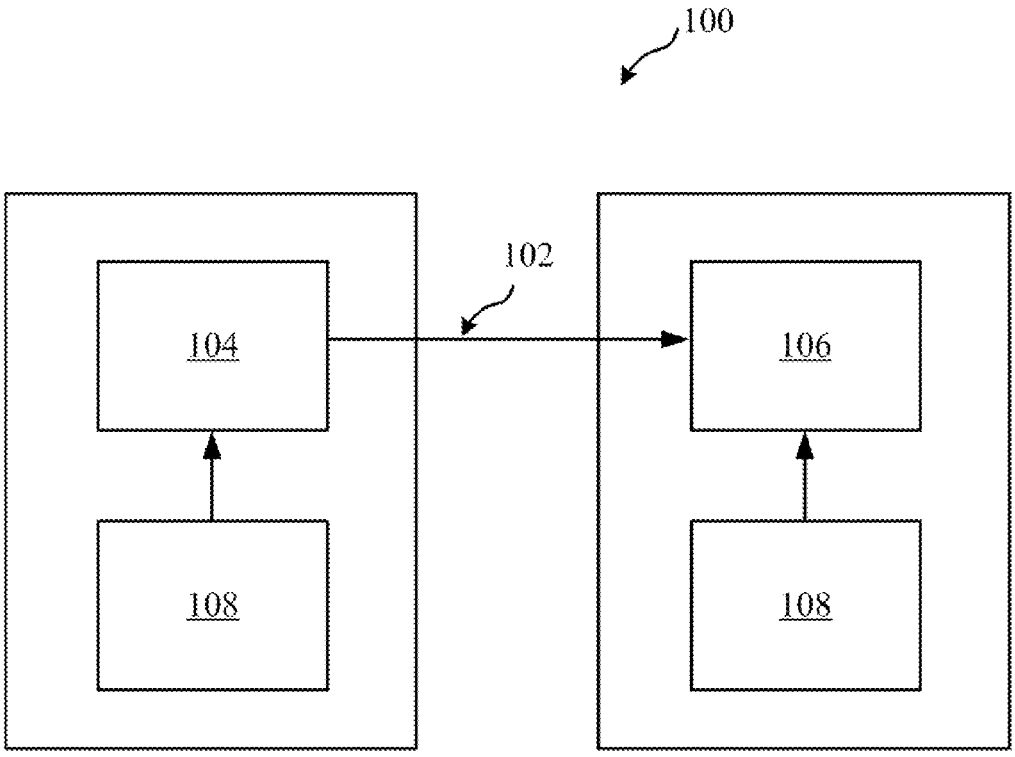


FIG. 1

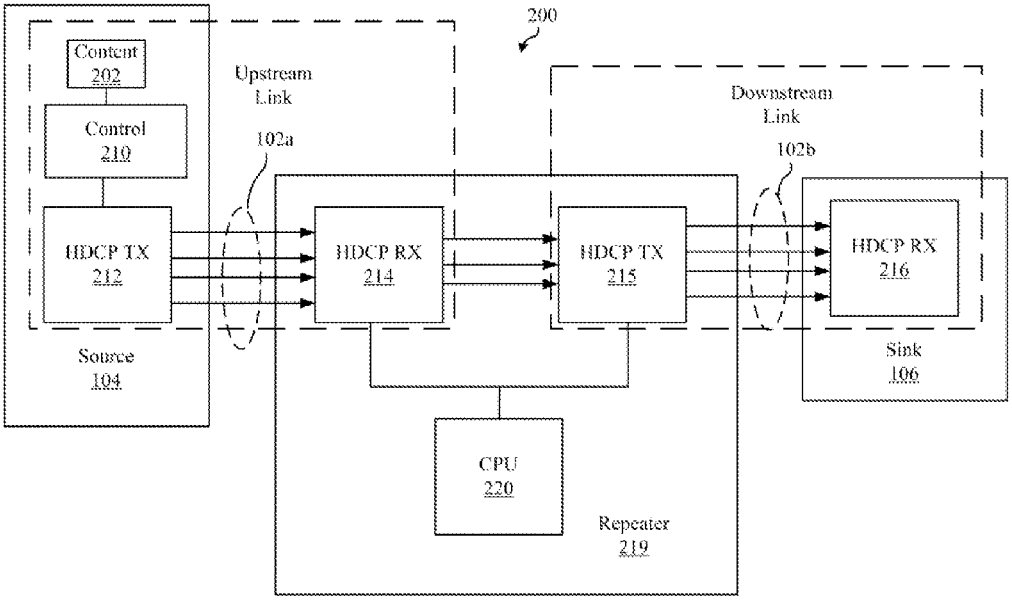

200
Content
202
Control
210
HDCP TX
212
Source
104
Upstream
Link
102a
HDCP RX
214
HDCP TX
215
Downstream
Link
102b
HDCP RX
216
Sink
106
CPU
220
Repeater
219

FIG. 2

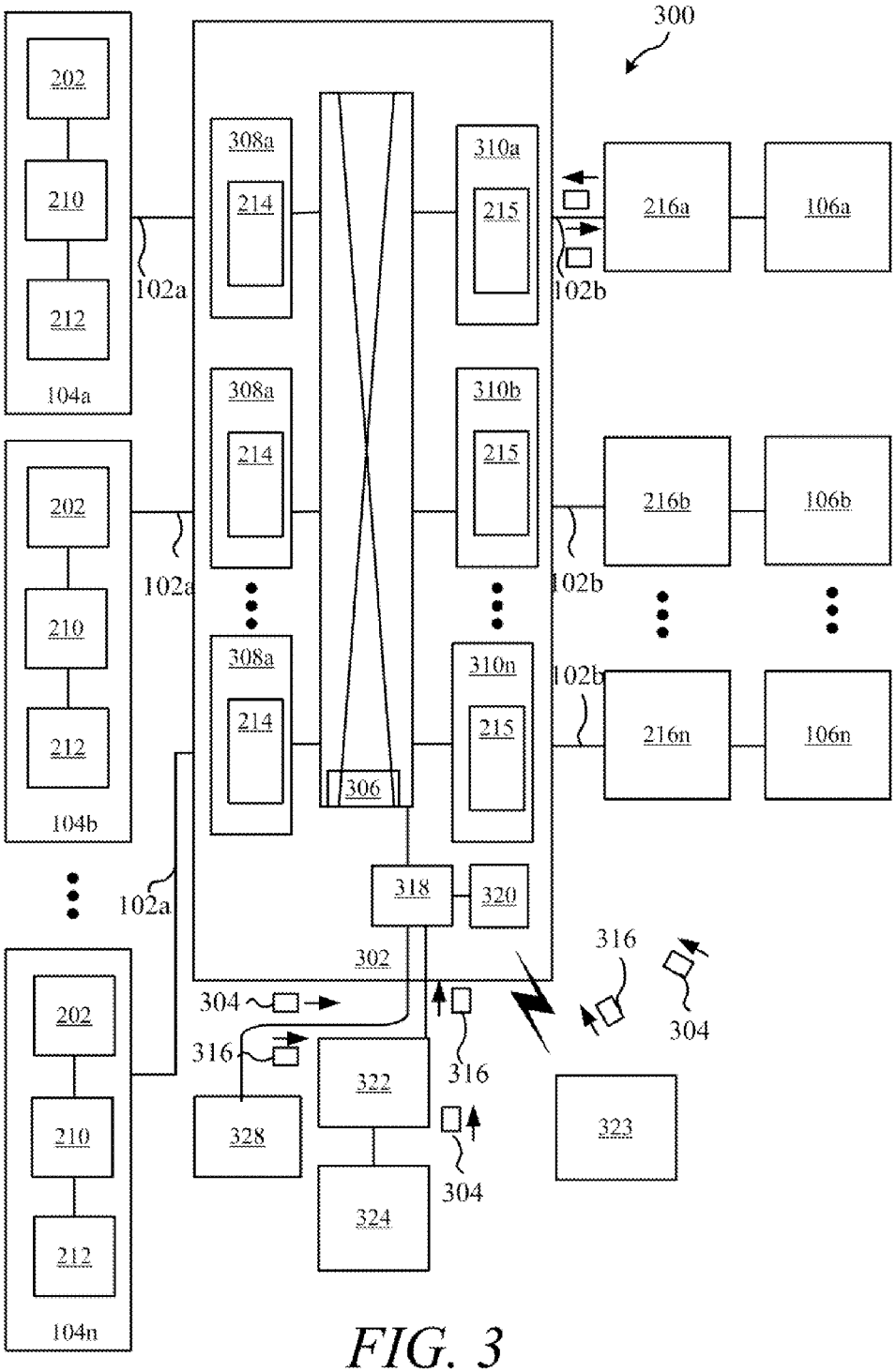

300
202
210
212
104a
102a
308a
214
310a
215
216a
106a
102b
308a
214
310b
215
216b
106b
202
210
212
104b
102a
102b
308a
214
310n
215
216n
106n
306
102a
318
320
302
316
304
316
304
202
210
212
104n
304
316
322
328
323
304
324

FIG. 3

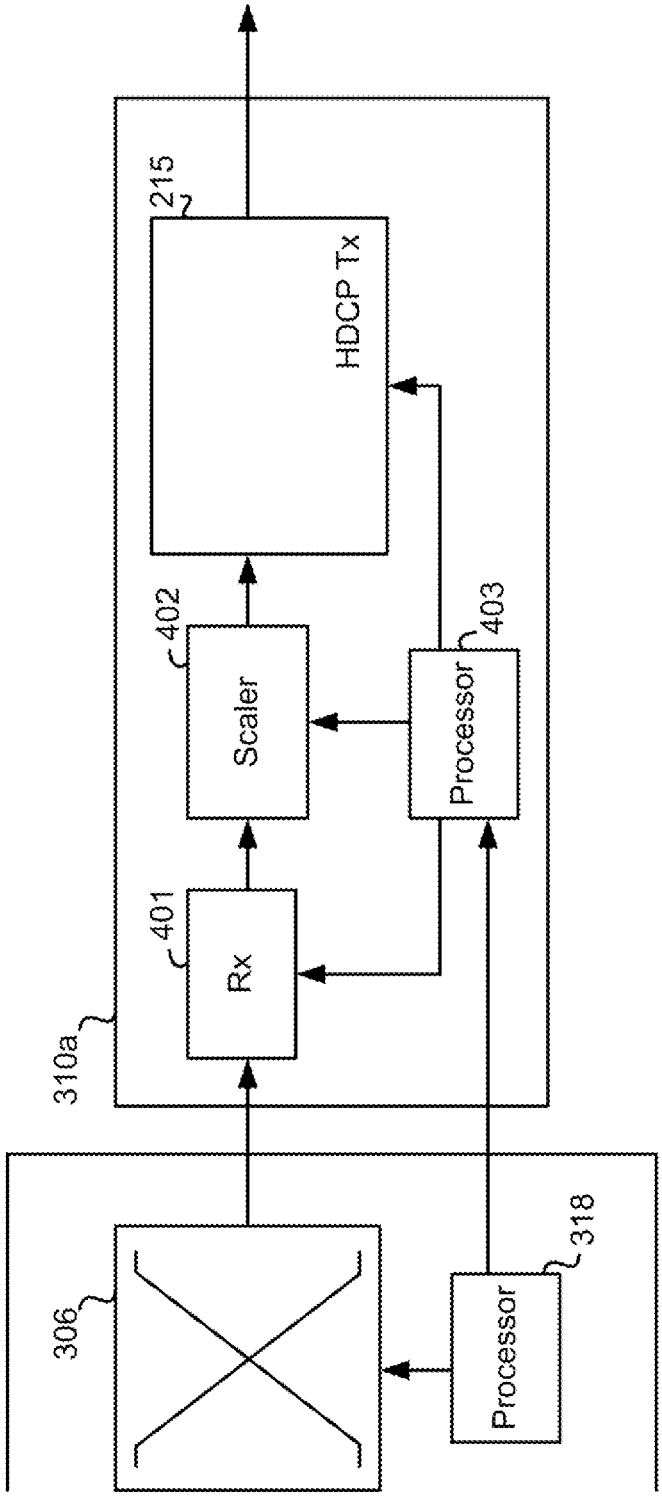

215
HDCP Tx
402
Scaler
403
Processor
401
Rx
310a
306
318
Processor

FIG. 4

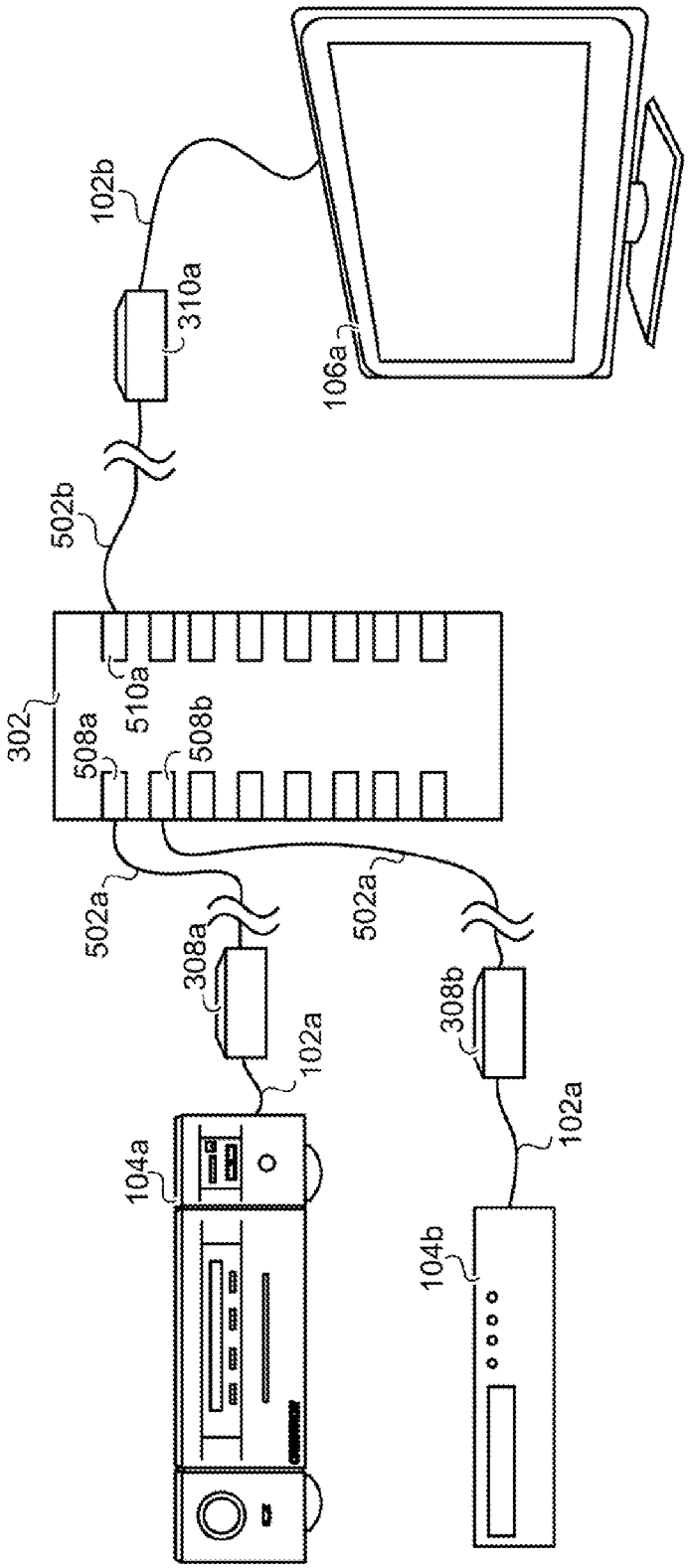

102b
310a
106a
502b
302
508a
510a
508b
502a
502a
308a
308b
102a
102a
104a
104b

FIG. 5

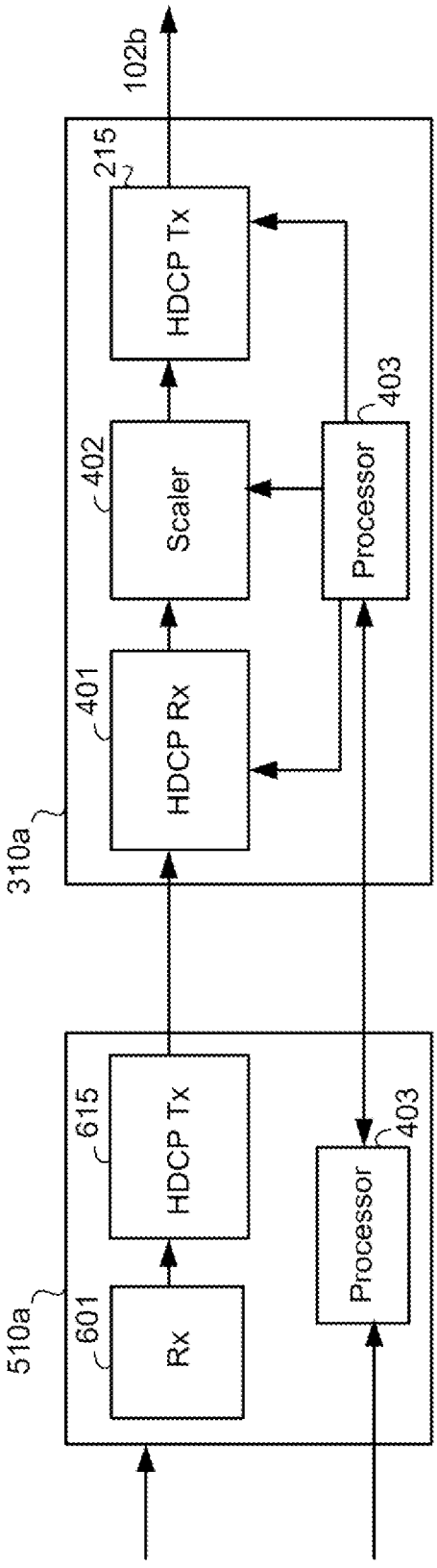

102b
215
HDCP Tx
403
402
Scaler
Processor
401
HDCP Rx
310a
615
HDCP Tx
403
Processor
601
Rx
510a

FIG. 6

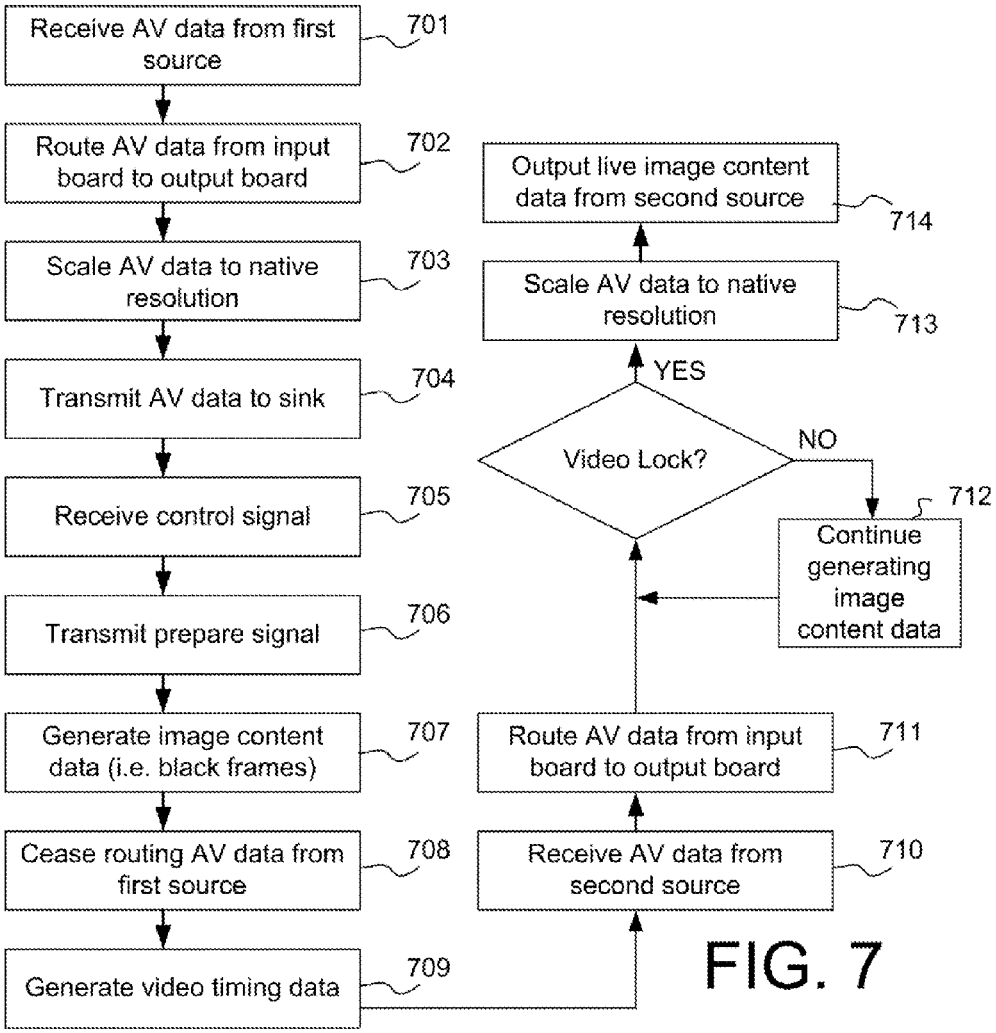

Receive AV data from first source
701
Route AV data from input board to output board
702
Scale AV data to native resolution
703
Transmit AV data to sink
704
Receive control signal
705
Transmit prepare signal
706
Generate image content data (i.e. black frames)
707
Cease routing AV data from first source
708
Generate video timing data
709
Receive AV data from second source
710
Route AV data from input board to output board
711
Video Lock?
YES
NO
712
Continue generating image content data
Scale AV data to native resolution
713
Output live image content data from second source
714

FIG. 7

SYSTEM AND METHOD FOR PROVIDING SUBSTANTIALLY UNINTERRUPTED DIGITAL VIDEO DURING A SWITCHING EVENT BETWEEN A FIRST DIGITAL VIDEO SOURCE AND A SECOND DIGITAL VIDEO SOURCE

PRIORITY INFORMATION

[0001] The present application claims priority under 35 U.S.C. §120 to U.S. Non-Provisional patent application Ser. No. 13/764,315, filed 11 Feb. 2013, and which itself claims priority to U.S. Provisional Patent Application Ser. No. 61/597,448, filed 10 Feb. 2012, the entire contents of all of which are expressly incorporated herein by reference.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] Related subject matter is disclosed in the following U.S. patent and co-pending U.S. Non-provisional patent applications, the entire contents of all of which are expressly incorporated herein by reference: U.S. Non-provisional patent application Ser. No. 14/500,938, filed 29 Sep. 2014, now U.S. Pat. No. 9,456,236 (Attorney Docket No. CP00190-02); U.S. Non-provisional patent application Ser. No. 15/272,787, filed 22 Sep. 2016 (Attorney Docket No. CP00190-03); and U.S. Non-provisional patent application Ser. No. 15/272,810, filed 22 Sep. 2016 (Attorney Docket No. CP00190-04).

BACKGROUND

[0003] Technical Field

[0004] Aspects of the embodiments relate generally to video distribution networks. More particularly, aspects of the embodiments relate to systems and methods for distributing video protected by a digital rights management scheme following switching events between different digital video sources.

[0005] Background Art

[0006] Video distribution networks are increasingly common installations in commercial and residential facilities. Components of a video distribution network are typically located throughout the facility and networked allowing video to be distributed from one or more video source to one or more video sinks. For example, a typical video distribution network in a home may comprise a multitude of video sources, such as Blu-Ray Disc Players, media servers, digital video disc (DVD) players, Digital Video Recorders (DVR), and cable boxes. These video sources may be centrally located such as in an equipment rack in a closet and distributed via a chain of switches and repeaters to various video sinks, such as television displays, computer monitors and projectors, throughout the home.

[0007] However, as the digital distribution of television, movies, and music expands, content providers are growing increasingly concerned about the simplicity with which content pirates can copy and share copyrighted material. Various digital rights management (DRM) schemes have been developed to ensure that television shows, movies and music can only be viewed or heard by authorized parties (i.e. paying customers). One DRM scheme to protect digital content as it is transmitted over cables between devices is known as High-Bandwidth Digital Content Protection (HDCP). HDCP is a specified method developed by Digital Content Protection, L.L.C. (DCP) for protecting copyrighted digital content as it travels across connection interfaces and protocols such as DisplayPort (DP), Digital Video Interface (DVI), High-Definition Multimedia Interface (HDMI). The HDMI specification defines an interface for carrying digital audiovisual content from a source such as a Blu-Ray Disc player, to a sink or display device such as a television (TV).

[0008] There are three facets to HDCP. First, there is the authentication protocol, through which a source verifies that a given sink is licensed to receive HDCP content. With the legitimacy of the sink determined, encrypted HDCP content may be transmitted between the two devices, based on shared secrets established during the authentication protocol. The use of such shared secrets prevents eavesdropping devices from utilizing the content. Finally, in the event that legitimate devices are compromised to permit unauthorized use of HDCP content, renewability allows a source to identify such compromised devices and prevent the transmission of HDCP content.

[0009] The HDCP authentication protocol is an exchange between an HDCP compliant source and an HDCP compliant sink that affirms to the source that the sink is authorized to receive HDCP content by demonstrating knowledge of a set of secret device keys by transmitting a key selection vector (KSV). Each HDCP device is provided with a unique set of these secret device keys, referred to as the Device Private Keys, from DCP. The communication exchange also provides for both the HDCP compliant source and sink to generate a shared secret value that cannot be determined by eavesdropping on that exchange. By having that shared secret information embedded into the demonstration of authorization, the shared secret can then be used as a symmetric key to encrypt HDCP content intended only for the authorized device. Thus, a communication path is established between the HDCP source and HDCP sink that only authorized devices can access.

[0010] In order for an HDCP compliant source to successfully transmit protected content to one or more HDCP compliant sinks through an HDCP compliant repeater, a more involved authentication process must first occur. To affirm the downstream sinks to the upstream sources, the HDCP repeater must pass along the KSVs of each downstream receiver to the upstream source. The HDCP source checks these KSVs against an HDCP Revocation List maintained by DCP, LLC ("HDCP blacklist") in order to determine if each of the downstream sinks are licensed to receive the protected content. If all the downstream sinks are determined to be licensed to receive the protected content, the upstream source transmits the protected content to the HDCP repeater. It is the responsibility of the HDCP repeater to then establish and periodically manage authenticated links with each of its connected HDCP receivers.

[0011] While HDCP offers the benefit of encrypted content transmission, the required authentication protocol increases the switching delay in video distribution networks. Each time a new path for video distribution is desired, the links forming those paths must be authenticated. For example, when a user desires to switch to a different video source, not only must the new video source authenticate with the repeater, but the repeater must also re-authenticate with the video sink. Increased switching times are disrupting and bothersome to users. In complex video distribution systems with multiple layers, this problem is even more amplified. Additionally, because HDCP scheme operates under the

surface, most users do not realize that the increased time is the result of copy protection schemes and often unfairly attribute them to the individual components in the video distribution network.

[0012] An additional factor in the high switching delay in video distribution units, is caused by the need for processing in video distribution networks. Scalers are employed to change the resolution or refresh rate of distributed video and are common components in video distribution networks, either as separate components or integrated into other components in the network. Each time a video scaler receives audiovisual data at a new resolution, there is a delay before the scaler outputs any new video. The video scaler must load data and format before outputting scaled video. This is known as achieving video lock. During a switching event, each scaler in the distribution path must achieve video lock in succession. In complex video distribution systems with multiple layers, this delay is amplified.

[0013] Additionally, dependent on the characteristics of the display, viewers may be subjected to disrupting video artifacts or snow during switches. Manufacturers handle disrupted video in different ways. Some displays may show "snow" when video is disrupted. Other may display pixilated images or ghost images. Many viewers find these display responses disturbing and lead some to believe that there is a problem with their equipment when no such problem exists. Users may experience the authentication process as a delayed period with snow or disorienting video artifacts.

[0014] There are certain problems, therefore, with the conventional systems, solutions, devices described above for viewing video when switching occurs. Accordingly, it would be desirable to provide methods, modes, and systems for distributing video protected by a digital rights management scheme following switching events between different digital video sources.

SUMMARY

[0015] It is to be understood that both the general and detailed descriptions that follow are exemplary and explanatory only and are not restrictive of the aspects of the embodiments.

[0016] Principles of the aspects of the embodiments provide a device and method for reducing the switching time of a video distribution network by maintaining an authenticated security protocol link on a downstream connection of a switcher device. For example, according to an aspect of the embodiments, a switcher device comprises at least two input boards, a multiplexer and an output board. Each of the at least two input boards are adapted to receive audiovisual data from a video source over a security protocol link. The multiplexer can be communicatively coupled between the at least two input boards and a transmitter board and adapted to dynamically route audiovisual data from the at least input boards to the transmitter board. The output board can be adapted to transmit audiovisual data to a video sink over a security protocol link and maintain the security protocol link as authentic.

[0017] According to a second aspect of the embodiments, a switcher device comprises at least two input boards, a multiplexer board and an output board. Each of the at least two input boards can be adapted to receive audiovisual data from a video source over an HDCP link. The multiplexer board comprises a multiplexer communicatively coupled between the at least two input boards and an output board and adapted to dynamically route audiovisual data from the at least two input boards to the output board and a processing unit in communication with the multiplexer and the output board and configured for transmitting a switch signal to the multiplexer and a prepare signal to the transmitter board prior to a switching event. The output board can be adapted to transmit audiovisual data to a video sink over and HDCP link, and comprises a receiver adapted to receive audiovisual data routed from the multiplexer, a scaler adapted to convert audiovisual data received via the multiplexer to video to a native resolution of the video sink, generate video timing data at the native resolution of the video sink during the switching event and generate image content data for a period of time until achieving video lock in response to receiving the prepare signal, and a transmitter adapted to encrypt and transmit generated audiovisual data to the video sink over an HDCP interface and maintain an authenticated interface with the video sink by outputting continuous audiovisual data during the switching event.

[0018] According to a second aspect of the embodiments, an output board for a switcher device can be adapted to transmit audiovisual data to a video sink over a security protocol link. The output board comprises a receiver, a scaler and a transmitter. The receiver can be adapted to receive audiovisual data. The scaler can be adapted to convert the audiovisual data to a native resolution of the video sink and adapted to generate audiovisual data during a switching event. The transmitter can be adapted to encrypt and transmit encrypting and transmitting the output of the scaler, and is further adapted to maintain an authenticated interface with the video sink.

[0019] According to further aspects of the embodiments, a method for reducing switching delay when switching sources in a video distribution network comprises receiving audiovisual data at a first input board from a first video sink over a security protocol link, routing audiovisual data from the first input board to an output board, transmitting audiovisual data from the output board to a video sink over a security protocol link, receiving a user control signal to switch to a second video source, generating video timing data at the output board during a delay between receiving audiovisual data from the first input board and receiving audiovisual data from the second input board to maintain authenticity of security protocol link between the output board and the video sink, receiving audiovisual data at a second input board from a second video sink over a security protocol link, routing audiovisual data from the second input board to the output board; and transmitting audiovisual data from the output board to the video sink over a security protocol link.

[0020] According to still further aspects of the embodiments, a computer program product for reducing the switching time in a video distribution network is provided, the computer program product comprising a computer readable storage medium having computer readable code embodied therewith. The computer readable program code comprises computer readable program code adapted to detect a user control signal to switch from a first video source to a second video source, transmit a prepare signal to a processing unit of an output board in response to the detection of the user control signal, detect the prepare signal, instruct a scaler to generate audiovisual data in response to the detection of the prepare signal, cease routing audiovisual data from a first

video source to the output board, continue generating video timing data at the scaler of the output board, begin routing audiovisual data from a second video source to the input board, cease generating image content data upon achieving video lock.

[0021] Aspects of the embodiments are directed to overcome or at least ameliorate one or more of several problems, including but not limited to: reducing the switching delay of a video distribution network transmitting protected video.

BRIEF DESCRIPTION OF DRAWINGS

[0022] The accompanying figures further illustrate aspects of the embodiments.

[0023] The components in the drawings are not necessarily drawn to scale, emphasis instead being placed upon clearly illustrating principles of aspects of the embodiments. In the drawings, like reference numerals designate corresponding parts throughout the several views.

[0024] FIG. **1** is a block diagram of a High-Bandwidth Digital Content Protection (HDCP) system according to aspects of the embodiments.

[0025] FIG. **2** is a block diagram of an HDCP system wherein two or more HDCP devices are interconnected through at least one HDCP-protected Interface according to aspects of the embodiments.

[0026] FIG. **3** is a block diagram of a switcher device according to aspects of the embodiments.

[0027] FIG. **4** is a block diagram of the switcher device shown in FIG. **3**, according to aspects of the embodiments.

[0028] FIG. **5** shows a video distribution network, according to aspects of the embodiments.

[0029] FIG. **6** is a block diagram of the output board shown in FIG. **5**, according to aspects of the embodiments.

[0030] FIG. **7** is a flowchart of a method for reducing the switching time in a video distribution network, according to aspects of the embodiments.

DETAILED DESCRIPTION

[0031] List of Reference Numbers for the Major Elements in the Drawing

[0032] The following is a list of the major elements in the drawings in numerical order.

[0033] **100** High Bandwidth Digital Content Protection System

[0034] **102** Interface Cable or Link

[0035] **104** Audio/Video Source

[0036] **106** Audio Video Sink

[0037] **108** Secret Device Keys

[0038] **200** High Bandwidth Digital Content Protection System

[0039] **202** HDCP Content (Audiovisual Data)

[0040] **210** Control Function

[0041] **212**, **215** HDCP Transmitter

[0042] **214**, **216** HDCP Receiver

[0043] **219** Repeater

[0044] **220** Central Processing Unit

[0045] **300** Video Distribution Network

[0046] **302** Switcher Device

[0047] **304** Control Signal

[0048] **306** Multiplexer

[0049] **308** Input board

[0050] **310** Output board

[0051] **316** User Control Signal

[0052] **318** Switcher Processing Unit

[0053] **320** Transceiver

[0054] **322** Control System

[0055] **323** User Interface Device (e.g., Wireless/Mobile Device)

[0056] **324** User Interface Device

[0057] **401** Receiver

[0058] **402** Output Scaler

[0059] **403** Output Processing Unit

[0060] **502** Interface Cable (Link)

[0061] **508** Extended Reception Board

[0062] **510** Extended Transmission Board

[0063] **601** Receiver

[0064] **615** HDCP Transmitter

[0065] **700** Method for Reducing Switching Time in a Video Distribution Network

[0066] **701-714** Steps of Method **700**

LIST OF ACRONYMS USED IN THE SPECIFICATION

[0067] The following is a list of the acronyms used in the specification in alphabetical order.

[0068] AV Audiovisual

[0069] CAT5e Category 5 Enhanced

[0070] DC Direct Current

[0071] DCP Digital Content Protection, LLC

[0072] DDC Display Data Channel

[0073] DM DigitalMedia

[0074] DRM Digital Rights Management

[0075] DVD Digital Video Disc

[0076] DVR Digital Video Recorder

[0077] EDID Extended Display Data Channel

[0078] HDCP High-Definition

[0079] HDMI High-Definition Multimedia Interface

[0080] PCB Printed Circuit Board

[0081] STP Shielded Twisted Pair

[0082] TMDS Transition Minimized Differential Signaling

[0083] UTP Unshielded Twisted Pair

[0084] Authorized device—An HDCP device that is permitted access to HDCP content. An HDCP transmitter may test if an attached HDCP receiver is an authorized device by successfully completing the first and, when applicable, second part of the authentication protocol. If the authentication protocol successfully results in establishing authentication, then the other device is considered by the HDCP transmitter to be an authorized device.

[0085] Downstream—Term used as an adjective to refer to being towards the sink/display of the HDCP content stream.

[0086] DVI—Short for Digital Video (or Visual) Interface, a digital interface standard created by the Digital Display Working Group (DDWG) to accommodate both analog and digital monitors.

[0087] HDCP—short for High-Bandwidth Digital Content Protection, a specified method developed by Digital Content Protection, L.L.C. (DCP) for protecting copyrighted digital content as it travels across connection interfaces and protocols such as DisplayPort (DP), Digital Video Interface (DVI), High-Definition Multimedia Interface (HDMI).

[0088] HDCP content—consists of audiovisual content that is protected by the HDCP system. HDCP content includes the audiovisual content in encrypted form as it is transferred from an HDCP transmitter to an HDCP receiver over an HDCP-protected Interface.

[0089] HDCP device—Any device that contains one or more HDCP-protected interface ports and is designed in adherence to HDCP.

[0090] HDCP Encryption—The encryption technology of HDCP when applied to the protection of HDCP content in an HDCP system.

[0091] HDCP-protected Interface—An interface for which HDCP applies.

[0092] HDCP-protected Interface Port—A connection point on an HDCP Device that supports an HDCP-protected Interface.

[0093] HDCP receiver—An HDCP device that can receive and decrypt HDCP content through one or more of its HDCP-protected interface ports.

[0094] HDCP repeater—An HDCP device that can receive and decrypt HDCP content through one or more of its HDCP-protected interface ports, and can also re-encrypt and emit the HDCP content through one or more of its HDCP-protected interface ports. An HDCP repeater may also be referred to as either an HDCP receiver or an HDCP transmitter when referring to either the upstream side or the downstream side, respectively.

[0095] HDCP transmitter—An HDCP device that can encrypt and emit HDCP content through one or more of its HDCP-protected interface ports.

[0096] HDMI—Short for High-Definition Multimedia Interface, an industry-supported, uncompressed, all-digital audio/video interface.

[0097] Upstream—Term used as an adjective to refer to being towards the source of the HDCP content stream. The antonym of "downstream," defined above.

[0098] FIGS. **1** and **2** illustrate examples of High-Bandwidth Digital Content Protection (HDCP) systems **100**, **200** according to aspects of the embodiments. Referring to FIG. **1**, HDCP system **100** encrypts the digital content transmission between video source **104** (set-top box, computer, DVD, among other type of devices) and sink or display **106** (Liquid Crystal Display, television, among other types of devices) via interface **102** such as a Digital Video Interface (DVI), a High-Definition Multimedia Interface (HDMI), and a DisplayPort interface.

[0099] FIG. **2** illustrates an HDCP system **200** wherein two or more HDCP devices **104**, **106** are interconnected through an HDCP repeater and two HDCP-protected Interfaces **102***a*, **102***b* (collectively **102**), according to aspects of the embodiments. Each point-to-point HDCP link involves one HDCP transmitter **212**, and one HDCP receiver **214**. As such, the HDCP repeater **219** can decrypt the HDCP content at the HDCP receiver **216** on each of its inputs. The repeater **219** can then re-encrypt the data with an HDCP transmitter **215** on each of its outputs. The repeater **219** can inform the upstream device of its downstream connection, but generally repeater **219** maintains those connections. The audiovisual content protected by HDCP, HDCP content **202**, flows from an upstream content control function **210** into HDCP system **200** at the most upstream transmitter **212**. From there, HDCP content **202**, encrypted by HDCP system **200**, flows through a tree-shaped topology of HDCP receivers **214** over HDCP-protected Interfaces **102**. Before sending data, each transmitter **212**, **215** checks that the HDCP receivers **214**, **216** are authorized to receive HDCP content **202**. If so, transmitter **212** encrypts HDCP content **202** to prevent eavesdropping as it flows to receiver **216**. Central processing unit **220** includes firmware to process HDCP content **202** and other information and control.

[0100] Device manufacturers typically buy HDCP chips from a DCP-licensed silicon vendor. These chips usually also provides transition minimized differential signaling (TMDS) encoders or decoders and other HDMI-specific features. Transmitters **212** can have at least one HDCP transmitter chip and receivers **216** can have at least one HDCP receiver chip. HDCP transmitters **212**, and receivers **216** frequently require a microprocessor to implement the authentication state machines. Transmitters **212**, **215** can be HDMI transmitters.

[0101] The Authentication and Encryption Protocols

[0102] HDCP authentication consists of three parts:

[0103] Part One: source **104** authenticates with sink/display **106** connected to its output. If successful, encryption is enabled and audiovisual (NV) content transmission begins.

[0104] Part Two: This part is used if the downstream device is repeater **219**. Repeater **219** authenticates with the devices connected to its output(s) and passes the HDCP tree topology information up to source **104**. Source **104** is the root and sinks/display **106** are the leaves, while repeaters **219** make up the branches of the tree.

[0105] Part Three: Source **104** performs periodic checks with sink/display **106** to ensure that encryption is in sync. As mentioned above, repeater **219** generally maintains its downstream connections. If any part of authentication fails or any revoked devices are found in the HDCP tree, transmitter **212** can stop sending protected content and authentication starts over at Part One.

[0106] Authentication Part One

[0107] Part One of authentication is a key exchange protocol. Transmitter **212** and receiver **216** calculate a common secret session key **108** to be used for encryption. If they cannot come up with the same key value, authentication fails and receiver **216** will not be able to decrypt the HDCP content **202**. The session key is derived from each device's private key according to the following protocol:

[0108] First transmitter **212** generates a random number "An" and sends it to receiver **216**. This value will be used later in the protocol. Devices **104**, **106** then exchange KSVs. Receiver **216** also sends its REPEATER bit, a flag that indicates whether or not it is part of a repeater. Now each device **104**, **106** has the other device's Key Selection Vector (KSV). Each device **104**, **106** uses the other device's Key Selection Vector to select twenty of its own keys. The forty bits in the KSV correspond to the indexes of each of the forty private keys. For every set bit in the received KSV, the local private key at that index is selected. All KSVs have twenty set bits, so twenty keys are selected. Devices **104**, **106** then each add up their selected keys to come up with the sums Km and Km', for the transmitter and receiver, respectively **212**, **216**. For authentication to succeed, Km and Km' must match. Each device **104**, **106** tells the other which of its own unique, secret keys to select, and they both come up with the same sum. That may seem counter-intuitive, but it is the aforementioned mathematical relationship between the keys and the KSVs that accounts for this behavior. Source **104** can then determine whether Km and Km' match. However, they are secret values, so they cannot be transmitted over interface cable **102** for the DDC. Each device **104**,**106** feeds Km (or Km'), the random number "An", and the REPEATER bit into their respective HDCP cipher engines in order for transmitter **212** to verify that the values match

without sending them across cable **213** for everyone to see. The resulting data stream is split into three values:

[0109] R0/R0': This return value can be shared between the devices **104**, **106** and is used to verify that authentication was successful.

[0110] Ks/Ks': This value is kept private and is used as the encryption session key for the HDCP cipher.

[0111] M0/M: This value is also kept private and is used in Part Two of authentication (if the downstream device is repeater **219**).

[0112] Receiver **219** sends R0' to transmitter **212**, which compares it against its' own R0 value. If they match, that proves that the sums Km and Km' matched, and authentication is successful. Furthermore, the session keys Ks and K match, so the receiver **214** will be able to decrypt the content encrypted by the transmitter. If Part One of authentication was successful, the transmitter **212** may begin sending encrypted HDCP content **202**. If the downstream device is repeater **219**, the repeater **219** must authenticate with its own downstream device according to the same protocol. Transmitter **212** then starts a 5-second timer to allow for repeater **219** to perform Part Two of authentication. If Part Two fails or times out, authentication fails and transmitter **212** must stop transmitting HDCP content **202**.

[0113] Authentication Part Two

[0114] Part Two of authentication only occurs if the downstream device is a repeater **219**. The purpose of Part Two is to inform source **104** of all downstream devices and the HDCP tree depth. Source **104** uses this information to ensure that the tree topology maximums have not been exceeded and to ensure that none of the downstream devices have been revoked by DCP. Repeater **219** first assembles a list of the KSVs of all downstream devices, as well as the device count and the tree depth. Repeater **219** then passes this information up to source **104**. To ensure that this information has not been tampered with during transmission, each device takes this list, appends its secret value M0/M0' from Part One, and calculates a SHA-1 hash of the whole thing. Transmitter **212** reads the hash result from receiver **214** and compares it against its own. If they match, Part Two of authentication is successful.

[0115] Authentication Part Three

[0116] All HDCP devices are considered authenticated after successful completion of Authentication Parts One and Two. Part Three is simply a link integrity check to ensure that encryption is in sync between all transmitter/receiver pairs **212**, **214**, **215**, **216** in the tree. To support link integrity checks, the return values Ri and Ri' roll over to a new value every 128 frames. Recall that the initial Ri values R0 and R0' were generated during Part One of authentication. Every two seconds, transmitter **212** compares receiver's **216** Ri' value against its own Ri value to see if they match. If they do not, encryption is out of sync and receiver **216** cannot correctly decrypt HDCP content **202**. The user will see a scrambled or "snowy" image on the screen. In this case transmitter **212** can then restart authentication from the beginning.

[0117] The three part authentication process increases switching delay when switching sources in a video distribution network. Switching delay is the delay between switching an aspect of incoming audiovisual data to a video sink, such as audiovisual data source, audiovisual data resolution and audiovisual data refresh rate, and the incoming audiovisual data being displayed on the video sink. Not only must devices authenticate the HDCP link before video transmission, each time an upstream HDCP link is switched, downstream HDCP links may be affected as well because audiovisual data transmission to downstream links is interrupted. Each time video transmission is interrupted between an HDCP transmitter and an HDCP receiver, the HDCP link fails Part Three of the authentication process and the authentication process must be restarted from Part One. This includes downstream connections that were previously authenticated with each other.

[0118] For example, in a video distribution network comprising a first HDCP-compliant video source and a second HDCP compliant video source connected to an HDCP compliant video sink via an HDCP compliant video switcher, when the video source transmitting HDCP content to the video sink is switched from the first video source to the second video source, not only must the second video source authenticate with the video switcher, but the downstream link between the video source and the video switcher must also be re-authenticated due to the disruption in video transmission. This despite the fact that the HDCP link between the video source and the video switcher was already authenticated. This issue becomes increasingly burdensome in expansive video distribution networks with many layers (i.e. a large tree topology).

[0119] Additionally, when video transmission is interrupted between an HDCP transmitter and an HDCP receiver due to upstream switching and HDCP authentication, any downstream video scalers must lock back on the incoming audiovisual data before outputting any scaled audiovisual data. This introduces delay in addition to the delay introduced by the HDCP authentication process. For example, each time video transmission to a sink is interrupted, video scaler internal to the sink will take anywhere between two and ten seconds to lock onto the incoming audiovisual data again. Those skilled in the art will recognize that scaler operation is unpredictable and varies due to hardware and firmware specification. Often, video scalers included in video sinks are not optimized for reducing switching delay. Also unpredictable is video sink response while embedded video scalers achieve video lock. Presented with interrupted video, the video sink may display snow, pixilated images, video artifacts or a blank screen while internal scaler achieves video lock dependent on video sink manufacturer.

[0120] Because the HDCP authentication process operates in the background, often unknown to the user, long switching delays are unfairly blamed on video distribution components. Users may experience the authentication process as a delayed period with snow or disorienting video artifacts. This could result in undeserved user dissatisfaction with the manufacturer of the components in the video distribution network.

[0121] As will be explained below, aspects of the embodiments disclose systems, apparatuses and methods for reducing the switching time in a video distribution network. Aspects of the embodiments are directed towards maintaining authentication of downstream link during a switching discontinuity, minimizing the interruption of video transmission resulting from switching events. By outputting continuous video timing data to a sink over a downstream HDCP link, even during switching discontinuities, the downstream HDCP link satisfies the maintenance check in step three of HDCP authentication. Accordingly, steps one and two of the HDCP authentication protocol need not be repeated. Additionally, as a result of maintaining the authen-

tication of the HDCP link by outputting continuous video timing data during switching discontinuities, video scalers downstream of the HDCP link (i.e. internal video sink scalers) will not lose video lock with the incoming video stream thereby reducing delay times further. Finally, by outputting black frames of image data, the content displayed during switching events is controlled.

[0122] FIG. **3** is a block diagram of switcher device **302** adapted to reduce switching time in a video distribution network according to aspects of the embodiments. Video distribution network **300** is an HDCP system and includes at least one source **104***a*, **104***b*, . . . , **104***n* (collectively **104**) and at least one sink or display **106***a*, **106***b*, . . . , **106***n* (collectively **106**). At least two sources **104** include HDCP transmitter **212**, such as an HDMI transmitter, adapted to transmit audiovisual data comprising video timing data and image content data to at least one sink **106**. Each source **104** further includes a graphic generator (not shown) to generate a graphic or image. HDCP transmitter **212** receives HDCP content **202** from upstream content control function **210**.

[0123] At least one sink includes an HDCP receiver, such as an HDMI receiver. Source **104** determines via the authentication process what content can be viewed, recorded, and shared based on sinks/displays **106** that support HDCP and sinks/displays **106** that does not support HDCP. The output of source **104** is connected to input board **308** for switcher device **302** through their HDCP-protected interfaces **304** and switcher device **302** serves as an HDCP repeater for HDCP compliant content. Output board **310** for switcher device **302** is connected to the input of sink/display **106** via another interface **102***b*. Interfaces **102***a*, **102***b* for the input board and the output board of switcher device **302** may be an HDMI cable that carries a variety of signals such as one or more transition minimized differential signaling (TDMS) data signals, digital display channel (DDC), hot plug detect (HPD), and RxSense. As will be described later, interfaces **102***a*, **102***b* for the input board and output board of switcher device **302** may also be a combination of one or more shielded twisted pairs (STP) and one or more unshielded twisted pairs (UTP), such as DigitalMedia (DM) cable available from Crestron Electronics, Inc. of Rockleigh, N.J.

[0124] When HDCP source **104** (more specifically source **104***a*) detects an RxSense signal from HDCP compliant sink/display **106** (more specifically sink/display **106***a*), source **104***a* will transmit HDCP content **202** to sink/display **106***a* after the authentication process is successful.

[0125] HDCP content **202** is encoded into three data channels. These channels and a TMDS clock are carried over four differential pairs from source **104** to sink/display **106**. The DDC is a communications interface similar to I2C. This interface provides two-way communication in a master-slave relationship. Upstream device **104** is the DDC master and downstream device **106** is the DDC slave. HDCP receiver **214** indicates its presence to HDCP transmitter **212** with the HPD signal. HDCP transmitter **212** is the HDCP Device most upstream, and receives HDCP content **202** from upstream content control function **210**.

[0126] Switcher device **302**, functioning as an HDCP repeater, is a fully modular and expandable matrix switcher offering low-latency digital video and audio switching, and HD lossless multi-room signal distribution, for all types of A/V sources. Switcher device **302** may be a Crestron Digital Media Switcher available from Crestron Electronics, Inc. of Rockleigh, N.J.

[0127] The Crestron Digital Media Switcher is field-configurable to handle, but not limited to, eight, sixteen, and thirty-two audiovisual sources of virtually any type via input boards. The outputs are also field-configurable to provide, but not limited to, eight, sixteen, and thirty-two room outputs and/or HDMI outputs in a single chassis. The chassis comprises slots for the insertion of input and output boards. As will be described later, the input boards and output boards may be input boards and output boards, respectively, of the switcher device **302**. Additionally, the input boards and output boards may operate external of the chassis of the Digital Media Switcher and be coupled to the Digital Media Switcher via intermediate cards inserted into slots in the chassis.

[0128] Switcher device **302** includes multiplexer **306** coupled in-between the at least one input board **308***a*, **308***b*, **308***n* (collectively **308**) and at least one output board **310***a*, **310***b*, **310***n* (collectively **310**). Multiplexer **306** may be, but is not limited to, a mechanical switch, electrically operated switch, solid state relay, latching relay, reed relay, single pole single throw (SPST) relay, single pole double throw (SPDT) relay, double pole single throw (DPST) relay, and double pole double throw (DPDT) relay.

[0129] Multiplexer **306** transmits HDCP content **202** from one of the at least two input boards **308** to first output board **310***a*. Multiplexer **306** dynamically switches between first input board **308***a* and at least second input board **308***b* based on user control signal **316** that selects either first video source **104***a* or second video source **104***b* to be displayed on video sink **106***a*. Output board **310** can be coupled to the at least one sink/display **106** via interface cable **102***b*. Interface cable **102***b* can be an HDMI cable. Switcher **302** further includes processing unit **318** coupled to multiplexer **306**. Processing unit **318** includes at least one transceiver **320** for bidirectional communications with end user device (e.g. **324**, **326**), in part, to receive user control signal **316**. End user device **324**, **326** transmits user control signal **316** from touch panel display **324** via control system **322**. An end user may also transmit user control signal **316** from wireless device **326**. Software tools **328** can be loaded onto the wireless device and/or touch panel **324** to assist the end user in selecting desired source **104** and sink **106**. In response to the user selecting desired source **104** for sink **106**, the end user device transmits user control signal **316** to switcher device **302**.

[0130] Upon the user selecting the desired source **104** for the at least one desired display **106**, source **104** can authenticate with switcher device **302** as described above. Switcher device **302** can authenticate with the at least one desired downstream sinks **106** as described above. Once the authentication is complete, source **104** can transmit the HDCP content (i.e. HDCP protected audiovisual data) via the HDCP link between the source and the repeater. This HDCP link comprises HDCP transmitter **212** of the source, an HDCP interface, and HDCP receiver **214** of first input board **308***a*. The HDCP receiver of input board **308***a* receives the HDCP content and provides the audiovisual data unencrypted to multiplexer **306**. Multiplexer **306**, dependent on user control signal **316** routes the unencrypted audiovisual data to the desired output board **310**. Output board **310** processes and encrypts the audiovisual data and then transmits the HDCP content to the desired sink **106** over an HDCP link between output board **310** and video sink **106**. The HDCP link between output board **310** and video sink

106 comprises HDCP transmitter **215** of the output board, HDCP interface and HDCP receiver of the video sink.

[0131] Multiplexer **306** can be adapted to dynamically route the audiovisual data according to the user control signal received at processing unit **318**. For example, a user viewing content from first source **104***a*, such as a cable tuner, may desire to switch to second source **104***b*, such as a Blu-ray disc player. When multiplexer **306** switches from routing audiovisual data from the first source to routing audiovisual data from second source **104***b*, output board **310** experiences a switching delay as a result of the delay caused by upstream HDCP authentication and multiplexer **306** operation. A similar switching discontinuity may also result from a change in resolution or change in refresh rate of the received audiovisual data.

[0132] Output board **310** of switcher device **302** according to aspects of the embodiments can be adapted to continuously output audiovisual data including video timing data and image content data during switching discontinuities such that the HDCP link between output board **310** and video sink **106** remains authenticated during the switch and an aesthetically pleasing display is shown during said switch. For example, output board **310** can output black frames of audiovisual data during switching discontinuities. Switching delay in video distribution network **300** is minimized by maintaining the authentication of the HDCP link by continuously outputting video timing data. Additionally, by continuously outputting video timing data to the video sink during switching discontinuities, video lock is maintained in video processing devices, such as scalers, downstream from output board **310** (i.e. scalers internal to video sink), thereby further minimizing switching delay.

[0133] FIG. **4** is a block diagram of a portion of switcher device **302** shown in FIG. **3** according to aspects of the embodiments. Output board **310***a* further comprises receiver **401**, output scaler **402**, output processing unit **403** and HDCP transmitter **215**. Receiver **401** can be adapted to receive audiovisual data routed from first input board **308***a* or second input board **308***b* via multiplexer **306**. As described below, according to aspects of the embodiments, receiver **401** can be an HDCP receiver adapted to receive HDCP encrypted content.

[0134] Output scaler **402** receives the audiovisual data from receiver **401** and can be adapted to convert the received audiovisual data to a native resolution of video sink **106**. Output board **310** can receive the native resolution of video sink **106** via an EDID channel. Those skilled in the art will recognize that the operation of video scalers embedded in end user devices are idiosyncratic depending on manufacturer and may perform substantially below par, resulting in poor video quality and delayed performance. Advantageously, by converting to the native resolution of video sink **106**, video processing is minimized in downstream embedded video scalers.

[0135] According to aspects of the embodiments, output scaler **402** of output board **310** can be adapted to operate in a pass through mode in which the output scaler detects the resolution of the incoming audiovisual data via the video timing data. The output scaler passes the incoming audiovisual data through to the HDCP transmitter if the audiovisual data is routed to the output board already at a native resolution of the video sink.

[0136] Output scaler **402** can be further adapted to generate audiovisual data comprising video timing data and image content data during switching discontinuities. For example, during a switching discontinuity between receiving audiovisual data from first source **104***a* and audiovisual data from second source **104***b*, output scaler **402** can output black frames. By outputting a continuous stream of audiovisual data, more specifically video timing data, to HDCP transmitter **215**, the HDCP link between output board **310** and the source is maintained as authenticated during the switch. In addition, by outputting black frames of audiovisual data, more specifically image content data, the end user experiences a clean transition from first source **104***a* to second source **104***b*. In other aspects of the embodiments, output scaler **402** can generate frames of image content data of a color other than black or may generate image content data comprising an image, such as a corporate logo.

[0137] Prior to outputting audiovisual data from second source **104***b*, output scaler **402** can wait until it receives a sufficient amount of audiovisual data from second source **104***b*. This is known as achieving video lock. Following a switching discontinuity, output scaler **402** is further configured to generate image content data until video lock is achieved. By generating image content data until output scaler **402** achieves video lock, the user is presented with a clean transition during switching events.

[0138] Output scaler **402** can be adapted to operate in a free run mode by automatically generating video timing data during switching discontinuities.

[0139] Output scaler **402** can be further adapted to generate image content data in response to control signals from output processing unit **403**. Upon receiving the user control signal to switch the source of audiovisual data and prior to transmitting a switching signal to multiplexer **306**, switcher processing unit **318** transmits a prepare signal to output processing unit **403**. Output processing unit **403** in turn instructs output scaler **402** to generate black frames of audiovisual data.

[0140] HDCP transmitter **215**, such as an HDMI transmitter, converts and encodes the audiovisual data output from output scaler **402** to one or more TDMS signals for transmission to video sink **106** over the HDCP interface. According to aspects of the embodiments, the HDMI transmitter comprises an HDCP transmitter chip and can further comprise TMDS encoders or decoders and other HDMI-specific features. The audiovisual data is re-encrypted in accordance with the shared secret from authentication between the HCDP repeater and the HDCP sink. HDCP transmitter **215** receives the native resolution and the native refresh of the sink via a Display Data Channel (DDC) of the interface. The HDCP interface between transmitter and the HDCP receiver may be HDMI.

[0141] FIG. **5** shows switcher device **302** in a video distribution network **300**, according to further aspects of the embodiments in which output board **310** is contained in a housing external to switcher device **302**. Video distribution network **300** comprises extended transmission board **510** coupled between the multiplexer **306** and output board **310**. Video distribution network **300** further comprises extended reception board **508**. According to aspects of the embodiments, the extended reception board **508** and extended transmission board **510** can be modular input and output boards, respectively, configured to be inserted into switcher device **302**. As described below, the extended transmission and reception boards allow for extended cable lengths that increases the functionality of video distribution network

300. For example, output board 310 can be collocated in the same area as its corresponding video sink 106. Switcher device 302 can be remotely located in a central location or out of view, such as in an equipment closet. Similarly, first input board 308*a* and second input board 308*b* may be collocated with first video source 104*a* and second video source 104*b*, respectively.

[0142] According to aspects of the embodiments, output board 310 can be adapted to receive encrypted audiovisual data via an HDCP link. Extended transmission board 510 is communicatively coupled between multiplexer 306 and output board 310, and is further adapted to encrypt the audiovisual data routed by multiplexer 306, and transmitting the encrypted audiovisual data to the output board 310 via an HDCP link. The HDCP link comprises HDCP transmitter 615 of extended transmission board 510, HDCP interface 502, and HDCP receiver 401 of output board 310. HDCP interface 502 can be made of one or more pairs of twisted cable or fiber optical cable, such as DigitalMedia cable available from Crestron Electronics, Inc. of Rockleigh N.J. Those skilled in the art will recognize that DigitalMedia cable is a multi-generational family of interface cables particularly designed for media transmission for extended lengths.

[0143] Within a single plenum-rated jacket, original DigitalMedia cable contains one high-bandwidth/low-crosstalk shielded 4-twisted pair (STP) cable, one CAT5e unshielded 4-twisted pair (UTP) cable, and one DMNet cable. The STP "Audiovisual data" cable is of a specialized construction designed to allow the longest possible cable lengths for transporting high-definition digital video and audio. The Cat5e "Data Management" cable carries high-speed Ethernet and other data, plus 5V direct current (DC) power. Finally, the DMNet cable carries additional proprietary control signals and 24V DC power. Original DigitalMedia cable is rated for up to 220 ft of audiovisual transmission.

[0144] FIG. 6 is a block diagram of the extended transmission board and the output board shown in FIG. 5, according to aspects of the embodiments. The block diagram of output board 310 in FIG. 5 is similar to the block diagram of output board 310 in FIG. 4, with the exception being that in FIG. 5, receiver 401 is an HDCP receiver adapted to receive HDCP content over HDCP interface 502. Extended transmission board 510 comprises receiver 601 and HDCP transmitter 615.

[0145] FIG. 7 is a flowchart illustrating method 700 for reducing the switching time in a video distribution network 300, according to aspects of the embodiments.

[0146] In step 701, switcher device 302 receives audiovisual data at first input board 308*a* via an HDCP link between first video sink 106*a* and first input board 308*a*.

[0147] In step 702, switcher device 302 routes audiovisual data from first input board 308*a* to output board 310*a*.

[0148] In step 704, output board 310 transmits audiovisual data to video sink 106 over a security protocol link. According to aspects of the embodiments, output board 310 scales the audiovisual data received from first input board 308*a* to the native resolution of video sink 106 (step 703) prior to transmitting to video sink 106.

[0149] In step 705, processing unit 318 of switcher device 302 receives a control signal to switch from routing audiovisual data from first input board 308*a* to routing audiovisual data from second input board 308*b*.

[0150] According to aspects of the embodiments, switching device processing unit 318 transmits a prepare signal to output board 310*a*, indicating that there will be a switching discontinuity (step 706).

[0151] According to aspects of the embodiments, output board 310*a* is adapted to generate image content data, such as black frames of video, in response to receiving the prepare signal from the switching device processing unit 318 (step 707). Scaler 402 outputs the generated image content data rather than the live image content data being routed to output board 310*a* from multiplexer 306.

[0152] In step 708, multiplexer 306 ceases routing audiovisual data from first input board 308*a*.

[0153] In step 709, output board 310 continues generating video timing data at a native resolution during the delay between receiving audiovisual data from first input board 308*a* and receiving audiovisual data from second input board 308*b*. By outputting a substantially continuous stream of video timing data, output board 310*a* maintains the authenticity of the security link between output board 310*a* and video sink 106.

[0154] In step 710, switcher device 302 receives audiovisual data at second input board 308*b* via an HDCP link between second video sink 106*b* and second input board 308*b*.

[0155] In step 711, switcher device 302 routes audiovisual data from second input board 308*b* to output board 310*a*.

[0156] In step 712, output board 310*a* continues generating and outputting image content data (i.e. black frames of video) until video lock is achieved.

[0157] In step 714, output board 310*a* transmits live image content data routed from second input board 308*a* to video sink 106 over an HDCP link. According to aspects of the embodiments, output board 310*a* scales the audiovisual data received from first input board 308*a* to the native resolution of video sink 106 (step 713) prior to transmitting the received audiovisual data to video sink 106.

[0158] The following is a pseudo-code representation of the operation in accordance with aspects of the embodiments.

[0159] (a) Detect a user control signal to switch from a first video source to a second video source;

[0160] (b) Transmit a prepare signal to a processing unit of an output board in response to the detection of the user control signal;

[0161] (c) Detect the prepare signal at the output board;

[0162] (d) Instruct scaler to generate image content data;

[0163] (e) Cease routing audiovisual data from a first video source to the output board;

[0164] (f) Continue generating video timing data at the scaler of the output board;

[0165] (g) Begin routing audiovisual data from a second video source to the input board; and

[0166] (h) Cease generating image content data upon achieving video lock.

[0167] Any process descriptions or blocks in flow charts should be understood as representing modules, segments or portions of code that include one or more executable instructions for implementing specific logic functions or steps in the process. Alternate implementations can be included within the scope of the aspects of the embodiments in which functions may be executed out of order from that shown or discussed, including substantial concurrence or reverse order, depending on the functionality involved, as would be

understood by those reasonably skilled in the aspects of the embodiments. Also, steps disclosed as separate can be performed concurrently or combined, and a step shown as discrete can be performed as two or more steps. Furthermore, numerical values and disclosures of specific hardware are illustrative rather than limiting. Moreover, while aspects of the embodiments have been disclosed in the context of HDMI, aspects of the embodiments can be implemented for use with another suitable interface that uses HDCP, such as DVI or any substantially HDMI-like interface. Therefore, aspects of the embodiments should be construed as limited by only the appended claims.

[0168] In this description, various functions and operations can be described as being performed by or caused by software code to simplify description. However, those skilled in the art will recognize what is meant by such expressions is that the functions result from execution of the code by a processor or processing unit, such as a microprocessor. Alternatively, or in combination, the functions and operations can be implemented using special purpose circuitry, with or without software instructions, such as using an application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA). Embodiments can be implemented using hardwired circuitry without software instructions, or in combination with software instructions. Thus, the techniques are limited neither to any specific combination of hardware circuitry and software, nor to any particular source for the instructions executed by the data processing system.

[0169] While some embodiments can be implemented in fully functioning computers and computer systems, various embodiments are capable of being distributed as a computing product in a variety of forms and are capable of being applied regardless of the particular type of machine of computer-readable media used to actually effect the distribution.

[0170] At least some aspects disclosed can be embodied, at least in part, in software. That is, the techniques may be carried out in a computer system or other data processing system in response to its processor/processing unit, such as a microprocessor, executing sequences of instructions contained in a memory, such as ROM, volatile RAM, non-volatile memory, cache or a remote storage device.

[0171] Routines executed to implement the embodiments can be implemented as part of an operating system, middleware, service delivery platform, SDK (software development kit) component, web services, or other specific application, component, program, object, module or sequence of instructions referred to as "computer programs". Invocation interfaces to these routines can be exposed to a software development community as an API (application programming interface). The computer programs typically comprise one or more instructions set at various times in various memory and storage devices in a computer, and that, when read and executed by one or more processors/processing units in a computer, cause the computer to perform operations necessary to execute elements involving the various aspects.

[0172] A machine readable medium can be used to store software and data which when executed by a data processing system causes the system to perform various methods. The executable software and data can be stored in various places, including for example ROM, volatile RAM, non-volatile memory and/or cache. Portions of this software and/or data can be stored in any of these storage devices. Further, the data and instructions can be obtained from centralized servers or peer to peer networks. Different portions of the data and instructions can be obtained from different centralized servers and/or peer-to-peer networks. Different portions of the data and instructions can be obtained from different communication sessions or in a same communication session. The data and instructions can be obtained in their entirety prior to the execution of the applications. Alternatively, portions of the data and instructions can be obtained dynamically, just in time, when needed for execution. Thus, it is not required that the data and instructions be on a machine readable medium in entirety at a particular instance of time.

[0173] Examples of computer-readable media include, but are not limited to, recordable and non-recordable type media, such as volatile and non-volatile memory devices, read-only memory (ROM), random access memory (RAM), flash memory devices, floppy and other removable disks, magnetic disk storage media, optical storage media (e.g. Compact Disc Read-Only Memory (CD ROM), Digital Versatile Discs (DVDs), etc.) among others. The instructions may be embodied in digital and analog communication links for electrical, optical, acoustical or other forms of propagated signals, such as carrier waves, infrared signals, digital signals, etc.

[0174] In general, a machine readable medium includes any mechanism that provides (i.e. stores and/or transmits) information in a form accessible by a machine (e.g. a computer, network device, personal digital assistant, manufacturing tool, any device with a set of one or more processors, etc.).

[0175] In various embodiments, hardwired circuitry may be used in combination with software instructions to implement the techniques. Thus, the techniques are neither limited to any specific combination or hardware circuitry and software nor to any particular source for the instructions executed by the data processing system.

[0176] Although some of the drawings illustrate a number of operations in a particular order, operations which are not order dependent may be reordered and other operations can be combined or broken out. While some reordering or other groupings are specifically mentioned, others will be apparent to those of ordinary skill in the art and so do not present an exhaustive list of alternatives. Moreover, it should be recognized that the stages could be implemented in hardware, firmware, software or any combination thereof.

[0177] Although illustrative aspects of the embodiments have been described herein with reference to the accompanying drawings, it is to be understood that the aspects of the embodiments are not limited to those precise embodiments, and that various other changes and modifications may be made therein by one skilled in the art without departing from the scope of the appended claims.

INDUSTRIAL APPLICABILITY

[0178] To solve the aforementioned problems, aspects of the embodiments are directed towards a unique device in which output board **310** with scaler **402** minimizes switching delay in video distribution network **300** by outputting a substantially continuous stream of audiovisual data during switching events.

ALTERNATE EMBODIMENTS

[0179] Alternate embodiments can be devised without departing from the spirit or the aspects of the embodiments. For example, during switching events, output scaler **402** can generate video information such that a switching graphic will be displayed on the screen or a color other than black.

What is claimed is:

1. A digital video switcher device (switcher device) comprising:
- an output board;
- at least two input boards, each of the at least two input boards adapted to receive digital audiovisual data from a digital video source over a security protocol link; and
- a multiplexer communicatively coupled between the at least two input boards and the output board, and wherein the multiplexer is adapted to
  - dynamically route the digital audiovisual data from the at least two input boards to the output board,
- and wherein the output board is adapted to
  - generate a continuous stream of uninterrupted digital video timing data in the absence of digital video timing data received from either or both of the at least two input boards.

2. The switcher device according to claim **1**, wherein
- the output board is further adapted to
  - transmit the digital audiovisual data to a downstream video sink over a security protocol link, and
  - maintain the security protocol link in an authenticated interface with the downstream video sink during a switching event between the at least two input boards by outputting a continuous stream of uninterrupted digital video timing data during the switching event.

3. The switcher device according to claim **2**, wherein the output board comprises:
- a scaler adapted to generate the continuous stream of uninterrupted digital video timing data in the absence of digital video timing data received from either or both of the at least two input boards.

4. The switcher device according to claim **3**, wherein the output board comprises:
- a receiver adapted to receive the digital audiovisual data routed from the multiplexer;
- a scaler adapted to
  - convert the digital audiovisual data received via the multiplexer to a native resolution of the digital video sink,
  - generate a continuous stream of uninterrupted video timing data during the switching event at the native resolution of the video sink during the switching event, and
  - generate image content data for a period of time until achieving video lock in response to receiving the prepare signal; and
- a transmitter adapted to encrypt and transmit digital audiovisual data to the digital video sink over an HDCP interface and maintain the security protocol link in an authenticated interface with the video sink by outputting the continuous stream of uninterrupted video timing data during the switching event.

5. The switching device according to claim **4**, wherein
- the scaler is further adapted to operate in a free running mode by generating digital video timing data during the switching event.

6. The switcher device according to claim **3**, wherein
- the scaler is further adapted to generate the continuous stream of uninterrupted digital video timing data in the absence of digital video timing data received from either or both of the at least two input boards at a native resolution of the digital video sink.

7. The switcher device according to claim **2** wherein
- the scaler is further adapted to generate black frames of digital image content data during the switching event.

8. The switcher device according to claim **7** wherein
- the scaler is further adapted to continue to generate black frames of digital image content data until receiving a sufficient amount of digital image content data to generate a stable output of converted digital image content data.

9. The switcher device according to claim **2**, wherein the security protocol comprises:
- High-Bandwidth Digital Content Protection (HDCP).

10. The switcher device according to claim **2** wherein the switching event comprises:
- at least one of
  - a switch from receiving first digital video from a first digital video source to receiving second digital video from a second digital video source,
  - a switch from receiving digital video at a first resolution to receiving digital video at a second resolution, and
  - a switch from receiving digital video at a first refresh rate to receiving digital video at a second refresh rate.

11. The switcher device according to claim **1** further comprising:
- a processing unit in communication with the multiplexer and the output board and wherein the processing unit transmits a prepare signal to the output board a predetermined amount of time before transmitting a switch signal to the multiplexer.

12. An output board in a digital video switcher device for use in a digital video transmission system, the digital video switcher device transmitting digital audiovisual data to a digital video sink over a security protocol link, the output board comprising:
- a receiver adapted to receive the digital audiovisual data from at least two input boards;
- a scaler adapted to convert the received digital audiovisual data to a native resolution of the video sink and to generate switched digital audiovisual data during a switching event between the at least two input boards, the switched digital audiovisual data comprising a substantially continuous stream of uninterrupted digital video timing data, wherein the substantially continuous stream of uninterrupted digital video timing data is generated in the absence of digital video timing data received from each of the at least two input boards; and
- a transmitter adapted to encrypt and transmit the output of the scaler, and is further adapted to maintain the security protocol link in an authenticated interface with the digital video sink.

13. The output board according to claim **12**, wherein the switching event comprises:
- at least one of
  - a switch from receiving audiovisual data from a first source to receiving audiovisual data from a second source,

a switch from receiving audiovisual data at a first resolution to receiving audiovisual data at a second resolution, and

a switch from receiving audiovisual data at a first refresh rate to receiving audiovisual data at a second refresh rate.

14. The output board according to claim **12**, wherein

the scaler is adapted to generate image content data during the switching event.

15. The output board according to claim **14**, wherein

the scaler is adapted to generate image content data after a switching event until receiving a sufficient amount of digital audiovisual data to generate a stable output of converted digital audiovisual data.

16. The output board of claim **12** wherein,

the security protocol comprises High-Bandwidth Digital Content Protection (HDCP).

17. A method for reducing switching delay when switching sources in a digital video distribution network, the method comprising:

receiving digital audiovisual data at a first input board from a first digital video source;

receiving digital audiovisual data at a second input board from a second digital video source;

routing audiovisual data from the first input board to an output board;

transmitting the digital audiovisual data from the output board to a digital video sink;

receiving a user control signal to switch from the first digital video source to the second digital video source;

generating a substantially continuous stream of uninterrupted digital video timing data at the output board during a delay when switching between digital audiovisual data from the first input board and digital audiovisual data from the second input board, the switching comprising a switching event, wherein the generated substantially continuous stream of uninterrupted digital video timing data is generated in the absence of digital video timing data received from either or both of the first input board and the second input board during the switching event.

18. The method according to claim **17**, further comprising:

routing the digital audiovisual data from the second input board to the output board; and

transmitting the digital audiovisual data from the output board to the video sink.

19. The method according to claim **17** further comprising:

scaling the digital audiovisual data received from the first input board to a native resolution of the display; and

scaling the digital audiovisual data received from the second input board to the native resolution of the display.

20. The method according to claim **17** further comprising:

generating image content data during the switching event.

21. The method according to claim **21** further comprising:

continuing to generate digital audiovisual data at the output board until an amount of digital audiovisual data sufficient to produce stable scaled digital audiovisual data is received from the second input board.

22. The method according to claim **17** further comprising:

transmitting a prepare signal to the output board.

23. The method according to claim **17**, wherein the step of generating a continuous stream of uninterrupted video timing data comprises:

automatically generating video timing data in a free funning mode at the output board.

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