(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
28 July 2005 (28.07.2005)

PCT

(10) International Publication Number
WO 2005/069372 A1

(51) International Patent Classification[7]: H01L 27/108

(21) International Application Number:
PCT/US2003/040295

(22) International Filing Date:
18 December 2003 (18.12.2003)

(25) Filing Language: English

(26) Publication Language: English

(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [—/—]; New Orchard Road, Armonk, NJ 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **FURUKAWA, Toshiharu** [JP/US]; 9 Oakwood Lane, Essex Junction, VT 05452 (US). **HAKEY, Mark, C.** [US/US]; P.O. Box 13, Fairfax, VT 05454 (US). **HOLMES, Steven, J.** [US/US]; 103 Guilder Lane, #11, Guilderland, NY 12084 (US). **HORAK, David, V.** [US/US]; 47 Briar Lane, Essex Junction, VT 05452 (US). **KOBURGER, Charles, W., III** [US/US]; 40 Roweland Avenue, Delmar, NY 12054 (US). **NESBIT, Larry, A.** [US/US]; 458 Wildflower Circle, Williston, VT 05495 (US).

(74) Agent: **ANDERSON, Jay, H.**; International Business Machines Corporation, ZIP 482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

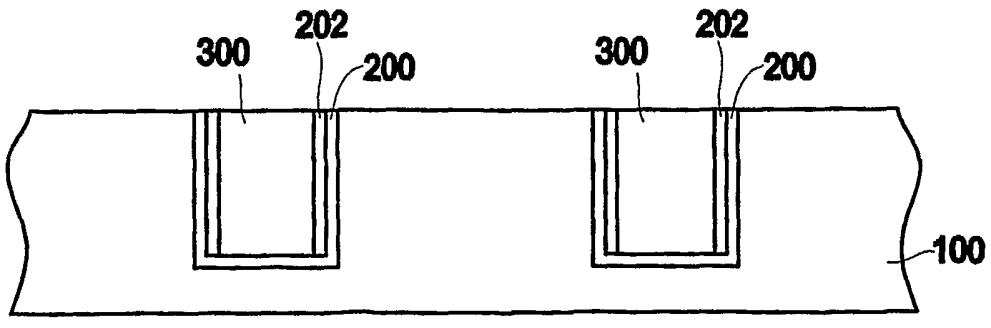
(84) Designated States *(regional)*: ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: CARBON NANOTUBE CONDUCTOR FOR TRENCH CAPACITORS



(57) Abstract: A trench-type storage device includes a trench in a substrate (100), with bundles of carbon nanotubes (202) lining the trench and a trench conductor (300) filling the trench. A trench dielectric (200) may be formed between the carbon nanotubes and the sidewall of the trench. The bundles of carbon nanotubes form an open cylinder structure lining the trench. The device is formed by providing a carbon nanotube catalyst structure on the substrate and patterning the trench in the substrate; the carbon nanotubes are then grown down into the trench to line the trench with the carbon nanotube bundles, after which the trench is filled with the trench conductor.

WO 2005/069372 A1

Carbon Nanotube Conductor for Trench Capacitors

Technical Field

The present invention generally relates to deep trench capacitors and more particularly to the use of a carbon nanotube film as a trench liner in deep trench capacitors.

Background Art

Most methods of fabricating DRAM trench storage nodes use silicon as a trench conductor material. As the trenches get deeper and achieve a higher aspect ratio, it requires more time to access the stored charge in the trench. It is difficult to use more conductive materials, such as aluminum, copper or platinum, in the trench due to the high thermal cycles that are required in the dynamic random access memory (DRAM) device fabrication.

Carbon nanotubes have recently attracted attention for use in very high-density integrated circuit devices. For example, U.S. Patent No. 6,515,325 describes a vertical transistor and capacitor cell using a single nanotube to form a device. U.S. Patent No. 6,566,704 describes a transistor including vertical nanotubes in which the source and drain are respectively formed at lower and upper parts of the nanotubes. These patents also describe processes for growing a nanotube on a substrate, where the nanotube is grown upwards from the substrate.

In order to employ carbon nanotubes in a trench-type capacitor memory device, it is necessary to form the nanotubes in a structure suitable for a storage node trench. This in turn requires that the nanotubes be grown down into the trench. The present invention addresses this problem.

Disclosure of Invention

The invention provides a trench-type storage device (capacitor) having conductive carbon nanotubes forming an open-ended cylinder structure lining the trench. A non-carbon based trench conductor (e.g., polysilicon, metals, alloys, etc.) fills the trench inside the open cylinder structure of carbon nanotube bundles. More specifically, in a process for making the invention, a carbon nanotube catalyst structure is formed on a substrate and at least one

trench is patterned in the substrate. Then, the process grows carbon nanotubes down into the trench to line the trench with carbon nanotubes bundles, after which the invention fills the trench with the trench conductor.

Prior to growing the carbon nanotubes, a porous cap may be formed over the carbon nanotube catalyst to further promote exposure of the catalyst to the carbon material. The process forms the carbon nanotubes catalyst structure by first forming a least one pad layer and then forming a carbon nanotube catalyst on the pad layer. After the trench is patterned, additional etching of the trench is performed to create an undercut beneath the carbon nanotube catalyst structure. Then, a portion of the pad layer is removed to expose the carbon nanotube catalyst. The process grows the carbon nanotubes from the top opening portion of the trench, down sidewalls of the trench, to the bottom closed portion of the trench. The carbon nanotubes form a consistent lining along approximately the entire length of sidewalls of the trench.

A trench dielectric can be positioned between the carbon nanotubes and sidewalls of the trench. The trench conductor comprises one or more of polysilicon, metal, an alloy, etc., and is carbon free. Further, in the final structure, the substrate is free of carbon nanotube catalyst materials because the catalyst is removed by the inventive process.

These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of Drawings

The invention will be better understood from the following detailed description with reference to the drawings, in which:

Figure 1 is a schematic diagram of a partially completed trench-type storage device;

Figure 2 is a schematic diagram of a partially completed trench-type storage device;

Figure 3 is a schematic diagram of a partially completed trench-type storage device; and

Figure 4 is a flow diagram illustrating a preferred method of the invention.

Best Mode for Carrying Out the Invention

The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

The present invention uses carbon nanotubes (CNT) to help form the conductive material in the trench. Most approaches to growing carbon nanotubes use a catalyst buried in the substrate and grow the carbon nanotubes up the trench from the bottom or middle. This approach does not work well for filling a deep trench because the trench becomes clogged with carbon nanotube material which blocks access of the source gas to the catalyst when the catalyst is placed at the bottom or sides of the trench. The present invention places the catalyst at the top of the trench, and allows the carbon nanotube to grow down into the trench, while fresh source gas is able to access the catalyst through a porous cap over the catalyst. The pores do not get clogged with carbon nanotubes because the tubes grow out from the catalyst surface rather than down into the catalyst.

The thicknesses and materials used in the following example explain one manner in which the invention is embodied. One ordinarily skilled in the art would understand that many different substances of many different thicknesses can be utilized in place of the materials and dimension mentioned below. Further, all measurements and chemical concentrations used herein are approximates. Therefore, as mentioned above, the following example should not be construed as limiting the scope of the invention. As shown in Figure 1, the invention starts with a pad structure on a substrate 100 that includes, for example, a 10

nm oxide layer (102), a 100 nm nitride layer (104) and 10 nm layer of Nickel, Iron, or Cobalt (or other suitable catalyst for carbon nanotube formation) 106. Item 108 represents a porous material, such as 200 nm of porous insulator (porous silicon oxide, such as formed from spun on glass (SOG) material with a component of volatile materials that escape during anneal). On top of the SOG, 500-800 nm of silicon oxide hard mask 110 is placed to mask the etch of the deep trench. On top of the oxide hard mask is placed 200 nm of silicon nitride hard mask 112, to provide a mask to etch the oxide 110.

The invention then applies an organic anti-reflective coating (ARC) and photoresist 114, and exposes the trench pattern into the photoresist 114. The invention performs the standard post exposure baking of the resist and developing of the resist pattern. Then, the invention etches the resist pattern into the nitride hard mask 112, and transfers the pattern through the rest of the pad stack and into the silicon substrate 100. After the trench is etched, the invention uses a brief isotropic silicon etch to perform additional trench widening and allow the pad structure to extend slightly over the trench, for example, about 10 nm per edge as shown by arrow 116. After the trench is widened, the trench dielectric 200 is formed according to methods known in the art; for example, deposition of silicon nitride of approximately 2 nm followed by thermal oxidation.

As shown in Figure 2, the process for making a preferred embodiment of the invention removes portions of the trench dielectric, the oxide layer 102 and the nitride layer 104 at the bottom of the pad structure, to expose the metallic catalyst 106 to the process ambient. This is done by isotropic etching (as indicated by arrows 204) of the trench dielectric, oxide 102 and nitride 104, while protecting the trench dielectric in the trench using a polymer fill. The polymer fill process is performed prior to the isotropic etch; an organic polymer is spun on the wafer to fill the trench, and the polymer is recessed by plasma etching to the top of the trench. After the isotropic etch, the polymer fill is ashed away using an oxygen plasma. If desired, the structure may then be annealed in Hydrogen, or Hydrogen/Carbon Monoxide to reduce the carbon nanotube catalyst 106 (the catalyst may become oxidized during trench dielectric formation, making this step unnecessary). This step would be necessary if the catalyst becomes oxidized, and the reduced metal is preferred as the catalyst. Iron and Nickel oxides can also act as carbon nanotube catalysts, so this reduction step may not be required.

The invention then introduces the carbon nanotube formation gas (such as carbon monoxide, acetylene, ethylene, or other suitable carbon sources) at elevated temperature (such as 500-900° C), to allow the carbon nanotube 202 to grow down into the trench from the catalyst at the bottom of the pad structure. As shown in Figure 3, the invention then fills the remaining portion of the trench with a trench conductor 300 (e.g., polysilicon, metal, alloy, etc.) as in a conventional fill process, and planarizes the structure.

A process for producing the structure of the present invention is shown in flowchart form in Figure 4. More specifically, the invention forms a carbon nanotube catalyst structure on a substrate and patterns at least one trench in the substrate. The invention forms the carbon nanotube catalyst structure by first forming a least one pad layer (step 402) and then forming a carbon nanotube catalyst on the pad layer (step 404). Prior to growing the carbon nanotubes, the invention can form a porous cap over the carbon nanotube catalyst (step 406). After the trench is patterned (step 408), the invention performs additional etching of the trench to create an undercut beneath the carbon nanotube catalyst structure (step 410). Next, the trench dielectric is formed on the trench sidewall (step 412).

A portion of the trench dielectric and a portion of the pad layer are then removed, to expose the carbon nanotube catalyst (step 414). Then, the invention grows carbon nanotubes down into the trench (step 416), after which the invention fills the trench with a conductor (step 418). The inventive process grows the carbon nanotubes from the top opening portion of the trench, down sidewalls of the trench, to the bottom closed portion of the trench. The carbon nanotubes form a consistent lining along approximately the entire length of sidewalls of the trench. The trench conductor comprises one or more of polysilicon, metal, an alloy, etc., and is carbon free. Lastly (step 420), the structure is planarized down to the top of the substrate 100. Thus, in the final structure, this area of the substrate is free of carbon nanotube catalyst materials.

As shown above, the present invention places the catalyst at the top of the trench, and allows the carbon nanotubes to grow down into the trench. This avoids the problems associated with conventional processes which cause the high aspect ratio trenches to be clogged with carbon nanotube material. Further, with the invention, fresh source gas is able to access the catalyst through a porous cap over the catalyst.

Industrial Applicability

The present invention is applicable to any type of electronic storage device that utilizes trench-type capacitors. In the particular example given above, the present invention has been described with reference to a dynamic random access memory (DRAM) capacitor structure.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

Claims

1. A trench-type storage device comprising:
a substrate (100);
at least one trench in said substrate;
conductive carbon nanotubes (202) lining said trench; and
a trench conductor (300) filling said trench.

2. The storage device in claim 1, further comprising a trench dielectric (200) between said carbon nanotubes and sidewalls of said trench.

3. The storage device in claim 1, characterized in that the conductive carbon nanotubes form an open cylinder structure lining said trench.

4. The storage device in claim 1, characterized in that the trench conductor comprises at least one of polysilicon, a metal, and an alloy thereof.

5. The storage device in claim 1, characterized in that the conductive carbon nanotubes and a separate trench conductor material are disposed in the trench, and the trench conductor material is carbon free.

6. The storage device in claim 1, characterized in that the substrate is free of carbon nanotube catalyst materials.

7. The storage device in claim 1, characterized in that the carbon nanotubes form a consistent lining along approximately the entire length of sidewalls of said trench.

8. The storage device in claim 1, characterized in that the device is planarized so that a top surface of the substrate is coplanar with respective top surfaces of the trench dielectric, the conductive carbon nanotube and the trench conductor.

9. The storage device in claim 1, characterized in that the conductive carbon nanotubes are grown downwards into the trench.

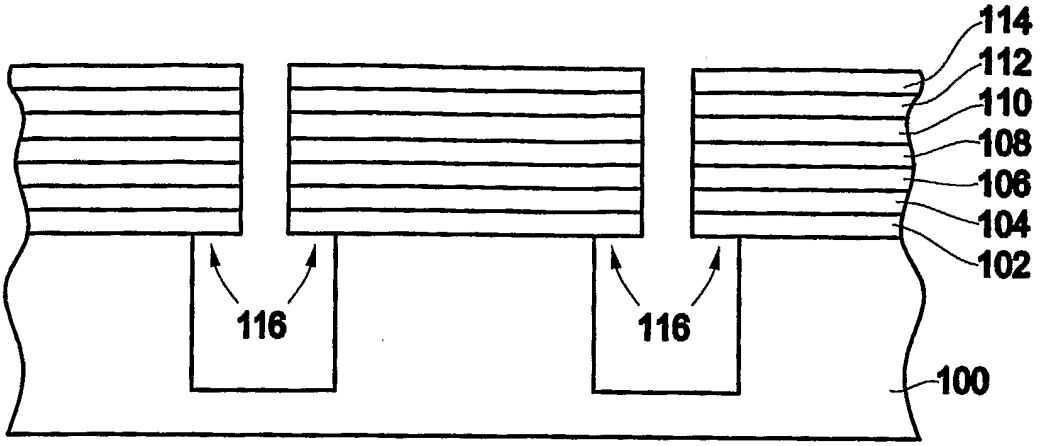


FIG.1

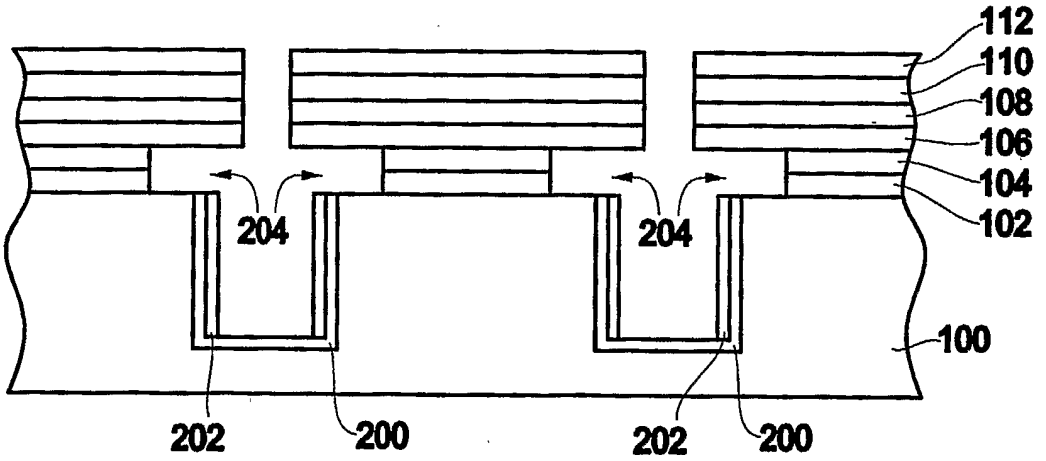


FIG.2

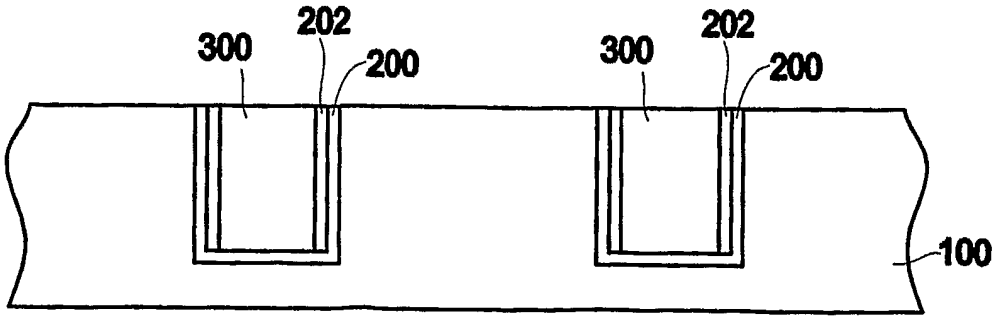


FIG.3

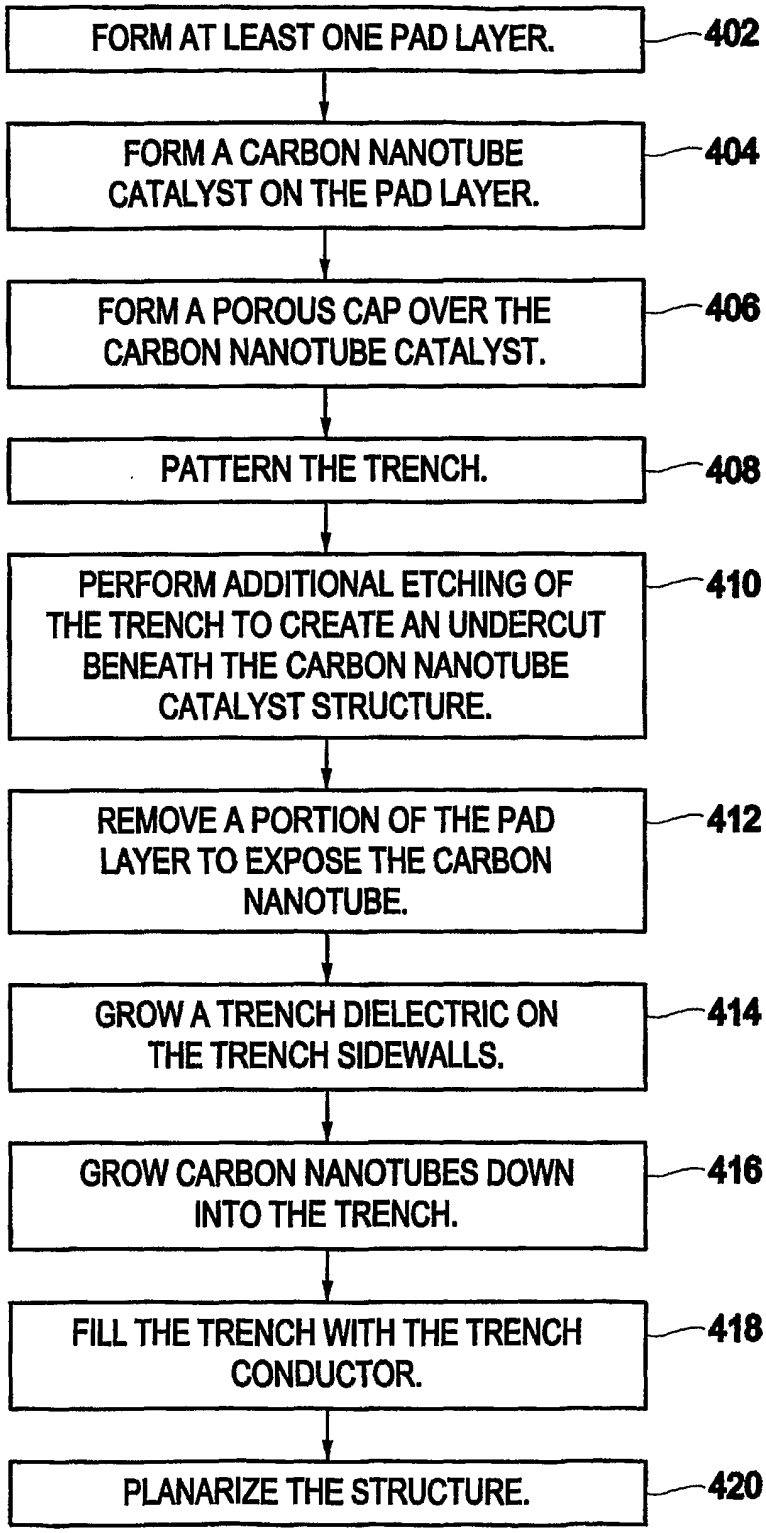

FORM AT LEAST ONE PAD LAYER.
402
FORM A CARBON NANOTUBE CATALYST ON THE PAD LAYER.
404
FORM A POROUS CAP OVER THE CARBON NANOTUBE CATALYST.
406
PATTERN THE TRENCH.
408
PERFORM ADDITIONAL ETCHING OF THE TRENCH TO CREATE AN UNDERCUT BENEATH THE CARBON NANOTUBE CATALYST STRUCTURE.
410
REMOVE A PORTION OF THE PAD LAYER TO EXPOSE THE CARBON NANOTUBE.
412
GROW A TRENCH DIELECTRIC ON THE TRENCH SIDEWALLS.
414
GROW CARBON NANOTUBES DOWN INTO THE TRENCH.
416
FILL THE TRENCH WITH THE TRENCH CONDUCTOR.
418
PLANARIZE THE STRUCTURE.
420

FIG.4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/40295

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01L 27/108
US CL : 257/301, 752
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/301, 306, 752,750, 753, 754, 758, 759, 760; 438/622, 623

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6,333,598 B1 (Hsu et al.) 25 December 2001 (25.12.2001), fig. 24, column7, lines 48-50, column 9 line 5, column 14 lines 15-55	1-9
A	US 2003/0211724 A1 (Haase) 13 November 2003 (13.11.2003), see entire document.	1-9
A	US 2003/0165418 A1 (Ajayan et al.) 04 Septemper 2003 (04.09.2003), see entire document.	1-9
A	US 2003/0100189 A1 (Lee et al.) 29 May 2003 (29.05.2003), see entire document.	1-9
A	US 2003/0179559 A1 (Engelhardt et al.) 25 Septemper 2003 (25.09.2003), see entire document.	1-9
A	US 6,599,808 B2 (Kim et al.) 29 July 2003 (29.07.2003), see entire document.	1-9
A	US 6,340,822 B1 (Brown et al.) 22 January 2002 (22.01.2002), see entire document.	1-9
A	US 6,286,226 B1 (Jin) 11 Septemper 2001 (11.09.2001), see entire document.	1-9
A	US 2002/0163079 A1 (Awano) 07 November 2002 (07.11.2002), see entire document.	1-9

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
21 April 2004 (21.04.2004)

Date of mailing of the international search report
06 AUG 2004

Name and mailing address of the ISA/US
Mail Stop PCT, Attn: ISA/US
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
Facsimile No. (703) 305-3230

Authorized officer
Wael M Fahmy

Telephone No. 703-308-0956

PCT/US03/40295

INTERNATIONAL SEARCH REPORT

C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,566,704 B2 (Choi et al.) 20 May 2003 (20.05.2003), see entire document.	1-9
A	US 6,548,313 B1 (Ravi et al.) 15 April 2003 (15.04.2003), see entire document.	1-9
A	US 2002/0167375 A1 (Hoppe et al.) 14 November 2002 (14.11.2002), see entire document.	1-9
A	US 2002/0125805 A1 (Hsu) 12 Septemper 2002 (12.09.2002), see entire document.	1-9