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Foss et al.

[11] **3,769,525**

[45] **Oct. 30, 1973**

[54] **BI-DIRECTIONAL AMPLIFYING BUS-SWITCH**

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[52] U.S. Cl. ..... **307/254**, 307/215, 307/241, 307/247 R, 307/289, 328/97, 328/99

[51] Int. Cl. **H03k 17/66**, H03k 17/16

[58] **Field of Search** 307/208, 215, 217, 307/239, 240, 241, 242, 243, 247, 289, 291, 292; 328/97, 99

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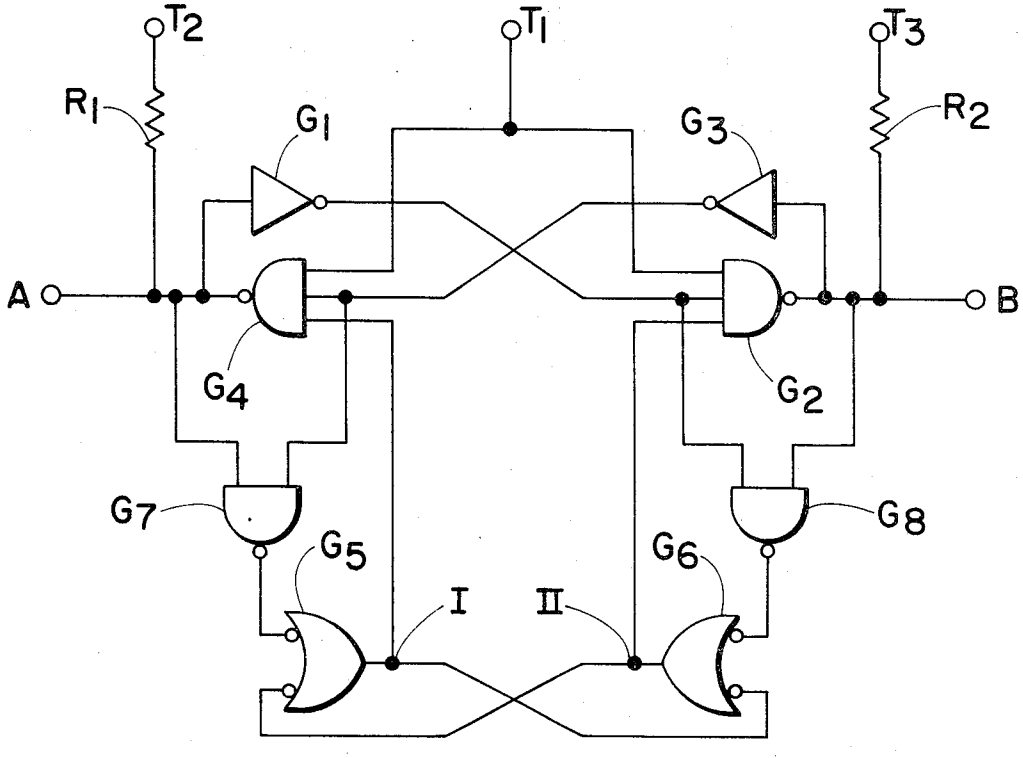
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Primary Examiner—John W. Huckert
Assistant Examiner—L. N. Anagnos
Attorney—Alfred A. DeLuca

[57] **ABSTRACT**

A bus-switch which permits data-transmission with amplification therethrough in a predetermined one of two directions. Transmission in the established direction is maintained regardless of conditions at the output side of the switch until data applied to the switch from such direction ceases. This is achieved by a logic network which includes memory means for remembering the direction of transmission which has priority.

17 Claims, 10 Drawing Figures



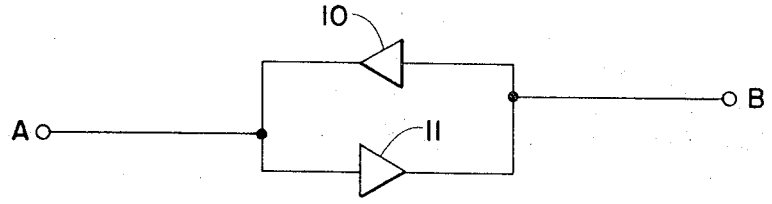


Fig. 1 (PRIOR ART)

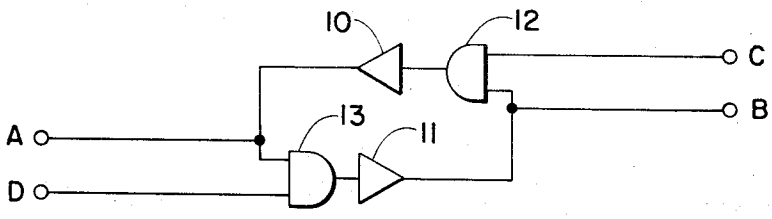


Fig. 2

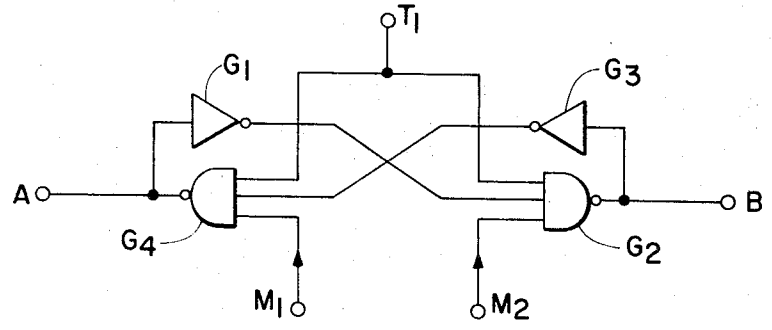


Fig. 3

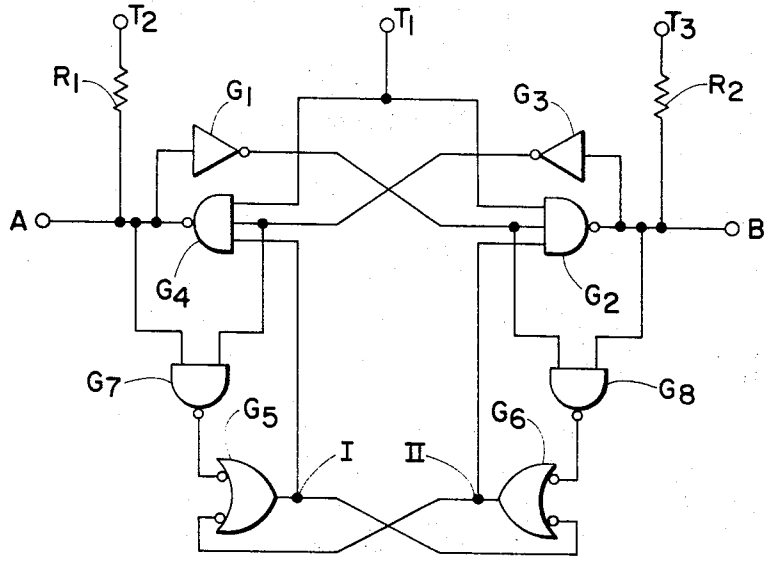


Fig. 4

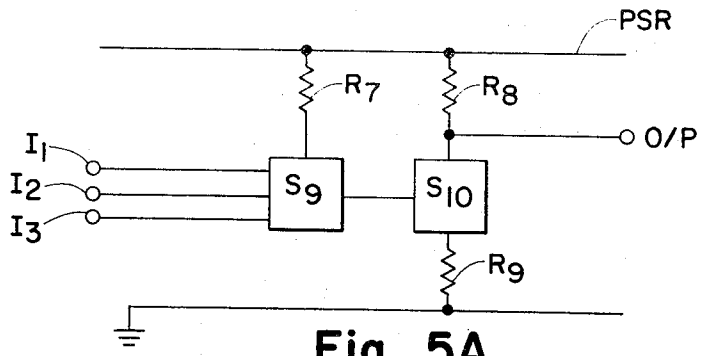


Fig. 5A

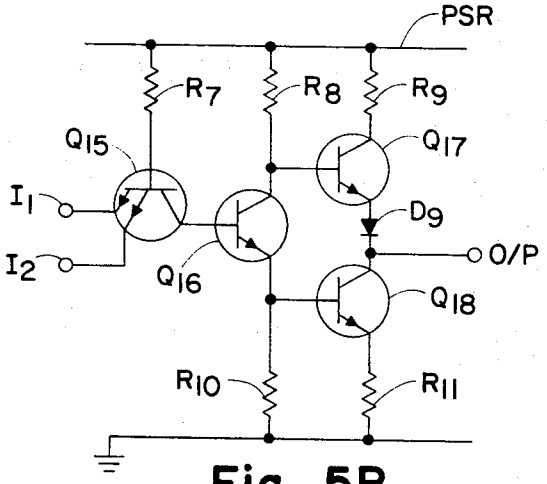


Fig. 5B

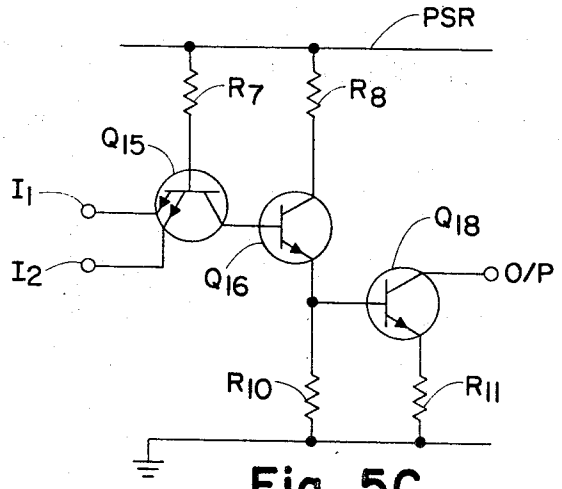


Fig. 5C

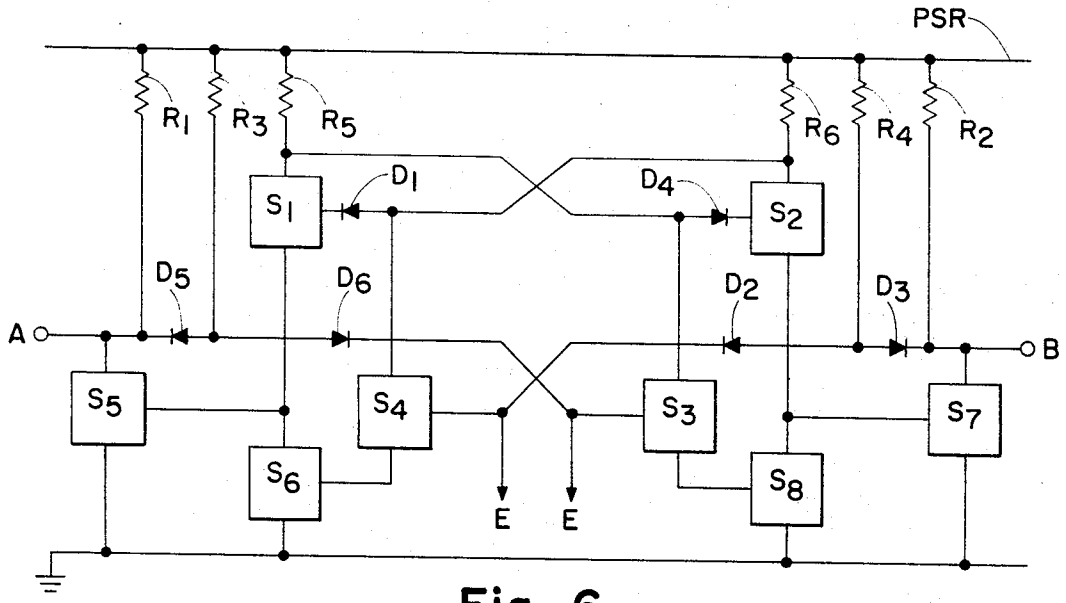


Fig. 6

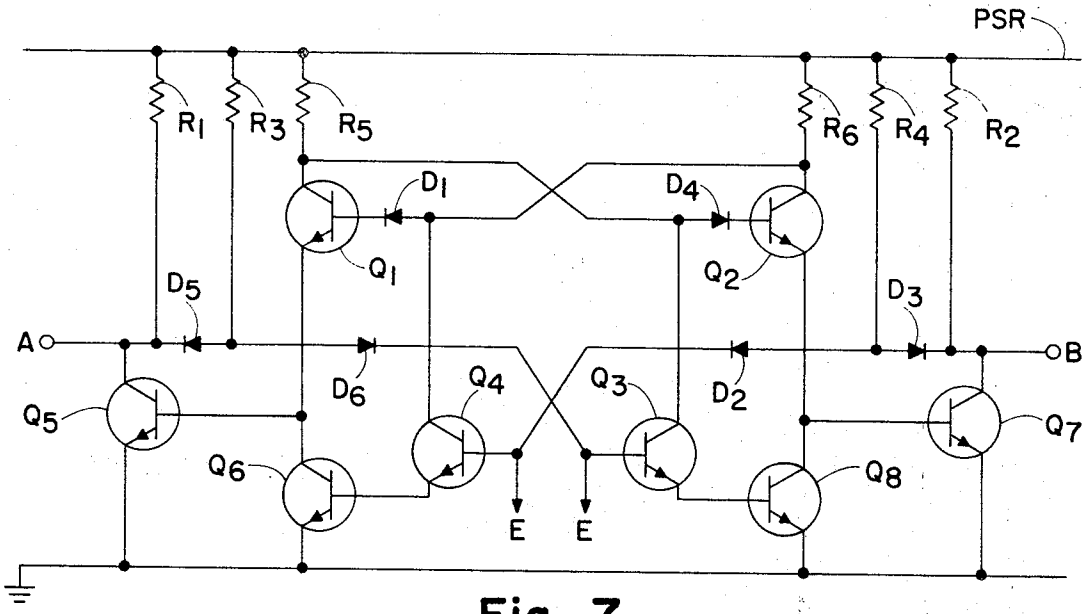

PSR
R1
R3
R5
R6
R4
R2
D1
D4
Q1
Q2
D5
D3
A
B
D6
Q4
Q3
D2
Q5
Q7
Q6
Q8
E
E

Fig. 7

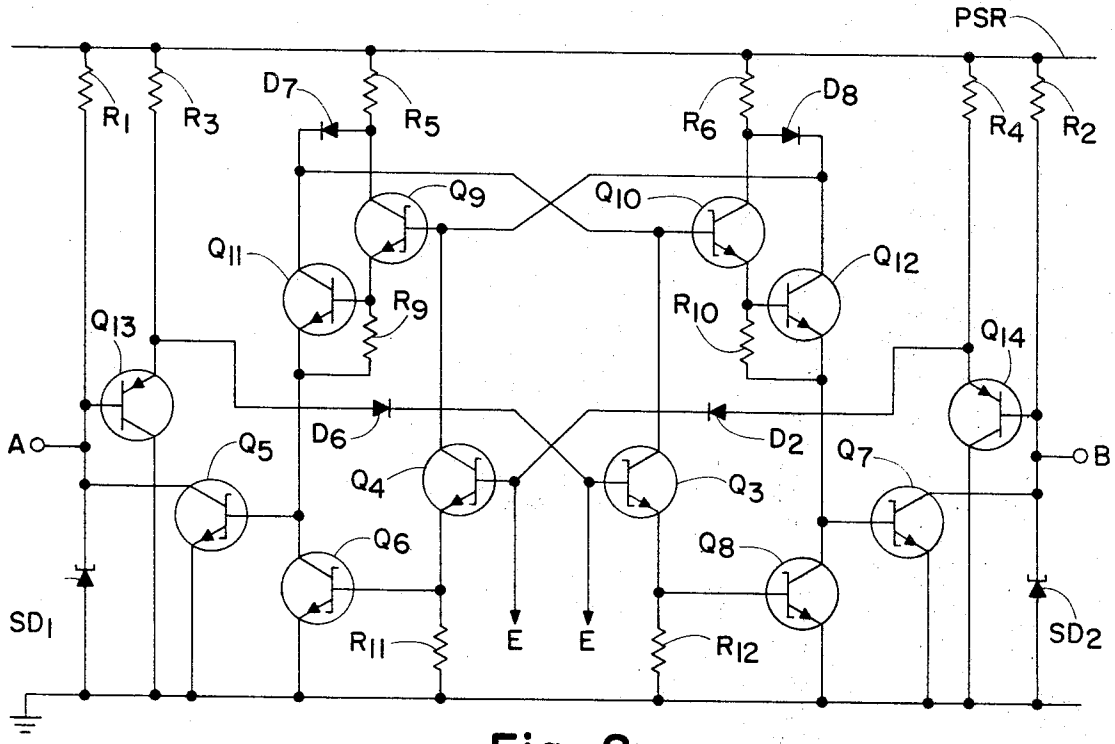

PSR
R1
R3
D7
R5
R6
D8
R4
R2
Q9
Q10
Q11
Q12
R9
R10
Q13
Q14
A
B
D6
D2
Q5
Q4
Q3
Q7
Q6
Q8
SD1
R11
E
E
R12
SD2

Fig. 8

BI-DIRECTIONAL AMPLIFYING BUS-SWITCH

The present invention relates to a bi-directional amplifying bus-switch.

There are many instances in the data-transmission art when it is necessary or desirable to transmit data in opposite directions and with amplification along a bus line. This requires two amplifying functions — one for amplifying data transmitted in one direction and the other for amplifying data transmitted in the opposite direction. This use of two amplifiers in a single loop gives rise to a serious oscillation problem, and it is this problem which the present invention seeks to avoid.

According to the present invention there is provided a bi-directional bus switch circuit having first and second terminal means for series connection into a bus-line, first amplifying gate means having its input connected to said first terminal means, second logic gate means having first, second and third inputs, its second input connected to the output from said first amplifying gate means, enabling means and memory means for said circuit, the first and third inputs of said second logic gate connected to said enabling means and said memory means respectively, the output from said second logic gate means connected to said second terminal means, third amplifying gate means having its input connected to said second terminal means, fourth logic gate means having first, second and third inputs, its second input connected to the output from said third amplifying gate means, said first and third inputs of said fourth logic gate connected to said enabling means and said memory means respectively, the output from said fourth logic gate means connected to said first terminal means, whereby, when the direction of data transmission is established from one of said first and second terminal means to the other, said memory means applies and maintains an input to the respective logic gate associated with said direction of data transmission such that the output level thereof corresponds to the input level at said one terminal means when an enabling signal is applied to the first input of said respective logic gate, said memory means further applying and maintaining an input to the other said logic gate such that the output thereof is constant regardless of the data input level at said other of said first and second terminal means, said memory means so functioning until the flow of data transmission in said established direction ceases.

In a preferred embodiment of the invention, said memory means comprises seventh and eighth NAND gate means each having first and second inputs, said first input of said seventh NAND gate means connected to said first terminal means and said second input of said seventh NAND gate means connected to said second input of said fourth NAND gate means, said first input of said eighth NAND gate means connected to said second terminal means and said second input of said eighth NAND gate means connected to said second input of said second NAND gate means, the output of said seventh NAND gate means connected to a first inverting input of a fifth OR gate means, the output of said fifth OR gate means connected to a second inverting input of a sixth OR gate means, said sixth OR gate means having its output connected to a second inverting input of said fifth OR gate means and said sixth OR gate means having a second inverting input connected to the output of said eighth NAND gate means, the outputs of said fifth and sixth OR gate means being connected to the third inputs of said fourth and second NAND gate means respectively.

By De Morgan's theorem, the invention also encompasses the obvious logical equivalents of the foregoing circuit elements and combinations thereof.

According to yet a further embodiment of the invention, a bi-directional bus-switch circuit comprises first and second terminal means for series connection into a bus-line, each of said first and second terminal means resistively coupled to means for connection to a power supply rail, said first terminal means connected through a fifth controllable switch means to means for connection to a reference ground potential rail and said second terminal means connected through a seventh controllable switch means to means for connection to said reference ground potential rail, fifth and sixth diode means series connected between said first terminal means and the control electrode of a third controllable switch means, second and third diode means series connected between said second terminal means and the control electrode of a fourth controllable switch means, fifth resistive means connected between means for connection to said potential supply rail and fourth diode means, the junction between said fifth resistive means and said fourth diode means being connected through said third controllable switch means to the control electrode of an eighth controllable switch means, said junction between said fifth resistive means and said fourth diode means being further connected through first and sixth controllable switch means to means for connection to said reference ground potential rail, sixth resistive means connected between means for connection to said potential supply rail and first diode means, the junction between said sixth resistive means and said first diode means being connected through said fourth controllable switch means to the control electrode of said sixth controllable switch means, said junction between said sixth resistive means and said first diode means being further connected through second and said eighth controllable switch means to means for connection to said reference ground potential rail, the side of said fourth diode means remote from said fifth resistive means connected to the control electrode of said second controllable switch means and the side of said first diode means remote from said sixth resistive means connected to the control electrode of said first controllable switch means, the junction of said first and sixth controllable switch means connected to the control electrode of said fifth controllable switch means and the junction of said second and eighth controllable switch means connected to the control electrode of said seventh controllable switch means, third and fourth resistive means connecting the junctions between said fifth and sixth and said second and third diode means respectively to means for connection to said potential supply rail and means connected to the control electrodes of said third and fourth controllable switch means for connection to a pulse potential supply means for selectively enabling and disabling said third and fourth controllable switch means.

In yet a further embodiment of the invention the aforesaid controllable switch means are bipolar transistors, the diode means are diodes and the resistive means are resistors.

The invention will now be described further by way of example only and with reference to the accompanying drawings, wherein:

FIG. 1 shows a bi-directional circuit with amplification according to the prior art;

FIG. 2 shows the prior art circuit of FIG. 1 with logic gates inserted therein according to the present invention; and

FIGS. 3, 4, 5(*a*, *b* and *c*), 6, 7 and 8 show bus-switch circuits according to various embodiments of the invention.

Referring now to the drawings, and particularly FIG. 1 thereof, there is shown a bus line having terminals A and B and two amplifiers 10 and 11 connected in parallel and inserted in the line, amplifier 10 for amplifying data transmitted from B to A and amplifier 11 for amplifying data transmitted from A to B. Immediately it will be seen that the loop formed by these amplifiers will quickly cause oscillation, effectively blocking accurate data transmission in either direction.

In the present invention, amplifier 11 is effectively disabled while data is being transmitted from B to A and amplifier 10 is disabled while data is being transmitted from A to B. This is accomplished by inserting a logic gate 12 or 13 in series with each respective amplifier, as shown in FIG. 2. One input to logic gate 12 is connected to terminal B and the other input to a terminal C. Similarly, one input to logic gate 13 is connected to terminal A and the input to a terminal D. Terminals C and D are connected to memory means for remembering which direction data transmission has been established and for ensuring that the logic gate controlling data flow in that direction remains enabled and the logic gate controlling data flow in the opposite direction is disabled until data flow in the originally established direction ceases.

In FIG. 2, gates 12 and 13 are shown as AND gates, but they may be any of the well known logic function gates depending upon the nature of the signals applied to terminal C and D from the memory means.

In the following description logic gates are extensively involved. Therefore, before proceeding further, a definition of such gates is given at this point.

A NAND gate is one wherein a LOW output is obtained only if all inputs are HIGH — otherwise the output is HIGH.

An OR gate is one wherein a HIGH output is obtained only if one or more inputs are HIGH.

A realization of the circuit of FIG. 2 is shown in FIG. 3. The amplifier 10 and gate 12 of FIG. 2 are replaced in FIG. 3 by a NAND gate G_4 and an amplifying inverter G_3. Similarly, the amplifier 11 and gate 13 are replaced by a NAND gate G_2 and an amplifying inverter G_1. An enabling input signal source for gates G_2 and G_4 is connected to terminal T_1. The third inputs of gates G_2 and G_4 are connected to a memory means M_1, M_2.

In FIG. 4, the memory means comprises a flip-flop comprising two cross-coupled inverting input OR gates G_5 and G_6, the output node I of G_5 being connected to an input to G_4 and the output node II of G_6 being connected to an input to G_2. The second input of inverting input OR gate G_5 is connected to the output of a NAND gate G_7, one input of which is connected to terminal A and the other is connected to the output of G_3. Similarly, the second input of inverting input OR gate G_6 is connected to the output of a NAND gate G_8, one input of which is connected to terminal B and the other is connected to the output of G_1.

The circuit operates as follows. Initially, both terminals A and B are pulled to a potential HIGH rail through resistors R_1 and R_2 and terminals T_2 and T_3. Let terminal B now be pulled to LOW condition by application of data thereto. Now G_7 inputs are HIGH (derived from the output of G_3) and HIGH (derived from terminal A). The output of G_7 is therefore LOW, which is applied to the inverting input of G_5. The output of G_5 — and therefore node I — is HIGH, and node II is consequently LOW. The inputs to G_4 are now HIGH (derived from node I), HIGH (derived from G_3) and — when T_1 is fed with a HIGH enabling signal — HIGH. Therefore, an amplified LOW signal is obtained at the output of G_4. Checking G_2, the input derived from node II is LOW and the output is therefore HIGH — i.e., G_2 is disabled.

Regardless of terminal A now going LOW, the input to G_8 derived from terminal B is LOW until the condition of this terminal changes. Therefore the output from G_8 remains HIGH, ensuring two HIGH inputs to G_6 and ensuring a LOW output therefrom at node II. Thus, the switch maintains its transmission of data from B to A, regardless of the state of terminal A, until terminal B returns to a HIGH level.

It will be appreciated that the logic circuit of FIG. 4 may equally well be represented in terms of its logic equivalents. For example, gate G_7 could be an AND gate and the input of gate G_5 made non-inverting. Taking this variation further, gate G_5 could have both inputs non-inverting and the output inverting, whereupon the input to G_4 connected to node I would be inverting. The second input to G_4 can also be inverting if the input to G_7 connected thereto is inverting and G_3 is non-inverting. The third input to G_4 can be inverting if the enable input from T_1 is LOW instead of HIGH. Now we have three inverting inputs to G_4 and an inverting output. This is, of course, by De Morgan's theorem, an OR gate. Exactly equivalent substitutions and modifications to the remaining gates in the circuit can be made having regard to the symmetry of the circuit. Also, according to De Morgan's theorem, the logical inverse function with HIGH and LOW states interchanged may be constructed.

FIG. 5A shows each of gates G_1 to G_8 inclusive of FIG. 4 in circuit block form. Each gate comprises a controllable switch means S_9 having multiple inputs I_1, I_2, I_3 . . . etc. The number of inputs provided is dependant upon the number of inputs required — i.e., G_1 and G_3 only have one operative input, G_2 and G_4 have three operative inputs and G_5 to G_8 inclusive have two operative inputs. All operative inputs must be HIGH before an output from S_9 is obtained. The control electrode of S_9 is connected through resistive means R_7 to a potential supply rail PSR. The output of S_9 is connected to the control electrode of a controllable switch means S_{10}, the input of which is connected through resistive means R_8 to potential supply rail PSR and the output of which is connected through resistive means R_9 to reference ground potential. The output O/P from the gate is derived from the input of S_{10}. The circuit operates as follows. When all inputs I_1, I_2, I_3 . . . are HIGH an output is derived from S_9 which enables S_{10}. The output node O/P derived from the potential supply rail PSR and which would normally be HIGH is now pulled down to LOW condition since S_{10} is draining current to ground.

Therefore O/P is LOW when all of I_1, I_2, I_3 . . . etc. are HIGH.

The circuit of FIG. 5A may be conveniently realized in two TTL (transistor-transistor-logic) forms, the first of which is shown in FIG. 5B and is applicable to gates G_1, G_3 and G_5 to G_8 of FIG. 4 inclusive. Switch S_9 of FIG. 5A is now realized by transistor Q_{15}, which has multiple emitters connected to inputs I_1 and I_2. Obviously, as many emitters as are required may be provided. The second switch means of FIG. 5A is realized by the network comprising transistors Q_{16}, Q_{17} and Q_{18}, diode D_9 and resistors R_8, R_9, R_{10} and R_{11}. When all of I_1, I_2 . . . etc are HIGH, an output is derived from Q_{15} which is applied to the base of Q_{16} enabling Q_{16}. The values of resistors R_8 and R_{10} are such that when Q_{16} is conducting, sufficient charge is applied to the bases of Q_{17} and Q_{18} to enable them. Now the output node is connected to the PSR rail through resistor R_9 and diode D_9 and to the ground rail through resistor R_{11}. The ratio of the series combination of R_9 and D_9 to R_{11} is so chosen that in this condition, the output node will be nearer ground, i.e., LOW. Suppose now that any or all of I_1, I_2 . . . etc. are LOW. Now the output from Q_{15} will be LOW and Q_{16} will be disabled. In this situation charge will be applied to the base of Q_{17} and Q_{17} will be enabled. Clearly, Q_{18} will be disabled. Now, the output node swings HIGH as current is drawn from PSR through R_9 and D_9.

Turning now to FIG. 5C, an open-collector TTL gate which may be used for switches G_2 and G_4 if FIG. 4 is shown. Transistors Q_{15}, Q_{16} and Q_{18} are similar to those of FIG. 5B and are likewise designated. However, bearing in mind the function of each of gates G_2 and G_4 is to selectively pull the nodes of respective terminals A and B LOW (see FIG. 4), the circuit of FIG. 5C has an open-collector configuration for output transistor Q_{18}. Thus, when all inputs I_1, I_2 . . . etc. of Q_{15} are HIGH, Q_{16} is enabled and with resistors R_8 and R_{10} appropriately ratioed Q_{18} is also enabled. As a result the output node O/P is connected to ground and related terminal A (for G_4) or B (for G_2) is also connected to ground. If now any or all of I_1, I_2 . . . etc. are LOW, Q_{16} is disabled and as a result, Q_{18} is also disabled, thereby allowing output node O/P to rise.

Referring now to FIG. 6, a circuit in block form according to a further embodiment of the invention has terminals A and B for connection into a bus-line. Normally, each of terminals A and B is held HIGH, being pulled to the value of a potential supply rail PSR through a resistor R_1 or R_2 respectively. Terminal A is also connected through a controllable switch means S_5 to a reference ground potential rail. Series connected between the potential supply rail PSR and a reference ground potential rail are a resistive means R_5, a controllable switch means S_1 and a controllable switch means S_6 respectively. The control electrode of controllable switch means S_5 connected to the junction between S_1 and S_6. The junction between R_5 and S_1 is connected through a diode means D_4 to the control electrode of a controllable switch means S_2. Series connected between the potential supply rail PSR and ground are respectively a resistive means R_6, the controllable switch means S_2 and a controllable switch means S_8. The junction between R_6 and S_2 is connected through a diode means D_1 to the control electrode of controllable switch means S_1. Terminal B is connected through a controllable switch means S_7 to the reference ground potential rail and the control electrode of S_7 is connected to the junction of S_2 and S_8. The junction of D_1 and R_6 is connected through a controllable switch means S_4 to the control electrode of S_6 and the junction of R_5 and D_4 is connected through a controllable switch means S_3 to the junction of S_8. The control electrode of S_4 is connected through back-to-back diodes D_2 and D_3 to terminal B and the control electrode of S_3 is connected through back-to-back diodes D_5 and D_6 to terminal A. The control electrodes of S_3 and S_4 are also connected to an enable/disable signal supply source, designated E,E. The junction between diodes D_2 and D_3 is connected through resistive means R_4 to the PSR rail and the junction between diodes D_5 and D_6 is connected to the PSR rail through resistive means R_3.

Referring to FIG. 7, a realization of the circuit of FIG. 6 is shown. Again, each of terminals A and B is normally held HIGH, being pulled up to the potential supply rail PSR through a resistor R_1 or R_2 respectively. Typically, the potential supply rail is at +5 volts. Terminal A is also connected through the collector-emitter path of a transistor Q_5 to a reference ground potential rail. The base of Q_5 is connected through the emitter-collector path of a transistor Q_1 to a diode D_4 and one end of a resistor R_5, the other end of which is connected to the potential supply rail. The base of Q_5 is also connected through the collector-emitter path of a transistor Q_6 to the reference ground potential rail. The base of Q_6 is connected through the emitter-collector path of a transistor Q_4 and a diode D_1 to the base of transistor Q_1. The base of transistor Q_4 is connected to terminal B through back-to-back diodes D_2 and D_3, the junction between said diodes being connected to the potential supply rail through a resistor R_4.

Terminal B is connected through the collector-emitter junction of a transistor Q_7 to a reference ground potential rail. The base of Q_7 is connected through the emitter-collector path of a transistor Q_2 to diode D_1 and one end of a resistor R_6, the other end of which is connected to the potential supply rail. The base of Q_7 is also connected through the collector-emitter path of a transistor Q_8 to the reference ground potential rail. The base of transistor Q_8 is connected through the emitter-collector path of a transistor Q_3 and diode D_4 to the base of transistor Q_2. The base of transistor Q_3 is connected through back-to-back diodes D_5 and D_6 to terminal A, the junction between D_5 and D_6 being connected to the potential supply rail through a resistor R_3.

The base electrode of each of transistors Q_3 and Q_4 is connected to a disabling signal input E, E. This is derived from a suitable input buffer accepting standard input logic signals and delivering current outputs into Q_3 and Q_4 base electrodes when it is desired that no transmission of data in either direction shall occur. This current turns on Q_3 and Q_4 and, hence, Q_6 and Q_8, ensuring that Q_1, Q_5, Q_2 and Q_7 are all disabled. This inhibits transmission of data in either direction.

Suppose now however, that the disabling current is not fed to Q_3 and Q_4. The circuit then operates as follows. Let both the inputs at A and B be HIGH. Suppose the input B now goes LOW. Current is now drawn through resistors R_2 and R_4. Assume that LOW level is reference ground potential and that one diode potential drop V_D is approximately equivalent to one base-emitter potential drop in any conducting transistor, i.e., V_{BE}. When B was HIGH, the potential at the anode of

diode D_3 was $3V_{BE}$ (one diode drop across D_2, and one V_{BE} drop across each of Q_4 and Q_6). When B goes LOW approaching zero the potential at the anode of D_3 is now only V_D — i.e., the drop across D_3. Thus, the potential at the base of Q_4 is essentially at ground and Q_4 is therefore disabled. Thus, no potential appears at the base of Q_6 and Q_8 is disabled. Because Q_4 is disabled current in R_6 can now flow into the path comprising diode D_1 and the base-emitter junctions of Q_1 and Q_5. Transistor Q_5 now conducts, pulling terminal A down to reference ground potential. Since A is now at reference ground potential — or LOW — the potential at the base of Q_3 goes to approximately ground, disabling Q_3 and hence Q_8. However, since there is still a current path through diode D_1 and the base-emitter junction of Q_1 and Q_5 to ground, the junction of resistor R_5 and the collector of Q_1 are only one V_{BE} drop through Q_5 above ground potential. Thus, the potential appearing at the base of Q_2 is essentially zero, since there is a diode drop across D_4. Thus, no current path is established through Q_2 and Q_7 remains disabled, maintaining point B in isolation from the reference ground potential rail. Therefore, transmission of data through the circuit from B to A is established regardless of the state of terminal A, until either a disabling signal is inputted or terminal B goes HIGH again.

Turning now to FIG. 8, there is shown a further embodiment of the invention wherein the novel bi-directional bus switch is in circuit form particularly suitable for integrated circuit fabrication techniques. The circuit is similar to that of FIG. 7 and like elements in FIGS. 7 and 8 are designated by like references.

The circuit of FIG. 8 contains the following elements which do not appear in FIG. 7. Schottky diodes SD_1 and SD_2 connected between the reference ground potential rail and terminals A and B respectively are anti-ringing devices which clamp the input line to one Schottky diode drop below reference ground potential. Transistors Q_{13} and Q_{14} are used in place of diodes D_5 and D_3 respectively, reducing the input current required. The only input current required is the base current drive on each of Q_{11} and Q_{12}. Transistor Q_1 and diode D_1 in FIG. 7 are replaced by transistors Q_{11} and Q_9 in FIG. 8. Similarly, transistors Q_{10} and Q_{12} replace transistor Q_2 and diode D_4 in FIG. 7. The purpose of these substitutions is to provide Darlington pairs Q_9, Q_{11} and Q_{10}, Q_{12}, which are faster switching, easier to fabricate in integrated — circuit form and have better gain characteristics than the transistor — diode combination. Each of resistors R_9, R_{10}, R_{11} and R_{12} are to ensure that the transistors with which they are associated — i.e., Q_9, Q_{10}, Q_4 and Q_3 — are more rapidly and completely disabled by pulling their base towards to reference ground potential. Finally, it will be noted that the majority of transistors used in the circuit of FIG. 8 are Schottky clamped transistors, which provide faster switching than conventional types.

Various alternatives and modifications to the embodiments disclosed herein will be readily apparent to those skilled in the art without departing from the spirit and scope of the invention as described by the disclosure and defined by the claims appended hereto.

What is claimed is:

1. A bi-directional bus switch circuit having first and second terminal means for series connection into a busline, first amplifying gate means having input and output parts, its input part connected to said first terminal means, second logic gate means having an output part and first, second and third input parts, its second input part connected to said output part of said first amplifying gate means, enabling means and memory means for said circuit, said first and third input parts of said second logic gate means connected to said enabling means and said memory means respectively, said output part of said second logic gate means connected to said second terminal means, third amplifying gate means having input and output parts, its input part connected to said second terminal means, fourth logic gate means having an output part and first, second and third input parts, its second input connected to the output from said third amplifying gate means, said first and third inputs of said fourth logic gate connected to said enabling means and said memory means respectively, said output part of said fourth logic gate means connected to said first terminal means;

whereby, when the direction of data transmission is established from one of said first and second terminal means to the other, said memory means applies and maintains an input to the respective logic gate associated with said direction of data transmission such that the output level thereof corresponds to the input level at said one terminal means when an enabling signal is applied to the first input part of said respective logic gate, said memory means further applying and maintaining an input to the other said logic gate such that the output thereof is constant regardless of the data input level at said other of said first and second terminal means, said memory means so functioning until the flow of data transmission in said established direction ceases;

2. The invention as defined in claim 1 wherein the first and third amplifying gate means are inverting gates, and wherein the second and fourth logic gate means are NAND gates.

3. The circuit of claim 2 wherein said memory means comprises seventh and eighth logic gate means each having first and second input parts, said first input part of said seventh logic gate means connected to said first terminal means and said second input part of said seventh logic gate means connected to said second input part of said fourth NAND gate means, said first input part of said eighth logic gate means connected to said second terminal means and said second input part of said eighth logic gate means connected to said second input part of said second NAND gate means, said memory means also comprises a fifth and sixth logic gate means cross connected as a storage element or flip-flop, the output part of said seventh logic gate means connected to a first input part of the fifth logic gate means, the output part of said fifth logic gate means connected to a second input part of the sixth logic gate means, said sixth logic gate means having its output part connected to a second input part of said fifth logic gate means and said sixth logic gate means having a first input part connected to the output part of said eighth logic gate means, the output parts of said fifth and sixth logic gate means being connected to the third input parts of said fourth and second NAND gate means respectively;

4. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are OR gates with inverting input parts.

5. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are AND gates with inverting input parts.

6. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are NAND gates.

7. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are NOR gates.

8. The invention as defined in claim 2 wherein said memory means comprises seventh and eighth logic gate means, each having first and second input parts, said first input part of said seventh logic gate means connected to said first terminal means and said second input part of said seventh logic gate means connected to said second input part of said fourth NAND gate means, said first input part of said eighth logic gate means connected to said second terminal means and said second input part of said eighth logic gate means connected to said second input part of said second NAND gate means, said memory means also comprises a fifth and a sixth logic gate means cross connected as a storage element or flip-flop, the output part of said seventh logic gate means connected to a first input part of the fifth logic gate means, the output part of said fifth logic gate means connected to a second input part of the sixth logic gate means, said sixth logic gate means having its output part connected to a second input part of said fifth logic gate means and said sxith logic gate means having a first input part connected to the output part of said eighth logic gate means, the output parts of said fifth and sixth logic gate means being connected to the third input parts of said second and fourth NAND gate means respectively.

9. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are NOR gates.

10. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are NAND gates.

11. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are OR gates with inverting input parts.

12. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are AND gates with inverting input parts.

13. The invention as defined in claim 1 wherein the first and third amplifying gate means are non-inverting gates, and wherein the second and fourth logic gate means are NOR gates.

14. A bi-directional bus switch circuit comprising first and second terminal means for series connection into a bus-line, each of said first and second terminal means resistively coupled to means for connection to a power supply rail, said first terminal means connected through a fifth controllable switch means to means for connection to a reference ground potential rail and said second terminal means connected through a seventh controllable switch means to means for connection to said reference ground potential rail, fifth and sixth diode means series connected between said first terminal means and the control electrode of a third controllable switch means, second and third diode means series connected between said second terminal means and the control electrode of a fourth controllable switch means, fifth resistive means connected between means for connection to said potential supply rail and fourth diode means, the junction between said fifth resistive means and said fourth diode means being connected through said third controllable switch means to the control electrode of an eighth controllable switch means, said junction between said fifth resistive means and said fourth diode means being further connected through first and sixth controllable switch means to means for connection to said reference ground potential rail, sixth resistive means connected between means for connection to said potential supply rail and first diode means, the junction between said sixth resistive means and said first diode means being connected through said fourth controllable switch means to the control electrode of said sixth controllable switch means, said junction between said sixth resistive means and said first diode means being further connected through second and said eighth controllable switch means to means for connection to said reference ground potential rail, the side of said fourth diode means remote from said fifth resistive means connected to the control electrode of said second controllable switch means and the side of said first diode means remote from said sixth resistive means connected to the control electrode of said first controllable switch means, the junction of said first and sixth controllable switch means connected to the control electrode of said fifth controllable switch means and the junction of said second and eighth controllable switch means connected to the control electrode of said seventh controllable switch means, third and fourth resistive means connecting the junctions between said fifth and sixth and said second and third diode means respectively to means for connection to said potential supply rail and means connected to the control electrodes of said third and fourth controllable switch means for connection to a pulse potential supply means for selectively enabling and disabling said third and fourth controllable switch means.

15. The circuit of claim 14 wherein said controllable switch means are bipolar transistors.

16. The circuit of claim 14 wherein said diode means are diodes.

17. The circuit of claim 14 wherein said resistive means are resistors.

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