A bus-switch which permits data-transmission with amplification therethrough in a predetermined one of two directions. Transmission in the established direction is maintained regardless of conditions at the output side of the switch until data applied to the switch from such direction ceases. This is achieved by a logic network which includes memory means for remembering the direction of transmission which has priority.

17 Claims, 10 Drawing Figures
Fig. 5A

Fig. 5B

Fig. 5C

Fig. 6
The present invention relates to a bi-directional amplifying bus-switch.

There are many instances in the data-transmission art when it is necessary or desirable to transmit data in opposite directions and with amplification along a bus line. This requires two amplifying functions — one for amplifying data transmitted in one direction and the other for amplifying data transmitted in the opposite direction. This use of two amplifiers in a single loop gives rise to a serious oscillation problem, and it is this problem which the present invention seeks to avoid.

According to the present invention there is provided a bi-directional bus switch circuit having first and second terminal means for series connection into a bus-line, first amplifying gate means having its input connected to said first terminal means, second logic gate means having first, second and third inputs, its second input connected to the output from said first amplifying gate means, enabling means and memory means for said circuit, the first and third inputs of said second logic gate means connected to said enabling means and said memory means respectively, the output from said second logic gate means connected to said second terminal means, third amplifying gate means having its input connected to said second terminal means, fourth logic gate means having first, second and third inputs, its second input connected to the output from said third amplifying gate means, said first and third inputs of said fourth logic gate connected to said enabling means and said memory means respectively, the output from said fourth logic gate means connected to said first terminal means, whereby, when the direction of data transmission is established from one of said first and second terminal means to the other, said memory means applies and maintains an input to the respective logic gate associated with said direction of data transmission such that the output level thereof corresponds to the input level at said one terminal means when an enabling signal is applied to the first input of said respective logic gate, said memory means further applying and maintaining an input to the other said logic gate such that the output thereof is constant regardless of the data input level at said other of said first and second terminal means, said memory means so functioning until the flow of data transmission in said established direction ceases.

In a preferred embodiment of the invention, said memory means comprises seventh and eighth NAND gate means each having first and second inputs, said first input of said seventh NAND gate means connected to said first terminal means and said second input of said seventh NAND gate means connected to said second terminal means and said second input of said seventh NAND gate means connected to said second input of said fourth NAND gate means, said first input of said eighth NAND gate means connected to said second terminal means and said second input of said eighth NAND gate means connected to said second input of said second NAND gate means, the output of said seventh NAND gate means connected to a first inverting input of a fifth OR gate means, the output of said fifth OR gate means connected to a second inverting input of a sixth OR gate means, said sixth OR gate means having its output connected to a second inverting input of said fifth OR gate means and said sixth OR gate means having a second inverting input connected to the output of said eighth NAND gate means, the outputs of said fifth and sixth OR gate means being connected to the third inputs of said fourth and second NAND gate means respectively.

By De Morgan's theorem, the invention also encompasses the obvious logical equivalents of the foregoing circuit elements and combinations thereof.

According to yet a further embodiment of the invention, a bi-directional bus-switch circuit comprises first and second terminal means for series connection into a bus-line, each of said first and second terminal means resistively coupled to means for connection to a power supply rail, said first terminal means connected through a fifth controllable switch means to means for connection to a reference ground potential rail and said second terminal means connected through a seventh controllable switch means to means for connection to said reference ground potential rail, fifth and sixth diode means series connected between said first terminal means and the control electrode of a third controllable switch means, second and third diode means series connected between said second terminal means and the control electrode of a fourth controllable switch means, fifth resistive means connected between means for connection to said potential supply rail and fourth diode means, the junction between said fifth resistive means and said fourth diode means being connected through said third controllable switch means to the control electrode of an eighth controllable switch means, said junction between said fifth resistive means and said fourth diode means being further connected through first and sixth controllable switch means to means for connection to said reference ground potential rail, sixth resistive means connected between means for connection to said potential supply rail and first diode means, the junction between said sixth resistive means and said first diode means being connected through said fourth controllable switch means to the control electrode of said sixth controllable switch means, said junction between said sixth resistive means and said first diode means being further connected through second and said eighth controllable switch means to means for connection to said reference ground potential rail, the side of said fourth diode means remote from said fifth resistive means connected to the control electrode of said second controllable switch means and the side of said first diode means remote from said sixth resistive means connected to the control electrode of said first controllable switch means, the junction of said first and sixth controllable switch means connected to the control electrode of said fifth controllable switch means and the junction of said second and eighth controllable switch means connected to the control electrode of said seventh controllable switch means, third and fourth resistive means connecting the junctions between said fifth and sixth and said second and third diode means respectively to means for connection to said potential supply rail and means connected to the control electrodes of said third and fourth controllable switch means for connection to a pulse potential supply means for selectively enabling and disabling said third and fourth controllable switch means.

In yet a further embodiment of the invention the aforesaid controllable switch means are bipolar transistors, the diode means are diodes and the resistive means are resistors.
The invention will now be described further by way of example only and with reference to the accompanying drawings, wherein:

FIG. 1 shows a bi-directional circuit with amplification according to the prior art;

FIG. 2 shows the prior art circuit of FIG. 1 with logic gates inserted therein according to the present invention; and

FIGS. 3, 4, 5(a, b and c), 6, 7 and 8 show bus-switch circuits according to various embodiments of the invention.

Referring now to the drawings, and particularly FIG. 1 thereof, there is shown a bus line having terminals A and B and two amplifiers 10 and 11 connected in parallel and inserted in the line, amplifier 10 for amplifying data transmitted from B to A and amplifier 11 for amplifying data transmitted from A to B. Immediately it will be seen that the loop formed by these amplifiers will quickly cause oscillation, effectively blocking accurate data transmission in either direction.

In the present invention, amplifier 11 is effectively disabled while data is being transmitted from B to A and amplifier 10 is disabled while data is being transmitted from A to B. This is accomplished by inserting a logic gate 12 or 13 in series with each respective amplifier, as shown in FIG. 2. One input to logic gate 12 is connected to terminal B and the other input to a terminal C. Similarly, one input to logic gate 13 is connected to terminal A and the input to a terminal D. Terminals C and D are connected to memory means for remembering which direction data transmission has been established and for ensuring that the logic gate controlling data flow in that direction remains enabled and the logic gate controlling data flow in the opposite direction is disabled until data flow in the originally established direction ceases.

In FIG. 2, gates 12 and 13 are shown as AND gates, but they may be any of the well known logic function gates depending upon the nature of the signals applied to terminal C and D from the memory means.

In the following description logic gates are extensively involved. Therefore, before proceeding further, a definition of such gates is given at this point.

A NAND gate is one wherein a LOW output is obtained only if all inputs are HIGH — otherwise the output is HIGH. An OR gate is one wherein a HIGH output is obtained only if one or more inputs are HIGH.

A realization of the circuit of FIG. 2 is shown in FIG. 3. The amplifier 10 and gate 12 of FIG. 2 are replaced in FIG. 3 by a NAND gate G3 and an inverting inverter G5. Similarly, the amplifier 11 and gate 13 are replaced by a NAND gate G4 and an amplifying inverter G5. An enabling input signal source for gates G3 and G4 is connected to terminal T1. The third inputs of gates G3 and G4 are connected to a memory means M1, M2.

In FIG. 4, the memory means comprises a flip-flop comprising two cross-coupled inverting input OR gates G5 and G6, the output node I of G3 being connected to an input to G5 and the output node II of G4 being connected to an input to G6. The second input of inverting input OR gate G5 is connected to the output of a NAND gate G7, one input of which is connected to terminal B and the other is connected to the output of G1. The circuit operates as follows. Initially, both terminals A and B are pulled to a potential HIGH rail through resistors R1 and R4 and terminals T2 and T5. Let terminal B now be pulled to LOW condition by application of data thereto. Now G1 inputs are HIGH (derived from the output of G3) and HIGH (derived from terminal A). The output of G5 is therefore LOW, which is applied to the inverting input of G6. The output of G6 — and therefore node 1 — is HIGH, and node II is consequently LOW. The inputs to G4 are now HIGH (derived from node 1), HIGH (derived from G2) and — when T4 is fed with a HIGH enabling signal — HIGH. Therefore, an amplified LOW signal is obtained at the output of G4. Checking G6, the input derived from node II is LOW and the output is therefore HIGH — i.e., G2 is disabled.

Regardless of terminal A now going LOW, the input to G5 derived from terminal B is LOW until the condition of this terminal changes. Therefore the output from G4 remains HIGH, ensuring two HIGH inputs to G4 and ensuring a LOW output therefrom at node II. Thus, the switch maintains its transmission of data from B to A, regardless of the state of terminal A, until terminal B returns to a HIGH level.

It will be appreciated that the logic circuit of FIG. 4 may equally well be represented in terms of its logic equivalents. For example, gate G3 could be an AND gate and the input of gate G2 made non-inverting. Taking this variation further, gate G3 could have both inputs non-inverting and the output inverting, whereinupon the input to G4 connected to node I would be inverting. The second input to G4 can also be inverting if the input to G3 connected thereto is inverting and G5 is non-inverting. The third input to G4 can be inverting if the enable input from T1 is LOW instead of HIGH. Now we have three inverting inputs to G4 and an inverting output. This is, of course, by De Morgan’s theorem, an OR gate. Exactly equivalent substitutions and modifications to the remaining gates in the circuit may be made having regard to the symmetry of the circuit. Also, according to De Morgan’s theorem, the logical inverse function with HIGH and LOW states interchanged may be constructed.

FIG. 5A shows each of gates G1 to G4 inclusive of FIG. 4 in circuit block form. Each gate comprises a controllable switch means S0 having multiple inputs I1, I2, I3 . . . etc. The number of inputs provided is dependent upon the number of inputs required — i.e., G1 and G2 only have one operative input, G3 and G4 have three operative inputs and G5 to G8 inclusive have two operative inputs. All operative inputs must be HIGH before an output from S0 is obtained. The control electrode of S0 is connected through resistive means R1 to a potential supply rail PSR. The output of S0 is connected to the control electrode of a controllable switch means S10, the input of which is connected through resistive means R2 to potential supply rail PSR and the output of which is connected through resistive means R3 to reference ground potential. The output O/P from the gate is derived from the input of S10. The circuit operates as follows. When all inputs I1, I2, I3 . . . are HIGH an output is derived from S0 which enables S10. The output node O/P derived from the potential supply rail PSR and which would normally be HIGH is now pulled down to LOW condition since S10 is draining current to ground.
Therefore O/P is LOW when all of I1, I2, I3, etc. are HIGH.

The circuit of Fig. SA may be conveniently realized in two TTL (transistor-transistor-logic) forms, the first of which is shown in Fig. SB and is applicable to gates G1, G2 and G4 to G8 of Fig. 4 inclusive. Switch S6 of Fig. SA is now realized by transistor Q10, which has multiple emitters connected to inputs I1 and I2. Obviously, as many emitters as are required may be provided. The second switch means of Fig. SA is realized by the network comprising transistors Q16, Q17 and Q18 or diode D3 and resistors R3, R4, R5 and R11. When all of I1, I2, ... etc. are HIGH, an output is derived from Q18 which is applied to the base of Q16 enabling Q16. The values of resistors R3 and R5 are such that when Q16 is conducting, sufficient charge is applied to the bases of Q17 and Q18 to enable them. Now the output node is connected to the PSR rail through resistor R4 and diode D3 and to the ground rail through resistor R11. The ratio of the series combination of R3 and R4 to R5 is so chosen that in this condition, the output node will be near ground, i.e., LOW. Suppose now that any or all of I1, I2, ... etc. are LOW. Now the output from Q18 will be LOW and Q16 will be disabled. In this situation, charge will be applied to the base of Q17 and Q18 will be enabled. Clearly, Q18 will be disabled. Now, the output node swings HIGH as current is drawn from PSR through R4 and D3.

Turning now to Fig. SC, an open-collector TTL gate which may be used for switches G2 and G4 if Fig. 4 is shown. Transistors Q12, Q17 and Q18 are similar to those of Fig. SB and are likewise designated. However, bearing in mind the function of each of gates G2 and G4, is to selectively pull the nodes of respective terminals A and B LOW (see Fig. 4), the circuit of Fig. SC has an open-collector configuration for output transistor Q12. Thus, when all inputs I1, I2, ... etc. of Q12 are HIGH, Q12 is enabled and with resistors R3 and R4 appropriately ratioed Q16 is also enabled. As a result the output node O/P is connected to ground and related terminal A (for G2) or B (for G4) is also connected to ground. If now any or all of I1, I2, ... etc. are LOW, Q16 is disabled and as a result, Q18 is also disabled, thereby allowing output node O/P to rise.

Referring now to Fig. 6, a circuit in block form according to a further embodiment of the invention has terminals A and B for connection into a bus-line. Normally, each of terminals A and B is held HIGH, being pulled to the value of a potential supply rail PSR through a resistor R or R2 respectively. Terminal A is also connected through a controllable switch means S5 to a reference ground potential rail. Series connected between the potential supply rail PSR and a reference ground potential rail are a resistive means R4, a controllable switch means S4, and a controllable switch means S5 respectively. The control electrode of controllable switch means S5 connected to the junction between S1 and S2. The junction between R4 and S5 is connected through a diode means D3 to the control electrode of a controllable switch means S5. Series connected between the potential supply rail PSR and ground are respectively a resistive means R6, the controllable switch means S5 and a controllable switch means S6. The junction between R4 and S6 is connected through a diode means D1 to the control electrode of controllable switch means S1. Terminal B is connected through a controllable switch means S1 to the reference ground potential rail and the control electrode of S1 is connected to the junction of S2 and S6. The junction of D1 and R4 is connected through a controllable switch means S3 to the control electrode of S4 and the junction of R5 and D2 is connected through a controllable switch means S2 to the junction of S6. The control electrode of S6 is connected through back-to-back diodes D2 and D3 to terminal B and the control electrode of S2 is connected through back-to-back diodes D4 and D5 to terminal A. The control electrodes of S3 and S4 are also connected to an enable/disable signal supply source, designated E/E. The junction between diodes D2 and D3 is connected through resistive means R1 to the PSR rail and the junction between diodes D4 and D5 is connected to the PSR rail through resistive means R2.

Referring to Fig. 7, a realization of the circuit of Fig. 6 is shown. Again, each of terminals A and B is normally held HIGH, being pulled up to the potential supply rail PSR through a resistor R1 or R2 respectively. Typically, the potential supply rail is at +5 volts. Terminal A is also connected through the collector-emitter path of a transistor Q1 to a reference ground potential rail. The base of Q1 is connected through the emitter-collector path of a transistor Q1 to a diode D1 and one end of a resistor R1, the other end of which is connected to the potential supply rail. The base of Q1 is also connected through the collector-emitter path of a transistor Q1 to the reference ground potential rail. The base of Q1 is connected through the emitter-collector path of a transistor Q1 and a diode D1 to the base of transistor Q1. The base of transistor Q1 is connected to terminal B through back-to-back diodes D4 and D5, the junction between said diodes being connected to the potential supply rail through a resistor R1.

Terminal B is connected through the collector-emitter junction of a transistor Q2 to a reference ground potential rail. The base of Q2 is connected through the emitter-collector path of a transistor Q1 to diode D1 and one end of a resistor R1, the other end of which is connected to the potential supply rail. The base of Q1 is also connected through the collector-emitter path of a transistor Q1 to the reference ground potential rail. The base of transistor Q1 is connected through the emitter-collector path of a transistor Q3 and diode D3 to the base of transistor Q2. The base of transistor Q2 is connected through back-to-back diodes D4 and D5 to terminal A, the junction between D6 and D4 being connected to the potential supply rail through a resistor R5.

The base electrode of each of transistors Q3 and Q4 is connected to a disabling signal input E/E. This is derived from a suitable input buffer accepting standard input logic signals and delivering current outputs into Q3 and Q4 base electrodes when it is desired that no transmission of data in either direction shall occur. This current turns on Q3 and Q4 and, hence, Q4 and Q5, ensuring that Q1, Q2, Q6 and Q7 are all disabled. This inhibits transmission of data in either direction.

Suppose now however, that the disabling current is not fed to Q3 and Q4. The circuit then operates as follows. Let both the inputs at A and B be HIGH. Suppose the input B now goes LOW. Current is now drawn through resistors R3 and R4. Assume that LOW level is reference ground potential and that one diode potential drop Vb is approximately equivalent to one base-emitter potential drop in any conducting transistor, i.e., VBE. When B was HIGH, the potential at the anode of
diode $D_2$ was $3V_{BE}$ (one diode drop across $D_2$, and one $V_{BE}$ drop across each of $Q_1$ and $Q_2$). When $B$ goes LOW approaching zero the potential at the anode of $D_2$ is now only $V_B$ — i.e., the drop across $D_2$. Thus, the potential at the base of $Q_1$ is essentially at ground and $Q_1$ is therefore disabled. Thus, no potential appears at the base of $Q_2$ and $Q_4$ is disabled. Because $Q_1$ is disabled current in $R_4$ can now flow into the path comprising diode $D_3$ and the base-emitter junction of $Q_1$ and $Q_2$. Transistor $Q_2$ now conducts, pulling terminal $A$ down to reference ground potential. Since $A$ is now at reference ground potential — or LOW — the potential at the base of $Q_2$ goes to approximately ground, disabling $Q_2$ and hence $Q_3$. However, since there is still a current path through diode $D_3$ and the base-emitter junction of $Q_1$ and $Q_2$ to ground, the junction of resistor $R_5$ and the collector of $Q_1$ are only one $V_{BE}$ drop through $Q_2$ above ground potential. Thus, the potential appearing at the base of $Q_2$ is essentially zero, since there is a diode drop across $D_2$. Thus, no current path is established through $Q_2$ and $Q_4$ remains disabled, maintaining point $B$ in isolation from the reference ground potential rail. Therefore, transmission of data through the circuit from $B$ to $A$ is established regardless of the state of terminal $A$, until either a disabling signal is inputted or terminal $B$ goes HIGH again.

Turning now to FIG. 8, there is shown a further embodiment of the invention wherein the novel bidirectional bus switch is in circuit form particularly suitable for integrated circuit fabrication techniques. The circuit is similar to that of FIG. 7 and like elements in FIGS. 7 and 8 are designated by like references.

The circuit of FIG. 8 contains the following elements which do not appear in FIG. 7. Schottky diodes $SD_1$ and $SD_2$ connected between the reference ground potential rail and terminals $A$ and $B$ respectively are antiringing devices which clamp the input line to one Schottky diode drop below reference ground potential. Transistors $Q_{14}$ and $Q_{10}$ are used in place of diodes $D_3$ and $D_2$ respectively, reducing the input current required. The only input current required is the base current drive on each of $Q_{11}$ and $Q_{12}$. Transistor $Q_1$ and diode $D_3$ in FIG. 7 are replaced by transistors $Q_{14}$ and $Q_4$ in FIG. 8. Similarly, transistors $Q_{16}$ and $Q_{12}$ replace transistor $Q_2$ and diode $D_3$ in FIG. 7. The purpose of these substitutions is to provide Darlington pairs $Q_{14}$, $Q_{14}$ and $Q_{16}$, the which are faster switching, easier to fabricate in integrated — circuit form and have better gain characteristics than the transistor — diode combination. Each of resistors $R_4$, $R_{10}$, $R_{11}$ and $R_{12}$ are to ensure that the transistors with which they are associated — i.e., $Q_{14}$, $Q_{10}$, $Q_4$, and $Q_{12}$ — are more rapidly and completely disabled by pulling their base towards reference ground potential. Finally, it will be noted that the majority of the transistors used in the circuit of FIG. 8 are Schottky clamped transistors, which provide faster switching than conventional types.

Various alternatives and modifications to the embodiments disclosed herein will be readily apparent to those skilled in the art without departing from the spirit and scope of the invention as described by the disclosure and defined by the claims appended hereto.

What is claimed is:
1. A bi-directional bus switch circuit having first and second terminal means for series connection into a bus line, first amplifying gate means having input and output parts, its input part connected to said first terminal means, second logic gate means having an output part and first, second and third input parts, its second input part connected to said output part of said first amplifying gate means, enabling means and memory means for said circuit, said first and third input parts of said second logic gate means connected to said enabling means and said memory means respectively, said output part of said second logic gate means connected to said second terminal means, third amplifying gate means having first input and output parts, its input part connected to said second terminal means, fourth logic gate means having an output part and first, second and third input parts, its second input part connected to the output from said third amplifying gate means, said first and third inputs of said fourth logic gate means connected to said enabling means and said memory means respectively, said output part of said fourth logic gate means connected to said first terminal means;
2. The invention as defined in claim 1 wherein the first and third amplifying gate means are inverting gates, and wherein the second and fourth logic gate means are NAND gates.
3. The circuit of claim 2 wherein said memory means comprises seventh and eighth logic gate means each having first and second input parts, said first input part of said seventh logic gate means connected to said first terminal means and said second input part of said seventh logic gate means connected to said second input part of said fourth NAND gate means, said first input part of said eighth logic gate means connected to said second terminal means and said second input part of said eighth logic gate means connected to said second input part of said NAND gate means, said memory means also comprises a fifth and sixth logic gate means cross connected as a storage element or flip-flop, the output part of said seventh logic gate means connected to a first input part of the fifth logic gate means, the output part of said fifth logic gate means connected to a second input part of the sixth logic gate means, said sixth logic gate means having its output part connected to a second input part of said fifth logic gate means and said sixth logic gate means having a first input part connected to the output part of said eighth logic gate means, the output parts of said fifth and sixth logic gate means being connected to the third input parts of said fourth and second NAND gate means respectively;
4. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are OR gates with inverting input parts.
5. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are AND gates with inverting input parts.

6. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are NAND gates.

7. The circuit as defined in claim 3 wherein the seventh and eighth logic gate means are NAND gates and wherein the fifth and sixth logic gate means are NOR gates.

8. The invention as defined in claim 2 wherein said memory means comprises seventh and eighth logic gate means, each having first and second input parts, said first input part of said seventh logic gate means connected to said first terminal means and said second input part of said seventh logic gate means connected to said second input part of said fourth NAND gate means, said first input part of said eighth logic gate means connected to said second terminal means and said second input part of said eighth logic gate means connected to said second input part of said second NAND gate means, said memory means also comprises a fifth and a sixth logic gate means cross connected as a storage element or flip-flop, the output part of said seventh logic gate means connected to a first input part of the fifth logic gate means, the output part of said fifth logic gate means connected to a second input part of the sixth logic gate means, said sixth logic gate means having its output part connected to a second input part of said fifth logic gate means and said sixth logic gate means having a first input part connected to the output part of said eighth logic gate means, the output parts of said fifth and sixth logic gate means being connected to the third input parts of said second and fourth NAND gate means respectively.

9. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are NOR gates.

10. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are NAND gates.

11. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are OR gates with inverting input parts.

12. The circuit as defined in claim 8 wherein the seventh and eighth logic gate means are AND gates and wherein the fifth and sixth logic gate means are AND gates with inverting input parts.

13. The invention as defined in claim 1 wherein the first and third amplifying gate means are non-inverting gates, and wherein the second and fourth logic gate means are NOR gates.

14. A bi-directional bus switch circuit comprising first and second terminal means for series connection into a bus-line, each of said first and second terminal means resistively coupled to means for connection to a power supply rail, said first terminal means connected through a fifth controllable switch means to means for connection to a reference ground potential rail and said second terminal means connected through a seventh controllable switch means to means for connection to said reference ground potential rail, fifth and sixth diode means series connected between said first terminal means and the control electrode of a third controllable switch means, second and third diode means series connected between said second terminal means and the control electrode of a fourth controllable switch means, fifth resistive means connected between means for connection to said potential supply rail and fourth diode means, the junction between said fifth resistive means and said fourth diode means being connected through said third controllable switch means to the control electrode of an eighth controllable switch means, said junction between said fifth resistive means and said fourth diode means being further connected through first and sixth controllable switch means to means for connection to said reference ground potential rail, sixth resistive means connected between means for connection to said potential supply rail and first diode means, the junction between said sixth resistive means and said first diode means being connected through said fourth controllable switch means to the control electrode of said sixth controllable switch means, said junction between said sixth resistive means and said first diode means being further connected through second and said eighth controllable switch means to means for connection to said reference ground potential rail, the side of said fourth diode means remote from said fifth resistive means connected to the control electrode of said second controllable switch means and the side of said first diode means remote from said sixth resistive means connected to the control electrode of said first controllable switch means, the junction of said first and sixth controllable switch means connected to the control electrode of said fifth controllable switch means and the junction of said second and eighth controllable switch means connected to the control electrode of said seventh controllable switch means, third and fourth resistive means connecting the junctions between said fifth and sixth and said second and third diode means respectively to means for connection to said potential supply rail and means connected to the control electrodes of said third and fourth controllable switch means for connection to a pulse potential supply means for selectively enabling and disabling said third and fourth controllable switch means.

15. The circuit of claim 14 wherein said controllable switch means are bipolar transistors.

16. The circuit of claim 14 wherein said diode means are diodes.

17. The circuit of claim 14 wherein said resistive means are resistors.