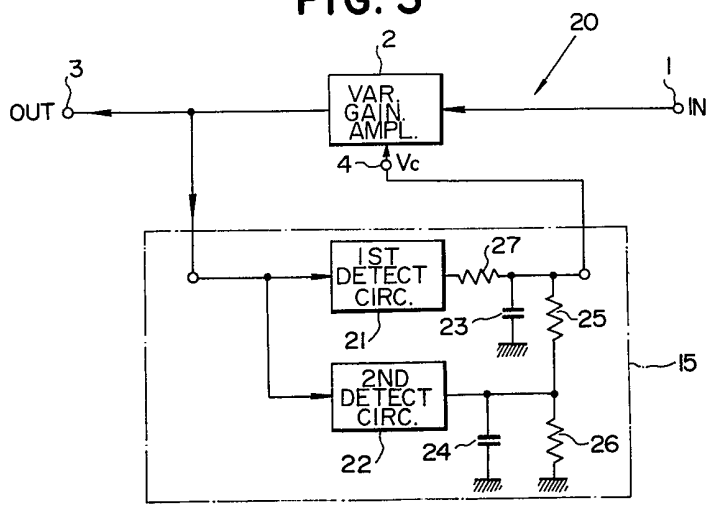
(12) UK Patent Application (19) GB (11) 2 073 977 A

(21) Application No **8108811**
(22) Date of filing **20 Mar 1981**
(30) Priority data
(31) **55/037112**
(32) **24 Mar 1980**
(33) **Japan (JP)**
(43) Application published
21 Oct 1981
(51) **INT CL³**
H03G 3/20
(52) Domestic classification
H3G 11X PT
(56) Documents cited
GB 1436627
GB 1424082
GB 1424081
GB 1217491
GB 1190763
GB 1172310
GB 1168212
GB 1149891
GB 961131
GB 807780
GB 642731
GB 640920
(58) Field of search
H3G
(71) Applicants
Sony Corporation,
7-35 Kitashinagawa-6,
Shinagawa-ku,
Tokyo,
Japan.
(72) Inventors
Kenzo Akagiri,
Masayuki Katakura.
(74) Agents
D. Young & Co.,
10 Staple Inn,
London WC1V 7RD.

(54) **Gain control circuits**

(57) A gain control circuit 20, which has particular utility in a compressor or expander of a noise reduction circuit, comprises first and second detectors 21, 22 for detecting the output signal from a variable gain amplifier 2 and providing respective detector outputs for charging first and second capacitors 23, 24, respectively. The first and second capacitors 23, 24 have discharge paths in which first and second resistors 25, 26 are respectively interposed, and the charge on the first capacitor 23 is employed as a control signal for determining the gain of the variable gain amplifier 2. Moreover, the first resistor 25 is connected between the first and second capacitors 23, 24 so that the discharge current through the first resistor 25 is dependent on the difference between the charge voltages on the first and second capacitors 23, 24, whereby a relatively long recovery time can be obtained without adversely affecting the attack time even when the input signal to the variable gain amplifier 2 is of low level.

FIG. 3



GB 2 073 977 A

FIG.1

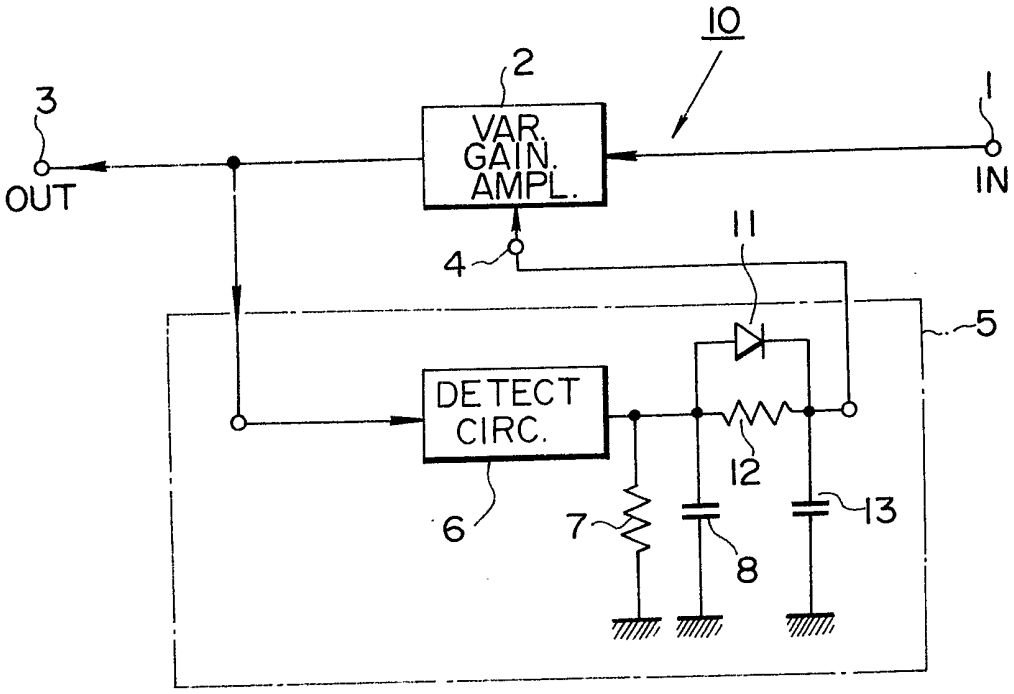
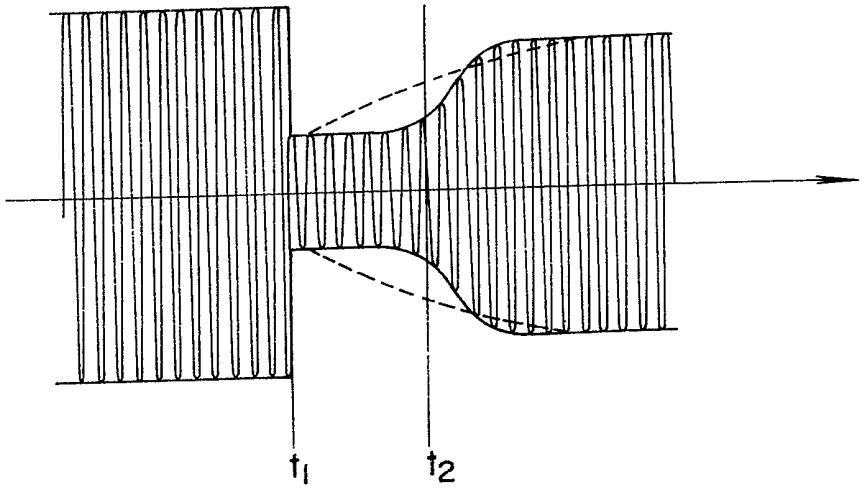


FIG.2



2073977

FIG. 3

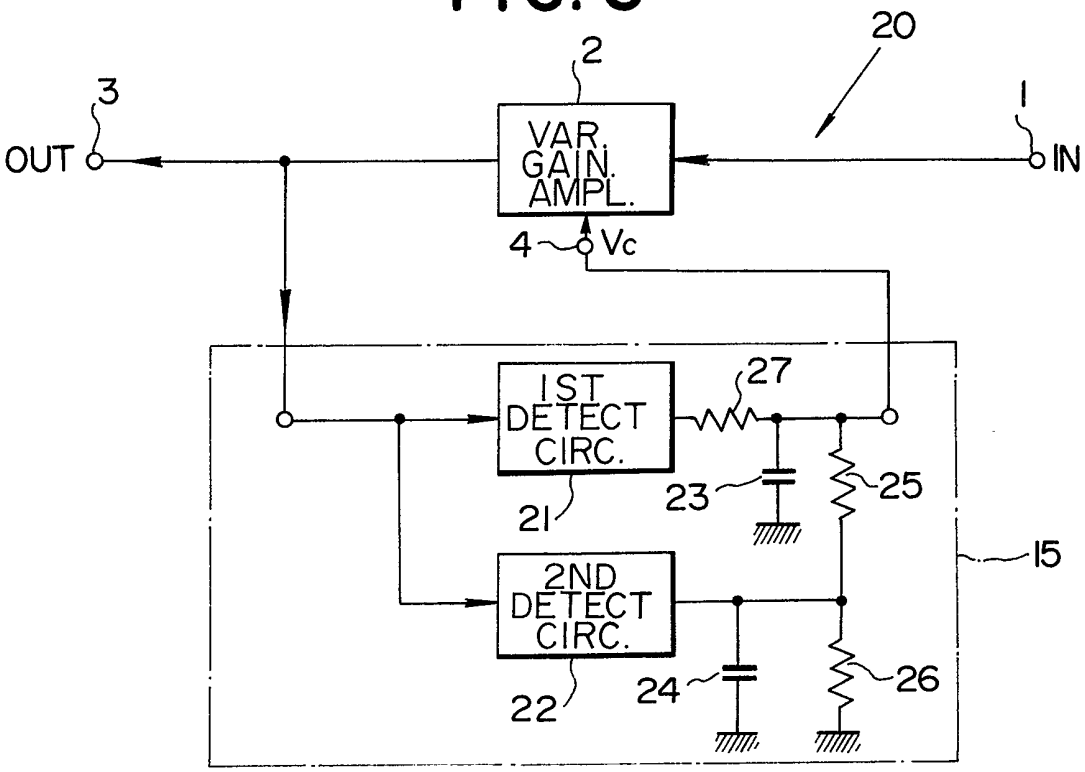
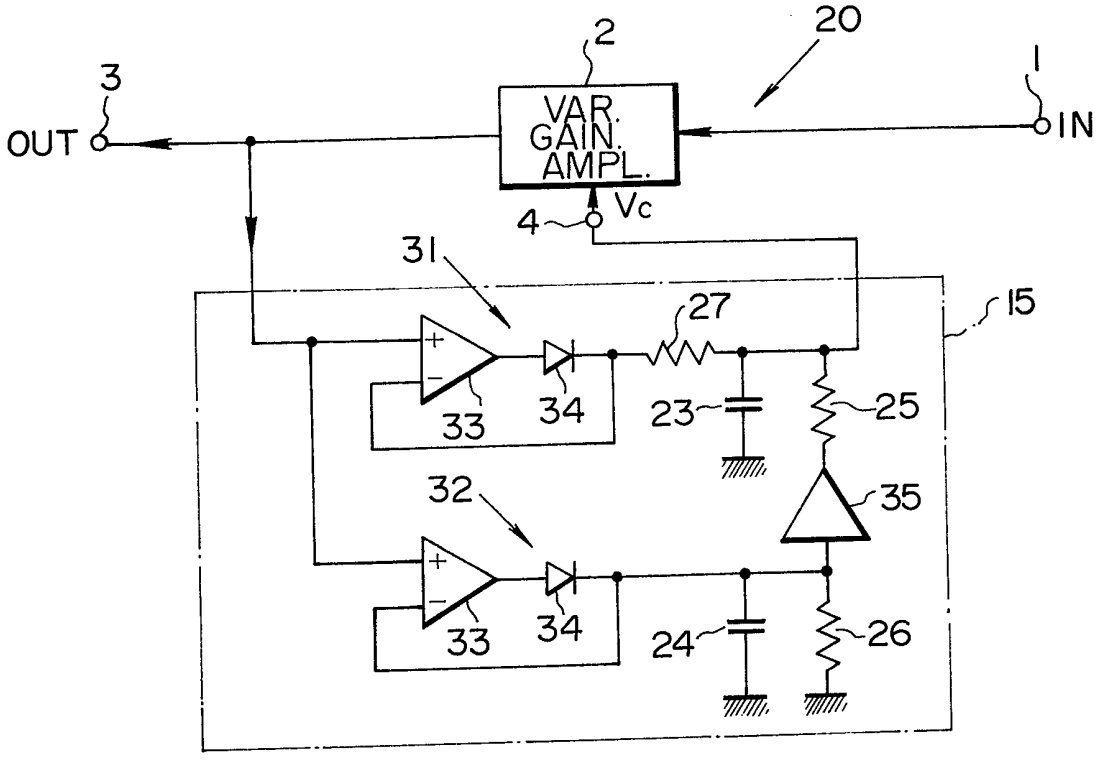


FIG. 4



2073977

FIG.5

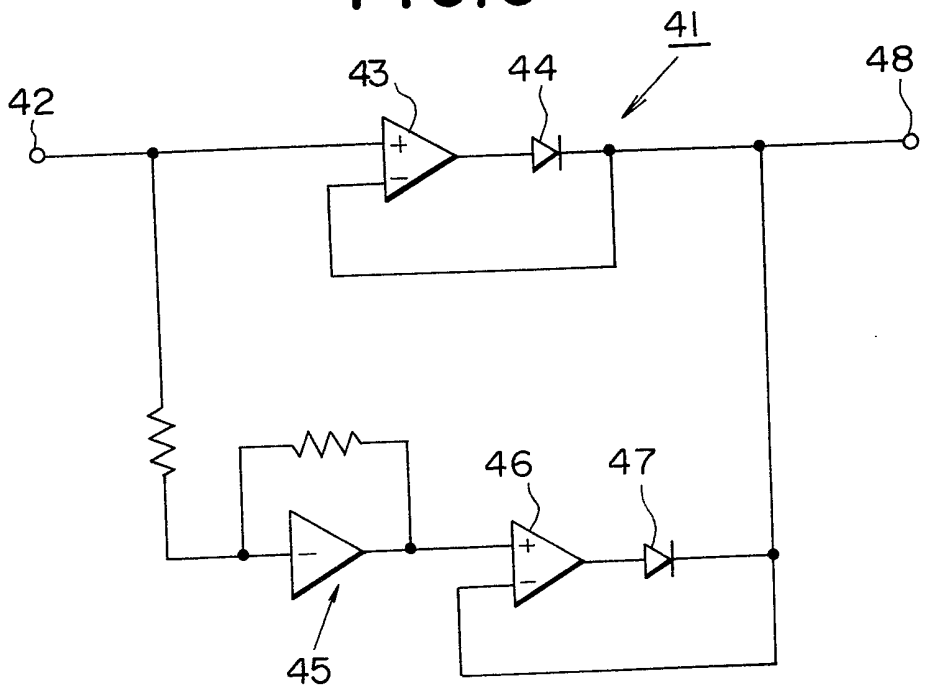


FIG.6A

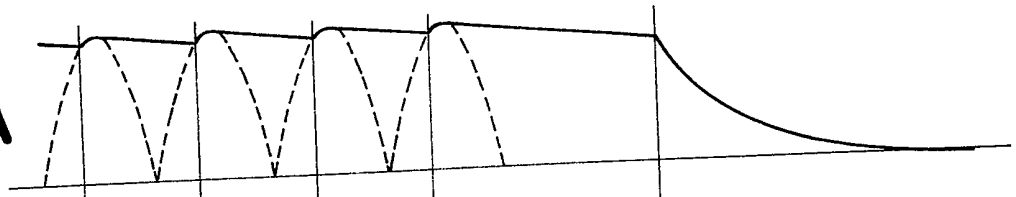


FIG.6B

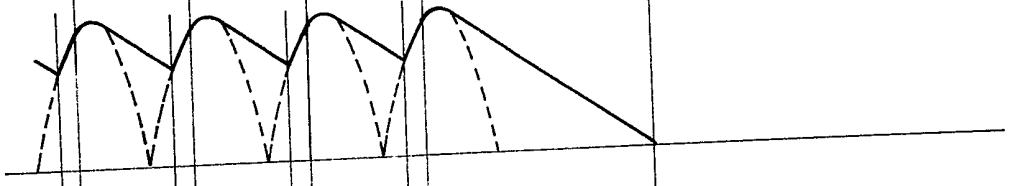


FIG.6C

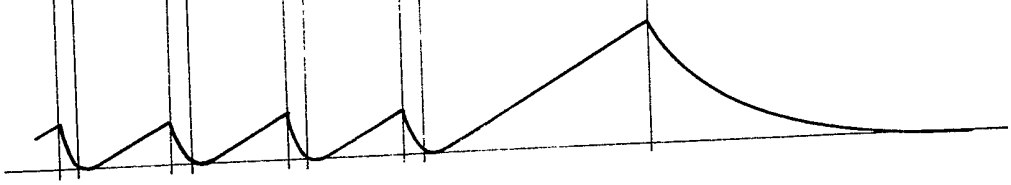
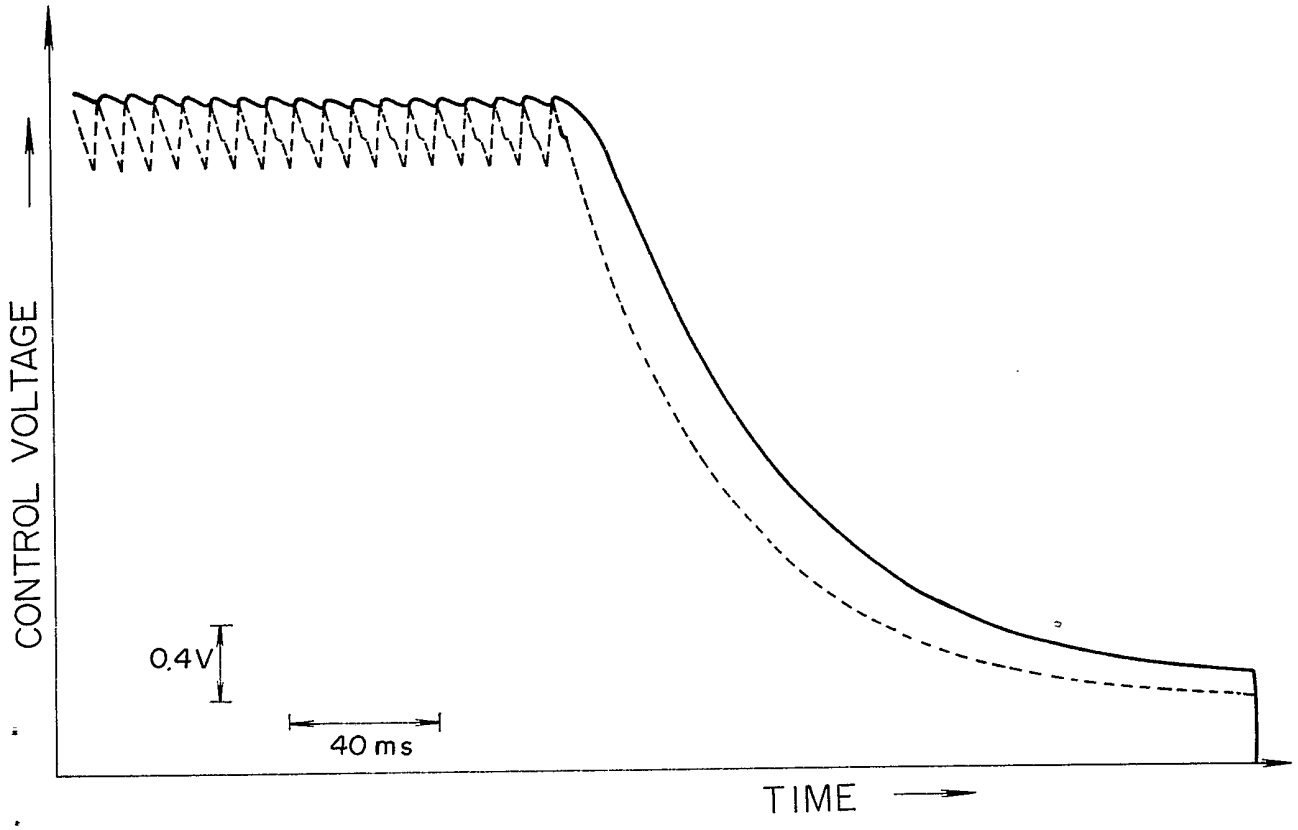


FIG.7



SPECIFICATION

Gain control circuits

This invention relates to gain control circuits. Embodiments of the invention are particularly, but not exclusively, suitable for use in compressors or expanders of noise reduction circuits.

Gain control circuits have been previously proposed in which the gain of a variable gain amplifier is automatically controlled by a gain control signal so as to decrease or increase the gain upon an increase or decrease, respectively, in the level of an input signal applied to the amplifier. In existing automatic gain control (AGC) circuits a detector senses the output signal from the variable gain amplifier and provides a detector output coupled, through a two-stage resistance capacitance (RC) circuit, to a control terminal of the amplifier. The two-stage RC circuit includes a first resistor and a first capacitor connected in parallel between the detector output and ground, a diode and a second resistor connected in parallel between the output side of the first capacitor and the control terminal of the variable gain amplifier, and a second capacitor connected between this control terminal and ground. In the operation of this gain control circuit, in the case of its recovery mode, for example, when the input signal to the variable gain amplifier changes suddenly from a high level to a low level, the first and second capacitors, which have been previously changed by the relatively high output of the detector, are discharged in sequence through the first and second resistors in response to the reduction of the detector output. More particularly, when the level of the input signal to the variable gain amplifier suddenly decreases, the control signal for varying the gain of the amplifier is changed only gradually for a period of time and, thereafter, the control signal is quickly reduced to increase the gain of the amplifier and quickly restore the level of the output signal therefrom. In the attack mode of this gain control circuit, that is, when the level of the input signal to the variable gain amplifier is increased quickly, it is intended that the diode is made conductive by the increase of the detector output so that the second capacitor is charged quickly similarly to increase the control signal and thereby achieve a fast attack time.

However, the fast attack time is achieved only when the input signal is increased suddenly from a substantial initial level. In other words, if there is a rapid increase in the input signal from a low level, then it is likely that the output voltage from the detector will be too low and make the diode conductive and, in such case, the second capacitor willbe charged relatively slowly through the second resistor. Therefore, with the described gain control circuit, in the case of a relatively low level input signal, the attack time may be as slow as several hundred milliseconds. Such a slow attack time will result in overshoots in the output signal from the variable gain amplifier and limitations are thereby imposed on the applications of the described gain control circuit.

According to the present invention there is provided a gain control circuit including a variable gain amplifier having input, output and control terminals, and control means for generating a control signal to be supplied to said control terminal for controlling the gain with which said variable gain amplifier amplifies an input signal supplied to said input terminal for providing an output signal to said output terminal, said control means comprising:

first and second detector circuits for detecting said output signal and providing respective first and second detector outputs;

first and second capacitors coupled at one side to said first and second detector circuits so as to be chargeable by said first and second detector outputs, respectively,

said one side of said first capacitor being coupled to said control terminal of the variable gain amplifier so that the charge on said first capacitor forms said control signal;

first and second resistors coupled to said first and second capacitors, respectively, for the discharge of said first and second capacitors through said first and second resistors, respectively; and

means coupling said first resistor between said one sides of said first and second capacitors.

According to the present invention there is also provided a gain control circuit including a variable gain amplifier having input, output and control terminals, and control means for generating a control signal to be supplied to said control terminal for controlling the gain with which said variable gain amplifier amplifies an input signal supplied to said input terminal for providing an output signal to said output terminal, said control means comprising:

first and second detector circuits for detecting said output signal from said variable gain amplifier means and providing respective first and second detector outputs;

a first smoothing circuit for smoothing said first detector output and including a first capacitor and a first resistor, said first smoothing circuit having an output coupled to said control terminal as said control signal; and second smoothing circuit for smoothing said second detector output and including a second capacitor and a second resistor, said second smoothing circuit having an output coupled to one end of said first resistor so that the discharge time constant of said first capacitor is varied in accordance with said second detector output.

The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram showing a previously proposed gain control circuit;

Figure 2 is a graph showing variations, with time, of the output signal from the gain control circuit of Figure 1 in the recovery mode thereof;

Figure 3 is a circuit diagram, similar to that of Figure 1, but showing an embodiment of the invention;

Figure 4 is a circuit diagram showing another embodiment of the invention, and further showing details of detector circuits that may be used in gain control circuits according to the invention;

Figure 5 is a circuit diagram showing details of

another form of detector circuit that may be used in gain control circuits according to the invention;

Figures 6a to *6C* are waveform diagrams to which reference will be made in explaining the operation of the gain control circuit of Figure 3; and

Figure 7 is a graph illustrating variations of the control voltage with time in a gain control circuit according to the invention.

To assist understanding of the ebodiments reference will first be made to Figure 1 which shows a previously proposed gain control circuit 10 including an input terminal 1 from which an input signal is supplied to a variable gain amplifier 2 having an output terminal 3 for supplying the amplified signal and a control terminal 4 for receiving, from a control circuit 5, a control signal by which the gain of the variable gain amplifier 2 is suitably varied. More particularly, the control signal from the control circuit 5 is effective to increase or decrease the gain of the variable gain amplifier 2 upon a decrease or increase, respectively, in the level of the input signal supplied to the input terminal 1. In the control circuit 5, a detector 6 detects the output signal from the variable gain amplifier 2 and provides a detector output which is coupled through a two-stage RC circuit to the control terminal 4. The two-stage RC circuit includes a first resistor 7 and a first capacitor 8 connected, in parallel, between the output of the detector 6 and ground, a diode 11 and a second resistor 12 connected, in parallel, between the output side of the capacitor 8, that is, the side connected to the output of the detector 6, and the control terminal 4, and a second capacitor 13 connected between the control terminal 4 and ground.

In the operation of the gain control circuit 10, the capacitors 8 and 13 are charged by the output of the detector 6 in response to the output signal from the variable gain amplifier 2. In the event of a sudden change of the input signal supplied to the input terminal 1 from a high level to a low level, that is, in the recovery mode of the gain control circuit 10, the output of the detector 6 is reduced to signal the reduction in the level of the output signal from the variable gain amplifier 2, and the capacitors 8 and 13 are discharged through the resistors 7 and 12 upon the reduction of the output of the detector 6. However, in such discharging of the capacitors 8 and 13, the capacitor 8 is first discharged through the resistor 7 to ground, and the capacitor 13 is discharged through the resistor 12 and the resistor 7 to ground only after the capacitor 8 has been discharged to a predetermined extent. It will be appreciated that, until the capacitor 8 is discharged to this predetermined extent, the terminal voltage across the resistor 12 will be low and the discharge current from the capacitor 13 through the resistor 12 will be correspondingly low. Thus, the control voltage supplied to the control terminal 4 is only gradually reduced until the capacitor 8 has been discharged beyond the predetermined extent, whereupon the capacitor 13 is relatively quickly discharged for similarly reducing the control signal supplied to the terminal 4 of the variable gain amplifier 2.

Thus, by way of example, and as shown in Figure 2, if the level of the input signal supplied to the input terminal 1 is suddenly reduced at a time t_1, the output signal from the output terminal 3 is only gradually restored by a correspondingly gradual increase in the gain of the amplifier 2 until, at a time t_2 which is a predetermined period after the time t_1, the control voltage supply by the control circuit 5 to the control terminal 4 is quickly reduced rapidly to increase the gain of the amplifier 2 and thereby similarly rapidly restore the output signal. If a single-stage RC circuit is used between the output of the detector 6 and the control terminal 4 in place of the two-stage RC circuit of Figure 1, the level of the output signal from the amplifier 2 will change exponentially, as indicated by the broken line curve in Fiure 2, in the recovery mode of the gain control circuit 10.

In the attack mode of the gain control circuit 10 of Figure 1, that is, when the level of the input signal supplied to the input terminal 1 is quickly increased, it is intended that the diode 11 should be made conductive by the resulting increase in the output voltage of the detector 6, with the result that the capacitor 13 is quickly charged through the conductive diode 11 for effecting a correspondingly quick decrease in the gain of the amplifier 2, that is, for obtaining a fast attack time. However, if the quick increase in the level of the input signal supplied to the input terminal 1 occurs from a low initial signal level, it is likely that the resulting output voltage from the detector 6 will not be sufficiently high to cause the diode 11 to become conductive. In such case, the capacitor 13 can be charged only relatively slowly through the resistor 12 in response to the increased output voltage of the detector 6. Therefore, with the gain control circuit 10 of Figure 1, in the case of a low level input signal, the attack time will be relatively slow, for instance several hundred milliseconds, which results in overshoots in the output signal, thereby limiting the possible applications of the gain control circuit 10 particularly in compresors or expanders of noise reduction circuits.

Referring now to Figure 3, it will be seen that an embodiment of a gain control circuit 20 according to the invention, has its components which correspond to those described previously with reference to Figure 1 identified by the same reference numerals. The variable gain amplifier 2 of the gain control circuit 20 may be a voltage controlled amplifier or any other well known amplifier circuit which need not be described in detail, and which has its gain varied in response to the voltage of a control signal v_c supplied to the control terminal 4 from a control circuit 15. If the gain control circuit 20 is used as an AGC circuit for a compressor in a noise reduction system, the variable gain amplifier 2 is suitably arranged so that its gain G is related to the control voltage v_c obtained by rectifying and smoothing the output signal from the output terminal 3 in accordance with the equation:

$$G = k/v_c \text{ or } G = Ke^{-v_c}$$

Thus, automatic gain control or signal compression is obtained with the gain G being decreased or

increased upon and increase or decrease, respectively, in the level of the signal supplied to the input terminal 1.

In the control circuit 15, the output signal from the output terminal 3 of the gain control circuit 20 is detected by first and second detector circuits 21 and 22. The control circuit 15 further includes first and second capacitors 23 and 24, and first and second resistors 25 and 26. More particularly, the output from the first detector circuit 21 is shown to be coupled through an additional resistor 27 to the control terminal 4 of the variable gain amplifier 2, and the junction between the resistor 27 and the control terminal 4 is connected to one side of the capacitor 23 which has its other side connected to ground. The resistor 25 is connected in parallel with the capacitor 23 to the junction between the resistor 27 and the control terminal 4 so that the capacitor 23 is charged by the output of the first detector circuit 21 and discharged through the resistor 25, and further so that the charge on the capacitor 23 forms the control voltage or signal v_c supplied to the terminal 4 for determining the gain of the variable gain amplifier 2. One side of the capacitor 24 is connected to the output of the second detector circuit 22 while the other side of the capacitor 24 is connected to ground so that the capacitor 24 is chargeable by the output of the second detector circuit 22. The resistor 26 is connected in parallel with the capacitor 24 so that the capacitor 24 can be discharged to ground through the resistor 26.

The capacitor 23 and the resistor 25 function as a first smoothing circuit for smoothing the output of the first detector circuit 21, and the output of this first smoothing circuit obtained at the side of the capacitor 23 connected to the first detector circuit 21, that is, the non-grounded or output side of the capacitor 23, is connected to the control terminal 4. Similarly, the capacitor 24 and the resistor 26 form a second smoothing circuit for smoothing the output of the second detector circuit 22, and the output of this second smoothing circuit obtained at the non-grounded or output side of the capacitor 24 is connected to the end of the resistor 25 remote from the end thereof connected to the capacitor 23. In other words,the resistor 25 is connected between the output sides of the capacitors 23 and 24 which are connected to the outputs of the detector circuits 21 and 22, respectively. By reason of the foregoing, the discharge time constant of the first capacitor 23 is varied in accordance with the output of the second detector circuit 22.

If it is desired to avoid the occurrence of a large transient current through the second detector circuit 22, a resistor (not shown) may be connected between the output of the second detector circuit 22 and the junction of the capacitor 24 and the resistor 26 similarly to the resistor 27 connected between the output of the first detector circuit 21 and the junction of the capacitor 23 and the resistor 25.

The first and second detector circuits 21 and 22 are preferably active detector circuits. For example, they may be constructed similarly to the first and second detector circuits 31 and 32 illustrated in Figure 4. More particularly, each of the active detector circuits 31 and 32 is shown in Figure 4 to include an operational amplifier 33 having a positive input connected to receive the output signal from the variable gain amplifier 2, a negative input and an output from the operational amplifier 33, a diode 34 connected to the output of the operational amplifier 33, and a negative feedback path from the output of the diode 34 to the negative input of the operational amplifier 33. As in the embodiment of Figure 4, the control circuit 15 may include a buffer amplifier 35 connected between the output of the second detector circuit 32 and the resistor 25.

Referring now to Figure 5, it will be seen that a detector circuit 41 of a full-wave rectifying type which may be employed for each of the first and second detector circuits 21 and 22 of Figure 3 or in place of each of the first and second detector circuits 31 and 32 Figure 4 includes an operational amplifier 43 and diode 44 connected to each other in the same manner as the operational amplifier 33 and diode 34 in Figure 4, with the positive input of the operational amplifier 43 being connected to a terminal 42 which receives the output signal from a variable gain amplifier, for example, the amplifier 2 in Figures 3 or 4. The output signal supplied to the terminal 42 from a variable gain amplifier is also supplied through an inverter 45 to a positive input of another operational amplifier 46, and a diode 47 is connected to the output of the operational amplifier 46 and has its output, in turn, supplied as a negative feedback to a negative input of the operational amplifier 46. The outputs of the diodes 44 and 47 are further shown to be connected together to a terminal 48 which is connected either through the resistor 27 to the non-grounded side of the capacitor 23 or to the non-grounded side of the capacitor 24, as shown in Figures 3 and 4.

In the operation of the gain control circuit 20, the capacitors 23 and 24 are charged by the outputs of the first and second detector circuits 21 and 22 or 31 and 32, respectively, in response to the output signal from the variable gain amplifier 2. In the event of a sudden change of the input signal supplied to the input terminal 1, for example, from a high level to a low level, that is, in the recovery mode of the gain control circuit 20, the outputs of the first and second detector circuits 21 and 22 or 31 and 32 are reduced to signal the reduction in the level of the output signal from the amplifier 2, and the capacitors 23 and 24 are discharged through the resistors 25 and 26 and the resistor 26, respectively. However, in such discharging of the capacitors 23 and 24, the capacitor 23 is discharged through the resistor 25 and the resistor 26 only after substantial discharge of the capacitor 24 through the resistor 26. This is because the voltage or charge on the capacitor 24 is supplied to the end of the resistor 25 connected through the resistor 26 to ground. Thus, the terminal voltage across the resistor 25 is initially low, with the result that the discharge current from the capacitor 23 through the resistor 25 is initially very small so as to cause a gradual decrease in the control signal voltage v_c supplied from the capacitor 23 to the control terminal 4. However, as the capacitor 24 is progressively discharged, the terminal voltage

across the resistor 25 is increased for correspondingly increasing the dischage current from the capacitor 23 and thereby quickly reducing the control voltage v_c supplied to the control terminal 4 and correspondingly quickly increasing the gain of the variable gain amplifier 2.

If the full-wave rectifying detector circuit 41 of Figure 5 is used for each of the first and second detector circuits 21 and 22 of Figure 3, then the outputs thereof are substantially represented by the broken line curves in Figures 6A abd 6B, respectively, and the voltages or charges on the capacitors 23 and 24 are represented by the curves in solid lines in Figures 6A and 6B, respectively. In such case, the terminal voltage across the resistor 25 is the difference between the voltages indicated by the solid line curves in Figures 6A and 6B, and is represented by the curve shown in Figure 6C.

Referring now to Figure 7, it is to be noted that the curve shown in solid lines thereon represents the control voltage v_c supplied from the control circuit 15 to the control terminal 4 of the variable gain amplifier 2 when a tone burst signal having a carrier frequency of 100 Hz is supplied to the control circuit 15, and when the time constant of the RC parallel circuit comprising the capacitor 23 and the resistor 25 is 100 milliseconds, and the time constant of the RC parallel circuit comprising the capacitor 24 and the resistor 26 is 20 milliseconds. The curve shown in borken lines in Figure 7 is given by way of reference and represents the control voltage obtained from the control circuit 15 in the even that the capacitor 25 and the resistor 26 are omitted.

It will be seen from Figure 7 that, in the gain conrol circuits 20, control signal ripple is extremely small even when the input signal frequency is as low as about 100 Hz, so that it is possible to obtain steady gain control free from waveform distortions. Moreover, the recovery time can be relatively short, typically about 100 milliseconds, which is comparable with that obtained when using a single-stage RC circuit.

Moreover, in the attack mode, the outputs of the first and second detector circuits 21 and 22 or 31 and 32 quickly charge the respective capacitors 23 and 24, so that the attack time is determined substantially by the time constant of the circuit comprising the resistor 27 and the capacitor 23, which time constant can readily be made very short, for example, about 300 to 500 microseconds. Moreover, in the attack mode, the operating characteristics are determined solely by the RC circuit elements associated with the first detector circuit 21 or 31 so that normal operation can be ensured in the attack mode even when a low level signal is being supplied to the input terminal 1.

When a buffer amplifier 35 is employed in the connection of the resistor 25 to the capacitor 24, as shown in Figure 4, the buffer amplifier 35 serves to prevent the flow into the capacitor 24 of the discharge current flowing from the capacitor 23 through the resistor 25 when the output voltage of the capacitor 24 has been reduced. Thus, the buffer amplifier 35 prevents unnecessary extension of the recovery time of the gain control circuit.

It will be appreciated from the foregoing that it is possible to provide gain control circuits which eliminate the described disadvantages of the previously proposed gain control circuits, such as extension of the attack time and limitations upon the input level range. Moreover, gain control circuits can be made substantially free of ripple, even when an input signal of a low frequency is supplied, and such gain control circuits are further able to have a recovery time as short as about 100 milliseconds.

CLAIMS

1. A gain control circuit including a variable gain amplifier having input, output and control terminals, and control means for generating a control signal to be supplied to said control terminal for controlling the gain with which said variable gain amplifier amplifies an input signal supplied to said input terminal for providing an output signal to said output terminal, said control means comprising:

first and second detector circuits for detecting said output signal and providing respective first and second detector outputs;

first and second capacitors coupled at one side to said first and second detector circuits so as to be chargeable by said first and second detector outputs, respectively,

said one side of said first capacitor being coupled to said control terminal of the variable gain amplifier so that the charge on said first capacitor forms said control signal;

first and second resistors coupled to said first and second capacitors, respectively, for the discharge of said first and second capacitors through said first and second resistors, respectively; and

means coupling said first resistor between said one sides of said first and second capacitors.

2. A gain conrol circuit according to claim 1 further comprising means for providing said first capacitor with a discharge time constant which is larger than the discharge time constant of said second capacitor.

3. A gain control circuit according to claim 2 wherein said means providing said first capacitor with said longer discharge time constant includes an additional resistor coupled between said first detector output and said one side of said first capacitor.

4. A gain control circuit according to claim 3 wherein said means coupling said first resistor between said one sides of said first and second capacitors includes a buffer amplifier coupled between said first resistor and said one side of said second capacitor.

5. A gain control circuit according to claim 4 wherein each of said first and second detector circuits includes an operational amplifier having a positive input connected to receive said output signal from the variable gain amplifier, a negative input and an output from said operational amplifier, diode means connected to said output of said operational amplifier, and a negative feedback path from the output of said diode means to said negative input of said operational amplifier.

6. A gain control circuit according to claim 5

wherein each of said first and second detector circuits includes another operational amplifier having positive and negative inputs and an output, an inverter through which said output signal from said variable gain amplifier is supplied to said positive input of said other operational amplifier, another diode means coupled to said output of said other operational amplifier, and a negative feedback path from the output of said other diode means to said negative input of said other operational amplifier, said output of said other diode means being coupled in parallel with the output of the first-mentioned diode means to form the respective detector output.

7. A gain control circuit according to claim 1 wherein said means connecting said first resistor between said one sides of said first and second capacitors includes buffer amplifier means coupled between said first resistor and said one side of said second capacitor.

8. A gain control circuit according to claim 1 wherein each of said first and second detector circuits includes an operational amplifier having a positive input to receive said output signal from said variable gain amplifier, a negative input and an output from said operational amplifier, diode means coupled to said output of said operational amplifier, and a negative feedback path from the output of said diode means to said negative input of said operational amplifier.

9. A gain control circuit according to claim 8 wherein each of said first and second detector circuits includes another operational amplifier having positive and negative inputs and an output, inverter means through which said output signal from said variable gain amplifier means is supplied to said positive input of said other operational amplifier, another diode means connected to said output of said other operational amplifier, and a negative feedback path from the output of said other diode means to said negative input of said other operational amplifier, said output of said other diode means being conncted in parallel with the output of the first-mentioned diode means to form the respective detector output.

10. A gain control circuit including a variable gain amplifier having input, output and control terminals, and control means for generating a control signal to be supplied to said control terminal for controlling the gain with which said variable gain amplifier amplifies an input signal supplied to said input terminal for providing an output signal to said output terminal, said control means comprising:

first and second detector circuits for detecting said output signal from said variable gain amplifier means and providing respective first and second detector outputs;

a first smoothing circuit for smoothing said first detector output and including a first capacitor and a first resistor, said first smoothing circuit having an output coupled to said control terminal as said control signal; and a second smooothing circuit for smoothing said second detector output and including a second capacitor and a second resistor, said second smoothing circuit having an output coupled to one end of said first resistor so that the discharge time constant of said first capacitor is varied in accordance with said second detector output.

11. A gain control circuit according to claim 10 further comprising means for providing said first capacitor with a discharge time constant which is larger than the discharge time constant of said second capacitor.

12. A gain control circuit according to claim 11 wherein said means providing said first capacitor with said longer discharge time constant includes an additional resistor coupled between said first detector output and said one side of said first capacitor.

13. A gain control circuit according to claim 10 further comprising buffer amplifier means coupled between said one end of said first resistor and said second capacitor.

14. A gain control circuit according to claim 10 wherein each of said first and second detector means includes an operational amplifier having a positive input coupled to receive said output signal from the variable gain amplifier means, a negative input and an output from said operational amplifier, diode means coupled to said output of said operational amplifier, and a negative feedback path from the output of said diode means to said negative input of said operational amplifier.

15. A gain control circuit according to claim 14 wherein each of said first and second detector circuits includes another operational amplifier having positive and negative inputs and an output, inverter means through which said output signal from said variable gain amplifier means is supplied to said positive input of said other operational amplifier, another diode means coupled to said output of said other operational amplifier, and a negative feedback path from the output of said other diode means to said negative input of said other operational amplifier, said output of said other diode means being coupled in parallel with the output of the first-mentioned diode means to form the respective detector output.

16. A gain control circuit substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

17. A gain control circuit substantially as hereinbefore described with reference to Figure 4 of the accompanying drawings.

18. A gain control circuit substantially as hereinbefore described with reference to Figure 3 as modified by Figure 5 of the accompanying drawings.

19. A gain control circuit substantially as hereinbefore described with reference to Figure 4 as modified by Figure 5 of the accompanying drawings.

Printed for Her Majesty's Stationery Office by Croydon Printing Company Limited, Croydon, Surrey, 1981.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.