



(11)

EP 4 310 824 A1

(12)

EUROPEAN PATENT APPLICATION
published in accordance with Art. 153(4) EPC

(43) Date of publication:
24.01.2024 Bulletin 2024/04

(51) International Patent Classification (IPC):
G09G 3/32 ^(2016.01)

(21) Application number: **22791953.7**

(52) Cooperative Patent Classification (CPC):
G09G 3/32

(22) Date of filing: **13.04.2022**

(86) International application number:
PCT/KR2022/005366

(87) International publication number:
WO 2022/225253 (27.10.2022 Gazette 2022/43)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(30) Priority: **23.04.2021 KR 20210053216**

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(54) **ELECTRONIC DEVICE COMPRISING DISPLAY, AND OPERATION METHOD THEREFOR**

(57) An electronic device comprises: a sub-pixel including a first circuit block, a second circuit block, and a light-emitting element; a display panel; a display driving circuit; and a processor, wherein the display driving circuit can store gradation data in a first gate terminal of a first output transistor in the first circuit block, input, into the first gate terminal, a control signal of which the potential varies with time, allow the voltage of a second gate

terminal of a second output transistor in the second circuit block to vary in response to the input of the control signal, control a light-emitting time by adjusting an on-state time of the second output transistor, and use a second initialization transistor connected to the second gate terminal to apply an initialization voltage to the second gate terminal two or more times for one frame, and thus perform initialization two or more times.

EP 4 310 824 A1

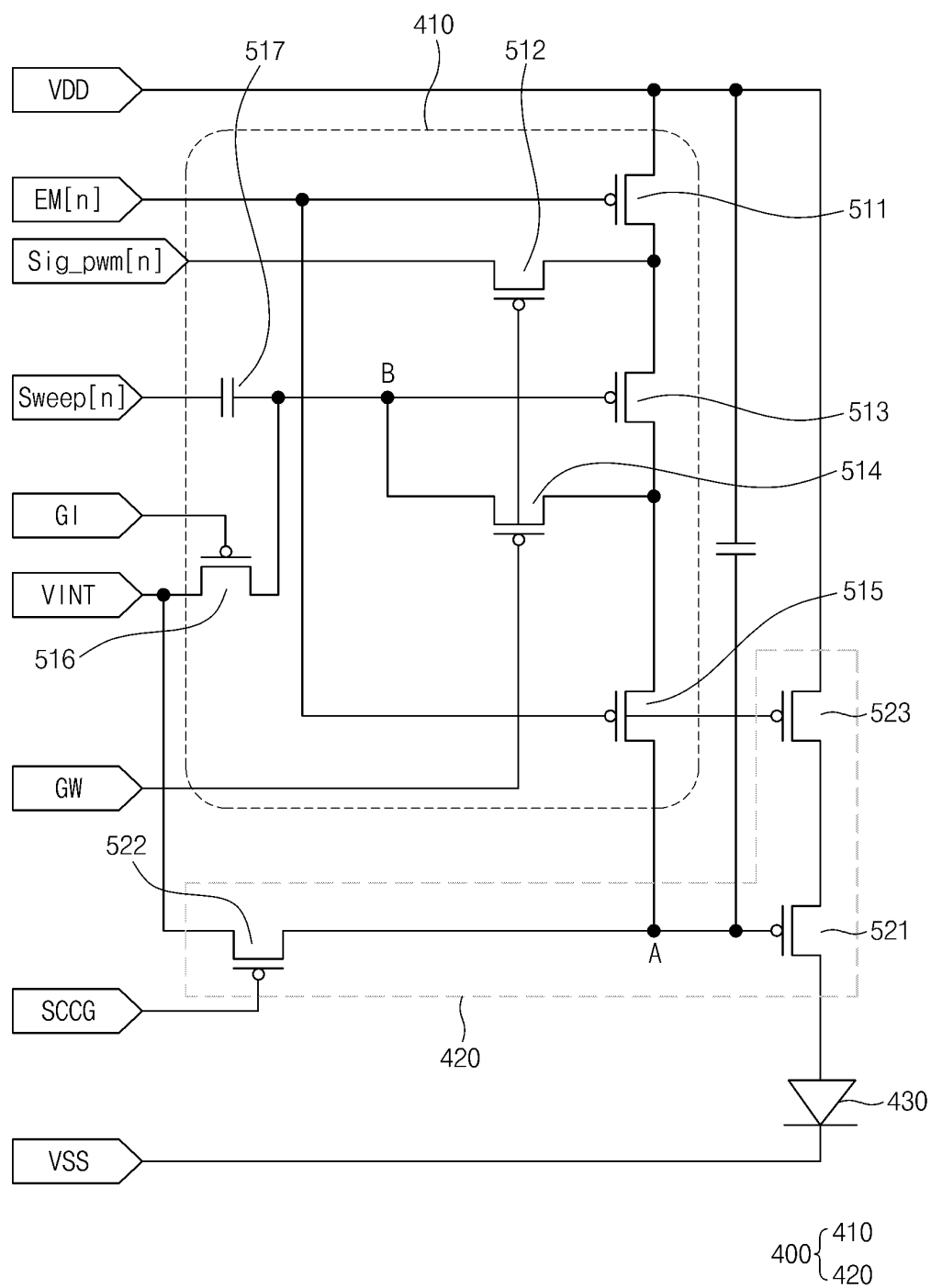


FIG.5

Description

[Technical Field]

[0001] Embodiments of the disclosure relates to an electronic device including a display having a pixel circuit in a PWM driving scheme and a method for operating the same.

[Background Art]

[0002] An electronic device including a display serves as an output device, which includes the display and a processor to control the display to operate in units of pixel or sub-pixel such that various colors are expressed. With the development of technology, higher brightness or higher resolution of the display has been increasingly demanded.

[0003] Liquid crystal displays (LCD), light emitting diodes (LED), and organic LED displays have been implemented in a pulse amplitude modulation (PAM) scheme to adjust the strength of the brightness of the display depending on the voltage strength of grayscale data.

[Disclosure]

[Technical Problem]

[0004] In case of a PAM driving scheme, especially a micro-LED device, where brightness is proportional to an amount of current flowing through the micro-LED device, a wavelength shift phenomenon arises giving an image quality characteristic in which the color sense is changed depending on the grayscale.

[0005] A pulse width modulation (PWM) driving scheme, which is to adjust a grayscale level based on time for emitting light, is employed to improve such image quality characteristics. However, existing PWM driving circuits include at least 13 transistors and a capacitor, so the PWM driving circuit is not applied to higher-resolution products. In addition, the circuit for the PWM driving scheme is complex and large, so the PWM driving scheme is difficult to apply in middle and smaller size displays.

[0006] Various embodiments of the disclosure are to provide an electronic device including a display and an operating method thereof improved in the change issue of a color sense depending on grayscale and brightness, suggesting a novel display pixel circuit using a PWM driving scheme that is simplified as compared to pixel circuits of a prior art.

[Technical Solution]

[0007] According to an embodiment of the disclosure, a method for driving a display of an electronic device including the display, may include storing grayscale data for one frame in a first gate terminal of a first output transistor

in a first circuit block included in a sub-pixel of the display, through a display driving circuit of the electronic device, inputting, into the first gate terminal of the first output transistor, a control signal having potential to change over time, changing a voltage of a second gate terminal of a second output transistor in a second circuit block included in the sub-pixel, as the first output transistor receives the control signal, controlling a time for emitting light of the light emitting element included in the sub-pixel, by adjusting a time in which the second output transistor is turned on, and controlling the second gate terminal at least twice, by applying an initialization voltage to the second gate terminal at least twice during one frame through a second initialization transistor connected to the second gate terminal.

[Advantageous Effects]

[0008] According to various embodiments of the disclosure, the electronic device including the display and the operating method thereof may suggest a PWM driving scheme that is simplified as compared to pixel circuits of the prior art, may be applied to high-resolution products and/or middle or small-sized display products without limitation, and may improve change issue of a color sense depending on grayscale and brightness.

[0009] Additionally, a variety of effects are provided that are directly or indirectly indicated in the disclosure.

[Description of Drawings]

[0010]

FIG. 1 is a block diagram illustrating an electronic device in a network environment, according to various embodiments;

FIG. 2 is a block diagram of a display module, according to various embodiments;

FIG. 3 is a block diagram illustrating a plurality of pixels of a display of an electronic device, according to an embodiment;

FIG. 4 is a block diagram illustrating the configuration of one sub-pixel of an electronic device, according to an embodiment;

FIG. 5 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device, according to an embodiment;

FIG. 6 is a view illustrating various signals for driving the circuit of FIG. 5 by an electronic device, over time, according to an embodiment;

FIG. 7 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device, according to an embodiment;

FIG. 8 is a view illustrating various signals for driving the circuit of FIG. 7 by an electronic device, according to an embodiment;

FIG. 9 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device,

according to an embodiment; and
FIG 10 is a view illustrating the difference between light emitting times resulting from a display pixel circuit structure of an electronic device, according to an embodiment.

[0011] In the following description made with respect to the accompanying drawings, similar components will be assigned with similar reference numerals.

[Mode for Invention]

[0012] Hereinafter, various embodiments of the disclosure may be described with reference to accompanying drawings. Accordingly, those of ordinary skill in the art will recognize that modification, equivalent, and/or alternative on the various embodiments described herein can be variously made without departing from the scope and spirit of the disclosure.

[0013] FIG. 1 is a block diagram illustrating an electronic device 101 in a network environment 100 according to various embodiments. Referring to FIG. 1, the electronic device 101 in the network environment 100 may communicate with an electronic device 102 via a first network 198 (e.g., a short-range wireless communication network), or an electronic device 104 or a server 108 via a second network 199 (e.g., a long-range wireless communication network). According to an embodiment, the electronic device 101 may communicate with the electronic device 104 via the server 108. According to an embodiment, the electronic device 101 may include a processor 120, a memory 130, an input module 150, a sound output module 155, a display module 160, an audio module 170, a sensor module 176, an interface 177, a connecting terminal 178, a haptic module 179, a camera module 180, a power management module 188, a battery 189, a communication module 190, a subscriber identification module (SIM) 196, or an antenna module 197. In some embodiments, at least one (e.g., the connecting terminal 178) of the components may be omitted from the electronic device 101, or one or more other components may be added in the electronic device 101. In some embodiments, some of the components may be implemented as single integrated circuitry. For example, some (e.g., the sensor module 176, the camera module 180, or the antenna module 197) of the components may be implemented as embedded in the display module 160 (e.g., a display).

[0014] The processor 120 may execute, for example, software (e.g., a program 140) to control at least one other component (e.g., a hardware or software component) of the electronic device 101 coupled with the processor 120, and may perform various data processing or computation. According to one embodiment, as at least part of the data processing or computation, the processor 120 may load a command or data received from another component (e.g., the sensor module 176 or the communication module 190) in a volatile memory 132, process

the command or the data stored in the volatile memory 132, and store resulting data in a non-volatile memory 134. According to an embodiment, the processor 120 may include a main processor 121 (e.g., a central processing unit (CPU) or an application processor (AP)), and an auxiliary processor 123 (e.g., a graphics processing unit (GPU), a neural processing unit (NPU), an image signal processor (ISP), a sensor hub processor, or a communication processor (CP)) that is operable independently from, or in conjunction with, the main processor 121. When the electronic device 101 includes the main processor 121 and the auxiliary processor, the auxiliary processor 123 may be adapted to consume less power than the main processor 121, or to be specific to a specified function. The auxiliary processor 123 may be implemented as separate from, or as part of the main processor 121.

[0015] The auxiliary processor 123 may control at least some of functions or states related to at least one component (e.g., the display module 160, the sensor module 176, or the communication module 190) among the components of the electronic device 101, instead of the main processor 121 while the main processor 121 is in an inactive (e.g., sleep) state, or together with the main processor 121 while the main processor 121 is in an active state (e.g., executing an application). According to an embodiment, the auxiliary processor 123 (e.g., an image signal processor or a communication processor) may be implemented as part of another component (e.g., the camera module 180 or the communication module 190) functionally related to the auxiliary processor 123. According to an embodiment, the auxiliary processor 123 (e.g., a neural network processing device) may include a hardware structure specified for processing an artificial intelligence (AI) model. The AI model may be generated through machine learning. The learning may be performed by the electronic device 101 performing the AI, and may be performed through an additional server (e.g., the server 108). A learning algorithm may include, for example, a supervised learning algorithm, an unsupervised learning algorithm, a semi-supervised learning algorithm, or a reinforcement learning algorithm, but the disclosure is not limited thereto. The AI model may include a plurality of artificial neural network (ANN) layers. The ANN may include a deep neural network (DNN), a convolutional neural network (CNN), a recurrent neural network (RNN), a restricted boltzman machine (RBM), a deep belief network (DBN), a bidirectional recurrent deep neural network (BRDNN), a deep Q-networks or the combination of the above networks, but the disclosure is not limited thereto. The AI model may additionally or alternatively include a software structure, in addition to a hardware structure.

[0016] The memory 130 may store various data used by at least one component (e.g., the processor 120 or the sensor module 176) of the electronic device 101. The various data may include, for example, software (e.g., the program 140) and input data or output data for a com-

mand related thereto. The memory 130 may include the volatile memory 132 or the non-volatile memory 134.

[0017] The program 140 may be stored in the memory 130 as software, and may include, for example, an operating system (OS) 142, middleware 144, or an application 146.

[0018] The input module 150 may receive a command or data to be used by other component (e.g., the processor 120) of the electronic device 101, from the outside (e.g., a user) of the electronic device 101. The input module 150 may include, for example, a microphone, a mouse, a keyboard, a key (e.g., a button), or a digital pen (e.g., a stylus pen).

[0019] The sound output module 155 may output sound signals to the outside of the electronic device 101. The sound output module 155 may include, for example, a speaker or a receiver. The speaker may be used for general purposes, such as playing multimedia or playing record, and the receiver may be used for an incoming calls. According to an embodiment, the receiver may be implemented as separate from, or as part of the speaker.

[0020] The display module 160 may visually provide information to the outside (e.g., a user) of the electronic device 101. The display module 160 may include, for example, a display, a hologram device, or a projector and control circuitry to control a corresponding one of the display, hologram device, and projector. According to an embodiment, the display module 160 may include touch sensor adapted to detect a touch, or a pressure sensor adapted to measure the intensity of force incurred by the touch.

[0021] The audio module 170 may convert a sound into an electrical signal and vice versa. According to an embodiment, the audio module 170 may obtain the sound via the input module 150, or output the sound via the sound output module 155 or an external electronic device (e.g., the electronic device 102) (e.g., speaker of headphone) directly (e.g., wiredly) or wirelessly coupled with the electronic device 101.

[0022] The sensor module 176 may detect an operational state (e.g., power or temperature) of the electronic device 101 or an environmental state (e.g., a state of a user) external to the electronic device 101, and then generate an electrical signal or data value corresponding to the detected state. According to an embodiment, the sensor module 176 may include, for example, a gesture sensor, a gyro sensor, an atmospheric pressure sensor, a magnetic sensor, an acceleration sensor, a grip sensor, a proximity sensor, a color sensor, an infrared (IR) sensor, a biometric sensor, a temperature sensor, a humidity sensor, or an illuminance sensor.

[0023] The interface 177 may support one or more specified protocols to be used for the electronic device 101 to be coupled with the external electronic device (e.g., the electronic device 102) directly (e.g., wiredly) or wirelessly. According to an embodiment, the interface 177 may include, for example, a high definition multimedia interface (HDMI), a universal serial bus (USB) inter-

face, a secure digital (SD) card interface, or an audio interface.

[0024] A connecting terminal 178 may include a connector via which the electronic device 101 may be physically connected with the external electronic device (e.g., the electronic device 102). According to an embodiment, the connecting terminal 178 may include, for example, a HDMI connector, a USB connector, a SD card connector, or an audio connector (e.g., a headphone connector).

[0025] The haptic module 179 may convert an electrical signal into a mechanical stimulus (e.g., a vibration or a movement) or electrical stimulus which may be recognized by a user via his tactile sensation or kinesthetic sensation. According to an embodiment, the haptic module 179 may include, for example, a motor, a piezoelectric element, or an electric stimulator.

[0026] The camera module 180 may capture a still image or moving images. According to an embodiment, the camera module 180 may include one or more lenses, image sensors, image signal processors, or flashes.

[0027] The power management module 188 may manage power supplied to the electronic device 101. According to one embodiment, the power management module 188 may be implemented as at least part of, for example, a power management integrated circuit (PMIC).

[0028] The battery 189 may supply power to at least one component of the electronic device 101. According to an embodiment, the battery 189 may include, for example, a primary cell which is not rechargeable, a secondary cell which is rechargeable, or a fuel cell.

[0029] The communication module 190 may support establishing a direct (e.g., wired) communication channel or a wireless communication channel between the electronic device 101 and the external electronic device (e.g., the electronic device 102, the electronic device 104, or the server 108) and performing communication via the established communication channel. The communication module 190 may include one or more communication processors that are operable independently from the processor 120 (e.g., the application processor (AP)) and supports a direct (e.g., wired) communication or a wireless communication. According to an embodiment, the communication module 190 may include a wireless communication module 192 (e.g., a cellular communication module, a short-range wireless communication module, or a global navigation satellite system (GNSS) communication module) or a wired communication module 194 (e.g., a local area network (LAN) communication module or a power line communication (PLC) module). The corresponding communication module from among the communication modules may communicate with the external electronic device via the first network 198 (e.g., a short-range communication network, such as Bluetooth™, wireless-fidelity (WiFi) direct, or infrared data association (IrDA)) or the second network 199 (e.g., a long-range communication network, such as a legacy cellular network, 5G network, next generation communication network, the Internet, or a computer network (e.g., LAN

or wide area network (WAN)). These various types of communication modules may be implemented as a single component (e.g., a single chip), or may be implemented as multi components (e.g., multi chips) separate from each other. The wireless communication module 192 may identify or authenticate the electronic device 101 in a communication network, such as the first network 198 or the second network 199, using subscriber information (e.g., international mobile subscriber identity (IMSI)) stored in the subscriber identification module 196.

[0030] The wireless communication module 192 may support a 5G network and a next-generation communication technology, for example, a new radio (NR) access technology after a 4G network. The NR access technology may support high-speed transmission for high capacity data (enhanced mobile broadband; eMBB), terminal power minimizing and multiple terminal access (massive machine type communication; mMTC), or ultra-reliable and low-latency communications (URLLC). The wireless communication module 192 may support a high-frequency band (e.g., mmWave band) to achieve, for example, a higher data rate. The wireless communication module 192 may support various technologies, for example, beamforming, massive multiple-input and multiple-output (MIMO), Full-dimensional MIMO, an array antenna, analog beamforming, or a large-scale antenna, to secure performance in high frequency bands. The wireless communication module 192 may support various requirements defined in the electronic device 101, the external electronic device (e.g., the electronic device 104) or the network system (e.g., the second network 199). According to one embodiment, the wireless communication module 192 may support a peak data rate (e.g., 20Gbps or more) for eMBB realization, loss coverage (e.g., 164 dB or less) for mMTC realization, or U-plane latency (e.g., 0.5 ms or less, or the round trip of 1 ms or less in each of a downlink (DL) and an uplink (UL)) for URLLC realization.

[0031] The antenna module 197 may transmit or receive a signal or power to or from the outside (e.g., the external electronic device) of the electronic device 101. According to an embodiment, the antenna module 197 may include an antenna including a radiating element composed of a conductive material or a conductive pattern formed in or on a substrate (e.g., PCB). According to an embodiment, the antenna module 197 may include a plurality of antennas (e.g., an array antenna). In such a case, at least one antenna appropriate for a communication scheme used in the communication network, such as the first network 198 or the second network 199, may be selected, for example, by the communication module 190 from the plurality of antennas. The signal or the power may then be transmitted or received between the communication module 190 and the external electronic device via the selected at least one antenna. According to an embodiment, another component (e.g., a radio frequency integrated circuit (RFIC)) other than the radiating element may be additionally formed as part of

the antenna module 197.

[0032] According to various embodiments, the antenna module 197 may form an mmWave antenna module. According to an embodiment, the mmWave antenna module may include a printed circuit board, an RFIC disposed on a first surface (e.g., a bottom surface) of the printed circuit board, or disposed adjacent to the first surface to support the specific high frequency band (e.g., mmWave band), and a plurality of antennas (e.g., an array antenna) disposed on a second surface (e.g., a top surface or a side surface) of the printed circuit board or disposed adjacent to the second surface to transmit or receive a signal having the specified high frequency band.

[0033] At least some of the above-described components may be coupled mutually and communicate signals (e.g., commands or data) therebetween via an inter-peripheral communication scheme (e.g., a bus, general purpose input and output (GPIO), serial peripheral interface (SPI), or mobile industry processor interface (MIPI)).

[0034] According to an embodiment, commands or data may be transmitted or received between the electronic device 101 and the external electronic device 104 via the server 108 coupled with the second network 199. Each of the external electronic devices 102 or 104 may be a device of a same type as, or a different type, from the electronic device 101. According to an embodiment, all or some of operations to be executed at the electronic device 101 may be executed at one or more of the external electronic devices 102, 104, or 108. For example, when the electronic device 101 should perform a function or a service automatically, or in response to a request from a user or another device, the electronic device 101, instead of, or in addition to, executing the function or the service, may request the one or more external electronic devices to perform at least part of the function or the service. The one or more external electronic devices receiving the request may perform the at least part of the function or the service requested, or an additional function or an additional service related to the request, and transfer an outcome of the performing to the electronic device 101. The electronic device 101 may provide the outcome, with or without further processing of the outcome, as at least part of a reply to the request. To that end, a cloud computing, distributed computing, mobile edge computing (MEC), or client-server computing technology may be used, for example. The electronic device 101 may provide an ultra-latency service by using, for example, distributed computing or mobile edge computing. According to various embodiments, the external electronic device 104 may include the Internet of things (IoT). The server 108 may be an artificial server using machine learning and/or a neural network. According to an embodiment, the external electronic device 104 or the server 108 may be included in the second network 199. The electronic device 101 may be applied to an artificial intelligence service (e.g., a smart home, a smart city, a smart car, or healthcare service) based on the 5G com-

munication technology and the IoT-related technology.

[0035] The electronic device according to various embodiments may be one of various types of electronic devices. The electronic devices may include, for example, a portable communication device (e.g., a smartphone), a computer device, a portable multimedia device, a portable medical device, a camera, a wearable device, or a home appliance. According to an embodiment of the disclosure, the electronic devices are not limited to those described above.

[0036] It should be appreciated that various embodiments of the disclosure and the terms used therein are not intended to limit the technological features set forth herein to particular embodiments and include various changes, equivalents, or replacements for a corresponding embodiment. With regard to the description of the drawings, similar reference numerals may be used to refer to similar or related elements. It is to be understood that a singular form of a noun corresponding to an item may include one or more of the things, unless the relevant context clearly indicates otherwise. As used herein, each of such phrases as "A or B," "at least one of A and B," "at least one of A or B," "A, B, or C," "at least one of A, B, and C," and "at least one of A, B, or C," may include any one of, or all possible combinations of the items enumerated together in a corresponding one of the phrases. As used herein, such terms as "1st" and "2nd," or "first" and "second" may be used to simply distinguish a corresponding component from another, and does not limit the components in other aspect (e.g., importance or order). It is to be understood that if an element (e.g., a first element) is referred to, with or without the term "operatively" or "communicatively", as "coupled with," "coupled to," "connected with," or "connected to" another element (e.g., a second element), it means that the element may be coupled with the other element directly (e.g., wiredly), wirelessly, or via a third element.

[0037] As used herein, the term "module" may include a unit implemented in hardware, software, or firmware, and may interchangeably be used with other terms, for example, "logic," "logic block," "part," or "circuitry". A module may be a single integral component, or a minimum unit or part thereof, adapted to perform one or more functions. For example, according to an embodiment, the module may be implemented in a form of an application-specific integrated circuit (ASIC).

[0038] Various embodiments as set forth herein may be implemented as software (e.g., the program 140) including one or more instructions that are stored in a storage medium (e.g., internal memory 136 or external memory 138) that is readable by a machine (e.g., the electronic device 101). For example, a processor (e.g., the processor 120) of the machine (e.g., the electronic device 101) may invoke at least one of the one or more instructions stored in the storage medium, and execute it, with or without using one or more other components under the control of the processor. This allows the machine to be operated to perform at least one function according to

the at least one instruction invoked. The one or more instructions may include a code generated by a compiler or a code executable by an interpreter. The machine-readable storage medium may be provided in the form of a non-transitory storage medium. Wherein, the term "non-transitory" simply means that the storage medium is a tangible device, and does not include a signal (e.g., an electromagnetic wave), but this term does not differentiate between where data is semi-permanently stored in the storage medium and where the data is temporarily stored in the storage medium.

[0039] According to an embodiment, a method according to various embodiments of the disclosure may be included and provided in a computer program product. The computer program product may be traded as a product between a seller and a buyer. The computer program product may be distributed in the form of a machine-readable storage medium (e.g., compact disc read only memory (CD-ROM)), or be distributed (e.g., downloaded or uploaded) online via an application store (e.g., PlayStore™), or between two user devices (e.g., smartphones) directly. If distributed online, at least part of the computer program product may be temporarily generated or at least temporarily stored in the machine-readable storage medium, such as memory of the manufacturer's server, a server of the application store, or a relay server.

[0040] According to various embodiments, each component (e.g., a module or a program) of the above-described components may include a single entity or multiple entities and some of multiple entities may be separately disposed on the other components. According to various embodiments, one or more of the above-described components may be omitted, or one or more other components may be added. Alternatively or additionally, a plurality of components (e.g., modules or programs) may be integrated into a single component. In such a case, according to various embodiments, the integrated component may still perform one or more functions of each of the plurality of components in the same or similar manner as they are performed by a corresponding one of the plurality of components before the integration. According to various embodiments, operations performed by the module, the program, or another component may be carried out sequentially, in parallel, repeatedly, or heuristically, or one or more of the operations may be executed in a different order or omitted, or one or more other operations may be added.

[0041] FIG. 2 is a block diagram 200 of a display module 160, according to various embodiments. Referring to FIG. 2, the display module 160 may include a display 210 and a display driver IC (DDI) 230 to control the display 210. The DDI 230 may include an interface module 231, a memory 233 (e.g., a buffer memory), an image processing module 235, or a mapping module 237. The DDI 230 may receive image information including, for example, image data or an image control signal corresponding to a command for controlling image data, from another component of the electronic device 101 through the interface

module 231. For example, according to an embodiment, the image information may be received from the processor 120 (e.g., the main processor 121) (e.g., an application processor) or the auxiliary processor 123 (e.g., the graphic processing device) operated independently from the function of the main processor 121). The DDI 230 may make communication with a touch circuit 250 or the sensor module 176 through the interface module 231. The DDI 230 may store at least some of the received image information in the memory 233, for example, in a unit of a frame. The image processing module 235 may perform pretreatment or post-treatment (e.g., adjusting a resolution, a brightness, or a size), with respect to, for example, at least some of the image data based at least on the characteristic of the image data or the characteristic of the display 210. The mapping module 237 may generate a voltage value or a current value corresponding to the image data subject to the pretreatment or the post-treatment through the image processing module 135. According to an embodiment, the voltage value and the current value may be generated based at least partially on attributes (e.g., the array (RGB stripe or pentile structure) of pixels of the display 210 or the size of each sub-pixel). At least some pixels of the display 210 may be driven based at least partially on, for example, the voltage value or the current value, such that visual information (e.g., a text, an image, or an icon) corresponding to the image data is displayed through the display 210.

[0042] According to an embodiment, the display module 160 may further include the touch circuit 250. The touch circuit 250 may include a touch sensor 251 and a touch sensor IC 253 for controlling the touch sensor 251. For example, the touch sensor IC 253 may control the touch sensor 251 to sense the touch input or the hovering input to a specified position of the display 210. For example, the touch sensor IC 253 may sense a touch input or a hovering input by measuring the change in the signal (e.g., a voltage, a light quantity, a resistance, or a charge amount) at a specific position of the display 210. The touch sensor IC 253 may provide, to the processor 120, information (e.g., a position, an area, pressure, or a time) on the sensed touch input or hovering input. According to an embodiment, at least a portion (e.g., the touch sensor IC 253) of the touch circuit 250 may be included in a portion of the display driver IC 230 or the display 210, or a portion of another component (e.g., the auxiliary processor 123) disposed outside the display module 160.

[0043] According to an embodiment, the display module 160 may further include at least one sensor (e.g., a fingerprint sensor, an iris sensor, a pressure sensor, or an illuminance sensor) of the sensor module 176 or a control circuit for the at least one sensor. In this case, the at least one sensor or the control circuit for the at least one sensor may be embedded in a portion (e.g., the display 210 or the DDI 230) of the display module 160 or a portion of the touch circuit 250. For example, when the sensor module 176 embedded in the display module 160 includes a biometric sensor (e.g., a finger-

print sensor), the biometric sensor may obtain biometric information (e.g., a fingerprint image) associated with a touch input through a partial area of the display 210. For another example, when the sensor module 176 embedded in the display module 160 includes a pressure sensor, the pressure sensor may obtain input information associated with the touch input through a partial area or the whole area of the display 210. According to an embodiment, the touch sensor 251 or the sensor module 176 may be disposed between pixels provided in a pixel layer of the display 210 or disposed on or under the pixel.

[0044] Hereinafter, an electronic device will be described with reference to FIGS. 3 and 4, according to an embodiment.

[0045] FIG. 3 is a block diagram illustrating a plurality of pixels of a display of an electronic device, according to an embodiment. FIG. 4 is a block diagram illustrating the configuration of one sub-pixel of an electronic device, according to an embodiment. The same components as those of the above described embodiment will be assigned with the same reference numerals.

[0046] Referring to FIG. 3, the electronic device (e.g., the electronic device 101 of FIG. 1) may include the processor 120, the display driving circuit 230 (e.g., the display driver IC 230 of FIG. 2), and the display 210.

[0047] According to an embodiment, the display 210 may include a plurality of pixels 340 arranged in the form of a matrix. In this case, each pixel 340 may include a plurality of sub-pixels 341, 342, and 342. For example, one pixel 340 included in the display 210 may include three types of sub-pixels including the red (R) sub-pixel 341, the green (G) sub-pixel 342, and the blue (B) sub-pixel 343. In addition, one set of R, G, and B sub-pixels may form one unit pixel 340 of the display 210.

[0048] The arrangement of the sub-pixels 341, 342, and 343 of FIG. 3 is only for illustrative purpose, and the plurality of sub-pixels 341, 342, and 343 may be disposed in various forms within each pixel 340 according to embodiments. In addition, one pixel 340 may be implemented with four types of sub-pixels of R, G, B, and W sub-pixels, which are different from those of FIG. 3. According to an embodiment, various numbers of sub-pixels may constitute one pixel.

[0049] According to an embodiment, the R sub-pixel 341 may include an R light emitting element and a driving circuit to drive the R light emitting element, the G sub-pixel 342 may include a G light emitting element and a driving circuit to drive the G light emitting element, and the B sub-pixel 343 may include a B light emitting element and a driving circuit to drive the B light emitting element.

[0050] Hereinafter, the configuration of one sub-pixel will be described with reference to FIG. 4. Although FIG. 4 illustrates the R sub-pixel 341 by way of example, the G sub-pixel 342 and the B sub-pixel 343 may have the same configuration.

[0051] Referring to FIG. 4, the R sub-pixel 341 may include a light emitting element 430 and a driving circuit 400 to drive the light emitting element 430.

[0052] According to an embodiment, the light emitting element 430 may be electrically connected to a first circuit block 410 and a second circuit block 420, and may emit light based on a driving current provided from the first circuit block 410 and the second circuit block 420. The light emitting element 430 may constitute the R sub-pixel 341 of the display 210 and may be the R light emitting element to emit red light.

[0053] According to an embodiment, the light emitting element constituting the G sub-pixel 342 may be a G light emitting element that emits green light, and the light emitting element constituting the B sub-pixel 343 may be the B light emitting element that emits blue light. In other words, the type of the sub-pixel may be determined depending on the type of the light emitting element. The driving circuit 400 to drive each light emitting element may be present for each sub-pixel.

[0054] According to an embodiment, the light emitting element 430 may be an inorganic light emitting element manufactured by using an inorganic material, which is different from an organic light emitting diode (OLED) manufactured by using the organic material, and may be a micro-light emitting diode (μ -LED). The micro-light emitting diode (μ -LED) may refer to an ultra-small inorganic light emitting element of 100 micrometers (μ m) or less, which self-emits light without a backlight or a color filter. However, the light emitting element 430 is not limited to the μ -LED.

[0055] According to an embodiment, the light emitting element 430 may emit light depending on a driving current provided by the first circuit block 410 and the second circuit block 420. Specifically, the light emitting element 430 may emit light with different brightness, depending on the amplitude or pulse width of the driving current provided by the first circuit block 410 and the second circuit block 420. In this case, the pulse width of the driving current may be expressed as the duty ratio of the driving current or the driving time (duration) of the driving current.

[0056] For example, as the amplitude of the driving current is increased, the light emitting element 430 may emit light with higher brightness. As the pulse width is increased (that is, as the duty ratio is increased, or the duration is increased), the light emitting element 430 may emit light with the higher brightness.

[0057] According to an embodiment, the driving circuit 400 including the first circuit block 410 and the second circuit block 420 may drive the light emitting element 430. The first circuit block 410 may be a pulse width modulation (PWM) block, and the second circuit block 420 may be a constant current generator (CCG) block. The first circuit block 410 may control the pulse width of the driving current for driving the light emitting element 430 by receiving a PWM data voltage from a data driver 320, and the second circuit block 420 may control the amplitude of the driving current.

[0058] According to an embodiment, the driving circuit 400 may control the pulse width and the amplitude of the

driving current for driving the light emitting element 430 to express various grayscale levels in units of sub-pixels. In the display 210, each sub-pixel is formed in units of the light emitting element 430. Accordingly, the driving circuit 400 may drive the light emitting element 430 to express various grayscale levels in units of sub-pixels. The method for driving the light emitting element 430 will be described in detail thereafter.

[0059] Referring back to FIG. 3, the display driving circuit 230 may include at least one gate driver 330 to drive the plurality of pixels 340 of the display 210, which are arranged in the form of a matrix, in units of horizontal lines (or the row line), and the data driver 320 provides a data voltage (e.g., a PWM data voltage) to each pixel 340 or the sub-pixels 341, 342, and 343.

[0060] According to an embodiment, the display 210 may be provided such that gate lines G1 to Gn cross data lines D1 to Dm, and the first circuit block 410 and the second circuit block 420 may be positioned at the crossing region such that the first circuit block 410 and the second circuit block 420 are connected to the gate line and the data line.

[0061] The display driving circuit 230 may drive the display 210 (in more detail, a plurality of driving circuits 400) under the control of the processor 120, and may include a timing controller 310, the data driver 320, and the gate driver 330.

[0062] The timing controller 310 may receive an input signal IS, a horizontal synchronization signal (Hsync), a vertical synchronization signal (Vsync), and a main clock signal (MCLK) from the outside to generate an image data signal, a scan control signal, a data control signal, and/or a light emitting control signal and may provide the generated signals to the display 210, the data driver 320, and/or the gate driver 330.

[0063] According to an embodiment, the timing controller 310 may apply at least one of various signals (e.g., EM, Sweep, or SCCG) to the first circuit block 410 and the second circuit block 420. In addition, according to an embodiment, a control signal for selecting one sub-pixel of the R, G, and B sub-pixels 341, 342, and 343 may be applied to the first circuit block 410 and/or the second circuit block 420.

[0064] The data driver 320 (or the source driver) serving as a unit to generate a data signal may receive image data of R/G/B components from the processor 120 to generate the data voltage (for example, the PWM data voltage). In addition, the data driver 320 may apply the generated data signal to the display 210.

[0065] The gate driver 330 serving as a unit to generate various control signals (e.g., EM, Sweep, or SCCG) may transmit various control signals to a specific row (or a specific horizontal line) of the display 210 or may transmit various control signals to whole lines. In addition, the gate driver 330 may apply a driving voltage VDD to a driving voltage terminal of the driving circuit 400, according to an embodiment.

[0066] According to an embodiment, the processor

120 may control the whole operation of the display module. The processor 120 may control the display driving circuit 230 to drive the display 210. To this end, the processor 120 may be implemented with at least one of a central processing unit (CPU), a microcontroller, an application processor (AP), a communication processor (CP), or an ARM processor.

[0067] Hereinafter, the configuration and the driving of one sub-pixel included in the display of the electronic device will be described in detail according to an embodiment with reference to FIGS. 5 and 6.

[0068] FIG. 5 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device according to an embodiment. FIG. 6 is a view illustrating various signals for driving the circuit of FIG. 5 by an electronic device, according to an embodiment. The same components as those of the above described embodiment will be assigned with the same reference numerals, and the duplication thereof will be omitted.

[0069] Hereinafter, devices including one sub-pixel and the connection relationship between the devices will be described with reference to FIG. 5. Referring to FIG. 5, one sub-pixel may include the light emitting element 430 and the driving circuit 400 to drive the light emitting element 430. The display 210 may include the light emitting element 430 and the driving circuit 400 of the light emitting element 430 with respect to each sub-pixel, as illustrated in FIG. 5. The light emitting element 430 may be a light emitting element having any one of R, G, and B.

[0070] According to an embodiment, the first circuit block 410 may be the PWM block. The first circuit block 410 may include a first transistor 511 having a source terminal connected to the terminal of the driving voltage VDD terminal and a drain terminal connected to a drain terminal of a second transistor 512 and a source terminal of a third transistor 513 in common, the second transistor 512 having a source terminal to receive a data signal Sig_pwm[n] and the drain terminal connected to the drain terminal of the first transistor 511 and the source terminal of the third transistor 513, the third transistor 513 having the source terminal connected to the drain terminal of the first transistor 511 and the drain terminal of the second transistor 512 in common, and a drain terminal connected to a drain terminal of a fourth transistor 514 and a source terminal of a fifth transistor 515 in common, the fourth transistor 514 interposed between the gate terminal and the drain terminal of the third transistor 513, and a first capacitor 517 having one terminal to receive a control signal Sweep[n], and an opposite terminal connected to the source terminal of a sixth transistor 516 and the gate terminal of the third transistor 513 in common.

[0071] According to an embodiment, the second circuit block 420 may be the CCG block. The second circuit block 420 may include a seventh transistor 521 having a source terminal connected to a drain terminal of a ninth transistor 523 and a drain terminal connected to the light emitting element 430, an eighth transistor 522 having a gate terminal to receive the control signal SCCG and a

drain terminal interposed between the drain terminal of the fifth transistor 515 and the gate terminal of the seventh transistor 521 in common, and the ninth transistor 523 having a source terminal connected to the driving voltage VDD terminal and a drain terminal connected to a source terminal of the seventh transistor 521.

[0072] Meanwhile, as described above, the transistors 511, 512, 513, 514, 515, 516, 521, 522, and 523 included in the driving circuit of the sub-pixel are implemented with P-channel Metal Oxide Semiconductor Field Effect Transistors (PMOSFET). However, an embodiment is not limited thereto. According to an embodiment, even a driving circuit in which transistors are implemented with N-channel Metal Oxide Semiconductor Field Effect Transistors (NMOSFET) may be implemented to perform the same operation as that of the above-described driving circuit. Alternatively, according to an embodiment, even a driving circuit, in which the transistors are implemented with the mixture of PMOSFETs and NMOSFETs, may be implemented to perform the same operation as that of the above-described driving circuit.

[0073] The driving circuit including the NMOSFET may perform the same operation as that of the driving circuit of FIG. 5 except for the difference (e.g., the difference in connection relationship between the devices and the difference in polarity between various signals applied) made due to the difference in type between transistors. Those skilled in the art may easily understand the operation of the driving circuit implemented with the NMOSFET through the description provided based on the PMOSFET. Accordingly, the details thereof will be omitted to avoid redundancy.

[0074] Hereinafter, the operation of the driving circuit 400 will be described in more detail with reference to FIGS. 5 and 6. FIG. 6 is a view illustrating various signals applied to the driving circuit 400 of FIG. 5 over time. According to an embodiment, various signals of FIG. 6 may be applied to the display driving circuit (e.g., the display driving circuit 230 of FIG. 3) under the control of the processor (e.g., the processor 120 of FIG. 4).

[0075] Referring to FIGS. 5 and 6, the driving circuit 400 of one sub-pixel may be driven in order of a first duration 610 serving as a first initialization duration, a second duration 620 serving as a second initialization duration, a third duration 630 serving as a compensating duration and a data voltage applying duration, a fourth duration 640 serving as a light emitting duration, a fifth duration 650 serving as a re-initialization duration, and a sixth duration 660 serving as a re-light emitting duration, to display one frame.

[0076] According to an embodiment, the first duration 610 may be a duration for initializing a gate node 'A' of the seventh transistor 521. For the first duration 610, the control signal EM[n] may have a high voltage. Therefore, the first transistor 511, the fifth transistor 515, and the ninth transistor 523 receiving the control signal EM[n] through the gate terminal may be turned off, and a current flowing from the terminal of the driving voltage VDD to

the seventh transistor 521 may be blocked.

[0077] The processor 120 may turn on the eighth transistor 522 and apply a bias to the seventh transistor 521 for a specific duration by changing the control signal SCCG to have a low voltage, thereby improving image quality degradation resulting from the bias condition of a previous frame of the seventh transistor 521 for the first duration 610. The processor 120 may adjust the time for applying the bias by adjusting the time in which the control signal SCCG has a low voltage. The processor 120 may reduce the shift difference of the threshold voltage of the seventh transistor 521, which is performed as the previous frame is driven, by applying the bias to the seventh transistor 521.

[0078] The processor 120 may turn on the eighth transistor 522 by maintaining the control signal SCCG to have a low voltage, in the state that the light emitting path is blocked by maintaining the control signal EM[n] to have a high voltage for the first duration 610. Accordingly, the processor 120 may initialize the gate terminal 'A' of the seventh transistor 521 and turn on the seventh transistor 521. The initialization voltage of the gate terminal 'A' of the seventh transistor 521 may be determined by a control signal VINT.

[0079] While the control signal EM[n] is maintained to have the high voltage, and the control signal SCCG is maintained to have the low voltage, the gate node 'A' of the seventh transistor 521 may be maintained to be initialized. According to an embodiment, the high voltage of the control signal EM[n] and the low voltage of the control signal SCCG may be maintained during the second duration 620, and the third duration 630 and until the first duration 610.

[0080] According to an embodiment, the second duration 620 may be a duration for initializing a gate terminal 'B' of the third transistor 513. The processor 120 may change a control signal GI to have the low voltage for the second duration 620. Accordingly, the sixth transistor 516 that receives the control signal GI through the gate terminal may be turned on, the gate voltage 'B' of the third transistor 513 may be initialized, and the third transistor 513 may be changed to be turned on. The initialization voltage of the gate terminal 'B' of the third transistor 513 may be determined by the control signal VINT. Since the control signal EM[n] is maintained to have the high voltage for the second duration 620, the flow of the current from the terminal of the driving voltage VDD to the third transistor 513 may be blocked by the first transistor 511.

[0081] According to an embodiment, the third duration 630 may be a compensating duration for the threshold voltage of the third transistor 513 and a duration for inputting a data voltage. The processor 120 may change the control signal GW to have a low voltage for the third duration 630. Accordingly, the second transistor 512 and the fourth transistor 514 to receive the control signal GW through the gate terminals may be changed to be turned on. According to an embodiment, the control signal GW is a signal for selecting a data signal for each gate line.

Accordingly, whether to change the control signal to be low voltage for lines may be varied depending on images to be output.

[0082] Accordingly, a data signal Sig_pmw[n] including grayscale data that controls a time for emitting light from the light emitting element 430 may be input to the source terminal of the second transistor 512, and stored in the first capacitor 517 having one terminal connected to the gate terminal 'B' of the third transistor 513 through the third transistor 513 and the fourth transistor 514. The first capacitor 517 may store a voltage of the gate terminal 'B' of the third transistor 513 for one frame. As the data signal Sig_pmw[n] is stored in the gate terminal 'B' of the third transistor 513 through the second transistor 512, the third transistor 513, and the fourth transistor 514 which are circuits for compensating for the distribution of the threshold voltage, the distribution of the threshold voltage of the third transistor 513 may be compensated.

[0083] In this case, the data signal Sig_pwm[n] may include a compensation value that compensates for the distribution of the threshold voltage of the seventh transistor 521 and the distribution of LED brightness formed in an optical compensation scheme. The compensation value for a device characteristic of the seventh transistor 521 which is an output transistor of the second circuit block 420 is reflected in the data signal Sig_pmw[n]. Accordingly, even if the same data is input for each data line of the display panel, a different voltage value may be input for each data line depending on the compensation values.

[0084] According to an embodiment, the fourth duration 640 may be a light emitting duration. The processor 120 may change the control signal EM to have a low voltage for the fourth duration 640. Accordingly, the first transistor 511, the fifth transistor 515, and the ninth transistor 523 may be turned on. Accordingly, a current flows from the terminal of the driving voltage VDD to the ninth transistor 523, the seventh transistor 521, the light emitting element 430, and the terminal of a ground voltage VSS to emit light from the light emitting element 430. According to an embodiment, the control signal EM may turn on/off a light emitting path to control light emission/non-emission of the driving circuit 400.

[0085] For the fourth duration 640, the processor 120 may input the control signal Sweep having a waveform having a slope to one terminal of the first capacitor 517. The voltage of the gate terminal 'B' of the third transistor 513 is coupled and changed as the grayscale data stored in the first capacitor 517 and the change of the input control signal Sweep. Accordingly, the third transistor 513 may be gradually turned on depending on the potential of the control signal Sweep.

[0086] As the third transistor 513 is changed to be turned on, a current flowing through the third transistor 513 is gradually increased, and the gate terminal of the seventh transistor 521 may be changed from a low voltage to a high voltage. Accordingly, after a specific period of time, the seventh transistor 521 turned on may be

turned off. When the seventh transistor 521 is turned off, the light emitting element 430 may be stopped to emit light.

[0087] In other words, the time for turning off the seventh transistor 521 may be adjusted depending on the data signal Sig_pwm[n] stored in the gate terminal 'B' of the third transistor 513. As the time in which the current flows through the seventh transistor 521 is adjusted, the PWM may be driven to adjust the grayscale.

[0088] According to an embodiment, the fifth duration 650 may be a duration for re-initializing the seventh transistor 521. The processor 120 may turn off the first transistor 511, the third transistor 513, the fifth transistor 515, and the ninth transistor 523 by changing the control signal EM and the control signal Sweep to have a high voltage for the fifth duration 650. Alternatively, the processor 120 may change the control signal SCCG to have the low voltage for the fifth duration 650 to change the eighth transistor 522 to be turned on. In addition, the seventh transistor 521 is re-initialized to change the seventh transistor 521 to be turned on.

[0089] According to an embodiment, the sixth duration 660 may be a duration for re-initializing the light emitting element 430. The processor 120 may change the control signal SCCG to have a high voltage, such that the eighth transistor 522 is turned off, and change the control signal EM to have a low voltage such that the first transistor 511, the fifth transistor 515, and the ninth transistor 523 are turned on to emit light from the light emitting element 430.

[0090] The processor 120 may change the third transistor 513 to be turned on by changing the control signal Sweep from the high voltage to the low voltage again for the sixth duration 660. The processor 120 may change the seventh transistor 521, which is turned on, to be turned off by using the grayscale data voltage stored in the first capacitor 517, thereby controlling the time for which a current is allowed to flow through the seventh transistor 521 again.

[0091] The processor 120 may perform duty driving by repeating the initialization and the PWM driving of the seventh transistor 521 for one frame. Although FIG. 6 illustrates that the seventh transistor 521 is initialized twice during one frame, the seventh transistor 521 may be initialized at least three times according to an embodiment, and may be driven in various duty cycles.

[0092] According to an embodiment of the disclosure, the pixel circuit structure includes a separate transistor (e.g., the eighth transistor 522 of FIG. 5) and the SCCG wire to apply the bias to the output transistor (e.g., the seventh transistor 521 of FIG. 5) of the CCG circuit block, thereby initializing the output transistor of the CCG circuit block at least twice per one frame. In addition, duty driving of repeating light emission or non-light emission several times in one frame may be provided by inputting the grayscale data once and using the grayscale data stored in a capacitor. In addition, the time for applying the bias of the output transistor of the CCG circuit block may be ad-

justed by adjusting the time for applying the low voltage of the control signal SCCG through the separate transistor and the SCCG wire, thereby improving the deterioration of the image quality caused by hysteresis.

[0093] According to an embodiment of the disclosure, in the pixel circuit structure, the display driving circuit or the processor may reflect the compensation value to the data signal Sig_pwm through an arithmetic operation, based on the characteristic distribution compensation data of the output transistor of the CCG circuit block, which is stored in an internal memory or an external memory of the display driving circuit, when the output transistor (e.g., the seventh transistor 521 of FIG. 5) of the CCG circuit block has no internal compensating circuit. Accordingly, the pixel circuit structure may be simplified. Accordingly, the pixel circuit structure applicable to a high resolution display and/or a middle/small display may be provided.

[0094] Hereinafter, the configuration and the driving of one sub-pixel included in the display of the electronic device will be described in detail according to an embodiment with reference to FIGS. 7 and 8.

[0095] FIG. 7 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device, according to an embodiment. FIG. 8 is a view illustrating various signals for driving the circuit of FIG. 7 by an electronic device, according to an embodiment. The same components as those of the above described embodiment will be assigned with the same reference numerals, and the duplication thereof will be omitted.

[0096] Hereinafter, devices including one sub-pixel and the connection between the devices will be described with reference to FIG. 7. Referring to FIG. 7, one sub-pixel may include the first circuit block 410, a second circuit block 710, and the light emitting element 430. The description about the first circuit block 410 and the light emitting element 430 will be the same as the description about the embodiment of FIG. 5. The following description will be made while focusing on the second circuit block 710 which makes a difference from the circuit structure according to an embodiment of FIG. 5.

[0097] According to an embodiment, the second circuit block 710 may be a CCG block. The second circuit block 710 includes a seventh transistor 711 which is an output transistor, an eighth transistor 712 connected to the gate terminal of the seventh transistor 711, and a ninth transistor 713 connected to the source terminal of the seventh transistor 711, which is the same as an embodiment of FIG. 5. However, the source terminal of the eighth transistor 712 may be connected to a separate input terminal to input the compensation signal Sig_ccg[n] instead of the input terminal of the control signal vint, which is different from the embodiment of FIG. 5. According to an embodiment, the line (not illustrated) to input the compensation signal Sig_ccg[n] may be formed in a vertical direction which is similar to a data line.

[0098] Hereinafter, the operation of the driving circuit 400 will be described in more detail with reference to

FIGS. 7 and 8. FIG. 8 is a view illustrating various signals applied to the driving circuit 400 of FIG. 7 over time. According to an embodiment, the various signals of FIG. 8 may be applied to the driving circuit 400 by the display driving circuit (e.g., the display driving circuit 230 of FIG. 3) under the control of the processor (e.g., the processor 120 of FIG. 4).

[0099] The description concerning the first duration 610, which is the first initialization duration of FIG. 8, the second duration 620 of the second initialization duration, the third duration 630 which is the data voltage input duration, the fourth duration 640 which is the light emitting duration, the fifth duration 650 which is the re-initialization duration, the sixth duration 660 which is the re-light emitting duration, is the same as the description provided for the FIG. 6 embodiment. However, according to an embodiment of FIG. 8, compensation durations 670 and 680 may be added to compensate for the device characteristic of the seventh transistor 711 before the light emitting duration 640 and the re-light emitting duration 660.

[0100] According to an embodiment, the processor 120 may input the compensation signal Sig_ccg[n] to the source terminal of the eighth transistor 712 for the compensation durations 670 and 680. The electronic device 101 may store the compensation data for the specific distribution of the seventh transistor 711 in the internal memory or the external memory of the display driving circuit 230. The processor 120 may input the compensation signal Sig_ccg[n] having the compensation value for the characteristic distribution of the seventh transistor 711, which is reflected in the compensation signal Sig_ccg[n], to the source terminal of the eighth transistor 712, for the compensation durations 670 and 680.

[0101] The control signal SCCG is in a low voltage state for the compensation durations 670 and 680. Accordingly, the eighth transistor 712 is turned on, and the compensation signal Sig_ccg[n] may be input to the gate terminal of the seventh transistor 711 through the eighth transistor 712. When the compensation value of the seventh transistor 711 is reflected for the compensation durations 670 and 680, the data signal Sig_pwm may not reflect the compensation value of the seventh transistor 711.

[0102] According to an embodiment of the disclosure, the display pixel circuit has a structure that reflects the compensation value to the gate terminal of the seventh transistor 711 whenever light is emitted, by adding an additional input line for the compensation signal Sig_ccg[n] to compensate for the device characteristic of the seventh transistor 711 which is the output transistor of the CCG circuit block. Accordingly, the reflection of the compensation value may be advanced, and the issue related to the wavelength shift may be improved. Accordingly, in addition, the processor 120 may apply a different voltage to each pixel through the line for the compensation signal Sig_ccg[n], and adjust the voltage of the compensation signal Sig_ccg[n], thereby adjusting the pulse size (pulse height) of the current flowing through the sev-

enth transistor 711.

[0103] Hereinafter, the configuration and the driving of one sub-pixel included in the display of the electronic device will be described in detail according to an embodiment with reference to FIGS. 9 and 10.

[0104] FIG. 9 is a circuit diagram corresponding to one sub-pixel included in a display of an electronic device, according to an embodiment. FIG. 10 is a view illustrating the difference in light emitting time due to a pixel circuit structure of a display of an electronic device, according to an embodiment. The same components as those of the above described embodiment will be assigned with the same reference numerals, and the duplication thereof will be omitted.

[0105] Hereinafter, devices including one sub-pixel and the connection between the devices will be described with reference to FIG. 9. Referring to FIG. 9, one sub-pixel may include the first circuit block 410, a second circuit block 910, and the light emitting element 430. The description about the first circuit block 410 and the light emitting element 430 may be the same as those according to an embodiment of FIG. 5. The following description will be made while focusing on the second circuit block 910 having the difference from the circuit structure according to an embodiment of FIG. 5.

[0106] The second circuit block 910 may be a CCG circuit block. In the pixel circuit structure described with reference to FIGS. 5 and 7, the output transistors in the CCG circuit block were all PMOSFETs. To the contrary, in the display pixel circuit structure of FIG. 9, a seventh transistor 911 which is an output transistor of the second circuit block 910 may be an NMOSFET.

[0107] The second circuit block 910 includes an eighth transistor 912 connected to the gate terminal of the seventh transistor 911, and a ninth transistor 913 connected to the source terminal of the seventh transistor 911, which is the same as an embodiment of FIG. 5. However, the source terminal of the eighth transistor 912 may be connected to an input terminal of the data signal Sig_pwm instead of the input terminal of the control signal VINT, which is different from the embodiment of FIG. 5. In addition, the light emitting element 430 may be connected to the source terminal of the ninth transistor 913 instead of the drain terminal of the seventh transistor 911.

[0108] Hereinafter, the operation of the driving circuit 400 will be described in more detail with reference to FIGS. 5, 9 and 10. A first drawing 1010 of FIG. 10 is a view illustrating various input signals and a light emitting time of a light emitting element in the circuit structure of FIG. 5 in which the output transistor of the CCG block is the PMOSFET. A second drawing 1020 of FIG. 10 is a view illustrating various input signals and a light emitting time of a light emitting element in the circuit structure of FIG. 9 in which the output transistor of the CCG block is the NMOSFET. The following description will be made while focusing on the difference in the type of the output transistor of the CCG block.

[0109] Referring to the first drawing 1010 of FIGS. 5

and 10, the source terminal of the eighth transistor 522 is connected to the input terminal of the control signal VINT. Accordingly, as the control signal SCCG[n] is changed to have the low voltage, the eighth transistor 522 is turned on. In this case, the low voltage is applied to the gate terminal of the seventh transistor 521 such that the seventh transistor 521 is turned on.

[0110] Accordingly, as the control signal EM[n] is changed to have the low voltage, the first transistor 511, the fifth transistor 515, and the ninth transistor 523 are turned on, and the light emitting path is formed. In this case, the light emitting element 430 may emit light.

[0111] The voltage of the gate terminal 'B' of the third transistor 513 is coupled depending on the change in potential of the control signal Sweep, so the third transistor 513 is gradually turned on. As the third transistor 513 is changed to be turned on, the gate terminal 'A' of the seventh transistor 521 is changed from the low voltage to the high voltage. Accordingly, the seventh transistor 521 turned on may be changed to be turned off.

[0112] The light emitting element 430 may maintain light emitted until the seventh transistor 521 is changed to be turned off. When the seventh transistor 521 is changed to be turned off, the light emission may be stopped.

[0113] Referring to the second drawing 1020 of FIGS. 9 and 10, the seventh transistor 911 may be initialized to a turn-off voltage. Accordingly, although the control signal EM[n] is changed to the low voltage, the first transistor 511, the fifth transistor 515, and the ninth transistor 913 are turned on, the seventh transistor 911 is turned off. Accordingly, the light emitting element 430 may not emit light. However, the voltage of the gate terminal 'B' of the third transistor 513 is coupled depending on the change in potential of the control signal Sweep, so the third transistor 513 is gradually turned on as the third transistor 513 turned off is changed to be turned on.

[0114] When the seventh transistor 911 is turned on, the light emitting element 430 may start to emit light and the control signal EM[n] is changed to the high voltage. As the re-initialization duration of the seventh transistor 911 is started the light emission is stopped.

[0115] The output transistor of the PMOSEFT is initialized to be turned on, and is gradually changed to be turned off depending on the change in potential of the control signal Sweep. Accordingly, it is difficult to express black and low grayscale levels. To the contrary, when the output transistor in the CCG circuit block includes an NMOSFET, the output transistor is initialized to be turned off, and is gradually turned on depending on the change in potential of the control signal Sweep. Accordingly, it is easy to implement low grayscale level and low brightness.

[0116] According to an embodiment of the disclosure, an electronic device may include a sub-pixel including a first circuit block, a second circuit block, and a light emitting element to emit light based on a driving current provided from the first circuit block and the second circuit

block, a display panel including a plurality of pixels including the sub-pixel, a display driving circuit electrically connected to the display panel, and a processor electrically connected to the display driving circuit. The display driving circuit may store grayscale data for one frame in a first gate terminal of a first output transistor in the first circuit block, input, into the first gate terminal of the first output transistor, a control signal having potential changed over time, change a voltage of a second gate terminal of a second output transistor in the second circuit block, as the first output transistor receives the control signal, control a time for emitting light from the light emitting element, by adjusting a time in which the second output transistor is turned on and control the second gate terminal at least twice, by applying an initialization voltage to the second gate terminal at least twice during one frame through a second initialization transistor connected to the second gate terminal.

[0117] According to an embodiment of the disclosure, the display driving circuit may control the light emitting element to emit light at least twice, for one frame based on the grayscale data for the one frame.

[0118] According to an embodiment of the disclosure, the display driving circuit may control a time for applying a bias of the second output transistor by adjusting the time in which the second initialization transistor is turned on.

[0119] According to an embodiment of the disclosure, the display driving circuit may reflect a compensation value for a device characteristic of the second output transistor in the grayscale data.

[0120] According to an embodiment of the disclosure, the information about the device characteristic of the second output transistor may be stored in a memory of the electronic device.

[0121] According to an embodiment of the disclosure, an initialization duration of the first output transistor may not be equal to an initialization duration of the second output transistor for the one frame.

[0122] According to an embodiment of the disclosure, the display driving circuit may input a first initialization signal to a gate terminal of a first initialization transistor to initialize the first output transistor, independently from a second initialization signal input to a gate terminal of the second initialization transistor.

[0123] According to an embodiment of the disclosure, the display driving circuit may compensate for a device characteristic of the first output transistor by using a compensation transistor connected between the first gate terminal of the first output transistor and a drain terminal of the first output transistor.

[0124] According to an embodiment of the disclosure, the second output transistor may be a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS-FET), and the display driving circuit may initialize the second output transistor such that the second output transistor is turned on, before the light is emitted from the light emitting element.

[0125] According to an embodiment of the disclosure, the second output transistor may be a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS-FET), and the display driving circuit may initialize the second output transistor, such that the second output transistor is turned off, before the light is emitted from the light emitting element.

[0126] According to an embodiment of the disclosure, a method for driving a display of an electronic device including the display, may include storing grayscale data for one frame in a first gate terminal of a first output transistor in a first circuit block included in a sub-pixel of the display, through a display driving circuit of the electronic device, inputting, into the first gate terminal of the first output transistor, a control signal having potential changed over time, changing a voltage of a second gate terminal of a second output transistor in a second circuit block included in the sub-pixel, as the first output transistor receives the control signal, controlling a time for emitting light of the light emitting element included in the sub-pixel, by adjusting a time in which the second output transistor is turned on, and controlling the second gate terminal at least twice, by applying an initialization voltage to the second gate terminal at least twice during one frame through a second initialization transistor connected to the second gate terminal.

[0127] According to an embodiment of the disclosure, the light emitting element may be controlled to emit light at least twice, for the one frame based on the grayscale data for the one frame through the display driving circuit.

[0128] According to an embodiment of the disclosure, a time for applying a bias of the second output transistor may be controlled by adjusting the time in which the second initialization transistor is turned on through the display driving circuit.

[0129] According to an embodiment of the disclosure, a compensation value for a device characteristic of the second output transistor may be reflected in the grayscale data through the display driving circuit.

[0130] According to an embodiment of the disclosure, information about the device characteristic of the second output transistor may be stored in a memory of the electronic device.

[0131] According to an embodiment of the disclosure, an initialization duration of the first output transistor may not be equal to an initialization duration of the second output transistor for the one frame.

[0132] According to an embodiment of the disclosure, the display driving circuit may input a first initialization signal to a gate terminal of a first initialization transistor to initialize the first output transistor, independently from a second initialization signal input to a gate terminal of the second initialization transistor.

[0133] According to an embodiment of the disclosure, the display driving circuit may compensate for a device characteristic of the first output transistor by using a compensation transistor connected between the first gate terminal of the first output transistor and a drain terminal of

the first output transistor.

[0134] According to an embodiment of the disclosure, the second output transistor may be a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOS-FET), and the second output transistor may be initialized through the display driving circuit such that the second output transistor is turned on, before the light is emitted from the light emitting element.

[0135] According to an embodiment of the disclosure, the second output transistor may be a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOS-FET), and the second output transistor may be initialized through the display driving circuit, such that the second output transistor is turned off, before the light is emitted from the light emitting element.

Claims

1. An electronic device comprising:

a sub-pixel including a first circuit block, a second circuit block, and a light emitting element to emit light based on a driving current provided from the first circuit block and the second circuit block;

a display panel including a plurality of pixels including the sub-pixel;

a display driving circuit electrically connected to the display panel; and

a processor electrically connected to the display driving circuit,

wherein the display driving circuit:

stores grayscale data for one frame in a first gate terminal of a first output transistor in the first circuit block;

inputs, into the first gate terminal of the first output transistor, a control signal having potential changed over time;

changes a voltage of a second gate terminal of a second output transistor in the second circuit block, as the first output transistor receives the control signal;

controls a time for emitting light from the light emitting element, by adjusting a time in which the second output transistor is turned on; and

controls the second gate terminal at least twice, by applying an initialization voltage to the second gate terminal at least twice during one frame through a second initialization transistor connected to the second gate terminal.

2. The electronic device of claim 1, wherein the display driving circuit controls the light emitting element to emit light at least twice, for one frame based on the

grayscale data for the one frame.

3. The electronic device of claim 1, wherein the display driving circuit controls a time for applying a bias of the second output transistor by adjusting the time in which the second initialization transistor is turned on. 5
4. The electronic device of claim 1, wherein the display driving circuit reflects a compensation value for a device characteristic of the second output transistor in the grayscale data. 10
5. The electronic device of claim 4, wherein information about the device characteristic of the second output transistor is stored in a memory of the electronic device. 15
6. The electronic device of claim 1, wherein an initialization duration of the first output transistor is not equal to an initialization duration of the second output transistor for the one frame. 20
7. The electronic device of claim 1, wherein the display driving circuit inputs a first initialization signal to a gate terminal of a first initialization transistor to initialize the first output transistor, independently from a second initialization signal input to a gate terminal of the second initialization transistor. 25
8. The electronic device of claim 1, wherein the display driving circuit compensates for a device characteristic of the first output transistor by using a compensation transistor connected between the first gate terminal of the first output transistor and a drain terminal of the first output transistor. 30 35
9. The electronic device of claim 1, wherein the second output transistor is a P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOSFET), and wherein the display driving circuit initializes the second output transistor such that the second output transistor is turned on, before the light is emitted from the light emitting element. 40
10. The electronic device of claim 1, wherein the second output transistor is a N-channel Metal Oxide Semiconductor Field Effect Transistor (NMOSFET), and wherein the display driving circuit initializes the second output transistor, such that the second output transistor is turned off, before the light is emitted from the light emitting element. 45 50
11. A method for driving a display of an electronic device including the display, the method comprising: 55

storing grayscale data for one frame in a first gate terminal of a first output transistor in a first circuit block included in a sub-pixel of the dis-

play, through a display driving circuit of the electronic device;

inputting, into the first gate terminal of the first output transistor, a control signal having potential changed over time;

changing a voltage of a second gate terminal of a second output transistor in a second circuit block included in the sub-pixel, as the first output transistor receives the control signal;

controlling a time for emitting light of the light emitting element included in the sub-pixel, by adjusting a time in which the second output transistor is turned on; and

controlling the second gate terminal at least twice, by applying an initialization voltage to the second gate terminal at least twice during one frame through a second initialization transistor connected to the second gate terminal.

12. The method of claim 11, further comprising: controlling the light emitting element to emit light at least twice, for the one frame based on the grayscale data for the one frame through the display driving circuit.
13. The method of claim 11, further comprising: controlling a time for applying a bias of the second output transistor by adjusting the time in which the second initialization transistor is turned on through the display driving circuit.
14. The method of claim 11, further comprising: reflecting a compensation value for a device characteristic of the second output transistor in the grayscale data through the display driving circuit.
15. The method of claim 14, wherein information about the device characteristic of the second output transistor is stored in a memory of the electronic device.

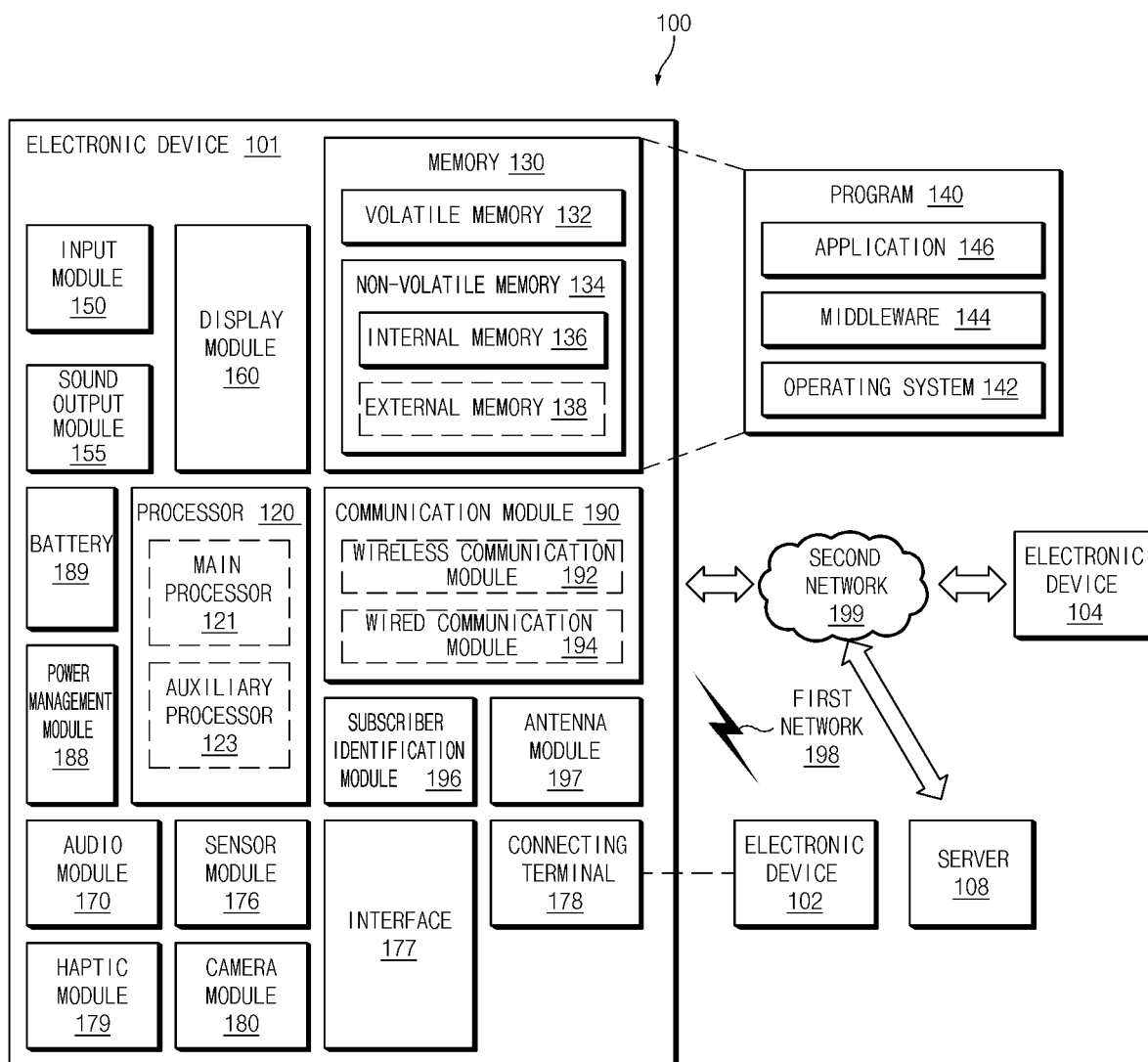


FIG.1

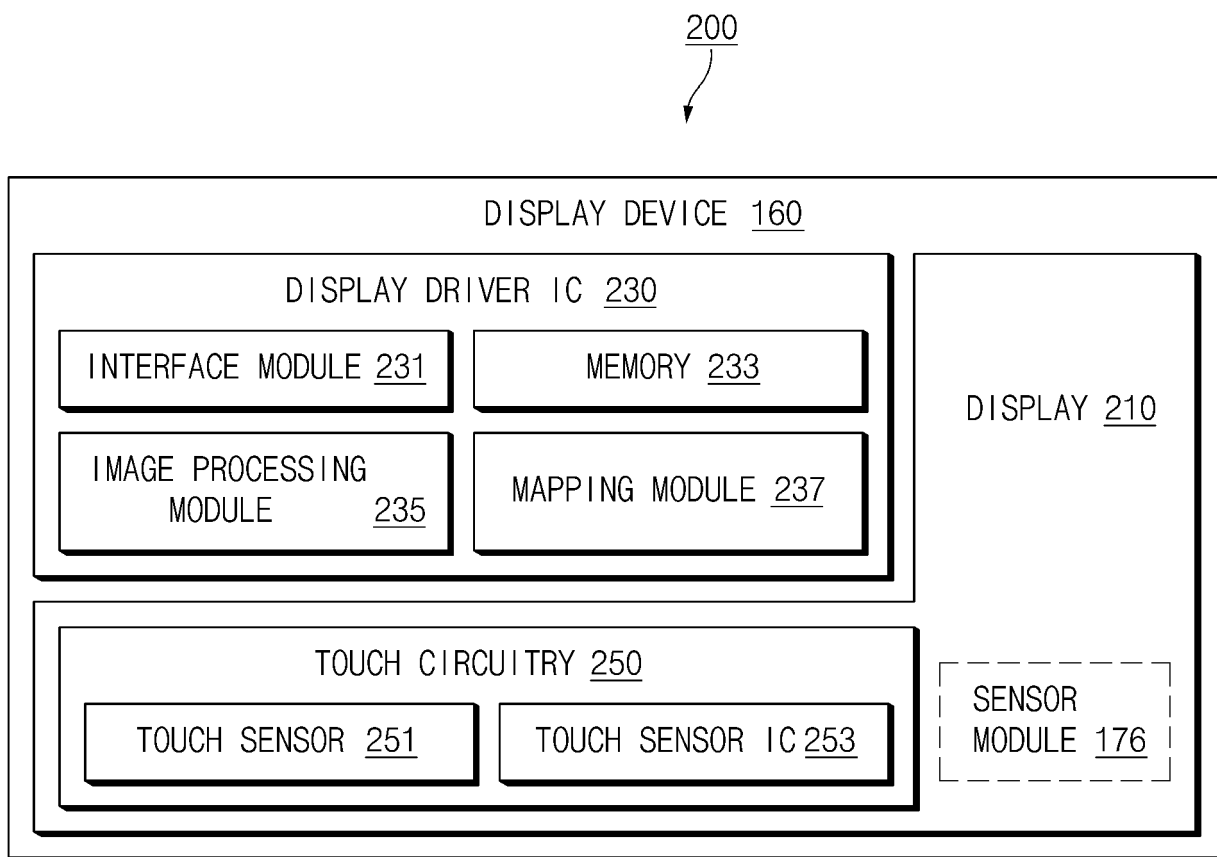


FIG.2

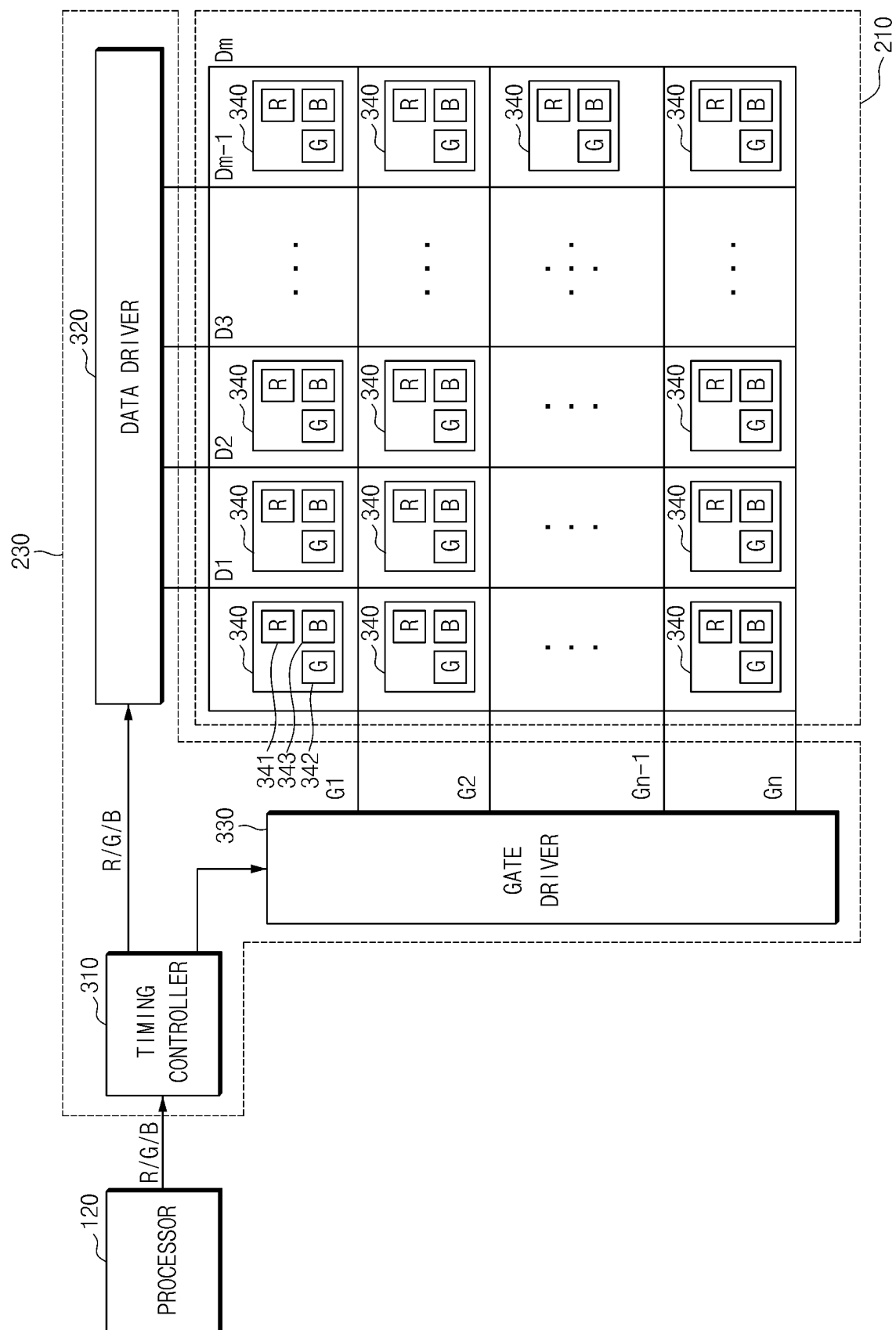


FIG. 3

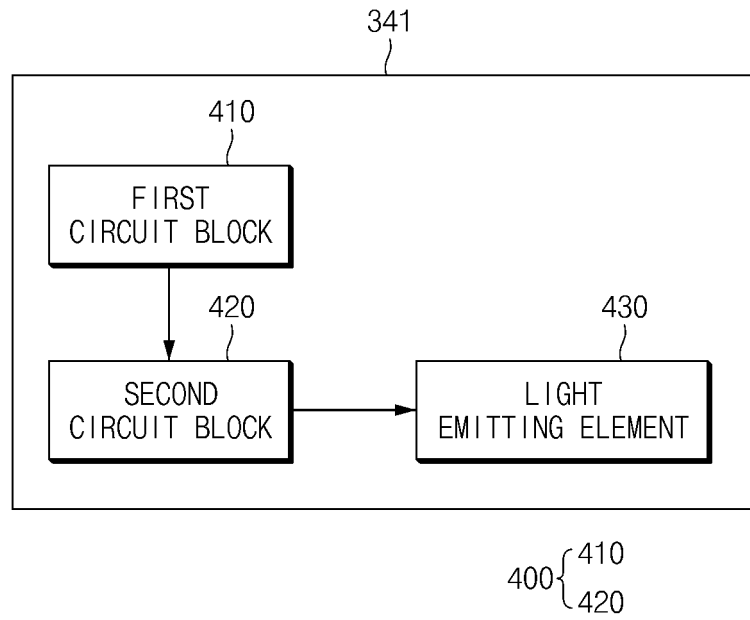


FIG.4

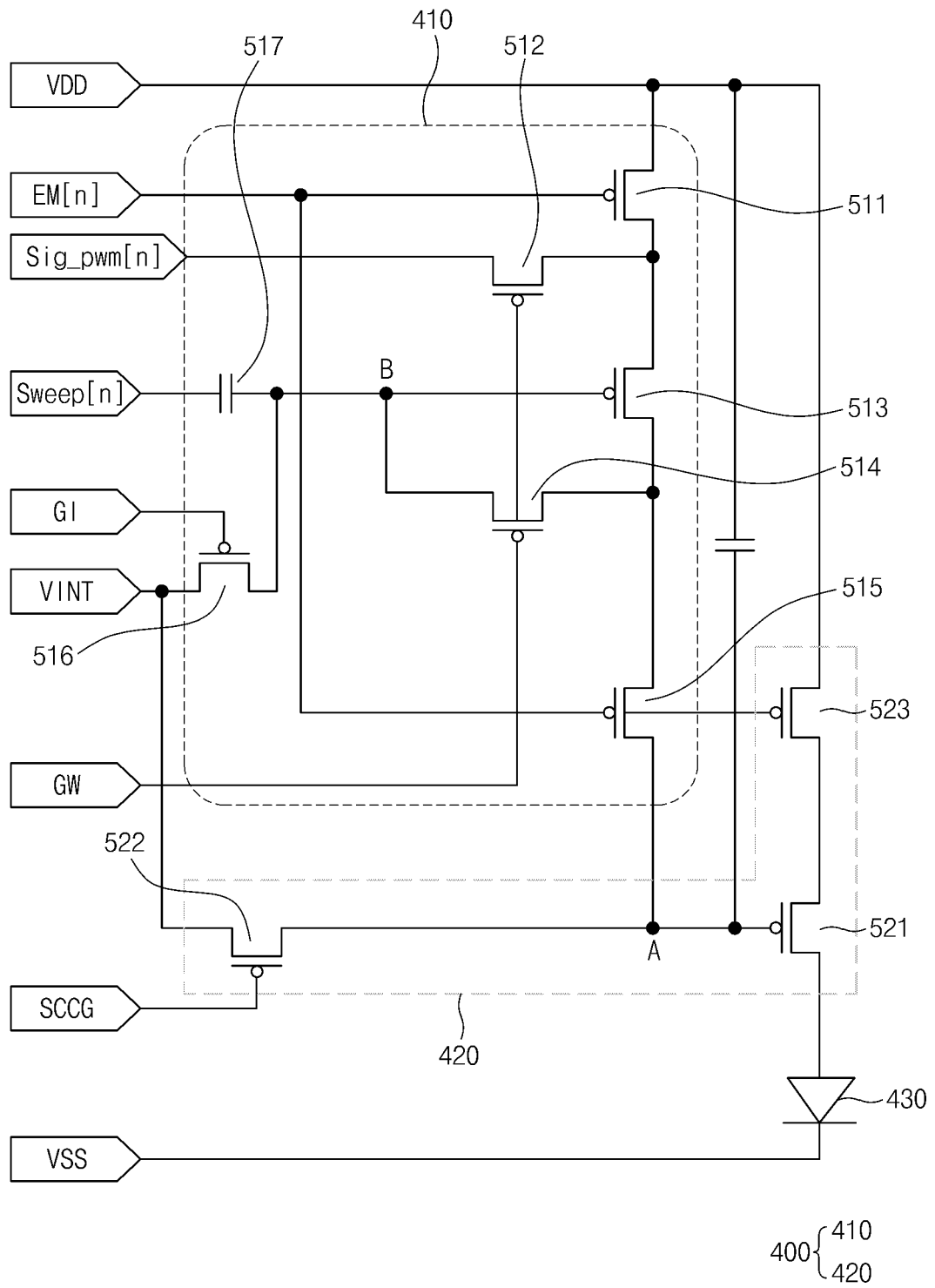


FIG.5

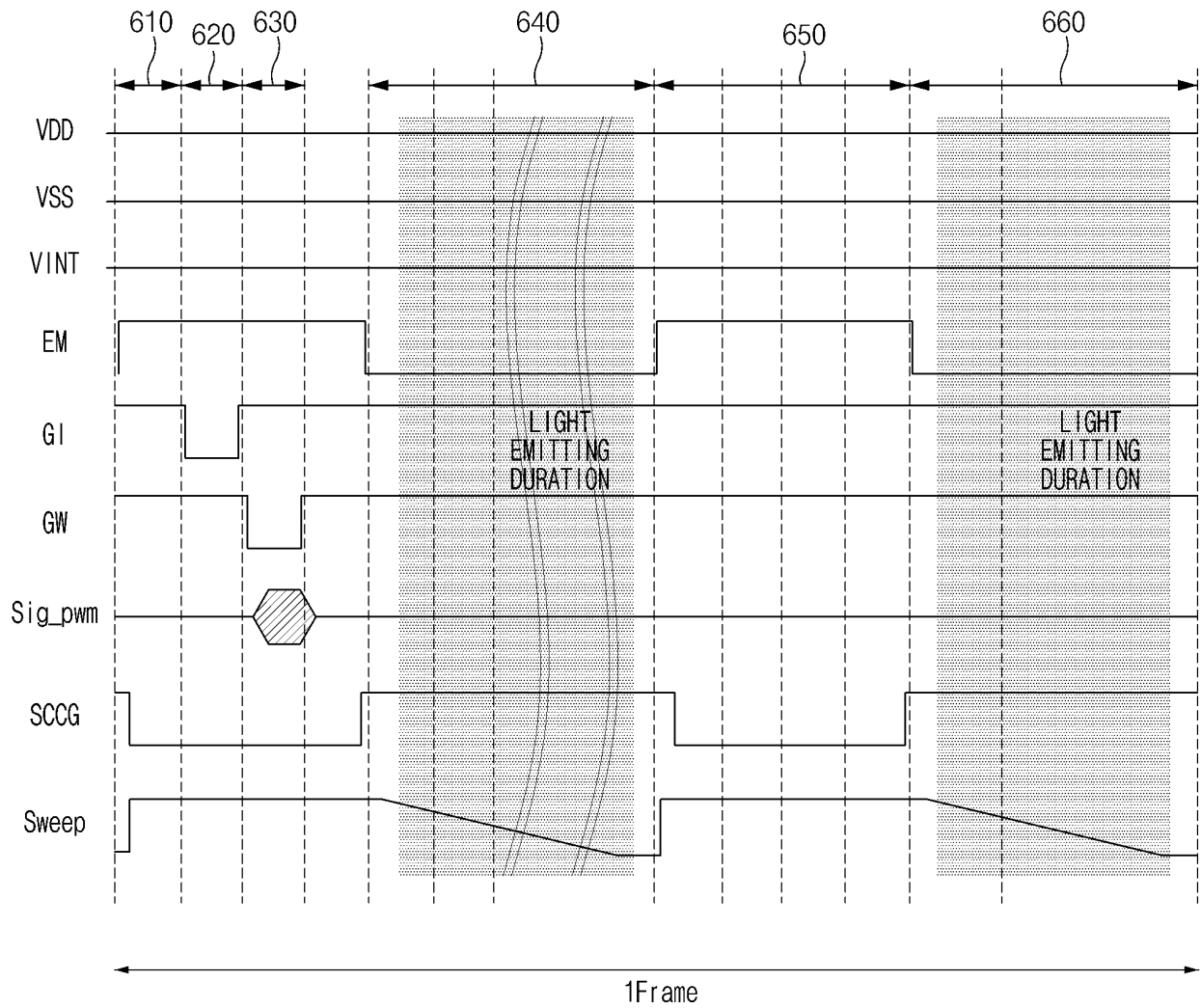


FIG.6

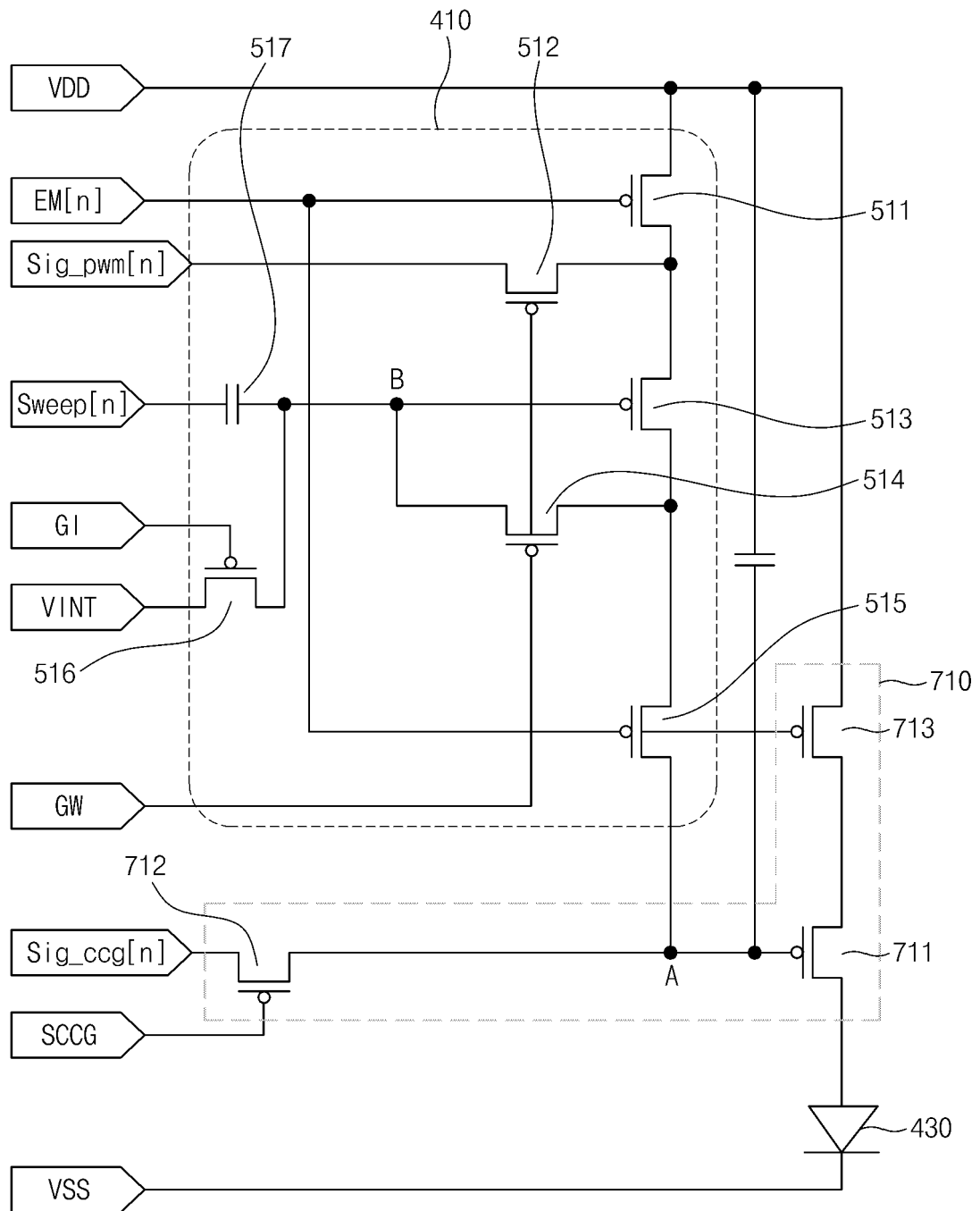


FIG.7

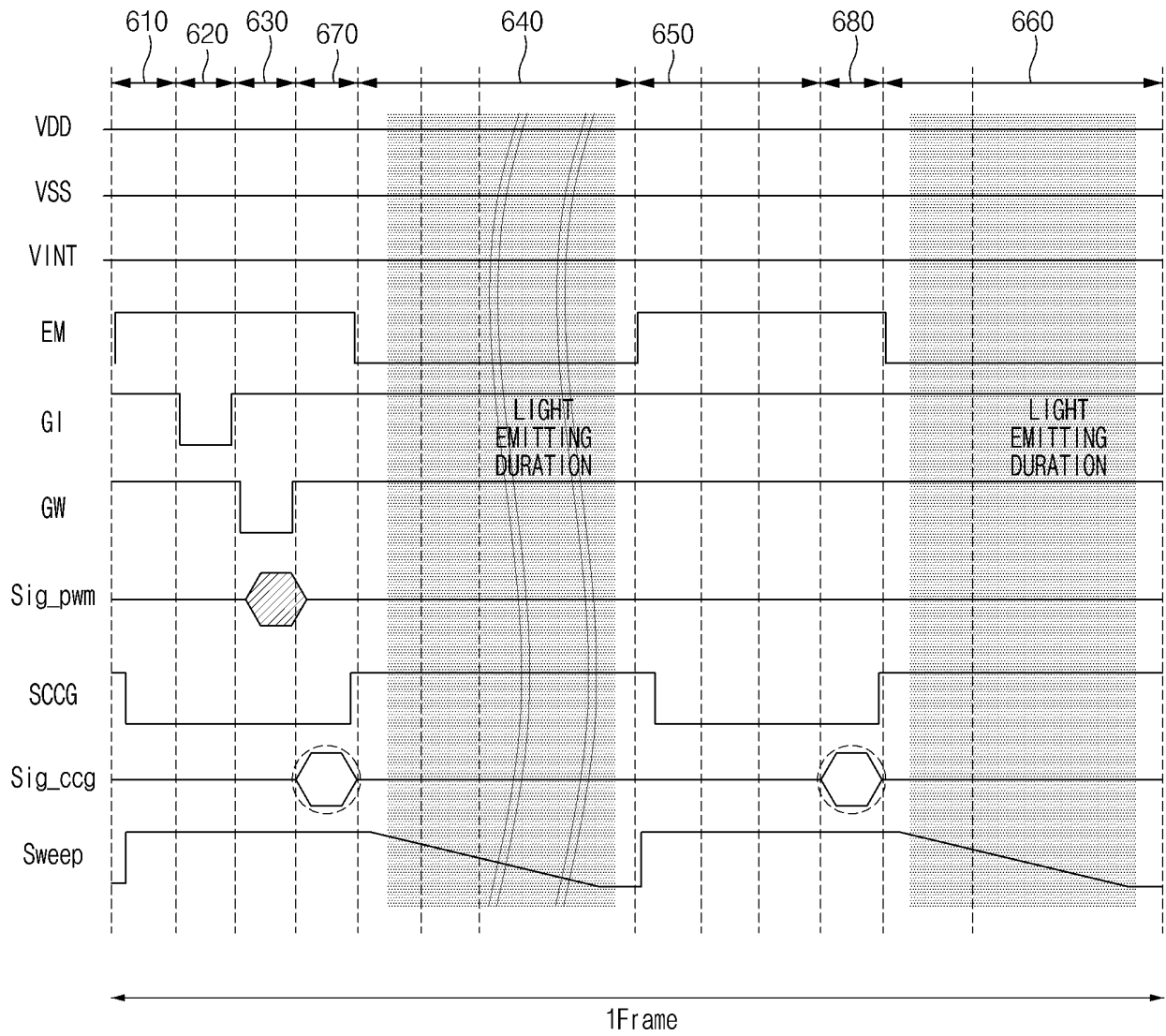


FIG.8

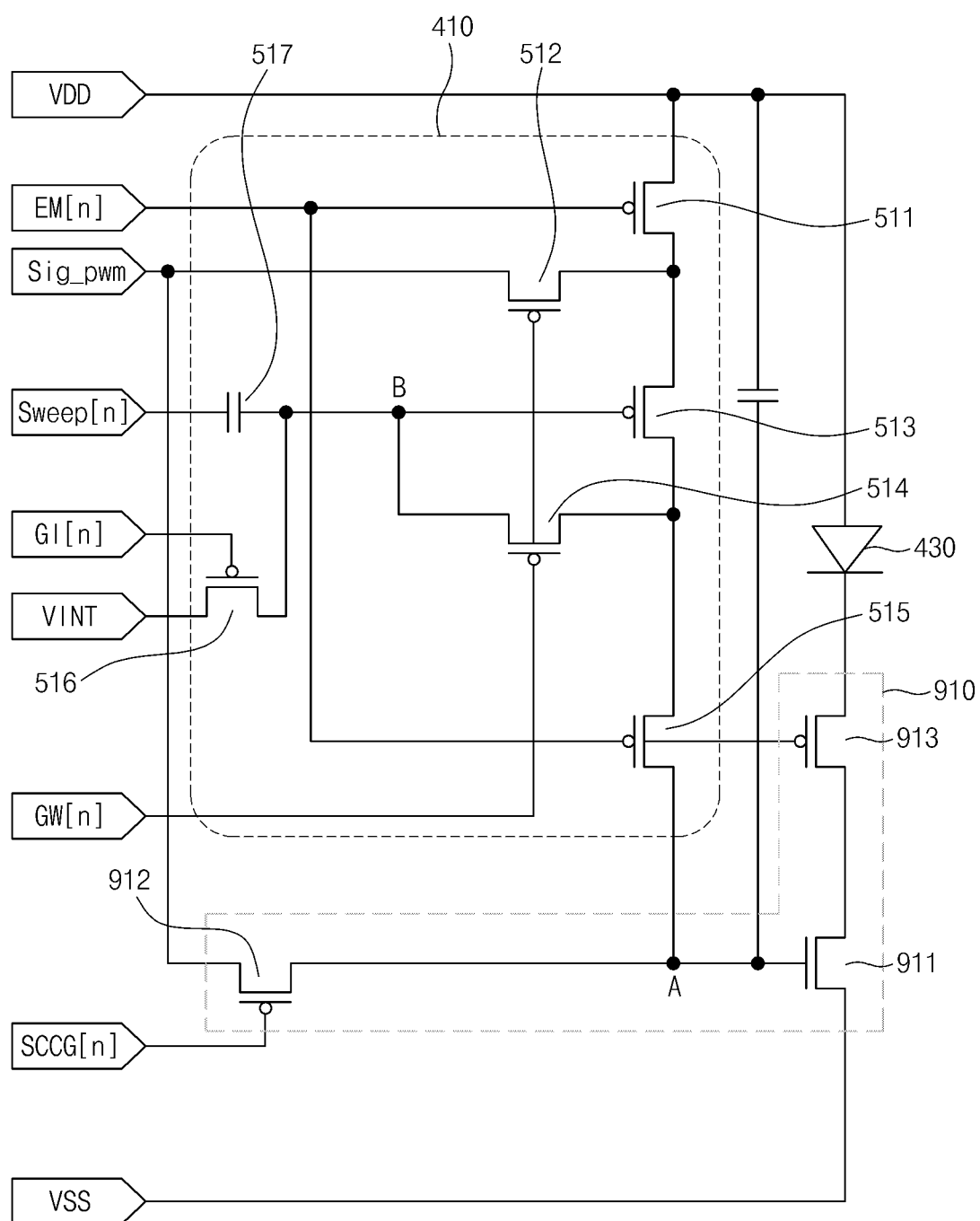


FIG. 9

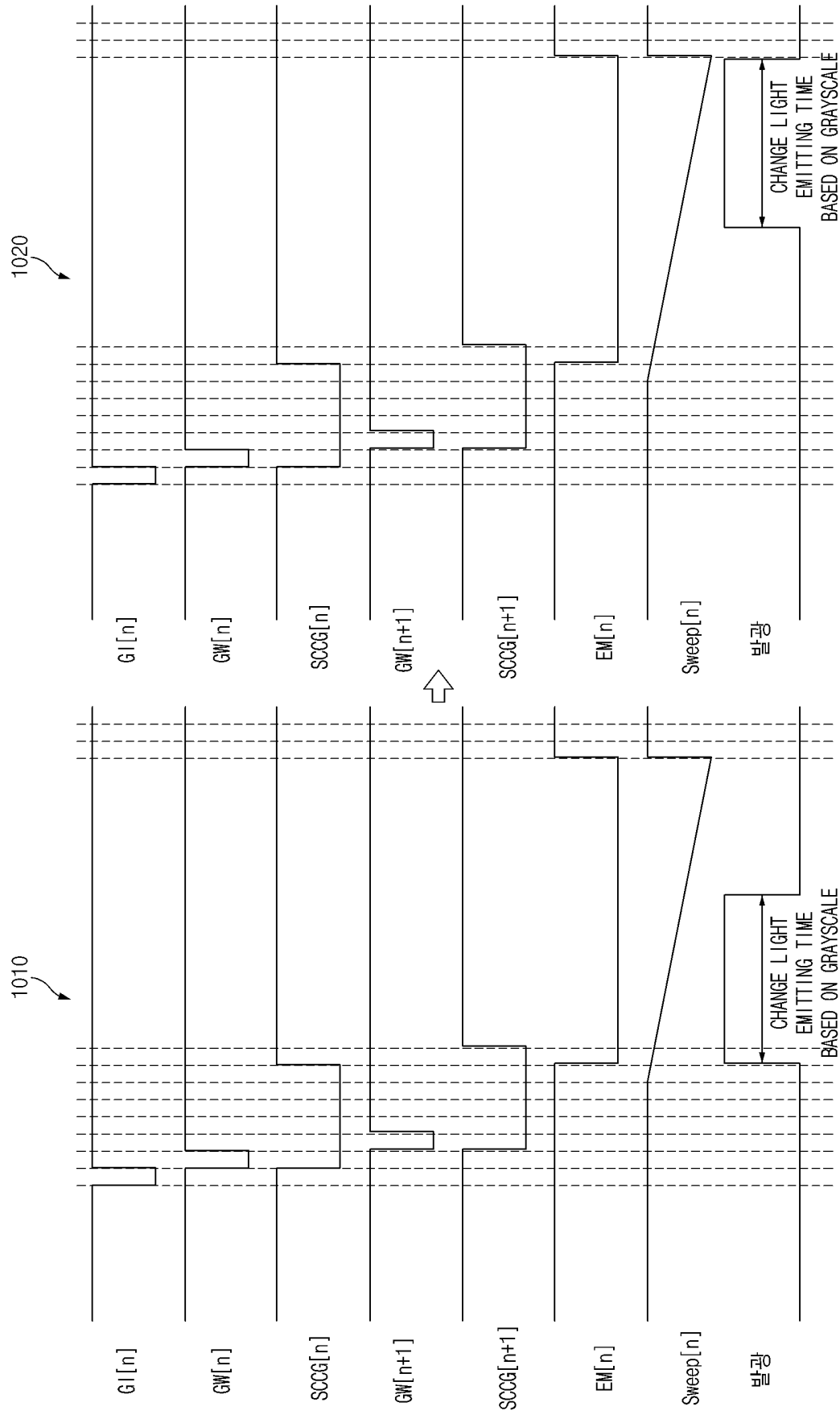


FIG.10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR2022/005366

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/32(2006.01); G09G 3/36(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models: IPC as above

Japanese utility models and applications for utility models: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIP0 internal) & keywords: 제1 회로 블록(first circuit block), 제2 회로 블록(second circuit block), 발광 소자(light emitting element), 구동 전류(driving current), 제1 출력 트랜지스터(first output transistor), 제2 출력 트랜지스터(second output transistor), 초기화(initialization)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 10-2020-0144050 A (SAMSUNG ELECTRONICS CO., LTD.) 28 December 2020 (2020-12-28) See paragraphs [0042]-[0155] and [0314]; and figures 3-7c.	1-15
Y	KR 10-2020-0085249 A (SAPIEN SEMICONDUCTORS INC.) 14 July 2020 (2020-07-14) See paragraphs [0083]-[0090]; claim 1; and figure 10.	1-15
A	KR 10-2020-0038735 A (SAMSUNG ELECTRONICS CO., LTD. et al.) 14 April 2020 (2020-04-14) See paragraphs [0122]-[0187]; and figures 9-10.	1-15
A	KR 10-2017-0035058 A (LG DISPLAY CO., LTD.) 30 March 2017 (2017-03-30) See paragraphs [0055]-[0090]; and figures 10-18.	1-15
A	US 2015-0002558 A1 (SAMSUNG DISPLAY CO., LTD.) 01 January 2015 (2015-01-01) See paragraphs [0046]-[0086]; and figures 1-7.	1-15

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"E" earlier application or patent but published on or after the international filing date	"&" document member of the same patent family
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search 22 July 2022	Date of mailing of the international search report 25 July 2022
Name and mailing address of the ISA/KR Korean Intellectual Property Office Government Complex-Daejeon Building 4, 189 Cheongsaro, Seo-gu, Daejeon 35208 Facsimile No. +82-42-481-8578	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 2019)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/KR2022/005366

Patent document cited in search report	Publication date (day/month/year)	Patent family member(s)	Publication date (day/month/year)
KR 10-2020-0144050 A	28 December 2020	CN 112102772 A	18 December 2020
		EP 3754639 A1	23 December 2020
		KR 10-2020-0144039 A	28 December 2020
		KR 10-2020-0144041 A	28 December 2020
		US 2020-0394953 A1	17 December 2020
		WO 2020-256385 A1	24 December 2020
KR 10-2020-0085249 A	14 July 2020	CN 111602191 A	28 August 2020
		KR 10-1942466 B1	17 April 2019
		KR 10-2020-0055593 A	21 May 2020
		KR 10-2021-0066764 A	07 June 2021
		KR 10-2131266 B1	07 July 2020
		KR 10-2256737 B1	31 May 2021
		US 11238783 B2	01 February 2022
		US 2021-0049957 A1	18 February 2021
		US 2021-0118358 A1	22 April 2021
		US 2022-0101784 A1	31 March 2022
		WO 2020-004705 A1	02 January 2020
		WO 2020-004743 A1	02 January 2020
KR 10-2020-0038735 A	14 April 2020	CN 111009210 A	14 April 2020
		TW 202015020 A	16 April 2020
		US 10706766 B2	07 July 2020
		US 2020-0111404 A1	09 April 2020
		WO 2020-071594 A1	09 April 2020
KR 10-2017-0035058 A	30 March 2017	None	
US 2015-0002558 A1	01 January 2015	JP 2015-011274 A	19 January 2015
		KR 10-2015-0003667 A	09 January 2015
		KR 10-2198874 B1	06 January 2021
		US 10068527 B2	04 September 2018
		US 2017-0004774 A1	05 January 2017
		US 9437136 B2	06 September 2016

Form PCT/ISA/210 (patent family annex) (July 2019)