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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: HIGH MOBILITY TRANSISTORS

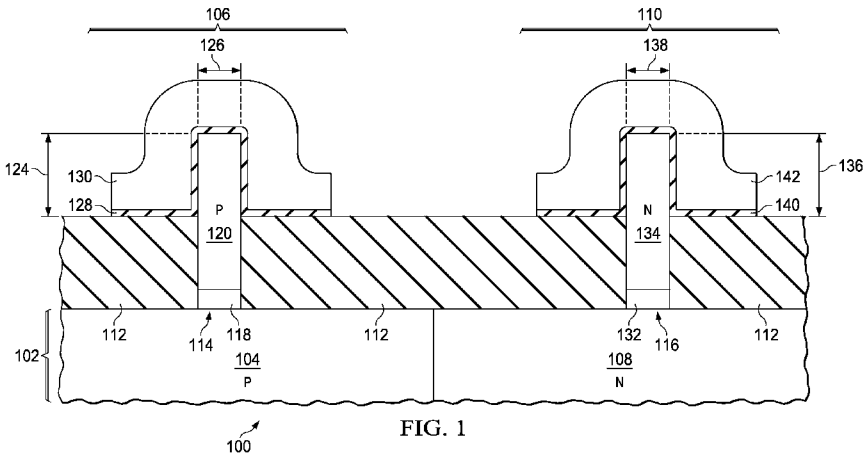

FIG. 1

(57) Abstract: An integrated circuit (100) containing an n-channel finFET (106) and a p-channel finFET (110) has a dielectric layer (112) over a silicon substrate (102). The fins of the finFETs (106, 110) have semiconductor materials with higher mobilities than silicon. A fin of the n-channel finFET (106) is on a first silicon-germanium buffer (118) in a first trench (114) through the dielectric layer (112) on the substrate (102). A fin of the p-channel finFET (110) is on a second silicon-germanium buffer (132) in a second trench (116) through the dielectric layer (112) on the substrate (102). The fins extend at least 10 nanometers above the dielectric layer (112). The fins are formed by epitaxial growth on the silicon-germanium buffers (118, 132) in the trenches (114, 116) in the dielectric layer (112), followed by CMP planarization down to the dielectric layer (112). The dielectric layer (112) is recessed to expose the fins. The fins may be formed concurrently or separately.

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HIGH MOBILITY TRANSISTORS

BACKGROUND

[0001] This relates in general to integrated circuits, and in particular to MOS transistors in integrated circuits.

[0002] Integrated circuits having fin field effect transistors (finFETs) attain high gate density, but lack transistor performance offered by planar transistors using high mobility materials, such as III-V materials or germanium. Integrating high mobility materials into high density integrated circuits has been problematic.

SUMMARY

[0003] An integrated circuit containing an n-channel finFET and a p-channel finFET may be formed by forming a dielectric layer over a silicon substrate. A first trench for a fin of the n-channel finFET is formed through the dielectric layer. A first silicon-germanium buffer is formed on the substrate in the first trench, and the n-channel fin of the n-channel finFET is formed by epitaxial growth on the first silicon-germanium buffer layer. A second trench for a p-channel fin of the p-channel finFET is formed through the dielectric layer. A second silicon-germanium buffer is formed on the substrate in the second trench, and the p-channel fin is formed by epitaxial growth on the second silicon-germanium buffer layer. Subsequently, the dielectric layer is recessed to expose the fins.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a cross section of an example integrated circuit containing an n-channel finFET and a p-channel finFET.

[0005] FIG. 2A through FIG. 2M are cross sections of the integrated circuit of FIG. 1, depicted in successive stages of an example fabrication sequence.

[0006] FIG. 3A through FIG. 3G are cross sections of the integrated circuit of FIG. 1, depicted in successive stages of another example fabrication sequence.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0007] An integrated circuit containing an n-channel finFET and a p-channel finFET may be formed by either of two process sequences. In the first sequence, a dielectric layer is formed over a silicon substrate. A first trench for an n-channel fin of the n-channel finFET is formed through the dielectric layer to expose the substrate. A first silicon-germanium buffer is formed on the substrate in the first trench, and the n-channel fin is formed by epitaxial growth of high

electron mobility material on the first silicon-germanium buffer layer, extending above the dielectric layer. An epitaxy blocking layer is formed over the dielectric layer and the n-channel fin. A second trench for a p-channel fin of the p-channel finFET is formed through the cap layer and the dielectric layer to expose the substrate. A second silicon-germanium buffer is formed on the substrate in the second trench, and the p-channel fin is formed by epitaxial growth of high hole mobility material on the second silicon-germanium buffer layer, extending above the dielectric layer. The n-channel fin and the p-channel fin may each be doped during growth. A cap layer is formed over the epitaxy blocking layer and the p-channel fin. A CMP process removes the cap layer and the epitaxy blocking layer and planarizes the n-channel fin and the p-channel fin down to the dielectric layer. Subsequently, the dielectric layer is recessed to expose the n-channel fin and the p-channel fin. Subsequently, gate dielectric layers are formed over the n-channel fin and the p-channel fin and gates are formed on the gate dielectric layer.

[0008] In the second sequence, a dielectric layer is formed over a silicon substrate, and the first trench for the n-channel fin and the second trench for the p-channel fin are formed concurrently through the dielectric layer to expose the substrate. The first silicon-germanium buffer and the second silicon-germanium buffer are concurrently formed on the substrate in the first trench and in the second trench, respectively. The n-channel fin and the p-channel fin are concurrently formed by epitaxial growth of high mobility material on the first silicon-germanium buffer and on the second silicon-germanium buffer layer, respectively, extending above the dielectric layer. The n-channel fin and the p-channel fin may possibly be doped during formation, and one fin implanted with dopants to counterdope the in-situ dopants. Alternatively, the n-channel fin and the p-channel fin may be implanted with dopants to provide desired doping densities. A cap layer is formed over the dielectric layer and the n-channel fin and the p-channel fin. A CMP process removes the cap layer and planarizes the n-channel fin and the p-channel fin down to the dielectric layer. Subsequently, the dielectric layer is recessed to expose the n-channel fin and the p-channel fin. Subsequently, gate dielectric layers are formed over the n-channel fin and the p-channel fin and gates are formed on the gate dielectric layer.

[0009] FIG. 1 is a cross section of an example integrated circuit containing an n-channel finFET and a p-channel finFET. The integrated circuit 100 is formed on a single crystal silicon substrate 102 which includes a p-type region 104 in an area for the n-channel finFET 106, and includes an n-type region 108 in an area for the p-channel finFET 110. The substrate 102 may

be a bulk silicon wafer, or an epitaxial layer on a silicon wafer. A dielectric layer 112 is disposed over the substrate 102. The dielectric layer 112 may include one or more layers of silicon dioxide, and possibly other dielectric material such as silicon oxynitride and/or boron phosphorus silicate glass (BPSG). The dielectric layer 112 may be 20 nanometers to 40 nanometers thick. A first trench 114 is disposed through the dielectric layer 112 in the area for the n-channel finFET 106. A second trench 116 is disposed through the dielectric layer 112 in the area for the p-channel finFET 110.

[0010] The n-channel finFET 106 includes a first silicon-germanium buffer 118 disposed on the p-type region 104 of the substrate 102 in the first trench 114. The first silicon-germanium buffer 118 may be 1 nanometer to 5 nanometers thick, and may have a graded composition such that the first silicon-germanium buffer 118 has a germanium atomic fraction at the substrate 102 of less than 20 percent and has a germanium atomic fraction at a top surface of the first silicon-germanium buffer 118 over 80 percent. The n-channel finFET 106 includes an n-channel fin 120 on the first silicon-germanium buffer 118, extending above a top surface 122 of the dielectric layer 112 by an exposure height 124 of at least 10 nanometers. The exposure height 124 may be 20 nanometers to 40 nanometers. An average width 126 of the n-channel fin 120 above the top surface 122 of the dielectric layer 112 may be less than 30 nanometers, such as 10 nanometers to 20 nanometers. The n-channel fin 120 substantially fills the first trench 114 at the top surface 122 of the dielectric layer 112. The n-channel fin 120 is doped p-type to provide a desired threshold voltage for the n-channel finFET 106. The n-channel fin 120 is primarily semiconductor material different from silicon, possibly with an electron mobility higher than silicon. For example, the semiconductor material may be a III-V compound semiconductor material, such as gallium arsenide, indium gallium arsenide, possibly with an indium to gallium ratio of 50:50 to 57:43, or indium phosphide. Alternatively, the semiconductor material may be germanium or silicon-germanium with a germanium atomic fraction greater than 80 percent. Forming the n-channel fin 120 with the semiconductor material having an electron mobility higher than silicon advantageously provides a desired on-state current in the n-channel finFET 106. The n-channel finFET 106 includes a first gate dielectric layer 128 disposed over, and extending along sides of, the n-channel fin 120. The n-channel finFET 106 includes a first gate 130 disposed over the first gate dielectric layer 128, extending at least partway down to the top surface 122 of the dielectric layer 112. The first gate 130 may include polycrystalline silicon,

referred to as polysilicon, may include metal silicide, or may be a metal gate.

[0011] The p-channel finFET 110 includes a second silicon-germanium buffer 132 disposed on the n-type region 108 of the substrate 102 in the second trench 116. The second silicon-germanium buffer 132 may also be 1 nanometer to 5 nanometers thick, and may also have a graded composition similar to the first silicon-germanium buffer 118. The p-channel finFET 110 includes a p-channel fin 134 on the second silicon-germanium buffer 132, extending above the top surface 122 of the dielectric layer 112 by an exposure height 136 of at least 10 nanometers. The exposure height 136 of the p-channel fin 134 may be substantially equal to the exposure height 124 of the n-channel fin 120. An average width 138 of the p-channel fin 134 above the top surface 122 of the dielectric layer 112 may also be less than 30 nanometers, such as 10 nanometers to 20 nanometers. The p-channel fin 134 substantially fills the second trench 116 at the top surface 122 of the dielectric layer 112. The p-channel fin 134 is doped n-type to provide a desired threshold voltage for the p-channel finFET 110. The p-channel fin 134 is primarily semiconductor material different from silicon, possibly with a hole mobility higher than silicon. For example, the semiconductor material may be a III-V compound semiconductor material, such as gallium arsenide, or may be germanium or silicon-germanium with a germanium atomic fraction greater than 80 percent. In one version of the instant example, the n-channel fin 120 and the p-channel fin 134 may be primarily formed of the same semiconductor material. Forming the p-channel fin 134 with the semiconductor material having a hole mobility higher than silicon advantageously provides a desired on-state current in the p-channel finFET 110. The p-channel finFET 110 includes a second gate dielectric layer 140 disposed over, and extending along sides of, the p-channel fin 134. The p-channel finFET 110 includes a second gate 142 disposed over the second gate dielectric layer 140, extending at least partway down to the top surface 122 of the dielectric layer 112. The second gate 142 may include polysilicon, may include metal silicide, or may be a metal gate.

[0012] FIG. 2A through FIG. 2M are cross sections of the integrated circuit of FIG. 1, depicted in successive stages of an example fabrication sequence. Referring to FIG. 2A, the silicon substrate 102 is provided for forming the integrated circuit 100. The dielectric layer 112 is formed over the substrate 102 with an initial thickness of 50 nanometers to 100 nanometers. The dielectric layer 112 may be formed by thermal oxidation of the silicon in the substrate 102, or may be formed by a deposition process, such as a plasma enhanced chemical vapor deposition

(PECVD) process using tetraethyl orthosilicate, also known as tetraethoxysilane (TEOS). The dielectric layer 112 may include one or more layers of other dielectric material such as silicon oxynitride or BPSG.

[0013] A first trench mask 144 is formed over the dielectric layer 112 so as to expose an area for the first trench 114 of FIG. 1 and to cover the area for the p-channel finFET 110. The first trench mask 144 may include an antireflection layer and a photoresist pattern formed by a photolithographic process.

[0014] Referring to FIG. 2B, the first trench 114 is formed through the dielectric layer 112 to expose the substrate 102 by etching the dielectric layer 112 in areas exposed by the first trench mask 144. The dielectric layer 112 may be etched using a reactive ion etch (RIE) process. After the first trench 114 is formed, the first trench mask 144 is removed, such as by ashing followed by a wet clean process.

[0015] Referring to FIG. 2C, the first silicon-germanium buffer 118 is formed on the substrate 102 in the first trench 114. Formation of the first silicon-germanium buffer 118 may be preceded by a hydrogen bake at 750 °C to 850 °C. The first silicon-germanium buffer 118 may be grown by an epitaxial process using silane or dichlorosilane and germane with hydrogen chloride at a temperature of 750 °C to 850 °C. The ratio of silane or dichlorosilane to germane may be varied so that the atomic fraction of germanium at the substrate 102 is less than 20 percent and the atomic fraction of germanium at the top of the first silicon-germanium buffer 118 is greater than 80 percent, to advantageously provide good lattice matching to the substrate 102 and to the to-be-formed n-channel fin 120. The epitaxy process used for forming the first silicon-germanium buffer 118 does not deposit silicon-germanium on sidewalls of the first trench 114 so as to significantly reduce a width of the first trench 114.

[0016] Referring to FIG. 2D, the n-channel fin 120 may be formed by a vapor phase epitaxial process on the first silicon-germanium buffer 118, extending past the top surface 122 of the dielectric layer 112. The first silicon-germanium buffer 118 advantageously facilitates epitaxial growth of the semiconductor material of the n-channel fin 120, which would be problematic to grow directly on the silicon substrate 102. In a version of the instant example in which the n-channel fin 120 is primarily indium gallium arsenide, the epitaxial process may use trimethyl indium, trimethyl gallium or triethyl gallium, and arsine at a pressure of 150 torr and a temperature of 750 °C to 850 °C. A ratio of the trimethyl indium to the trimethyl gallium may

be varied to obtain a desired ratio of indium to gallium in the n-channel fin 120. In a version of the instant example in which the n-channel fin 120 is primarily gallium arsenide, the epitaxial process may use trimethyl gallium or triethyl gallium and arsine. In a version of the instant example in which the n-channel fin 120 is primarily indium phosphide, the epitaxial process may use trimethyl indium and phosphine. In a version of the instant example in which the n-channel fin 120 is primarily germanium, the epitaxial process may use germane. In a version of the instant example in which the n-channel fin 120 is primarily silicon-germanium, the epitaxial process may use silane or dichlorosilane and germane. Alternatively, the n-channel fin 120 may be formed by a molecular beam epitaxy (MBE) process.

[0017] Referring to FIG. 2E, an epitaxy blocking layer 146 is formed over the dielectric layer 112, covering the n-channel fin 120. The epitaxy blocking layer 146 may include silicon nitride or silicon oxynitride, 20 nanometers to 30 nanometers thick. The epitaxy blocking layer 146 may be formed by a low pressure chemical vapor deposition (LPCVD) process using dichlorosilane and ammonia at 650 °C to 750 °C.

[0018] Referring to FIG. 2F, a second trench mask 148 is formed over the epitaxy blocking layer 146 so as to expose an area for the second trench 116 of FIG. 1 and to cover the area for the n-channel finFET 106. The second trench mask 148 may include an antireflection layer and a photoresist pattern formed by a photolithographic process.

[0019] Referring to FIG. 2G, the second trench 116 is formed through the epitaxy blocking layer 146 and the dielectric layer 112 to expose the substrate 102 by etching the epitaxy blocking layer 146 and the dielectric layer 112 in areas exposed by the second trench mask 148. The epitaxy blocking layer 146 and the dielectric layer 112 may be etched using an RIE process. After the second trench 116 is formed, the second trench mask 148 is removed, such as by ashing followed by a wet clean process.

[0020] Referring to FIG. 2H, the second silicon-germanium buffer 132 is formed on the substrate 102 in the second trench 116. Formation of the second silicon-germanium buffer 132 may use a same or similar process as used for forming the first silicon-germanium buffer 118. The atomic fraction of germanium at the substrate 102 may be less than 20 percent and the atomic fraction of germanium at the top of the second silicon-germanium buffer 132 may be greater than 80 percent, to advantageously provide good lattice matching to the substrate 102 and to the to-be-formed p-channel fin 134.

[0021] Referring to FIG. 2I, the p-channel fin 134 is formed on the second silicon-germanium buffer 132, extending past the top surface 122 of the dielectric layer 112, and possibly past a top surface of the epitaxy blocking layer 146 as shown in FIG. 2H. The second silicon-germanium buffer 132 advantageously facilitates epitaxial growth of the semiconductor material of the p-channel fin 134, which would be problematic to grow directly on the silicon substrate 102. The p-channel fin 134 may be primarily germanium, or primarily silicon-germanium, and may be formed by a vapor phase epitaxial process as described in reference to FIG. 2D. Alternatively, the p-channel fin 134 may be formed by an MBE process.

[0022] Referring to FIG. 2J, a cap layer 150 is formed over the epitaxy blocking layer 146, covering the p-channel fin 134. The cap layer 150 may include silicon dioxide, silicon nitride, and/or silicon oxynitride, 20 nanometers to 30 nanometers thick. The cap layer 150 may be formed by a PECVD process using TEOS for silicon dioxide and/or bis (tertiary-butylamino) silane (BTBAS) for silicon nitride, at 500 °C to 600 °C.

[0023] Referring to FIG. 2K, a CMP process 152, depicted schematically as a CMP Pad 152, removes the cap layer 150 of FIG. 2J and the epitaxy blocking layer 146 and planarizes the n-channel fin 120 and the p-channel fin 134 down to the dielectric layer 112. An endpoint for the CMP process 152 may be provided by a change in polishing resistance between the epitaxy blocking layer 146 and the dielectric layer 112, due to the epitaxy blocking layer 146 including silicon nitride or silicon oxynitride, and the dielectric layer 112 including silicon dioxide.

[0024] FIG. 2L depicts the integrated circuit 100 after the CMP process 152 of FIG. 2K is completed. The n-channel fin 120 and the p-channel fin 134 may be substantially coplanar with the top surface 122 of the dielectric layer 112.

[0025] Referring to FIG. 2M, the dielectric layer 112 is recessed without significantly removing semiconductor material from the n-channel fin 120 and the p-channel fin 134 so that the n-channel fin 120 and the p-channel fin 134 extend at least 10 nanometers above the recessed dielectric layer 112. The dielectric layer 112 may be recessed by a plasma etch which is selective to the dielectric material, such as silicon dioxide, of the dielectric layer 112 relative to the semiconductor material of the n-channel fin 120 and the p-channel fin 134. Alternatively, the dielectric layer 112 may be recessed by a wet etch, such as a dilute buffered aqueous solution of hydrofluoric acid, which is selective to the dielectric material, such as silicon dioxide, of the dielectric layer 112 relative to the semiconductor material of the n-channel fin 120 and the

p-channel fin 134. After the dielectric layer 112 is recessed, gate dielectric layers and gates are formed over the n-channel fin 120 and the p-channel fin 134 to provide the structure of FIG. 1. The structure of FIG. 2M may also be obtained by an alternative example fabrication sequence in which the p-channel fin 134 is formed before the n-channel fin 120.

[0026] FIG. 3A through FIG. 3G are cross sections of the integrated circuit of FIG. 1, depicted in successive stages of another example fabrication sequence. Referring to FIG. 3A, the silicon substrate 102 is provided for forming the integrated circuit 100. The dielectric layer 112 is formed over the substrate 102 with an initial thickness of 50 nanometers to 100 nanometers. A trench mask 154 is formed over the dielectric layer 112 so as to expose areas for the first trench 114 and the second trench 116 of FIG. 1. The first trench 114 and the second trench 116 are formed through the dielectric layer 112 to expose the substrate 102 by etching the dielectric layer 112 in areas exposed by the trench mask 154. After the first trench 114 and the second trench 116 are formed, the trench mask 154 is removed.

[0027] Referring to FIG. 3B, the first silicon-germanium buffer 118 and the second silicon-germanium buffer 132 are formed concurrently on the substrate 102 in the first trench 114 and the second trench 116, respectively, as described in reference to FIG. 2C and FIG. 2H. In the instant example, the first silicon-germanium buffer 118 and the second silicon-germanium buffer 132 have a same composition and same profile of the germanium atomic fraction.

[0028] The n-channel fin 120 and the p-channel fin 134 are formed concurrently on the first silicon-germanium buffer 118 and the second silicon-germanium buffer 132, respectively, extending past the top surface 122 of the dielectric layer 112, as described in reference to FIG. 2D and FIG. 2I. In the instant example, the n-channel fin 120 and the p-channel fin 134 have a same composition. The semiconductor material of the n-channel fin 120 and the p-channel fin 134 has a higher electron mobility and a higher hole mobility than silicon. The semiconductor material of the n-channel fin 120 and the p-channel fin 134 may be substantially undoped or lightly doped, may be doped n-type during the epitaxial growth process, or may be doped p-type during the epitaxial growth process. Forming the n-channel fin 120 and the p-channel fin 134 concurrently may advantageously reduce fabrication cost and complexity of the integrated circuit 100.

[0029] Referring to FIG. 3C, an optional first implant mask 156 may be formed over the dielectric layer 112 so as to expose the p-channel fin 134 and to cover the n-channel fin 120.

N-type dopants 158 such as phosphorus and possibly arsenic may be implanted into the p-channel fin 134, if needed, at a dose which provides a desired threshold voltage for the p-channel finFET 110. The dose will depend on the desired threshold voltage and on a height of the p-channel fin 134. The first implant mask 156 is removed after the n-type dopants 158 are implanted. An anneal operation is subsequently performed to activate the implanted n-type dopants 158.

[0030] Referring to FIG. 3D, an optional second implant mask 160 may be formed over the dielectric layer 112 so as to expose the n-channel fin 120 and to cover the p-channel fin 134. P-type dopants 162 such as boron may be implanted into the n-channel fin 120, if needed, at a dose which provides a desired threshold voltage for the n-channel finFET 106. The dose will depend on the desired threshold voltage and on a height of the n-channel fin 120. The second implant mask 160 is removed after the p-type dopants 162 are implanted. An anneal operation is subsequently performed to activate the implanted p-type dopants 162.

[0031] Referring to FIG. 3E, the cap layer 150 is formed over the dielectric layer 112, covering the n-channel fin 120 and the p-channel fin 134. In the instant example, the cap layer 150 may include silicon nitride, and/or silicon oxynitride, 20 nanometers to 30 nanometers thick. The cap layer 150 may be formed as described in reference to FIG. 2J.

[0032] Referring to FIG. 3F, a CMP process 152, depicted schematically as a CMP Pad 152, removes the cap layer 150 and planarizes the n-channel fin 120 and the p-channel fin 134 down to the dielectric layer 112. An endpoint for the CMP process 152 may be provided by a change in polishing resistance between the cap layer 150 and the dielectric layer 112, due to the cap layer 150 including silicon nitride or silicon oxynitride, and the dielectric layer 112 including silicon dioxide.

[0033] Referring to FIG. 3G, the dielectric layer 112 is recessed without significantly removing semiconductor material from the n-channel fin 120 and the p-channel fin 134 so that the n-channel fin 120 and the p-channel fin 134 extend at least 10 nanometers above the recessed dielectric layer 112, as described in reference to FIG. 2M. After the dielectric layer 112 is recessed, gate dielectric layers and gates are formed over the n-channel fin 120 and the p-channel fin 134 to provide the structure of FIG. 1.

[0034] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a substrate including silicon, the substrate having a p-type region in an area for an n-channel fin field effect transistor (finFET) and having an n-type region in an area for a p-channel finFET;

a dielectric layer disposed over the substrate, the dielectric layer having a first trench down to the substrate in the area for the n-channel finFET and having a second trench down to the substrate in the area for the p-channel finFET;

a first silicon-germanium buffer disposed on the p-type region of the substrate in the first trench;

a second silicon-germanium buffer disposed on the n-type region of the substrate in the second trench;

an n-channel fin of the n-channel finFET disposed on the first silicon-germanium buffer, the n-channel fin extending at least 10 nanometers above a top surface of the dielectric layer, the n-channel fin having p-type doping, the n-channel fin including semiconductor material different from silicon; and

a p-channel fin of the p-channel finFET disposed on the second silicon-germanium buffer, the p-channel fin extending at least 10 nanometers above the top surface of the dielectric layer, the p-channel fin having n-type doping, the p-channel fin including semiconductor material different from silicon.

2. The integrated circuit of claim 1, wherein:

the first silicon-germanium buffer has a germanium atomic fraction at the substrate of less than 20 percent and has a germanium atomic fraction at a top surface of the first silicon-germanium buffer over 80 percent; and

the second silicon-germanium buffer has a germanium atomic fraction at the substrate of less than 20 percent and has a germanium atomic fraction at a top surface of the second silicon-germanium buffer over 80 percent.

3. The integrated circuit of claim 1, wherein the n-channel fin includes gallium arsenide.

4. The integrated circuit of claim 1, wherein the n-channel fin includes indium gallium arsenide.

5. The integrated circuit of claim 4, wherein the n-channel fin has an indium to gallium ratio of 50:50 to 57:43.

6. The integrated circuit of claim 1, wherein the n-channel fin includes indium phosphide.

7. The integrated circuit of claim 1, wherein the n-channel fin includes germanium.

8. The integrated circuit of claim 1, wherein the p-channel fin includes silicon-germanium.

9. The integrated circuit of claim 1, wherein the p-channel fin includes germanium.

10. A method of forming an integrated circuit, the method comprising:

providing a substrate including silicon, the substrate having a first region of a first conductivity type in an area for a first polarity finFET and having a second region of a second, opposite, conductivity type in an area for a second, opposite, polarity finFET;

forming a dielectric layer 50 nanometers to 100 nanometers thick over the substrate;

forming a first trench in the dielectric layer down to the substrate in the area for the first polarity finFET;

forming a first silicon-germanium buffer 1 nanometer to 5 nanometers thick on the substrate in the first trench;

forming a first polarity fin of the first polarity finFET on the first silicon-germanium buffer, so that the first polarity fin extends above a top surface of the dielectric layer;

forming an epitaxial blocking layer over the dielectric layer so as to cover the first polarity fin;

forming a second trench in the epitaxial blocking layer and the dielectric layer down to the substrate in the area for the second polarity finFET;

forming a second silicon-germanium buffer 1 nanometer to 5 nanometers thick on the substrate in the second trench;

forming a second polarity fin of the second polarity finFET on the second silicon-germanium buffer, so that the second polarity fin extends above a top surface of the dielectric layer;

forming a cap layer of dielectric material over the epitaxial blocking layer so as to cover the second polarity fin;

removing the cap layer and the epitaxial blocking layer by a chemical mechanical polish (CMP) process so as to planarize the first polarity fin and the second polarity fin down to the dielectric layer; and

recessing the dielectric layer so that the first polarity fin and the second polarity fin extend at least 10 nanometers above the dielectric layer.

11. The method of claim 10, wherein:

the first silicon-germanium buffer is formed to have a germanium atomic fraction at the substrate of less than 20 percent and a germanium atomic fraction at a top surface of the first silicon-germanium buffer over 80 percent; and

the second silicon-germanium buffer is formed to have a germanium atomic fraction at the substrate of less than 20 percent and a germanium atomic fraction at a top surface of the second silicon-germanium buffer over 80 percent.

12. The method of claim 10, wherein the n-channel fin includes gallium arsenide.

13. The method of claim 10, wherein the n-channel fin includes indium gallium arsenide.

14. The method of claim 13, wherein the n-channel fin has an indium to gallium ratio of 50:50 to 57:43.

15. The method of claim 10, wherein the n-channel fin includes indium phosphide.

16. The method of claim 10, wherein the n-channel fin includes germanium.

17. The method of claim 10, wherein the p-channel fin includes germanium.

18. A method of forming an integrated circuit, the method comprising:

providing a substrate including silicon, the substrate having a first region of a first conductivity type in an area for a first polarity finFET and having a second region of a second, opposite, conductivity type in an area for a second, opposite, polarity finFET;

forming a dielectric layer 50 nanometers to 100 nanometers thick over the substrate;

concurrently forming a first trench in the dielectric layer down to the substrate in the area for the first polarity finFET and a second trench in the dielectric layer down to the substrate in the area for the second polarity finFET;

concurrently forming a first silicon-germanium buffer 1 nanometer to 5 nanometers thick on the substrate in the first trench and a second silicon-germanium buffer 1 nanometer to 5 nanometers thick on the substrate in the second trench;

concurrently forming a first polarity fin of the first polarity finFET on the first silicon-germanium buffer and a second polarity fin of the second polarity finFET on the second silicon-germanium buffer, so that the first polarity fin and the second polarity fin extend above a top surface of the dielectric layer;

forming a cap layer of dielectric material over the dielectric layer so as to cover the first polarity fin and the second polarity fin;

removing the cap layer by a CMP process so as to planarize the first polarity fin and the second polarity fin down to the dielectric layer; and

recessing the dielectric layer so that the first polarity fin and the second polarity fin extend at least 10 nanometers above the dielectric layer.

19. The method of claim 18, wherein the first silicon-germanium buffer and the second silicon-germanium buffer are formed to have germanium atomic fractions at the substrate of less than 20 percent and germanium atomic fractions at top surfaces of the first silicon-germanium buffer and the second silicon-germanium buffer over 80 percent.

20. The method of claim 18, wherein the first polarity fin and the second polarity fin include germanium.

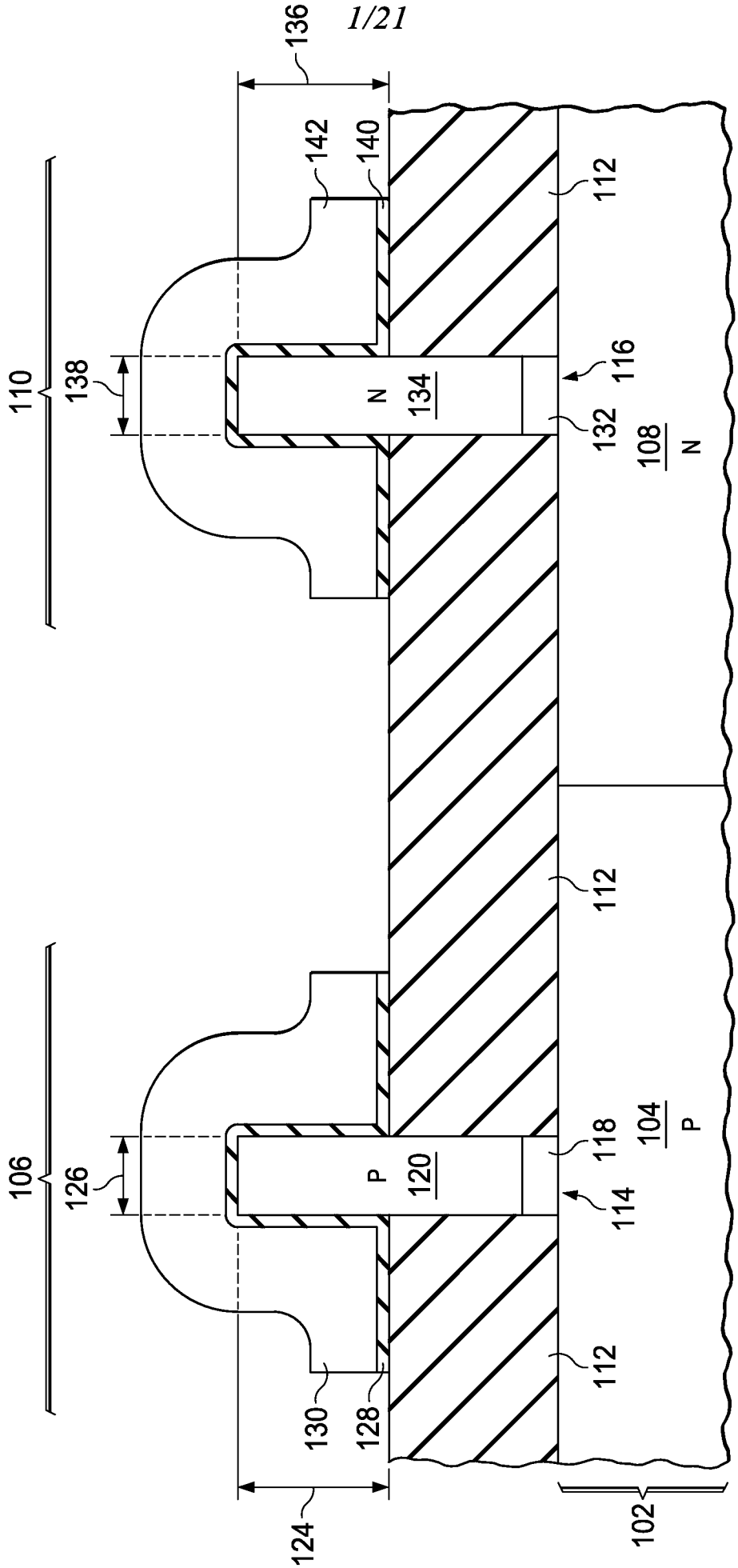
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FIG. 1

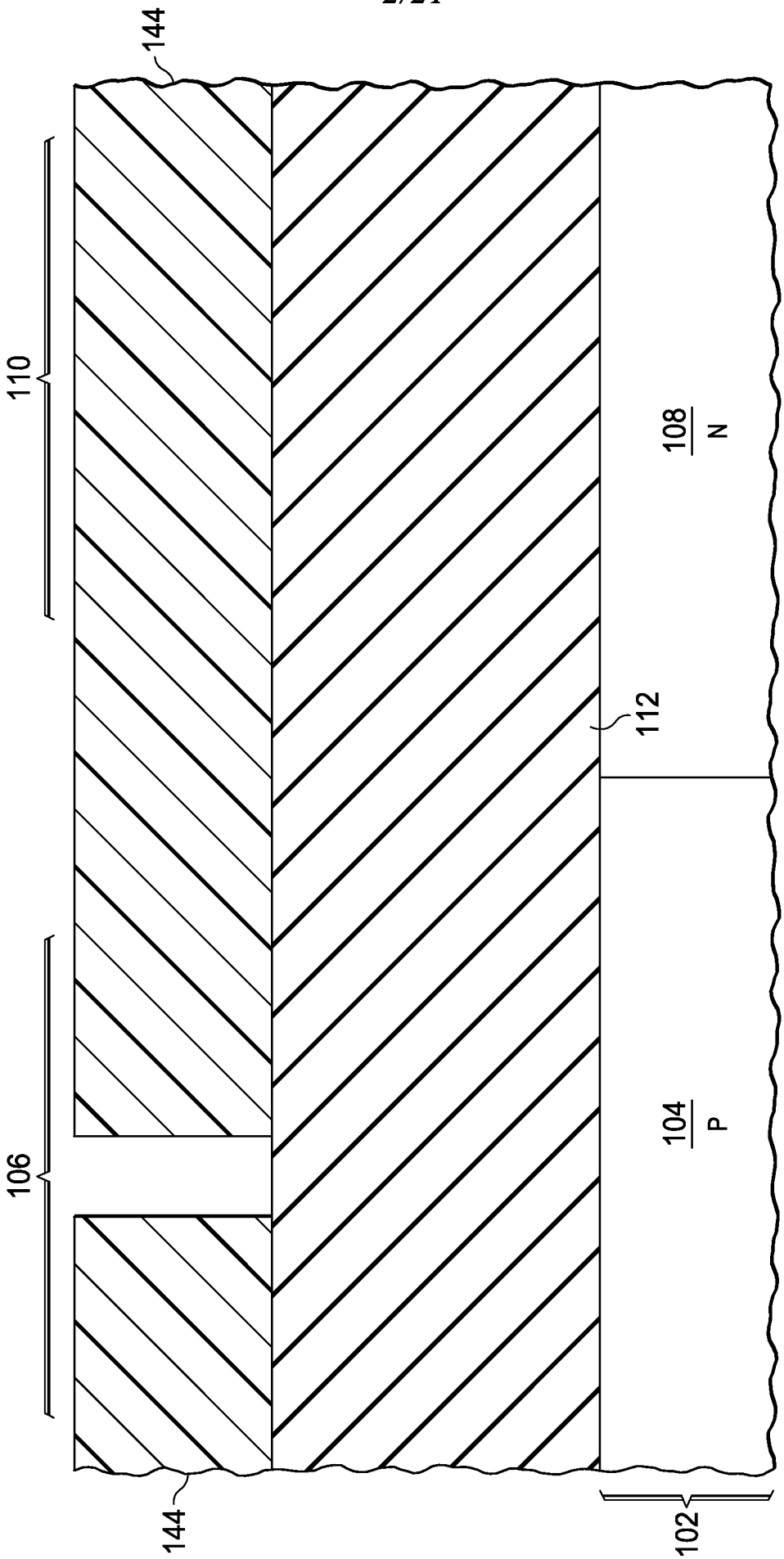

FIG. 2A

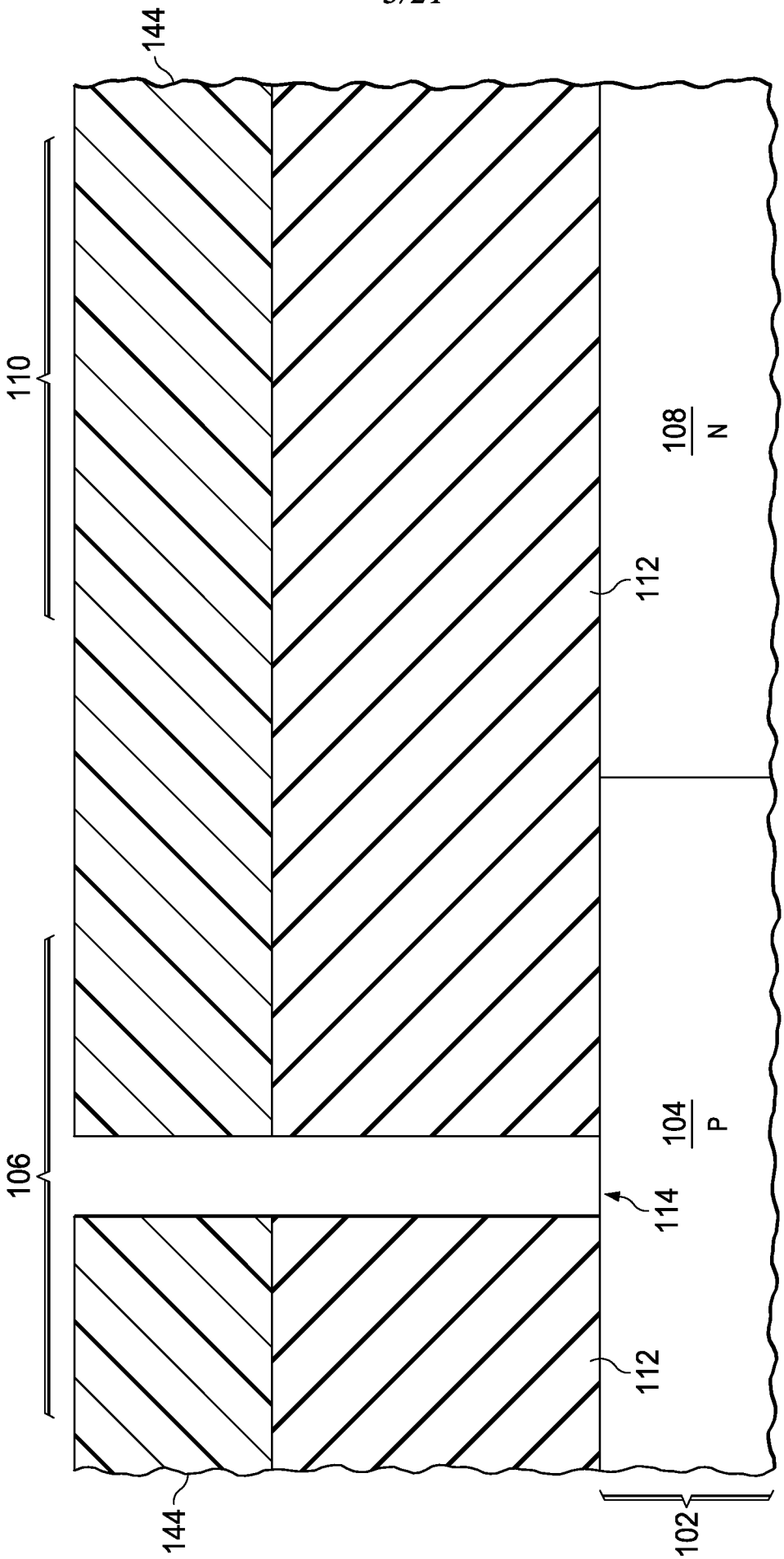

FIG. 2B

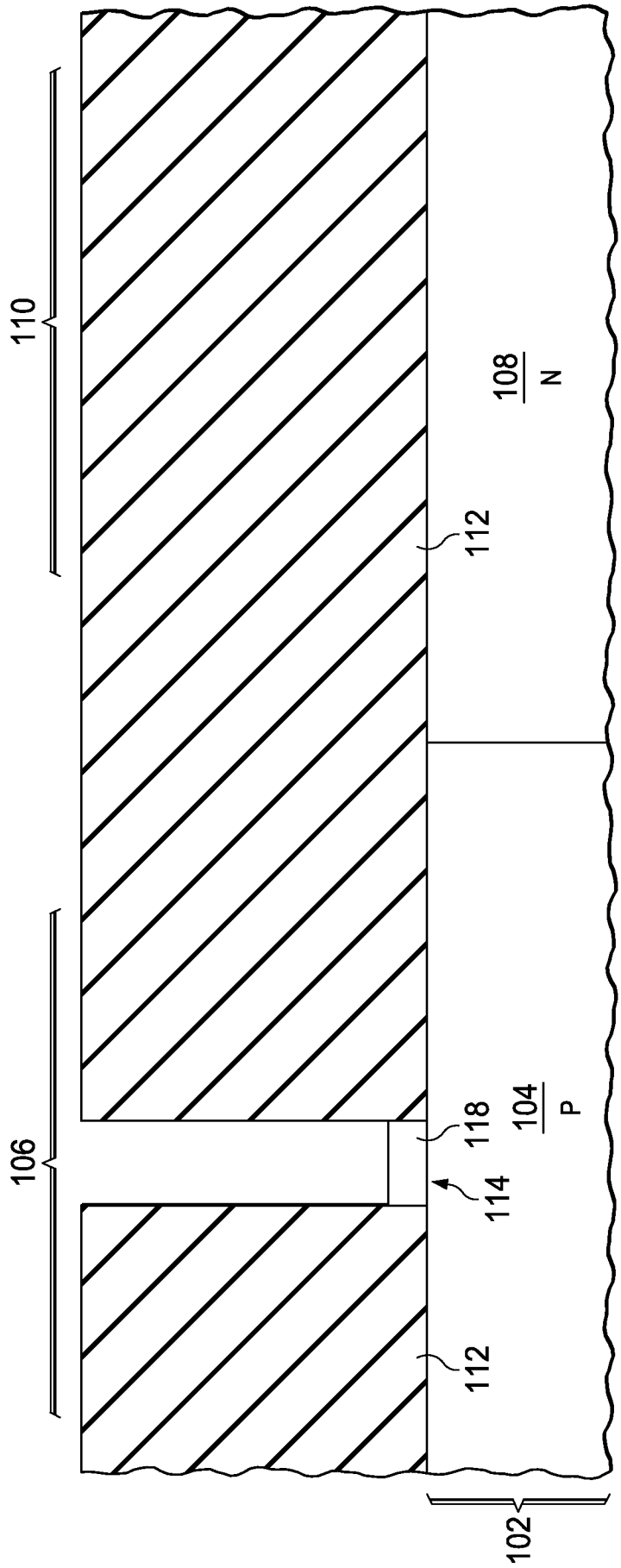

FIG. 2C

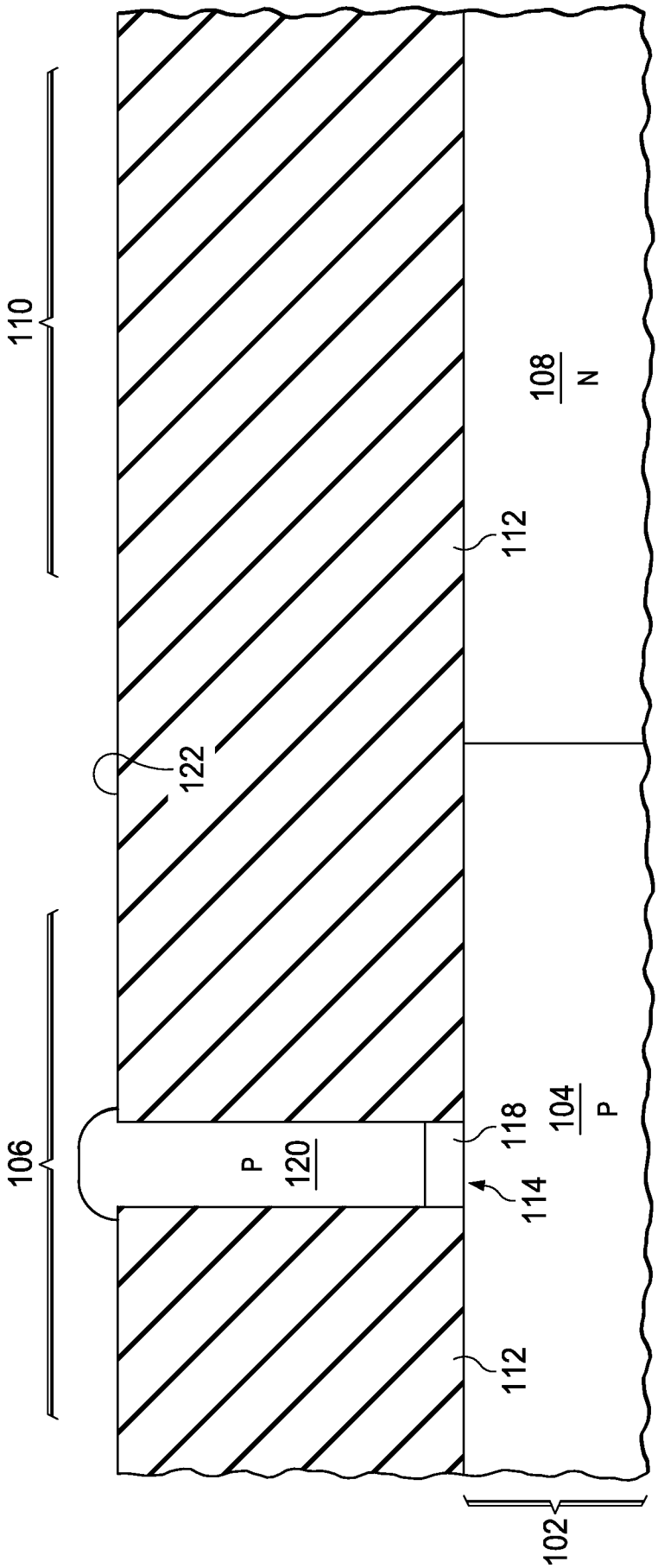

FIG. 2D

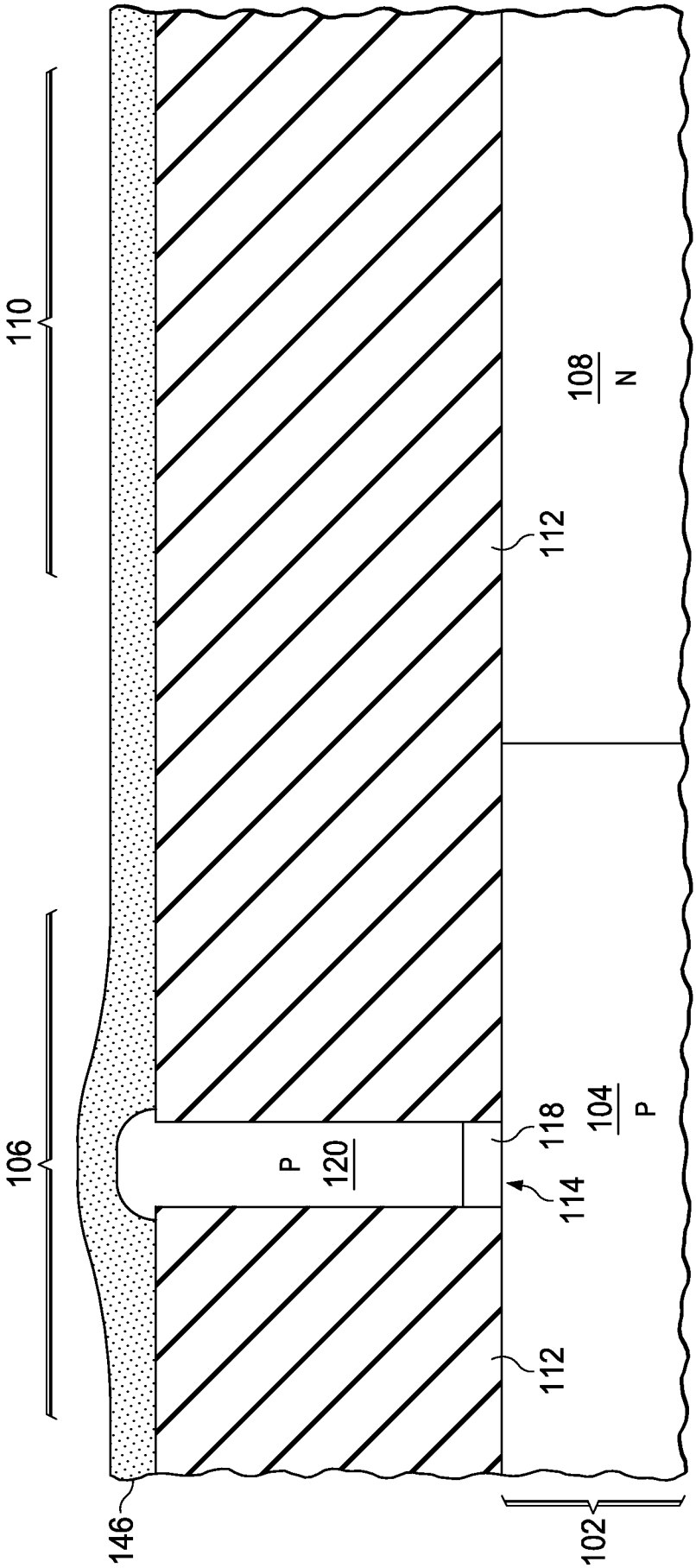

FIG. 2E

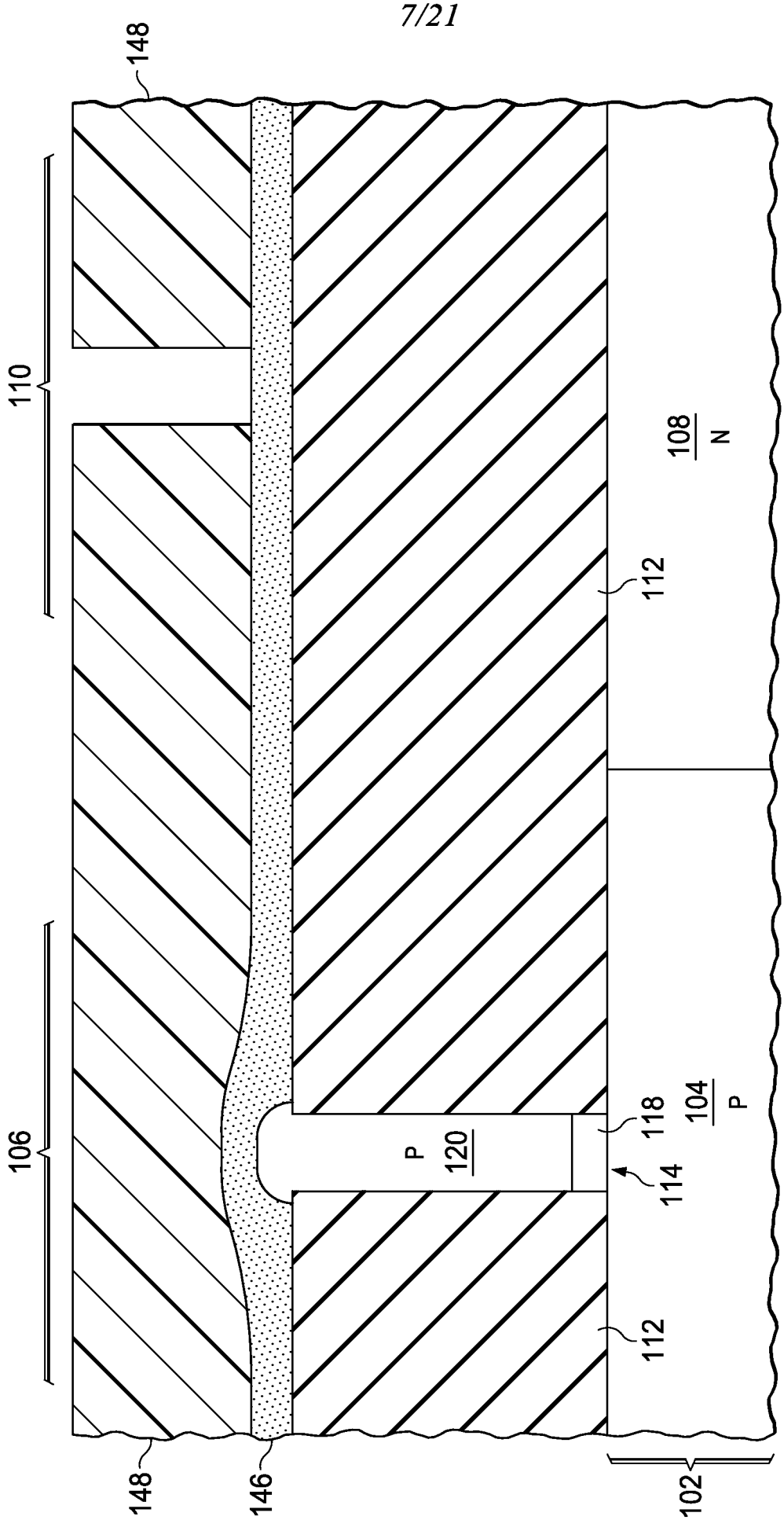

FIG. 2F

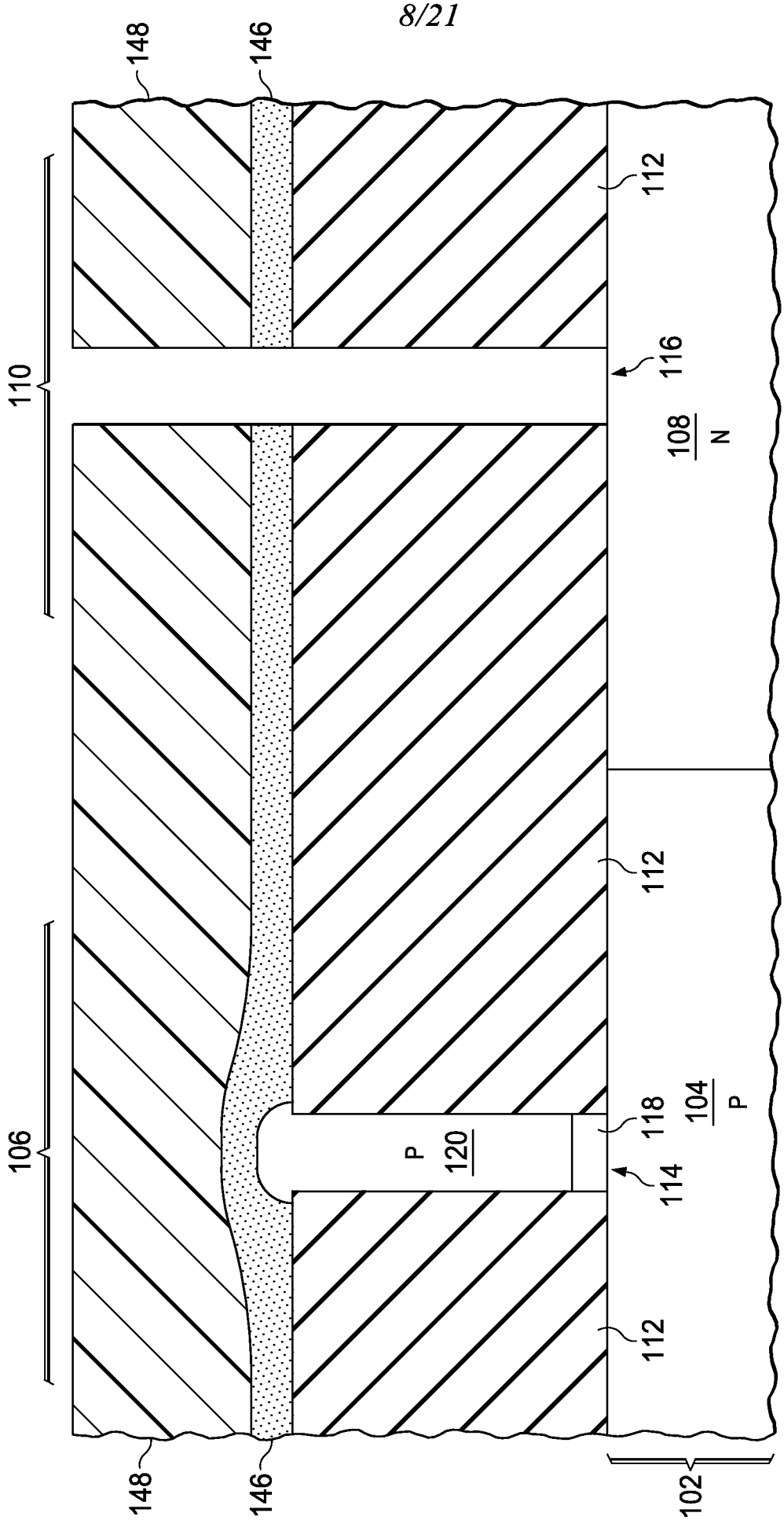
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FIG. 2G

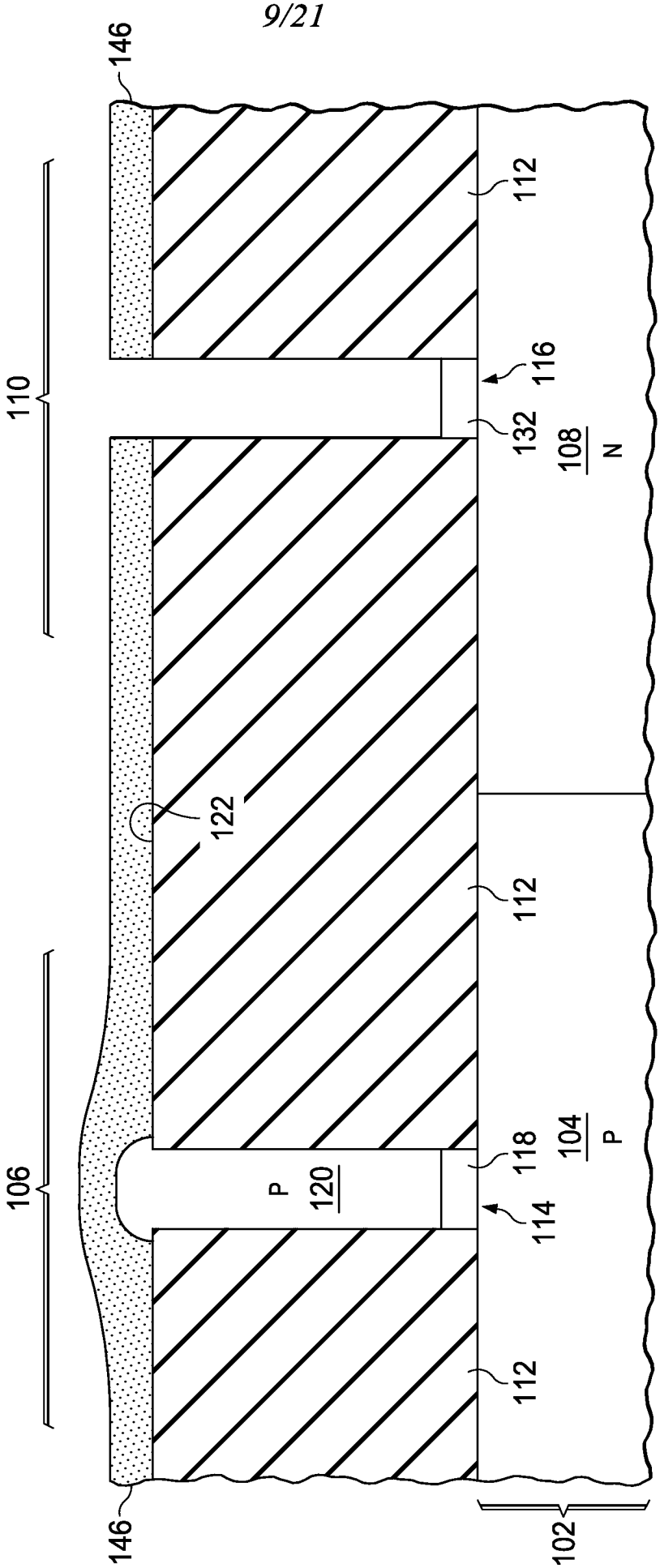
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FIG. 2H

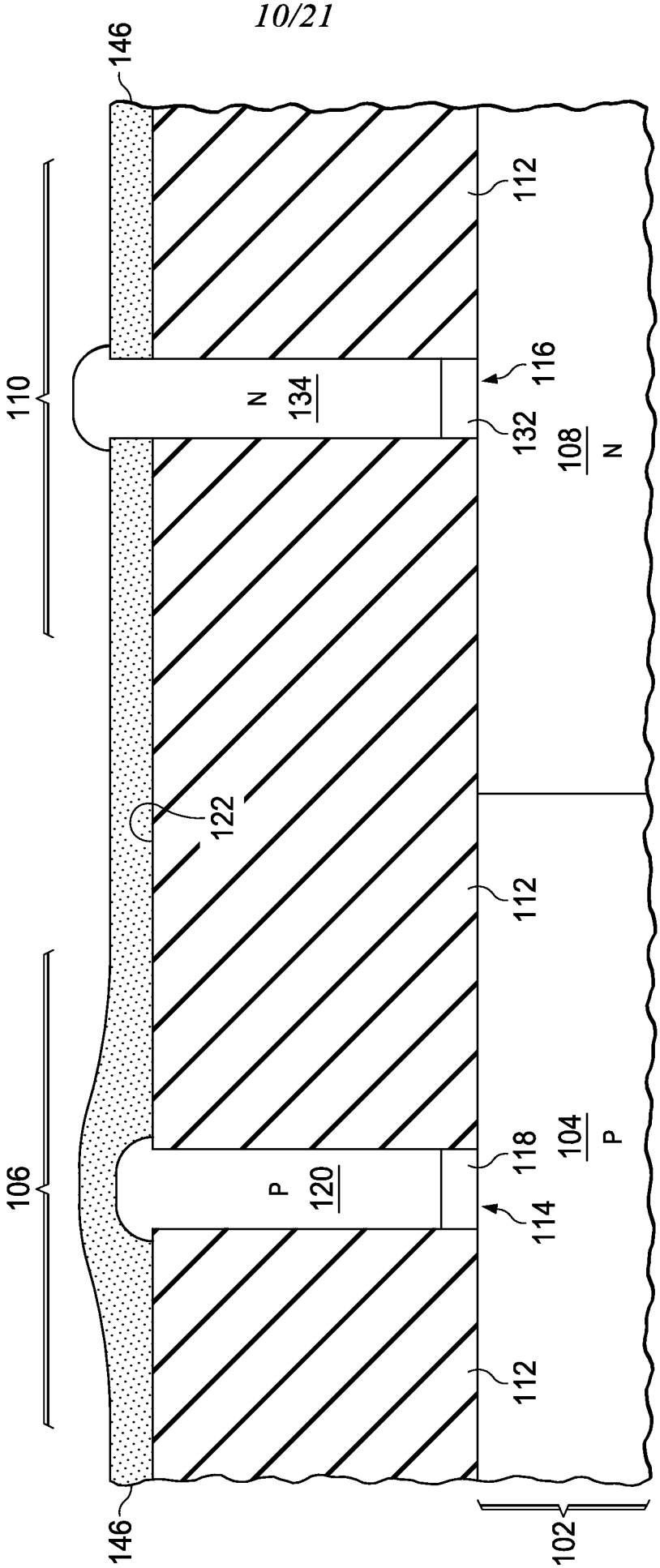
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FIG. 2I

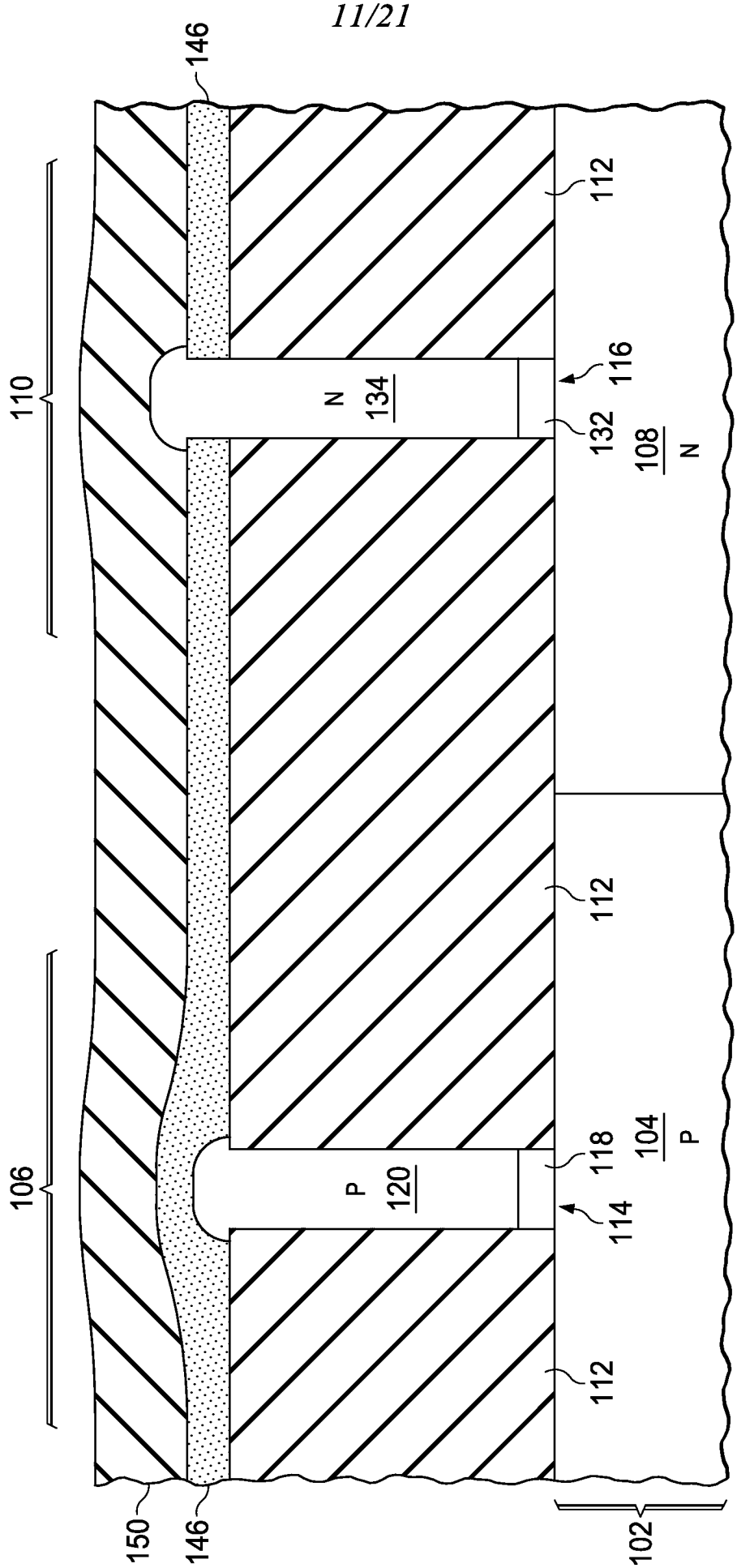
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FIG. 2J

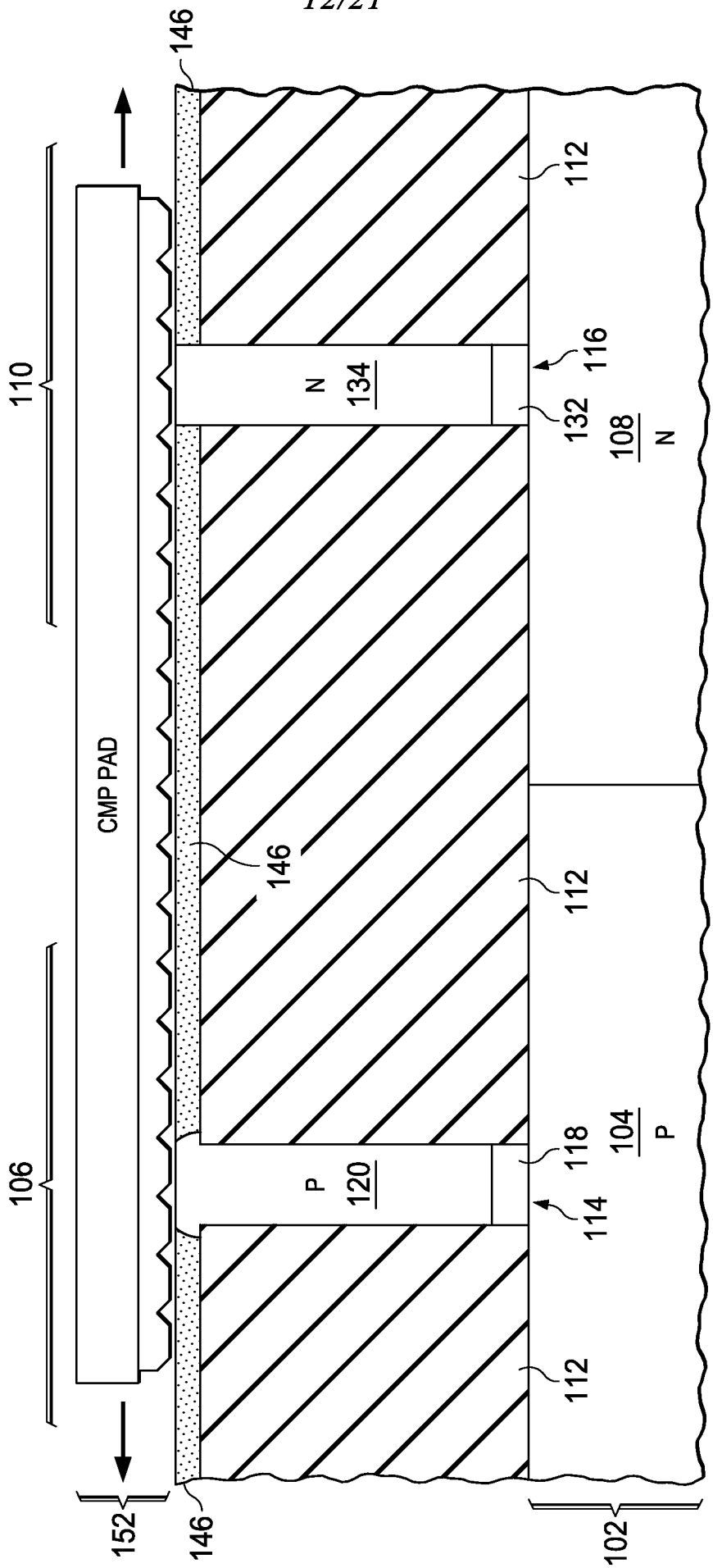
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FIG. 2K

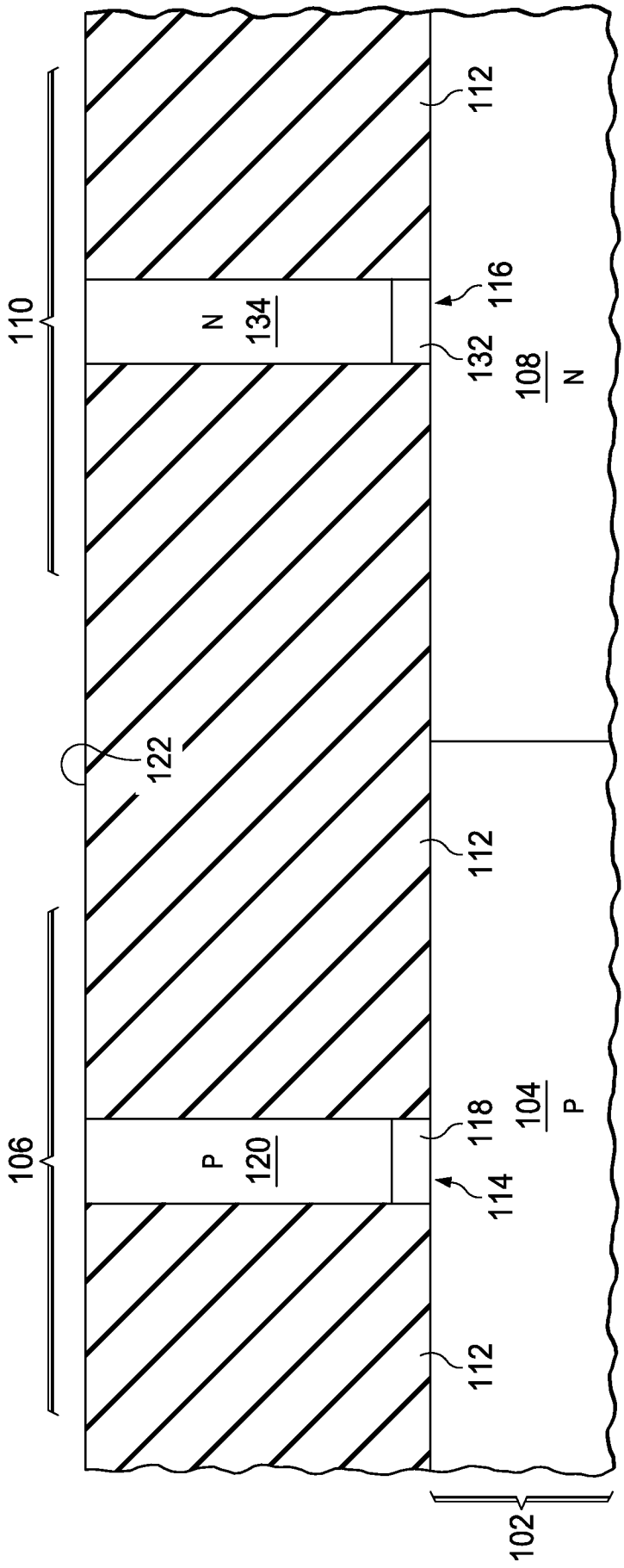
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FIG. 2L

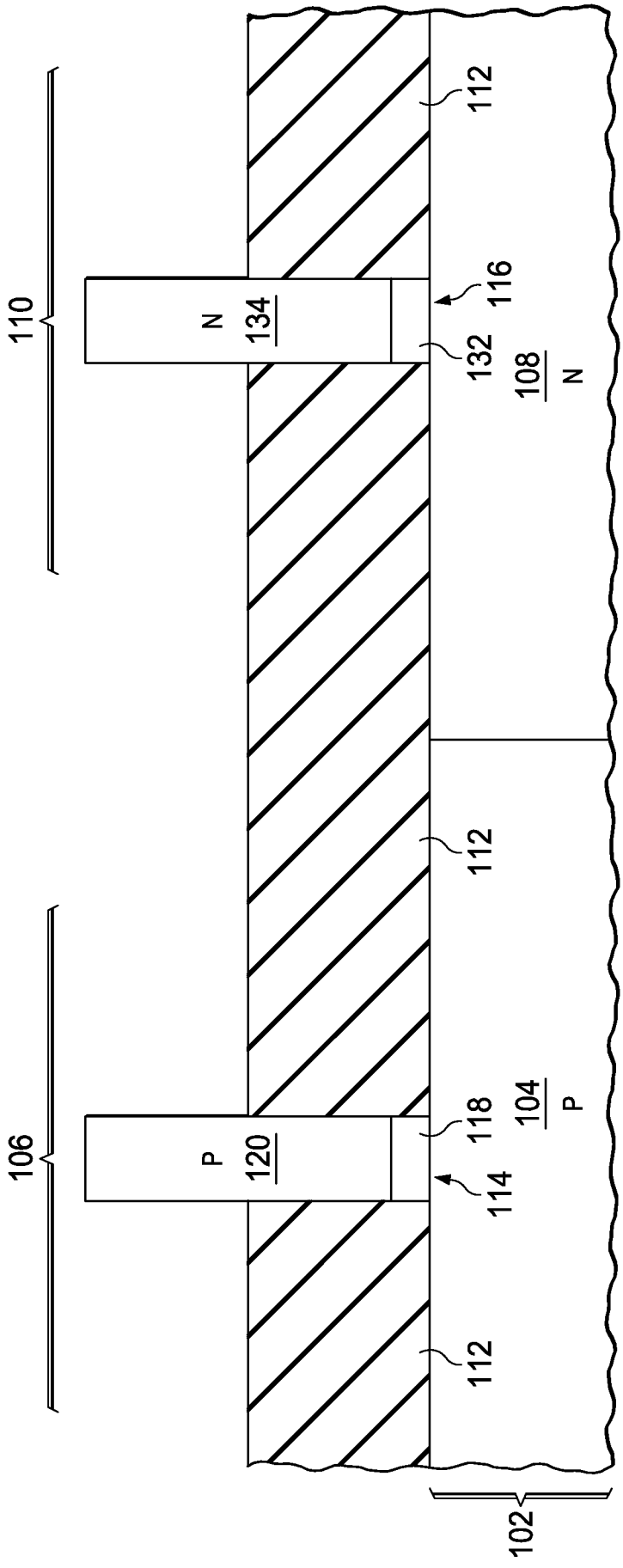

FIG. 2M

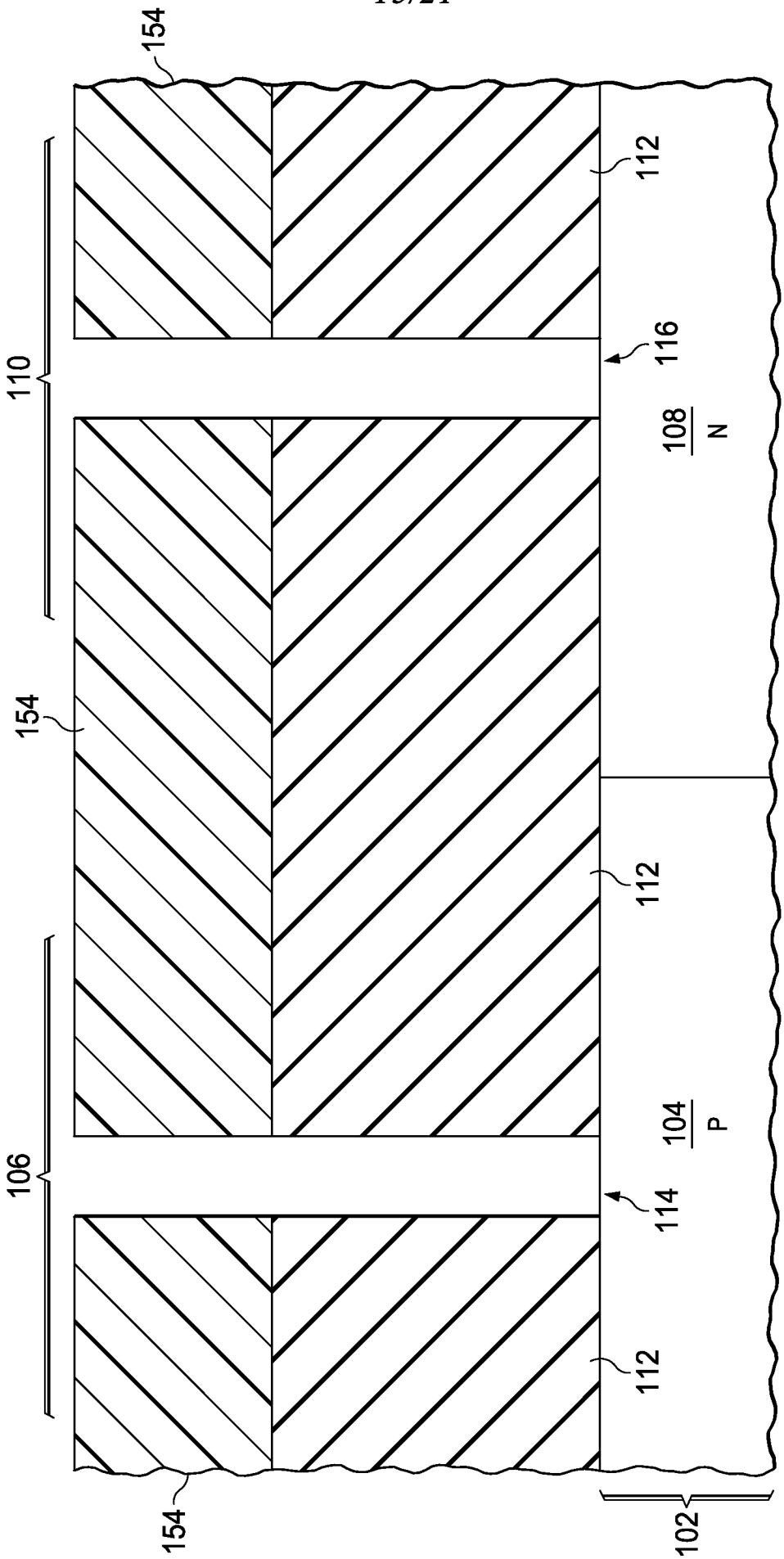

FIG. 3A

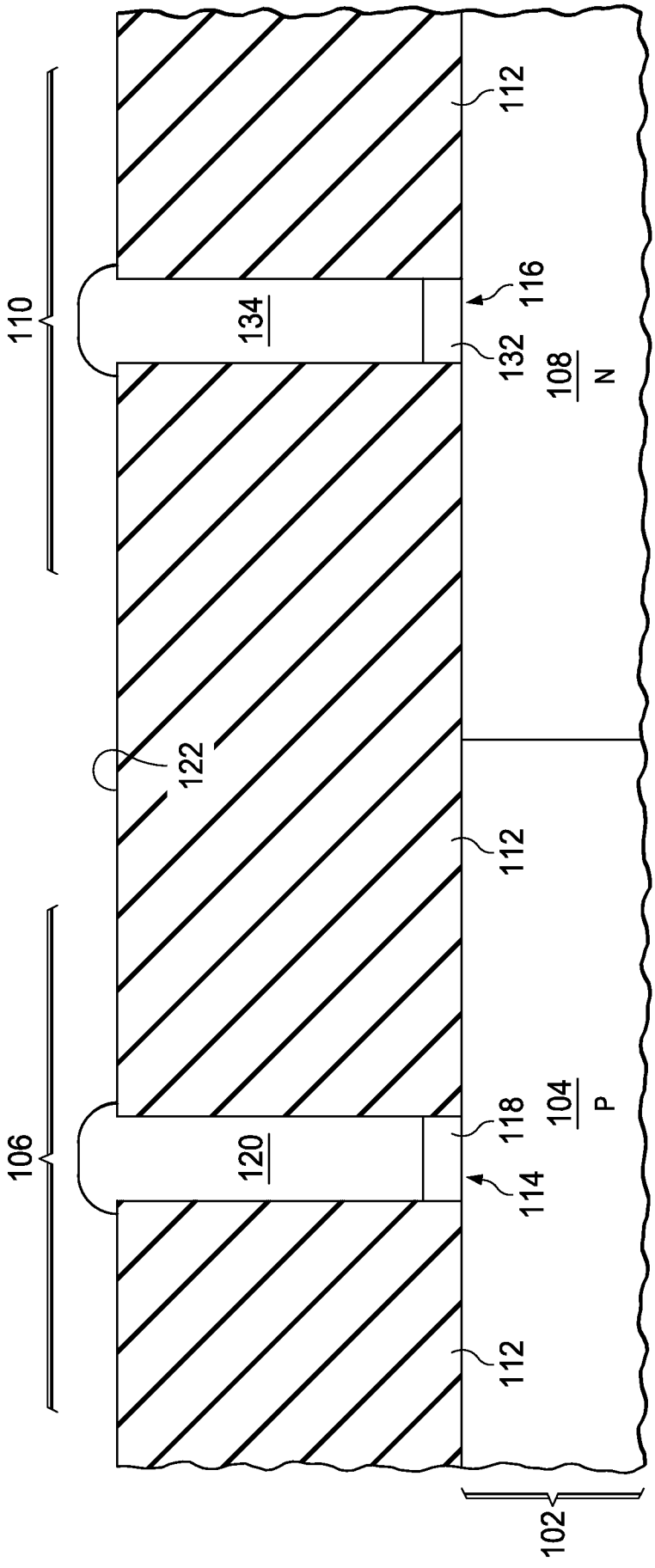

FIG. 3B

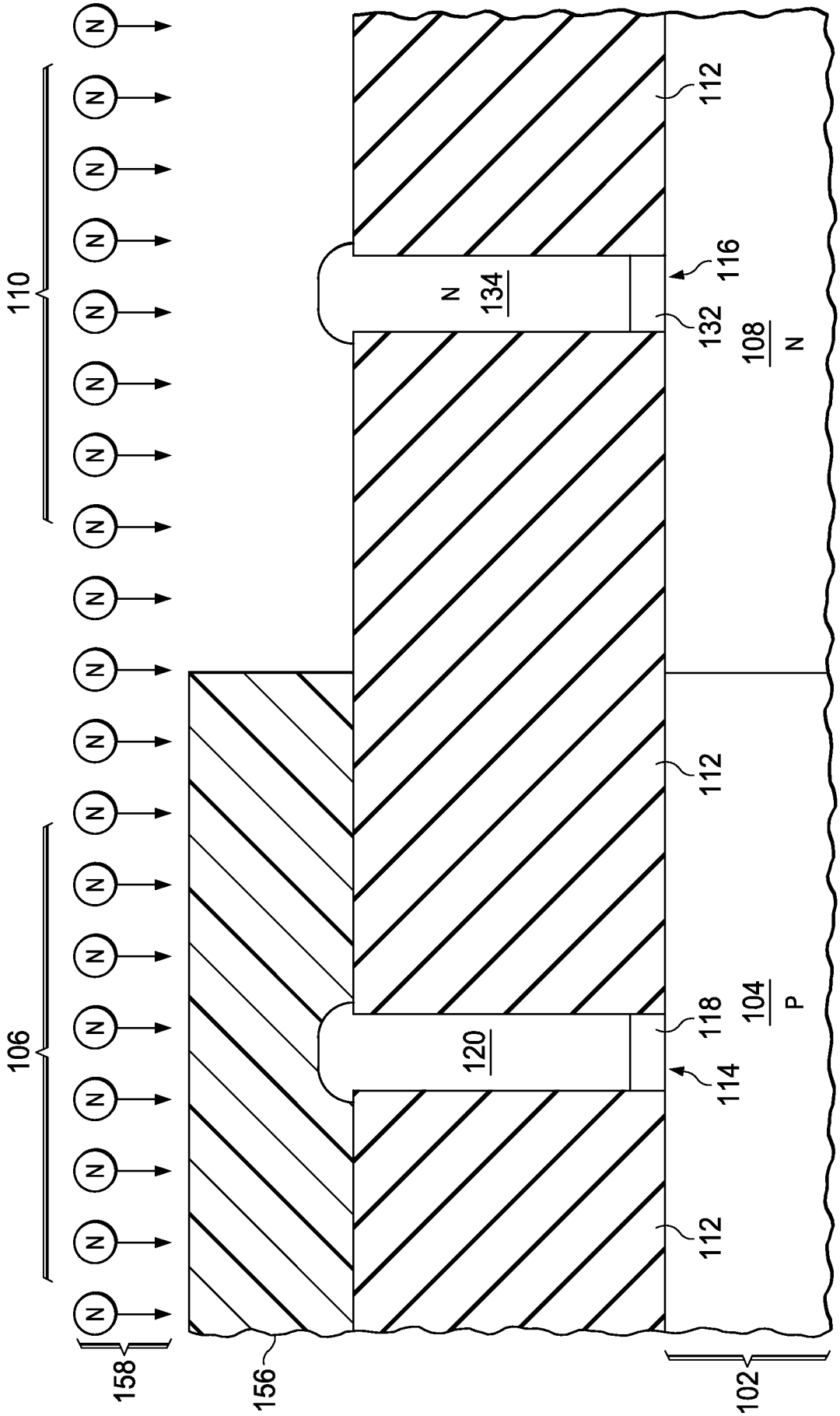

FIG. 3C

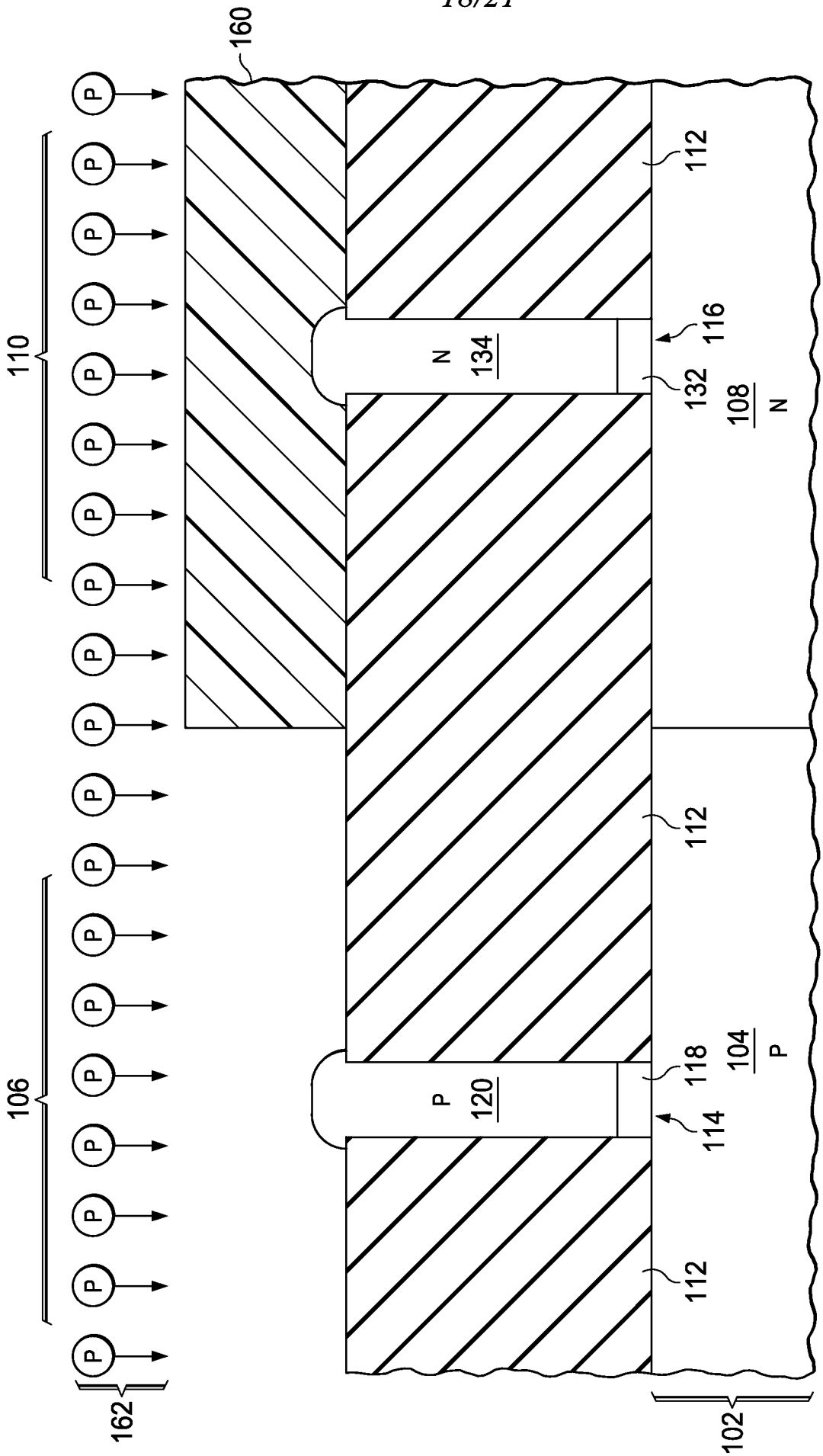
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FIG. 3D

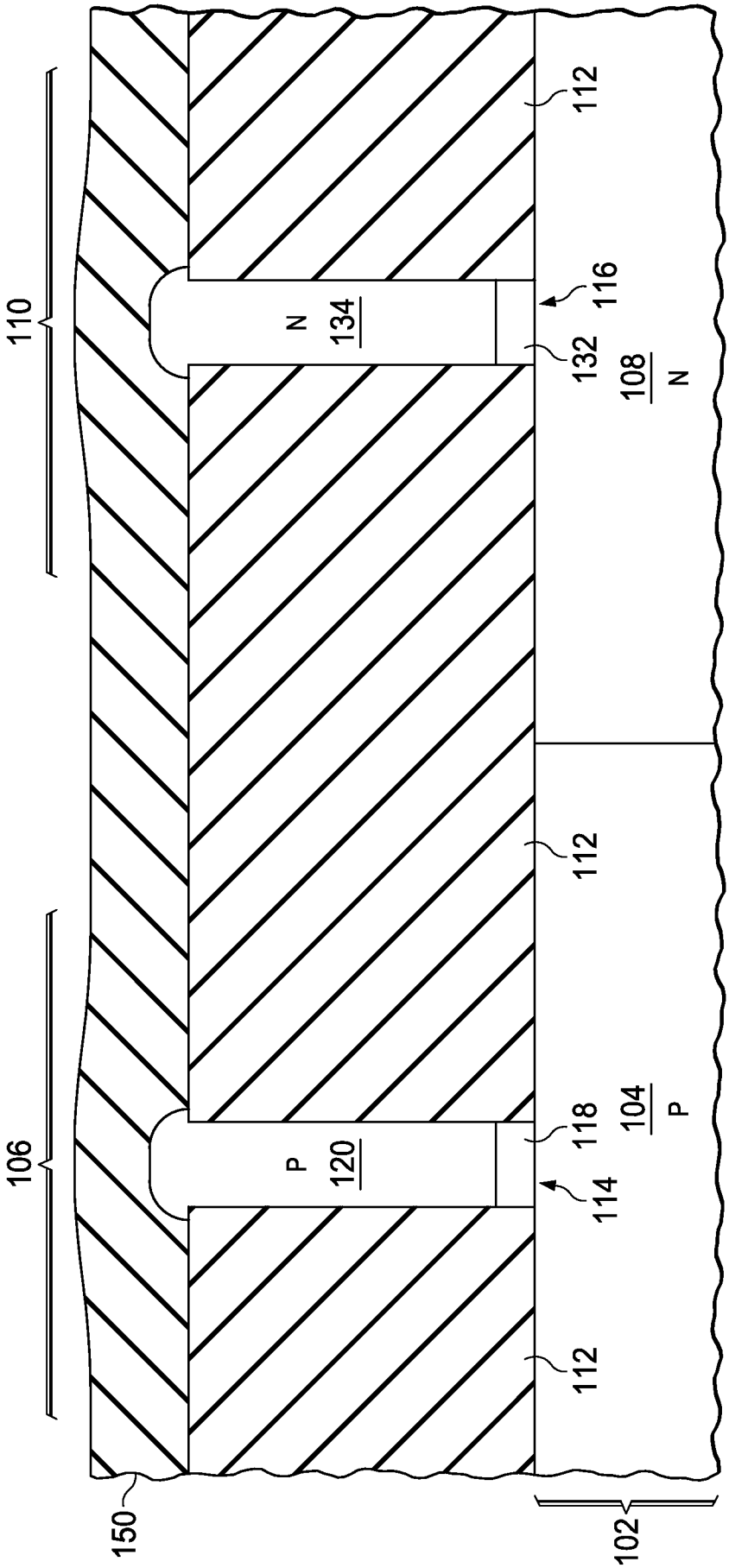
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FIG. 3E

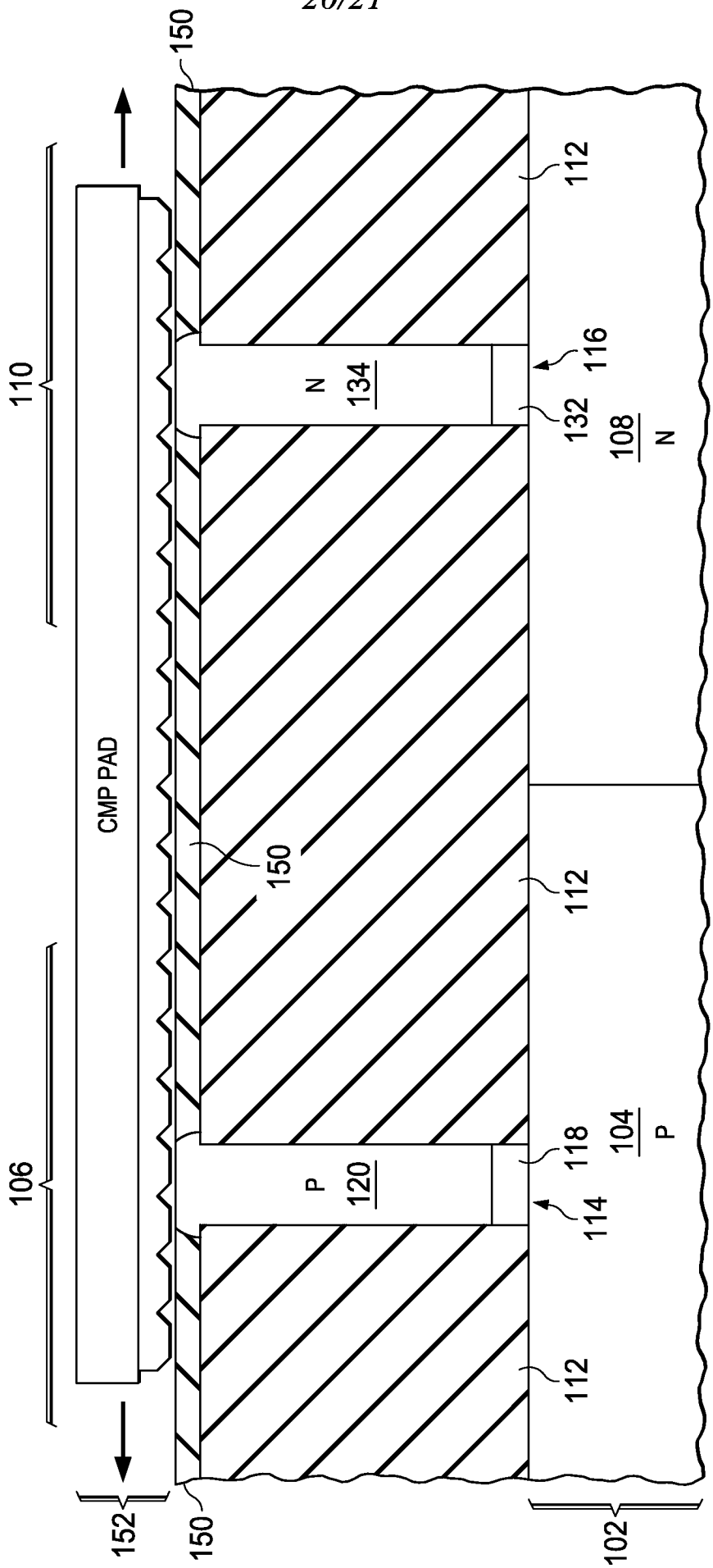
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FIG. 3F

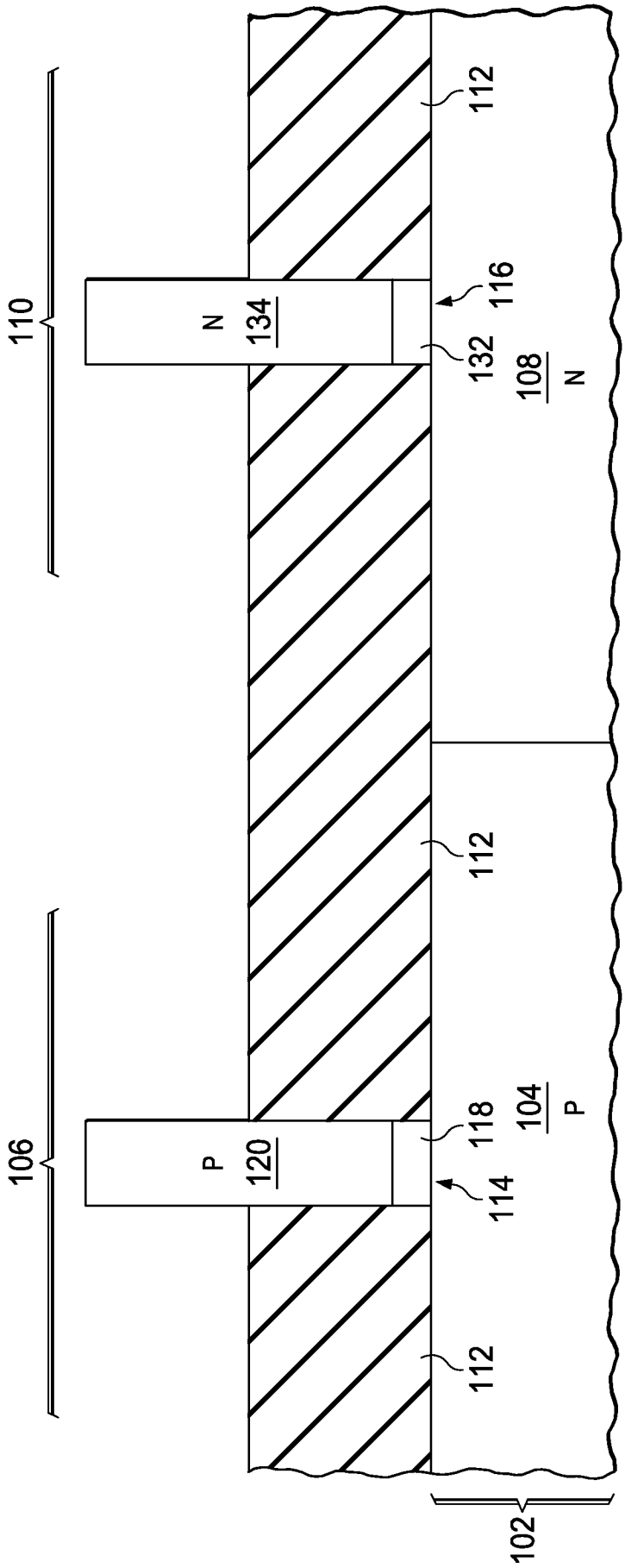

FIG. 3G

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2014/072585

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/092 *(2006.01)*
H01L 21/8238 *(2006.01)*
B82Y 40/00 *(2011.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/82-21/8238, 27/088-27/095, B82B 3/00, B82Y 40/00

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, Esp@cenet, DWPI, EAPATIS, PATENTSCOPE, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2013/0240979 A1 (MANUFACTURING COMPANY, LTD. TAIWAN SEMICONDUCTOR et al.) 19.09.2013	1-20
A	US 2011/0068407 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 24.03.2011	1-20
A	US 2013/0334606 A1 (TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.) 19.12.2013	1-20

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 March 2015 (26.03.2015)	09 April 2015 (09.04.2015)
Name and mailing address of the ISA/RU: Federal Institute of Industrial Property, Berezhkovskaya nab., 30-1, Moscow, G-59, GSP-3, Russia, 125993 Facsimile No: (8-495) 531-63-18, (8-499) 243-33-37	Authorized officer I. Baginskaya Telephone No. 499-240-25-91