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(12) (A)

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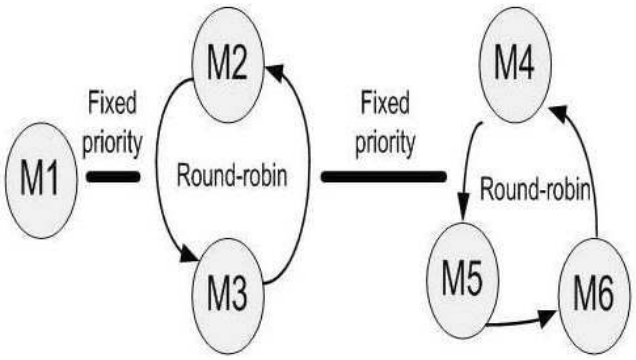
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, ,
(Hybrid bus a arbitration policy)
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1 ,

, TDMA,

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3

1 ,

(ARM) 1 , (Ethernet)

2 , DMA 3 ,

1 3

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[0001] ,

(Hybrid bus a arbitration policy) .

[0002] (Chip)

SoC(System on Chip) . , SoC(System on Chip)

,

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[0003] SoC (Master) (Arbiter), (Slave)

(Shared Bus) . (CPU), DMA(Direct

Memory Access), DSP(digital signal processor) , SDRAM, SRAM
.

[0004] SoC , 1 , ,
. ,
( ) ,
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[0005] ,
( ) . ,
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.

[0006] 1 . 1
AMBA(Advanced Micro-controller Bus Architecture) ,
2 .

[0007] 1 , (1) 1 (10), (30, 32), (40,
42) (10) (20) .

[0008] (30, 32) (40, 42) , (30, 32)
(40, 42) , (40, 42) , (20)
(10) . , (20) (30,
32) (10) , (20) (10)
(10) (40, 42) .

[0009] , 1 (30) 1 (40) , 2 (32) 2
(42) , (20) (10)
, CPU, ARM
(10) . , (20)
(Fixed Priority) (Round Robin Priority)
.

[0010] 2a 2b .

[0011] 2a ,
. (ARM, CPU),
DSP, DMA1, DMA2 1, 2, 3, 4 ,
, .

[0012] , 2b , (Round Robin Priority)
. , ,
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[0013] , , ,
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[0014] , ,
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[0015] , 3
, TDM (Lottery Bus) .

[0016] TDM (starvation)
, .

[0017] (Lottery Bus)

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[0018]

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[0019] ,

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[0020]

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[0021] ,

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[0022]

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[0023] ,

, TDMA, .

[0024] , (ARM)

1 , (Ethernet) 2 , DMA 3

, 1 3

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[0025]

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[0026]

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[0027] ,

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[0028] ,

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[0029] , ,

(Hybrid bus a arbitration policy)

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[0030] , .

[0031] 4 , 5

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[0032] , 4 .

[0033] 4 , (100) (110, 112), (130, 140, 142, 150, 152, 154), (160, 162, 164, 166), (120, 122) (170) .

[0034] (130, 140, 142, 150, 152, 154) ARM, CUP , (Ethernet), DMA, DSP , (160, 162, 164, 166) SDRAM, SRAM USB(Universal Serial Bus), UART(Universal Asynchronous Receiver Transmitter) . .

[0035] (130, 140, 142, 150, 152, 154) (110, 112) (160, 162, 164, 166) , (160, 162, 164, 166) , (120, 122) (110, 112) (160, 162, 164, 166) , (160, 162, 164, 166) .

[0036] (120, 122) (110, 112) , (130, 140, 142, 150, 152, 154) (160, 162, 164, 166) , 5 , (110, 112) .

[0037] , (Fixed Priority) , (Round Robin Priority) , TDMA, Lottery Bus .

[0038] (110, 112) , . , (120, 122) (110, 112) .

[0039] 4 AHB(Advanced High-performance Bus) , AHB ASB(Advanced System Bus), APB(Advanced peripheral Bus) .

[0040] 4 , 1(130), 2(140), 3(142) 1 (120) 1 (110) , 4(150), 5(152), 6(154) 2 (122) 2 (112) .

[0041] (170) 1 (110) 2 (112) , , (170) .

[0042] , 5 .

[0043] , , (Fixed Priority) , (Round Robin Priority) , TDMA, Lottery Bus . 5 (Fixed Priority) .

[0044] , . , . , , TDMA, .

[0045] , , CPU, ARM , (Ethernet) , DMA .

[0046] , ARM, CPU (130) 1 1 , (Ethernet) (140, 142) 2 1 1 2 , DMA (150, 152, 154) 3 2 3 .

[0047] , 1 3 , 5 .

[0048] , , , , .

[0049] , , .

[0050] , , .

[0051] 6 .

[0052] , 6 .

[0053] 6 4 (IEEE 802.11) , 6 ( ) .

[0054] , 6 1 .

1

마스터	버스이용 요청빈도
마스터1	***3***
마스터2	***2***
마스터3	***2***
마스터4	***1***
마스터5	***1***
마스터6	***1***

[0055]

[0056] 1 , 1 , 1 , 2 3 , 4, 5, 6 .

[0057] 1 , 2 , 6 , .

2

마스터 그룹	마스터	버스이용 우선순위
제 *1* 마스터 그룹	마스터*1*	*1*
제 *2* 마스터 그룹	마스터*2*, 마스터*3*	*2*
제 *3* 마스터 그룹	마스터*4*, 마스터*5*, 마스터*6*	*3*

[0058]

[0059] 2 , 1 1 , 2 3 2 , 4, 5 6 3 . , , .

[0060] 6 , , 6 , 1 . , TDMA, Lottery (F-P) 1 , , , 1 .

[0061] , , , . 1 .

[0062] , .

[0063] , , , (,) .

[0064] , .

[0065] . , . , .

[0066] 1 .

[0067] 2a 2b .

[0068] 3a TDM .

[0069] 3b (Lottery bus) .

[0070] 4 .

[0071] 5 .

[0072] 6 .

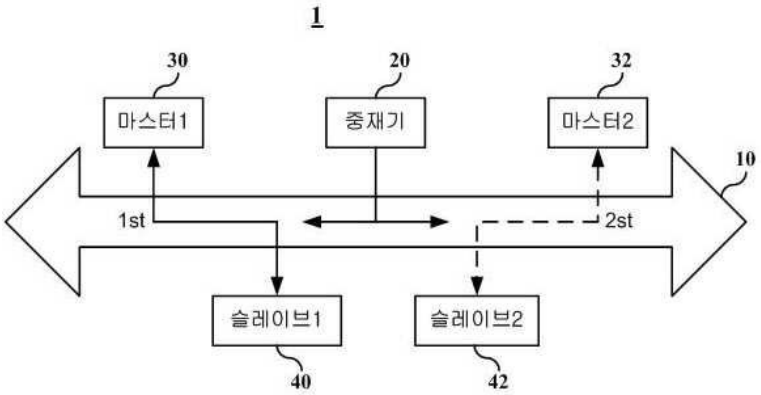
[0073] < >

[0074] 100: 110, 112:

[0075] 120, 122: 130, 140, 150:

[0076] 160, 162: 170:

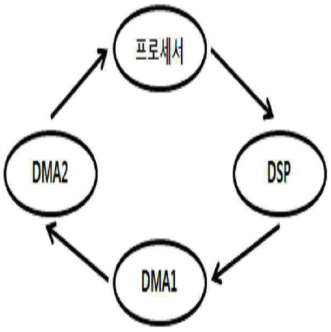
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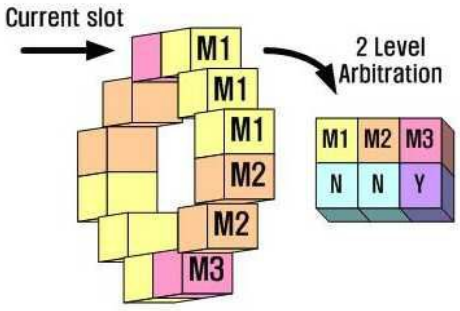
2a

우선 순위	마스터
1	프로세서
2	DSP
3	DMA1
4	DMA2

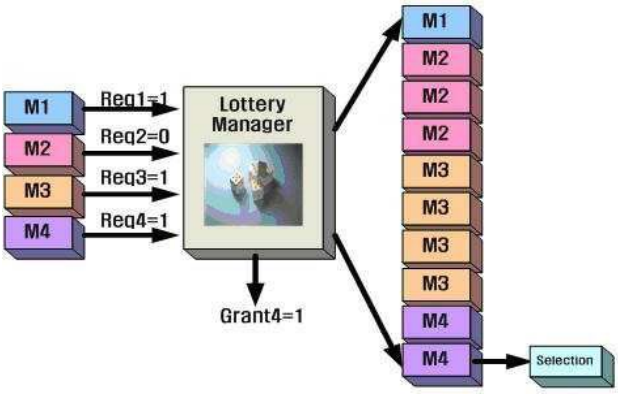
2b



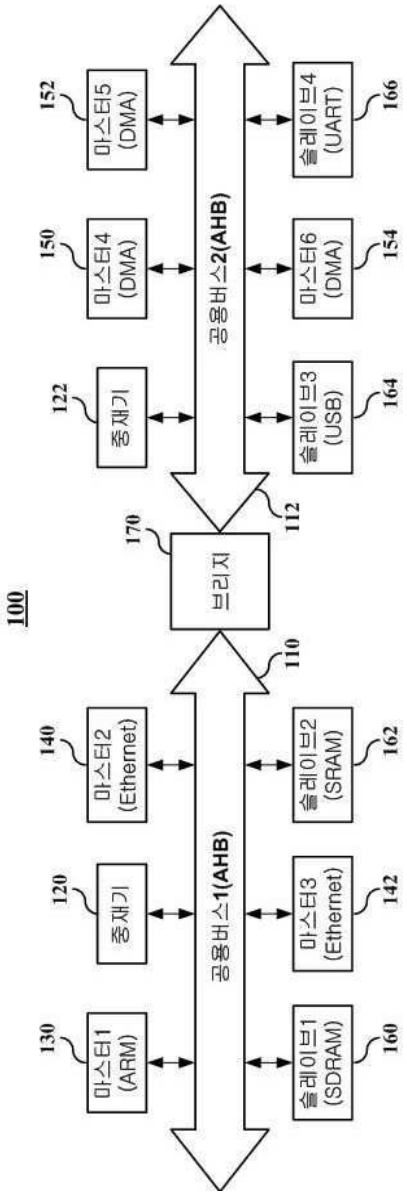
3a


Current slot
M1
M1
M1
M2
M2
M3
2 Level
Arbitration
M1 M2 M3
N N Y

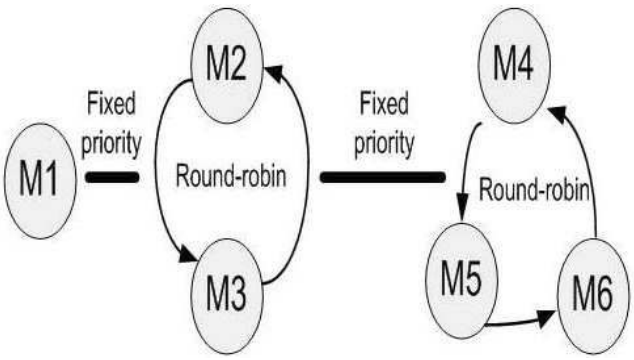
3b


M1
M2
M3
M4
Req1=1
Req2=0
Req3=1
Req4=1
Lottery
Manager
Grant4=1
M1
M2
M2
M2
M3
M3
M3
M3
M4
M4
Selection

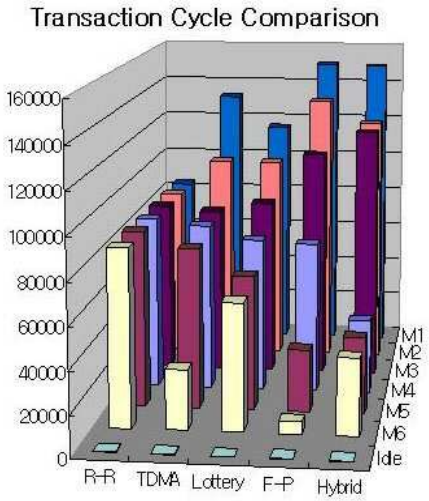
4


100
공용버스1(AHB)
공용버스2(AHB)
브리지
110
112
170
마스터1 (ARM)
130
중재기
120
마스터2 (Ethernet)
140
슬레이브1 (SDRAM)
160
마스터3 (Ethernet)
142
슬레이브2 (SRAM)
162
중재기
122
마스터4 (DMA)
150
마스터5 (DMA)
152
슬레이브3 (USB)
164
마스터6 (DMA)
154
슬레이브4 (UART)
166

5


M1
Fixed priority
M2
Round-robin
M3
Fixed priority
M4
Round-robin
M5
M6

6


Transaction Cycle Comparison
160000
140000
120000
100000
80000
60000
40000
20000
0
R-R
TDMA
Lottery
F-P
Hybrid
M1
M2
M3
M4
M5
M6
Idle