PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03M 3/02 | A1

(11) International Publication Number: WO 96/18242

(43) International Publication Date: 13 June 1996 (13.06.96)

(21) International Application Number: PCT/US95/14357

(22) International Filing Date: 2 November 1995 (02.11.95)

(30) Priority Data:
08/352,665 9 December 1994 (09.12.94) US

(71) Applicant: ADVANCED MICRO DEVICES, INC. [US/US]; 901 Thompson Place, Sunnyvale, CA 94088-3453 (US).

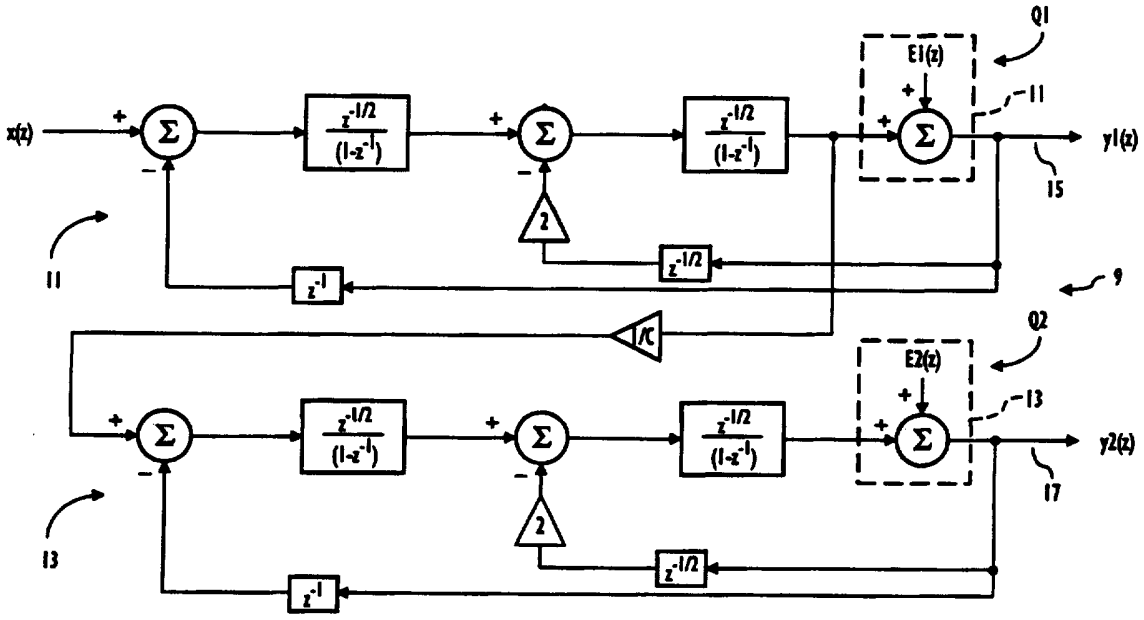
(72) Inventor: CABLER, Carlin, Dru; 12101 Corner Brook Pass, Austin, TX 78739 (US).

(74) Agents: KOCH, Robert, J.; Fulbright & Jaworski L.L.P., 801 Pennsylvania Avenue, Washington, DC 20004-2604 (US) et al.

(81) Designated States: JP, KR, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SIGMA-DELTA MODULATOR WITH REDUCED DELAY FROM INPUT TO OUTPUT



(57) Abstract

This invention includes a second and a fourth-order sigma-delta modulator system having one-half unit delay integrators and feedback.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

SIGMA-DELTA MODULATOR WITH REDUCED DELAY FROM INPUT TO OUTPUT

Specification

Background of the Invention

1. Field of the Invention.

This invention relates to high resolution analog-to-digital and digital-to-analog converters, and in particular, to oversampled, noise shaping analog-to-digital and digital-to-analog converters.

2. Brief Description of the Related Technology and Prior Art.

The use of sigma-delta modulators in analog-to-digital (A/D) and digital-to-analog (D/A) converter circuits is increasing. It is well known in the art that so-called higher order sigma-delta modulators have an inherently higher signal-to-noise ratio than lower ordered sigma-delta modulators. For many practical applications, fourth-order sigma-delta modulators have become the higher-order modulator of choice because they strike an appropriate balance between analog circuit complexity and accompanying digital filtering complexity. Various fourth-order sigma-delta modulators for A/D circuits are described in the following applications assigned to the common assignee of the present invention: application Serial No. 08/112,610, filed August 26, 1993, entitled "Fourth-Order Cascaded Sigma-Delta Modulator;" application Serial No. 08/147,062, filed November 3, 1993, entitled "Fourth-Order Cascaded Sigma-Delta Modulator;" and application Serial No. 08/171,091, filed December 21, 1993, entitled "Fourth-Order Cascaded Sigma-Delta Modulator." Another fourth-order sigma-delta modulator is described by *Karema, et al*, in U. S. Patent No. 5,061,928. The aforementioned applications describe sigma-

delta modulators created by connecting two, second-order sigma-delta modulators, each such modulator being characterized as having two associated unit delays from input to output. In each of the above applications, a unique post-quantization network combines the output of the two, second-order sigma-delta modulators in a manner such that a single modulated multi-bit data stream, with fourth-order shaping, results. The modulators in all of the examples given above are characterized as having four unit delays from input to final output.

A need has developed for a fourth-order sigma-delta modulator with fewer than four unit delays from input to output in order to overcome disadvantages associated with those fourth-order modulators having four unit delays from input to output. Prior art fourth-order sigma-delta modulators implemented as A/D converters suffer from increased operational amplifier and post-quantization network complexity. Additionally, when such sigma-delta modulators are used in the feedback loop of such circuits as echo cancelers, stability may be difficult to obtain due to the amount of delay from input to output through the sigma-delta modulator.

The sigma-delta modulator of Fig. 1 is an example of a fourth-order sigma-delta modulator which is formed by connecting two, second-order sigma-delta modulators. This is similar to the fourth-order modulator described in U.S. Patent No. 5,061,928 by *Karema, et al.* This modulator is characterized as a cascade of two second-order modulators. These second-order modulators are characterized as including two integrators each of which can be characterized as having the following transfer function:

$$H(z) = z^{-1}/(1-z^{-1})$$

As can be seen in the above equation, there is a single unit delay in such an integrator due to the z^{-1} term in the numerator. Additionally, such second-order modulators are also characterized as having a quantizer, which typically is used to quantize only the sign of the signal presented at its input. This is commonly modeled as a summing node where one input is the input to the quantizer (Q) and the other input is a noise source (E) which represents the quantization noise of the quantizer. Such a model is shown

in Fig. 1 as Q_1 and Q_2. The overall transfer function of such a second-order modulator is typically given by the following equation:

$$y(z) = z^{-2}x(z) + E(z)(1-z^{-1})^2$$

where y(z) is the output of the modulator, x(z) is the sampled input to the modulator, and E(z) is the quantization noise of the quantizer within the modulator.

When two such second-order modulators are connected together as shown in Fig. 1, the transfer function at output y1(z) can be characterized by the following equation:

$$y_1(z) = z^{-2}\, x(z) + E_1(z)(1-z^{-1})^2$$

where x(z) is the sampled input to the modulator and $E_1(z)$ is the quantization noise of quantizer Q_1. Output $y_2(z)$ can be characterized by the following equation:

$$y_2(z) = z^{-2}\, E_1(z) + KE_2(z)(1-z^{-1})^2$$

where $E_1(z)$ is the quantization noise due to quantizer Q_1, K is a constant that is frequently used as a scaling factor for the connection between the first and second modulator, and $E_2(z)$ is the quantization noise due to the quantizer Q_2.

The two modulator outputs, $y_1(z)$ and $y_2(z)$ are typically combined using a post-quantization network which results in a final modulator output $y_{out}(z)$. An appropriate post-quantization network for use with the circuit of Fig. 1 is shown in Fig. 2. Such a circuit along with the two, second-order sigma-delta modulators shown in Fig. 1 will result in an overall fourth-order sigma-delta modulator which may be characterized by the following equation:

$$y_{out}(z) = z^{-4}x(z) + KE_2(z)(1-z^{-1})^4$$

Essentially, the post-quantization circuit of Fig. 2 removes the quantization noise $E_1(z)$ due to quantizer Q_1. It also results in an overall fourth-order high pass filtering function on the quantization noise $E_2(z)$ due to quantizer Q_2. As can be seen in the above equation, such a modulator has an overall constant group delay of four sample periods due to the z^{-4} term in front of the x(z) term.

In application Serial No. 08/147,062, described previously, a fourth-order sigma-delta modulator is formed by connecting two, second-order sigma-

delta modulators together such that only the input of the first quantizer is fed to the second, second-order sigma-delta modulator. The output of each quantizer for each second-order sigma-delta modulator is then fed to a post-quantization network which removes the quantization noise of the first, second-order sigma-delta modulator and shapes the quantization noise of the second, second-order sigma-delta modulator with a fourth-order high pass filter function. Such a sigma delta modulator is shown in Figs. 3 and 4 and can be characterized by the same equation that characterizes the operation of the fourth-order sigma-delta modulator described by *Karema, et al.* That is, the output of the fourth-order sigma-delta modulator described in the aforementioned application also has a constant group delay of four sample periods.

It is an object of the present invention to provide a fourth-order sigma-delta modulator which has high resolution, but with an overall constant group delay of two sample periods. This is to be accomplished by connecting together two, second-order sigma-delta modulators, each being characterized as having an overall constant group delay of one sample period. An example of a prior art second-order modulator having unit delays less than one is described in the *IEEE Journal of Solid State Circuits*, Vol. 25, no. 4, Aug. 1990, pp. 979-986, in the article entitled "The Implementation of Digital Echo Cancellation in Codecs," by Friedman, et al. Friedman describes a second-order modulator characterized as having integrators with 1/2 unit delays from input to output. Furthermore, the second-order sigma-delta modulator of *Friedman* is characterized as requiring two flip-flops two perform delay functions in the feedback of the modulator to obtain the desired transfer function. Such a second-order sigma-delta modulator is shown in Fig. 5.

It is, therefore, a further object of the present invention to describe a second-order sigma-delta modulator which does not require two flip-flops in the feedback of the sigma-delta modulator, thus reducing the manufacturing cost of such a sigma-delta modulator.

It is a further object of the present invention to utilize two such second-order sigma-delta modulators, which are to be connected together, to form a portion of a fourth-order sigma-delta modulator.

It is still a further object of the present invention to connect two such second-order modulators to a post-quantization network to form an overall fourth-order sigma-delta modulator with a total of two unit sample delays.

It is yet another object of the present invention to provide a sigma-delta modulator which can be fabricated using switched capacitor circuitry in such a fashion as to form an A/D converter.

It is still another object of the present invention to provide a sigma-delta modulator which can be used as a digital noise shaper for a D/A converter.

Summary of the Invention

The fourth-order sigma-delta modulator of the present invention utilizes two, second-order sigma-delta modulators connected together. Each second-order sigma-delta modulator is characterized as including integrators with a 1/2 sample period delay from input to output. A second-order sigma-delta modulator including such integrators exhibits a single sample period delay from input to output. A fourth-order sigma-delta modulator which includes two such second-order sigma-delta modulators exhibits a delay of two sample periods from input to output.

In a preferred embodiment, a fourth-order analog-to-digital converter circuit is described by combining two such second-order sigma-delta modulators which include the characteristic that all capacitors which are connected to the output of each op amp within the sigma-delta modulator would be charged on the same clock phase. Because of this characteristic, glitches between clock phases are avoided and performance of the analog-to-digital converter is improved.

In another embodiment, the two second-order sigma-delta modulators, and a portion of the post-quantization network, are constructed as a digital circuit that can be used as a digital noise shaper for a D/A converter. The resultant outputs of the post-quantization network may then be input into a

plurality of D/A converters whose outputs are summed to form a single analog output.

Brief Description of the Drawings

Fig. 1 is a block diagram of a fourth-order sigma-delta modulator of the prior art;

Fig. 2 is a block diagram of a post-quantization circuit of the prior art;

Fig 3 is a block diagram of a fourth-order sigma-delta system of the prior art;

Fig. 4 is a block diagram of a post-quantization circuit of the prior art;

Fig. 5 is a block diagram of a second-order sigma-delta modulator of the prior art;

Fig. 6 is a block diagram of a second-order sigma-delta modulator of the present invention;

Fig. 7 is an embodiment of two integrators, each having one-half unit delay;

Fig. 8 is an embodiment of two integrators, each having one unit delay;

Fig. 9 is a timing diagram of the timing signals, Φ_1 and Φ_2, used with the switching capacitors of the present invention;

Fig. 10 is a block diagram of a fourth-order sigma-delta modulator of the present invention;

Fig. 11 is a block diagram of a post-quantization network of the present invention;

Fig. 12 is a block diagram of a second-order sigma-delta modulator of the present invention;

Fig. 13 is a block diagram of a fourth-order sigma-delta modulator of the present invention;

Fig. 14 is an embodiment of a fourth-order sigma-delta modulator of the present invention, which utilizes summing integrators;

Fig. 15 is a timing diagram showing the relationship between the switch capacitor timing signals, Φ_1 and Φ_2, and the outputs y1a, y1b, y2a, and y2b, of Fig. 14 of the present invention;

Fig. 16 shows an alternative embodiment of an integration stage of a sigma-delta modulator of the present invention;

Fig. 17 illustrates an additional embodiment of an integration stage of a sigma-delta modulator of the present invention;

Fig. 18 is a timing diagram showing the timing of the switches in the sigma-delta embodiment illustrated in Fig. 19;

Fig. 19 is an embodiment of an integration stage of a sigma-delta modulator of the present invention;

Fig. 20 is a graphic illustration of a plat of simulated signal noise plus distortion ratio levels (SNDR), with an oversampling ratio of 64, of a sigma-delta modulator of the present invention; and

Fig. 21 is a post-quantization network for a D/A modulator of the present invention.

Detailed Description of the Preferred Embodiment

Fig. 6 is a functional block diagram of a second-order sigma-delta modulator 5 of the present invention. Integrators 12 and 14, each having a 1/2 unit delay with the following transfer function, are utilized:

$$H_1(z) = z^{-1/2} / (1 - z^{-1})$$

A more common form of integrator is characterized by the following transfer function:

$$H_2(z) = z^{-1} / (1 - z^{-1})$$

Fig. 7 schematically depicts a single-ended implementation of two integrators in series with half unit delays in each integrator. Fig. 8 is a single-ended implementation of two integrators in series with unit delays in each integrator. In Figs. 7 and 8, Φ_1 and Φ_2 are two-phase non-overlapping clocks and are characterized such that neither clock is at a logic '1' during the same instant in time. An example of such clocks is shown in Fig. 9. When Φ_1 is at a logic '1' any switch which is denoted as being controlled by Φ_1 is closed. Such a switch is open at all other times. Likewise, when Φ_2 is at a logic '1' any switch is denoted as being controlled by Φ_2 is closed. Such a switch is open at all other times.

In Fig. 8, charge is added to capacitor C_2 while Φ_2 is at a logic '1'. Once Φ_2 becomes a logic '0' and Φ_1 becomes a logic '1', the op amp 16a must charge capacitor C_3 from 0 volts to the voltage that the output of op amp 16a had achieved during the time Φ_2 was a logic '1'. Since practical implementations of op amps have a finite output impedance, gain, and bandwidth, the output of op amp 16a will glitch at the beginning of the time during which Φ_1 is a logic '1'. This is undesirable and may lead to reduced performance if such a structure is used in a sigma-delta modulator which performs an analog-to-digital conversion.

In Fig. 7, capacitor 24 and capacitor 22 are charging on the same clock phase. Because of this, op amp output node 28 does not glitch between clock phases. Such a structure may have the added benefit of increased performance when used in a sigma-delta modulator which is configured as an A/D converter circuit.

For reasons previously stated, it is desirable to have a second-order sigma-delta modulator circuit with only one unit delay. Such a modulator, as shown in Fig. 6, would have the desired transfer function given by the following equation:

Equation A: $y(z) = z^{-1}x(z) + E(z)(1-z^{-1})^2$

In Equation A, E(z) represents the quantization noise of a quantizer Q_1 modelled as a summing node 30 in Fig. 6, where y(z) represents the output signal 6 of modulator 5 and x(z) represents a sampled analog input signal 7.

Referring to Fig. 6, y(z) can be represented by the following equation:

Equation 1: $y(z) = E(z) + C(z)$

Solving the block diagram given in Fig. 6 for C(z) yields the following equation:

Equation 2: $C(z) = \{z^{-1}x(z) - y(z)[z^{-(Q+1)} + 2z^{-(P+1/2)} - 2z^{-(P+3/2)}] / (1-z^{-1})^2\}$

Now, after substituting C(z) in Equation 2 into Equation 1 and solving algebraically, the following equation results:

$$y(z)\,(1-z^{-1})^2 = E(1-z^{-1})^2 + z^{-1}x(z) - y(z)[z^{-(Q+1)} + 2z^{-(P+1/2)} - 2z^{-(P+3/2)}]$$

The above equation can be algebraically rearranged into the following equation:

$$y(z)\,[1 - 2z^{-1} + z^{-2} + z^{-(Q+1)} + 2z^{-(P+1/2)} - 2z^{-(P+3/2)}] = z^{-1}x(z) + E(z)(1-z^{-1})^2$$

The right hand side of the equation above is identical to the right hand side of Equation A, *supra*. Algebraically, this is true only if the following identity is true:

$$1 - 2z^{-1} + z^{-2} + z^{-(Q+1)} + 2z^{(P+1/2)} - 2z^{-(P+3/2)} = 1$$

Rearranging the above equation yields:

$$- 2z^{-1} + z^{-2} + z^{-(Q+1)} + 2z^{-(P+1/2)} - 2z^{-(P+3/2)} = 0$$

With $Q = 1$ and $P = 1/2$, the above equation is correctly resolved. Thus, the desired equation, $y(z) = z^{-1}\,x(z) + E(z)(1-z^{-1})^2$, is the transfer function for the block diagram shown in Fig. 6 when $Q = 1$ and $P = 1/2$. In other words, in order to satisfy the desired transfer function, there would be a delay of 1/2 of a sample period from the output of the quantizer Q_1 to the input of the gain of 2 block 15. Also, there would be a full sample period delay from the output of the quantizer Q_1 to the input of summing node 10.

Figure 10 illustrates the functional block diagram implementation of the current invention illustrated by a fourth-order sigma-delta modulator 9 formed by connecting together two, second-order sigma-delta modulators 11 and 13, each including 1/2 unit delay integrators associated therewith. The output signal 15, $y_1(z)$, in Fig. 10 is represented by the following equation:

$$y_1(z) = z^{-1}x(z) + E_1(z)(1-z^{-1})^2$$

The equation for output signal 17, $y_2(z)$, can be represented by the following equation:

$$y_2(z) = (1/C)z^{-1}y_1(z) - (1/C)z^{-1}E_1(z)$$

The term $E_1(z)$ is removed in equations for $y_1(z)$ and $y_2(z)$ so the following desired fourth-order output equation of the fourth-order modulator, as shown in Fig. 10, is achieved.

$$y_{out}(z) = z^{-2}x(z) + CE_2(z)(1-z^{-1})^4$$

To accomplish this, the following steps occur: Firstly, the $y_2(z)$ equation is multiplied by C, C representing a constant, which yields $y_3(z)$ as follows:

$$y_3(z) = z^{-1}y1(z) - z^{-1}E_1(z) + CE_2(z)(1-z^{-1})^2$$

Secondly, the term $z^{-1}y_1(z)$ is subtracted from $y_3(z)$ yielding the equation $y_4(z)$ as follows:

$$y_4(z) = -z^{-1}E_1(z) + CE_2(z)(1-z^{-1})^2$$

Next, $y_4(z)$ is multiplied by the term $(1-z^{-1})^2$ yielding the equation $y_5(z)$ as follows:

$$y_5(z) = -z^{-1}(1-z^{-1})^2E_1(z) + C(1-z^{-1})^4E_2(z)$$

Equation $y_1(z)$ is then multiplied by the term z^{-1} which yields equation y_6, as follows:

$$y_6(z) = z^{-2}x(z) + z^{-1}E_1(z)(1-z^{-1})^2$$

Finally, equation $y_5(z)$ is added to equation $y_6(z)$ yielding the desired equation for $y_{out}(z)$, as follows:

$$y_{out}(z) = z^{-2}x(z) + CE_2(z)(1-z^{-1})^4$$

Fig. 11 illustrates the post-quantization network 23 which corresponds to the aforementioned equations that results in the above equation for $y_{out}(z)$, 21. Output signals 15 and 17, $y_1(z)$ and $y_2(z)$ from Fig. 10 are connected to $y_1(z)$ and $y_2(z)$, respectively, in Fig. 11.

Thus, in an A/D converter application, the output signal 21, $y_{out}(z)$, in Fig. 11 is available as an input signal to additional circuitry, such as a decimator filter.

Fig. 12 illustrates how scaling is employed in the design of the second-order modulator 25 to prevent the integrators 36 and 38 from clipping, while not affecting the transfer function of the second-order sigma-delta modulator 25. The scaling is accomplished by using constants K_1 and K_2. Thus, the integrator in Fig. 12, is shown within the dashed area 36, which includes summing node 10, 1/2 unit delay integrator block 12 and a scaling factor $1/K_1$. Likewise, the other integrator in Fig. 5, shown within the dashed area 38,

includes summing node 11, 1/2 unit delay integrator block 14, and constants K_1, $1/K_2$ and 2. Since $1/K_1$ in integrator 36 is compensated by factor K_1 in integrator 38, no net change occurs in the transfer function due to scaling factor $1/K_1$. The quantizer Q_1, denoted by summing node 13, with noise $E_1(z)$ as an input, is typically a comparator which quantizes only the sign of the signal input to it. Thus, the term $1/K_2$ can be of arbitrary size and will not affect the transfer function of the second-order sigma-delta modulator 25.

When two second-order sigma delta modulator sections, as shown in Fig. 13, are connected together to form a fourth-order modulator, the term $1/K_2$ acts as the 1/C scaling factor shown in Fig. 10. The resulting fourth-order modulator 27 is shown in Fig. 13. The post-quantization network which combines outputs $y_1(z)$ and $y_2(z)$ for sigma-delta modulator 27 shown in Fig. 13 is identical to the post-quantization correction network 23 shown in Fig. 11, with the constant C in Fig. 11 being replaced by the constant K_2.

Fig. 14 depicts an embodiment of the analog portion of the fourth-order sigma-delta A/D converter of the present invention. The implementation shown is a single ended configuration. If output signal CMP_1 is a logic '1' and output signal CMP_1* is a logic '0', then negative reference voltage DNEG is selected as an input to the summing integrator 40 and positive reference voltage DPOS is selected as an input to the summing integrator 41. If output signal CMP_1 is a logic '0' and output signal CMP_1* is a logic '1' then reference voltage DPOS is selected as an input to the summing integrator 40 and reference voltage DNEG is selected as an input to the summing integrator 41.

If output signal CMP_2 is a logic '1' and output signal CMP_2* is a logic '0' then reference voltage DNEG is selected as an input to the summing integrator 42 and reference voltage DPOS is selected as an input to the summing integrator 43. Likewise if CMP_2 is a logic '0' and CMP_2* is a logic '1' then reference voltage DPOS is selected as an input to the summing integrator 42 and reference voltage DNEG is selected as an input to the summing integrator 43.

Figure 15 is a timing diagram illustrating the timing relationships between the following signals which are shown in Fig. 14: Φ_1, Φ_2, the output

$y_1a(z)$ of integrator 40, the output $y_1b(z)$ of integrator 41, the output $y_2a(z)$ of integrator 42, and the output $y_2b(z)$ of integrator 43.

The transfer function of summing integrator 40 in Fig. 14 can be represented by the following equation:

$$y_1a(z) = [(C_1/C_3)x(z) - z^{-1}(C_2/C_3)y_1(z)]z^{-1/2}/(1-z^{-1})$$

Since the output of $y_1(z)$ is sampled on Φ_2, there is a 1/2 sample period delay in the feed-forward path of the integrator which is represented by the $z^{-1/2}$ term in the above equation. The logic value of CMP_1 and CMP_1* determine whether DPOS or DNEG is connected to the input A of integrator 40 in Fig. 14. Since CMP_1 (which corresponds to $y_1(z)$) connects reference voltage DNEG to the input A of integrator 40, an inherent negation is performed on $y_1(z)$ as it is fed into input A of integrator 40. Thus the summing integrator 40 acts to effectively calculate the scaled difference between the input signal $y_1(z)$ and the output signal $y_1(z)$. Also, since the actual value of $y_1(z)$, which is used in the subtraction process and whose output is sampled during the Φ_2 clock phase is actually the output $y_1(z)$ which was calculated at the previous Φ_2 clock phase, an inherent unit delay exists in the feedback path from $y_1(z)$ to the input A of integrator 40. This is represented by the z^{-1} term before the $y_1(z)$ term in the above equation. Since an inherent delay exists in the feedback path from $y_1(z)$ to the input A of integrator 40, no explicit latch is required to perform this function.

The output $y_1(z)$, which is essentially $y_1b(z)$ that has been sampled during the Φ_2, can be represented by the following equation:

$$y_1(z) = [(C_4/C_6)y_1a(z) - (C_5/C_6)z^{-1/2}y_1(z)]z^{-1/2}/(1-z^{-1})$$

There is an extra one-half sample delay in front of the $y_1(z)$ term in the above equation which is represented by the $z^{-1/2}$ term. This is because the actual value of $y_1(z)$ which is used is the value of $y_1(z)$ which existed during the Φ_1 cycle prior to the Φ_2 cycle during which the output $y_1b(z)$ is sampled.

Referring to the block diagram in Fig. 12, it can be seen that the desired equation for $y_1d_1(z)$ is as follows:

$$y_1d_1(z) = (1/K_1)[x(z) - z^{-1}y_2d_1(z)]z^{-1/2}(1-z^{-1})$$

One can see that the above equation is of the same form as the equation for $y_1a(z)$ given previously. In the above equation, the term $1/K_1$ is realized by the capacitor ratio C_1/C_3 as well as the ratio C_2/C_3 in Fig. 14.

Likewise, referring to Fig. 12, the desired equation for $y_2d_1(z)$ can be represented by the following equation:

$$y_2d_1(z) = [(K_1/K_2)y_1d(z) - (2/K_2)z^{-1/2}y_2d_1(z)]z^{-1/2}/(1-z^{-1})$$

This equation is of the same form given for the equation for $y_1(z)$, given previously. In this case, the ratio K_1/K_2 is realized by the capacitor ratio C_4/C_6 in Fig. 14. Likewise, the term $2/K_2$ would be realized by the capacitor ratio C_5/C_6. As explained previously in this disclosure, any effective scaling immediately before the quantizer will have no effect on the overall transfer function since a 1 bit quantizer only quantizes the sign of the signal at its input. Thus, the second-order sigma-delta modulator shown in Fig. 14, which includes integrator 40, integrator 41, and comparator 47, can be represented by the following equation:

$$y_1(z) = z^{-1}x(z) + E_1(z)(1-z^{-1})^2$$

In the above equation, $y_1(z)$ is the output of comparator 47, $x(z)$ is the sampled analog input to the sigma-delta modulator and $E_1(z)$ is the quantization noise due to comparator 47.

Using similar arguments as have been used in the foregoing discussion, appropriate equations for the second, second-order modulator shown in Fig. 14 which includes integrator 42, integrator 43, and comparator 49, can be developed. Thus, it can be seen that the two sigma-delta modulators which are shown in Fig. 14 are an appropriate practical embodiment of the two sigma-delta modulators shown in block diagram form in Fig. 10.

A preferred method of implementing the analog portion of the architecture is to utilize fully differential design techniques. Examples of differential differencing integrators, which may replace the summing integrators 40 - 43 shown in Fig. 14, are shown in Figs. 16 and 17. The timing shown in Figs. 16 and 17 is preferred where the differential differencing integrators shown therein replace summing integrators 40 and

42 in Fig. 14. When the integrators of Figs. 16 and 17 are substituted for integrators 41 and 43 in Fig. 14, the clocks Φ_1 and Φ_2 shown within hashed area A of Figs. 16 and 17 are reversed (i.e., Φ_1 clocks become Φ_2 and vice versa).

Other integrators have been described in the literature, including correlated-double-sampled and chopper stabilized integrators. These techniques may also be used to implement the aforementioned integrators. Three-phase clocking may also be employed which would allow both the input signal and the DPOS/DNEG signals to be double-sampled.

To reduce signal dependent charge injection and its accompanying harmonic distortion, clock phases Φ_1 and Φ_2 can be implemented as four clocks, as shown in Fig. 18. This technique is described by Kuang-Lu Lee and Robert G. Meyer, *IEEE JSSC*, Dec. 1985, Vol. SC-20, No. 6, pp. 1103-1113, entitled, *Low-Distortion Switched Capacitor Filter Design Techniques*, incorporated herein for all purposes.

As shown in Fig. 19, utilizing the four clock technique of Fig. 18, switches controlled by S_3 open slightly before switches controlled by S_1 and switches controlled by S_4 open slightly before switches controlled by S_2. When switches controlled by S_3 open, charge is injected onto capacitors C_1A and C_1B. Since switches controlled by S_3 previously connected one plate of C_1A and one plate of C_1B to a reference point, the charge that is injected due to switches controlled by S_3 opening is not input signal dependent. When switches controlled by S_1 open, capacitors C_1A and C_1B already have one plate floating. Thus, the action of switches controlled by S_1 cannot inject charge onto C_1A or C_1B. Likewise, since before opening, switches controlled by S_4 were previously connected to a virtual ground node, no input signal dependent charge is injected onto capacitors C_1A, C_1B, C_3A, or C_3B. When switches controlled by S_2 open, capacitors C_1A and C_1B already have one plate floating. Thus, the action of opening switches controlled by S_2 cannot inject charge onto capacitors C_1A and C_1B.

Fig. 20 graphically illustrates the plot of simulated signal to noise plus distortion ratio levels (SNDR) for $K_1=4$, $K_2=8$, $K_3=4$, and $K_4=8$ with an oversampling ratio of 64. Zero dB is defined as a full-scale input voltage

which is one-half the D/A converter reference voltage, which for a differential implementation of Figs. 16 and 17 would be the voltage defined by DPOS-DNEG.

In another embodiment, the invention disclosed herein may be used as a digital noise shaper for a D/A converter implementation. In that case, the two second-order sigma-delta modulators which are connected together in Fig. 10 would be implemented as digital circuitry comprised of appropriate adders, subtractors, accumulators, multipliers, and quantizers. The post-quantizer circuitry shown in Fig. 11 would be modified as shown in Fig. 21. Digital signal $y_6(z)$ would be converted to an analog signal by D/A converter 32. Likewise, digital signal $y_5(z)$ would be converted to an analog signal by D/A converter 34. The resultant signals, $y_6a(z)$ and $y_5a(z)$, respectively would then be summed together by an analog summing node 72. There are numerous methods by which two analog signals may be summed together which are well known by those skilled in the art. Likewise, there are numerous methods which are known by those skilled in the art by which a digital signal may be converted to an analog signal. Any such method would be appropriate for D/A converters 32 and 34 in Fig. 21.

If the quantizer Q_1 in the second-order sigma-delta modulator 11 shown in Fig. 10 quantizes only the sign of the signal input to it, signal $y_1(z)$, and thus signal $y_6(z)$, would be represented by a 1-bit digital signal. A D/A converter which converts a 1-bit digital signal to an analog signal would result in an analog signal with only two output voltage, or current levels, possible. Such a D/A converter would be inherently linear and thus would contribute no distortion terms to the final analog signal, y_{out}. If the quantizer Q_2 in the second-order sigma-delta modulator 13 shown in Fig. 10 likewise quantizes only the sign of the signal input to it, then signal $y_2(z)$ would also be represented by a 1-bit digital signal. After being processed according to the aforementioned equations as illustrated in the block diagram shown in Fig. 21, it is clear that signal $y_5(z)$ would be represented by a plurality of bits for any value of C greater than one. Thus, the D/A converter 34 would convert a signal represented by a plurality of bits to an analog signal would

have a plurality of possible output voltages, or currents, which correspond to any possible code represented by $y_5(z)$.

As stated previously herein, signal $y_5(z)$ can be represented by the following equation:

$$y_5(z) = -z^{-1}(1-z^{-1})^2E_1(z) + C(1-z^{-1})^4E_2(z)$$

As shown in the above equation, $y_5(z)$ contains no terms which represent the input signal, x(z). Thus, the D/A converter 34 in Fig. 21 will add no terms which would cause harmonic distortion in the final output signal y_{out} if there are any nonidealities in the D/A converter 34. If D/A converter 34 is nonideal, signal $y_5a(z)$ may be represented by the following equation:

$$y_5a(z) = R[-z^{-1}(1-z^{-1})^2E_1(z) + C(1-z^{-1})^4E_2(z)]$$

In the above equation, R is a term which represents any nonidealities, or nonlinearities, in D/A converter 34 in Fig. 21. If D/A converter 32 in Fig. 21 is ideal, then the following equation would represent $y_6a(z)$:

$$y_6a(z) = z^{-2}x(z) + z^{-1}E_1(z)(1-z^{-1})^2$$

The final output signal, $y_{out}(z)$ would then be the sum of $y_5a(z)$ and $y_6a(z)$ and would be represented by the following equation:

$$y_{out}(z) = z^{-2}x(z) + E_1(z)z^{-1}(1-z^{-1})^2(1-R) + RCE_2(z)(1-z^{-1})^4$$

It can be seen by the above equation that if D/A converter 34 of Fig. 4a is not perfect, then the quantization noise of the first, second-order sigma-delta modulator would not be perfectly canceled and thus, some quantization noise $E_1(z)$ would be present in the final output, $y_{out}(z)$. Also, the quantization noise $E_2(z)$ would be modified slightly. Thus, it can be seen that while additional noise may be introduced due to nonidealities, additional harmonic distortion will not be produced.

The foregoing disclosure and description of the invention are illustrative and explanatory of the preferred embodiments, and changes in the individual components, elements or connections may be made without

departing from the spirit of the invention and the scope of the following claims.

What is claimed is:

CLAIMS

1. A second-order sigma-delta modulator for an A/D converter, comprising:

an analog input signal;

a digital output signal;

a first summing node, including a first input connected to said analog input signal,

a second input connected to a unit delay feedback delay block, and an output connected to an input of a first integrator, wherein said first integrator includes a one-half unit delay associated therewith;

a second summing node, including a first input connected to an output of said one-half unit delay first integrator, a second input connected to an output of a one-half unit delay feedback delay block, and an output connected to an input of a second integrator, wherein said second integrator includes a one-half unit delay associated therewith;

a quantizer, including an input connected to an output of said one-half unit delay second integrator, and an output connected to an input of said one-half unit delay feedback delay block, connected to an input of said unit delay feedback delay block and connected to said digital output signal.

2. The second-order modulator of claim 1, wherein said output of said one-half unit delay feedback delay block is multiplied by a factor of 2 prior to being input to said second input of said second summing node.

3. A second-order sigma-delta modulator, for an A/D converter, comprising:

a first summing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to an analog input signal, wherein said first and second switched

capacitors are also selectively connected to a first input of a first summing integrator and wherein a second input of said first summing integrator is connected to ground;

a second summing integrator circuit, which includes:

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to an output of said first summing integrator, wherein said third and fourth switched capacitors are also selectively connected to a first input of a second summing integrator and wherein a second input of said second summing integrator is connected to ground;

a comparator having a differential output, wherein an output of said second summing integrator is input to said comparator.

4. The second-order modulator of claim 3, further comprising:

a first feedback capacitor connected between said first input of said first summing integrator and said output of said first summing integrator, and a second feedback capacitor connected between said first input of said second summing integrator and said output of said second summing integrator.

5. The second-order modulator of claim 4, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said analog input signal, said third switched capacitor is connected to said one of two said reference voltages, and said third and said fourth switched capacitors are connected to said first input of said second summing integrator; and

wherein during a second clock signal Φ_2, where said second clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of said first clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first summing integrator, said output of said first summing integrator is connected to said fourth switched capacitor, and said differential output of said comparator is valid.

6. A fourth-order sigma-delta modulator for an A/D converter, comprising:

a first second-order sigma-delta modulator, including:

a first summing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to an analog input signal, wherein said first and second switched capacitors are also selectively connected to a first input of a first summing integrator and wherein a second input of said first summing integrator is connected to ground;

a second summing integrator circuit, which includes:

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to an output of said first summing integrator, wherein said third and fourth switched capacitors are also selectively connected to a first input of a second summing integrator and wherein a second input of said second summing integrator is connected to ground;

a first comparator having a differential output, wherein an output of said second summing integrator is input to said first comparator;

a second-order sigma-delta modulator, including:

a third summing integrator circuit, which includes:

a fifth switched capacitor selectively connected to one of two said reference voltages;

a sixth switched capacitor selectively connected to said output of said second summing integrator, wherein said fifth

and sixth switched capacitors are also selectively connected to a first input of a third summing integrator and wherein a second input of said third summing integrator is connected to ground;

a fourth summing integrator circuit, which includes:

a seventh switched capacitor selectively connected to one of two said reference voltages;

an eighth switched capacitor selectively connected to an output of said third summing integrator, wherein said seventh and eighth switched capacitors are also selectively connected to a first input of a fourth summing integrator and wherein a second input of said fourth summing integrator is connected to ground;

a second comparator, having a differential output, wherein an output of said fourth summing integrator is input to said second comparator.

7. The fourth-order modulator of claim 6, further comprising:

a first feedback capacitor connected between said first input of said first summing integrator and said output of said first summing integrator, a second feedback capacitor connected between said first input of said second summing integrator and said output of said second summing integrator, a third feedback capacitor connected between said first input of said third summing integrator and said output of said third summing integrator, and a fourth feedback capacitor connected between said first input of said fourth summing integrator and said output of said fourth summing integrator.

8. The fourth-order modulator of claim 7, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said analog input signal, said third switched capacitor is connected to one of two said reference voltages, said third and said fourth switched

capacitors are connected to said first input of said second summing integrator, said fifth switched capacitor is connected to one of two said reference voltages, said sixth switched capacitor is connected to said output from said first comparator, said seventh switched capacitor is connected to one of two said reference voltages, and said seventh and eighth switched capacitors are connected to said first input of said fourth summing integrator; and

wherein during a second clock signal Φ_2, where clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first summing integrator, said output of said first summing integrator is connected to said fourth switched capacitor, said differential output of said first comparator is valid, said fifth and seventh switched capacitor are connected to said first input of said third summing integrator, said output of said third summing integrator is connected to said eighth switched capacitor and said differential output of said second comparator is valid.

9. A fourth-order sigma-delta modulator for an A/D converter, comprising:

an analog input signal;

a first digital output signal;

a first summing node, including a first input of said first summing node connected to said analog input signal;

a second input of said first summing node connected to a first unit delay feedback block, and an output of said first summing node connected to an input of a first integrator, wherein said first integrator includes a one-half unit delay associated therewith;

a second summing node, including a first input of said second summing node connected to an output of said one-half unit delay first integrator, a second input of said second summing node connected to an output of a first one-half unit delay feedback block, and an output

of said second summing node connected to an input of a second integrator, wherein said second integrator includes a one-half unit delay associated therewith;

a first quantizer, including a first quantizer input connected to an output of said one-half unit delay second integrator, and a first quantizer output connected to: an input of said first one-half unit delay feedback block, to an input of said first unit delay feedback block and to said first digital output signal;

a second digital output signal;

a third summing node, including a first input of said third summing node connected to said first quantizer input;

a second input of said third summing node connected to a second unit delay feedback block, and an output of said third summing node connected to an input of a third integrator, wherein said third integrator includes a one-half unit delay associated therewith;

a fourth summing node, including a first input of said fourth summing node connected to an output of said one-half unit delay third integrator, a second input of said fourth summing node connected to an output of a second one-half unit delay feedback block, and an output of said fourth summing node connected to an input of a fourth integrator, wherein said fourth integrator includes a one-half unit delay associated therewith;

a second quantizer, including a second quantizer input connected to an output of said one-half unit delay fourth integrator, and a second quantizer output connected to: an input of said second one-half unit delay feedback block, to an input of said second unit delay feedback block and to said second digital output signal.

10. The fourth-order sigma-delta modulator of claim 9, wherein:

the second-order system of claim 1, wherein said output of said first one-half unit delay feedback block is multiplied by a factor of 2 prior to being input to said second input of said second summing node; and

wherein said output of said second one-half unit delay feedback block is multiplied by a factor of 2 prior to being input to said second input of said fourth summing node.

11. A second-order sigma-delta modulator for an A/D converter, comprising:

a first differential differencing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to a first analog differential input signal, wherein said first and second switched capacitors are also selectively connected to a first input of a first differential differencing integrator;

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to a second differential analog input signal, wherein said third and fourth switched capacitors are also selectively connected to a second input of said first differential differencing integrator;

a second differential differencing integrator circuit, which includes:

a fifth switched capacitor selectively connected to one of two said reference voltages;

a sixth switched capacitor selectively connected to a first differential output of said first differencing integrator, wherein said fifth and sixth switched capacitors are also selectively connected to a first input of a second differential differencing integrator;

a seventh switched capacitor selectively connected to one of two said reference voltages;

an eighth switched capacitor selectively connected to a second differential output of said first differencing integrator, wherein said seventh and eighth switched capacitors are also

selectively connected to a second input of said second differencing integrator; and

a comparator having a differential input and output, wherein a differential output of said second differencing integrator is input to said comparator differential input, and wherein said comparator output is a one-bit digital signal.

12. The second-order sigma-delta modulator of claim 11, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said first differential analog input signal, said third switched capacitor is connected to one of two said reference voltages, said fourth switched capacitor is connected to said second differential analog input signal, said fifth and said seventh switched capacitors are connected to one of two said reference voltages, said fifth and sixth switched capacitors are connected to said first input of said second differencing integrator, said seventh and eight switched capacitors are connected to said second input of said second differencing integrator; and

wherein during a second clock signal Φ_2, where clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first differencing integrator, said third and fourth switched capacitors are connected to said second input of said first differencing integrator, said first and second differential outputs of said first differencing integrator are connected to said sixth and eighth switched capacitors, respectively, and said differential output of said first comparator is valid.

13. A fourth-order sigma-delta modulator for an A/D converter, comprising:

a first second-order sigma-delta modulator, including:

a first differential differencing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to a first analog differential input signal, wherein said first and second switched capacitors are also selectively connected to a first input of a first differential differencing integrator;

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to a second differential analog input signal, wherein said third and fourth switched capacitors are also selectively connected to a second input of said first differential differencing integrator;

a second differential differencing integrator circuit, which includes:

a fifth switched capacitor selectively connected to one of two said reference voltages;

a sixth switched capacitor selectively connected to a first differential output of said first differencing integrator, wherein said fifth and sixth switched capacitors are also selectively connected to a first input of a second differential differencing integrator;

a seventh switched capacitor selectively connected to one of two said reference voltages;

an eighth switched capacitor selectively connected to a second differential output of said first differencing integrator, wherein said seventh and eighth switched capacitors are also selectively connected to a second input of said second differencing integrator;

a first comparator having a differential input and output, wherein a differential output of said second differencing integrator is input to said first comparator differential input;

a second second-order sigma-delta modulator, including:

a third differential differencing integrator circuit, which includes:

a ninth switched capacitor selectively connected to one of two said reference voltages;

a tenth switched capacitor selectively connected to said differential output of said second differencing integrator, wherein said ninth and tenth switched capacitors are also selectively connected to a first input of a third differential differencing integrator;

an eleventh switched capacitor selectively connected to one of two said reference voltages;

a twelfth switched capacitor selectively connected to said differential output of said second differential integrator, wherein said eleventh and twelfth switched capacitors are also selectively connected to a second input of said third differential differencing integrator;

a fourth differential differencing integrator circuit, which includes:

a thirteenth switched capacitor selectively connected to one of two said reference voltages;

a fourteenth switched capacitor selectively connected to a first differential output of said third differencing integrator, wherein said thirteenth and fourteenth switched capacitors are also selectively connected to a first input of a fourth differential differencing integrator;

a fifteenth switched capacitor selectively connected to one of two said reference voltages;

a sixteenth switched capacitor selectively connected to a second differential output of said third differencing integrator, wherein said fifteenth and sixteenth switched capacitors are also selectively connected to a second input of said fourth differencing integrator;

a second comparator having a differential input and output, wherein a differential output of said fourth differencing integrator is input to said first comparator differential input, and wherein said second comparator output is a one-bit digital signal.

14. The fourth-order sigma-delta modulator of claim 13, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said first differential analog input signal, said third switched capacitor is connected to one of two said reference voltages, said fourth switched capacitor is connected to said second differential analog input signal, said fifth and said seventh switched capacitors are connected to one of two said reference voltages, said fifth and sixth switched capacitors are connected to said first input of said second differencing integrator, said seventh and eight switched capacitors are connected to said second input of said second differencing integrator, said ninth switched capacitor is connected to one of two said reference voltages, said tenth switched capacitor is connected to said differential output of said second differencing integrator, said eleventh switched capacitor is connected to one of two said reference voltages, said twelfth switched capacitor is connected to said differential output of said second differencing integrator, said thirteenth and said fifteenth switched capacitors are connected to one of two said reference voltages, said thirteenth and fourteenth switched capacitors are connected to said first input of said fourth differencing integrator, said fifteenth and sixteenth switched capacitors are connected to said second input of said fourth differencing integrator; and

wherein during a second clock signal Φ_2, where clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first differencing integrator, said third and fourth

switched capacitors are connected to said second input of said first differencing integrator, said first and second differential outputs of said first differencing integrator are connected to said sixth and eighth switched capacitors, respectively, said differential output of said first comparator is valid, said ninth and tenth switched capacitors are connected to said first input of said third differencing integrator, said eleventh and twelfth switched capacitors are connected to said second input of said third differencing integrator, said first and second differential outputs of said third differencing integrator are connected to said fourteenth and sixteenth switched capacitors, respectively, and said differential output of said second comparator is valid.

15. A second-order sigma-delta modulator for an A/D converter, comprising:

a first differential differencing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to a first or a second analog differential input signal, wherein said first and second switched capacitors are also selectively connected to a first input of a first differential differencing integrator;

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to said first or second differential analog input signal, wherein said third and fourth switched capacitors are also selectively connected to a second input of said first differential differencing integrator;

a second differential differencing integrator circuit, which includes:

a fifth switched capacitor selectively connected to one of two said reference voltages;

a sixth switched capacitor selectively connected to a first or second differential output of said first differencing integrator, wherein said fifth and sixth switched capacitors are also selectively connected to a first input of a second differential differencing integrator;

a seventh switched capacitor selectively connected to one of two said reference voltages;

an eighth switched capacitor selectively connected to said first or second differential output of said first differencing integrator, wherein said seventh and eighth switched capacitors are also selectively connected to a second input of said second differencing integrator; and

a comparator having a differential input and output, wherein a differential output of said second differencing integrator is input to said comparator differential input, and wherein said comparator output is a one-bit digital signal.

16. The second-order sigma-delta modulator of claim 11, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said first differential analog input signal, said third switched capacitor is connected to one of two said reference voltages, said fourth switched capacitor is connected to said second differential analog input signal, said fifth and said seventh switched capacitors are connected to one of two said reference voltages, said fifth and sixth switched capacitors are connected to said first input of said second differencing integrator, said sixth switched capacitor is connected to said second differential analog input signal, said seventh and eight switched capacitors are connected to said second input of said second differencing integrator, and said eighth switched capacitor is connected to said first differential analog input signal; and

wherein during a second clock signal Φ_2, where clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first differencing integrator, said second switched capacitor is connected to said second differential analog input signal, said third and fourth switched capacitors are connected to said second input of said first differencing integrator, said fourth switched capacitor is connected to said first differential analog input signal, said first and second differential outputs of said first differencing integrator are connected to said sixth and eighth switched capacitors, respectively, and said differential output of said comparator is valid.

17. A fourth-order sigma-delta modulator for an A/D converter, comprising:

a first second-order sigma-delta modulator, including:

a first differential differencing integrator circuit, which includes:

a first switched capacitor selectively connected to one of two reference voltages;

a second switched capacitor selectively connected to a first or a second analog differential input signal, wherein said first and second switched capacitors are also selectively connected to a first input of a first differential differencing integrator;

a third switched capacitor selectively connected to one of two said reference voltages;

a fourth switched capacitor selectively connected to said first or second differential analog input signal, wherein said third and fourth switched capacitors are also selectively connected to a second input of said first differential differencing integrator;

a second differential differencing integrator circuit, which includes:

a fifth switched capacitor selectively connected to one of two said reference voltages;

a sixth switched capacitor selectively connected to a first or second differential output of said first differencing integrator, wherein said fifth and sixth switched capacitors are also selectively connected to a first input of a second differential differencing integrator;

a seventh switched capacitor selectively connected to one of two said reference voltages;

an eighth switched capacitor selectively connected to said first or second differential output of said first differencing integrator, wherein said seventh and eighth switched capacitors are also selectively connected to a second input of said second differencing integrator;

a first comparator having a differential input and output, wherein a differential output of said second differencing integrator is input to said first comparator differential input, wherein said first comparator output is a one-bit digital signal;

a second second-order sigma-delta modulator, including:

a third differential differencing integrator circuit, which includes:

a ninth switched capacitor selectively connected to one of two reference voltages;

a tenth switched capacitor selectively connected to a first or a second analog differential input signal, wherein said ninth and tenth switched capacitors are also selectively connected to a first input of a third differential differencing integrator;

an eleventh switched capacitor selectively connected to one of two said reference voltages;

a twelfth switched capacitor selectively connected to said first or second differential analog input signal, wherein said eleventh and twelfth switched capacitors are also selectively

connected to a second input of said third differential differencing integrator;

a fourth differential differencing integrator circuit, which includes:

a thirteenth switched capacitor selectively connected to one of two said reference voltages;

a fourteenth switched capacitor selectively connected to a first or second differential output of said third differencing integrator, wherein said thirteenth and fourteenth switched capacitors are also selectively connected to a first input of a fourth differential differencing integrator;

a fifteenth switched capacitor selectively connected to one of two said reference voltages;

a sixteenth switched capacitor selectively connected to said first or second differential output of said third differencing integrator, wherein said fifteenth and sixteenth switched capacitors are also selectively connected to a second input of said fourth differencing integrator; and

a second comparator having a differential input and output, wherein a differential output of said fourth differencing integrator is input to said second comparator differential input, and wherein said second comparator output is a one-bit digital signal.

18. The fourth-order sigma-delta modulator of claim 13, wherein during a first clock signal Φ_1:

said first switched capacitor is connected to one of two said reference voltages, said second switched capacitor is connected to said first differential analog input signal, said third switched capacitor is connected to one of two said reference voltages, said fourth switched capacitor is connected to said second differential analog input signal, said fifth and said seventh switched capacitors are connected to one of two said reference voltages, said fifth and sixth switched capacitors are

connected to said first input of said second differencing integrator, said sixth switched capacitor is connected to said second differential analog input signal, said seventh and eight switched capacitors are connected to said second input of said second differencing integrator, said eighth switched capacitor is connected to said first differential analog input signal, said ninth switched capacitor is connected to one of two said reference voltages, said tenth switched capacitor is connected to said differential output of said second differencing integrator, said eleventh switched capacitor is connected to one of two said reference voltages, said twelfth switched capacitor is connected to said differential output of said second differencing integrator, said thirteenth and said fifteenth switched capacitors are connected to one of two said reference voltages, said thirteenth and fourteenth switched capacitors are connected to said first input of said fourth differencing integrator, said fourteenth switched capacitor is connected to said second differential analog input signal, said fifteenth and sixteenth switched capacitors are connected to said second input of said fourth differencing integrator, said sixteenth switched capacitor is connected to said first differential analog input signal; and

wherein during a second clock signal Φ_2, where clock signal Φ_2 has a leading edge that occurs subsequent in time to a leading edge of clock signal Φ_1:

said first and second switched capacitors are connected to said first input of said first differencing integrator, said second switched capacitor is connected to said second differential analog input signal, said third and fourth switched capacitors are connected to said second input of said first differencing integrator, said fourth switched capacitor is connected to said first differential analog input signal, said first and second differential outputs of said first differencing integrator are connected to said sixth and eighth switched capacitors, respectively, said differential output of said first comparator is valid, said ninth and tenth switched capacitors are connected to said first input of said third differencing integrator, said tenth switched

capacitor is connected to said second differential analog input signal, said eleventh and twelfth switched capacitors are connected to said second input of said third differencing integrator, said twelfth switched capacitor is connected to said first differential analog input signal, said first and second differential outputs of said third differencing integrator are connected to said fourteenth and sixteenth switched capacitors, respectively, and said differential output of said second comparator is valid.

19. A post-quantization network for a fourth-order sigma-delta modulator for an A/D converter, comprising:

a first digital input, output from a first second-order sigma-delta modulator;

a second digital input, output from a second second-order sigma-delta modulator; and

a digital output;

wherein said first digital input is connected to an input of a delay block and said second input is multiplied by a constant;

wherein an output of said delay block is connected to a first input of a first summing node and to a first input of a second summing node;

wherein said multiplied second input is connected to a second input of said first summing node;

wherein an output of said second summing node is provided to an input of a differentiator;

wherein an output of said differentiator is provided to a second input of said second summing node; and

wherein said digital output is provided by an output of said second summing node.

20. The fourth-order modulator of claim 9, further comprising:

a first post-quantization network input, output from said first quantizer output;

a second post-quantization network input, output from said second quantizer output; and

a post-quantization network digital output;

wherein said first network input is connected to an input of a network delay block and said second network input is multiplied by a constant;

wherein an output of said network delay block is connected to a first input of a first network summing node and to a first input of a second network summing node;

wherein said multiplied second network input is connected to a second input of said first network summing node;

wherein an output of said second network summing node is provided to an input of a differentiator;

wherein an output of said differentiator is provided to a second input of said second network summing node; and

wherein said network digital output is connected to an output of said second summing network node.

21. A post-quantization network for a fourth-order sigma-delta modulator for a D/A converter, comprising:

a first digital input, output from a first second-order sigma-delta modulator;

a second digital input, output from a second second-order sigma delta modulator; and

an analog output;

wherein said first digital input is connected to an input of a delay block;

wherein said second digital input is multiplied by a constant and is then provided to a first input of a first summing node;

wherein an output of said delay block is provided to a second input of said first summing node and to an input of a first D/A converter;

wherein an output of said first summing node is connected to an input of a differentiator;

wherein an output of said differentiator is input to a second D/A converter;

wherein an output of said first D/A converter is provided to a first input of a second summing node and an output of said second D/A converter is provided to a second input of said second summing node; and

wherein said analog output is connected to an output of said second summing node.

22. The network of claim 21, wherein said first D/A converter is a one-bit D/A converter.

23. The network of claim 21, wherein said second D/A converter is a multi-bit D/A converter.

24. A fourth-order sigma-delta modulator system for a D/A converter, comprising:

a digital input signal;

an analog output signal;

a first summing node, including a first input connected to said digital input signal,

a second input of said first summing node connected to a first unit delay feedback block, and an output of said first summing node connected to an input of a first integrator, wherein said first integrator includes a one-half unit delay associated therewith;

a second summing node, including a first input of said second summing node connected to an output of said one-half unit delay first integrator, a second input of said second summing node connected to

an output of a first one-half unit delay feedback block, and an output of said second summing node connected to an input of a second integrator, wherein said second integrator includes a one-half unit delay associated therewith;

a first quantizer, including a first quantizer input connected to an output of said one-half unit delay second integrator, and a first quantizer output connected to: an input of said first one-half unit delay feedback block, to an input of said first unit delay feedback block and to said first digital output signal;

a second digital output signal;

a third summing node, including a first input of said third summing node connected to said first quantizer input;

a second input of said third summing node connected to a second unit delay feedback block, and an output of said third summing node connected to an input of a third integrator, wherein said third integrator includes a one-half unit delay associated therewith;

a fourth summing node, including a first input of said fourth summing node connected to an output of said one-half unit delay third integrator, a second input of said fourth summing node connected to an output of a second one-half unit delay feedback block, and an output of said fourth summing node connected to an input of a fourth integrator, wherein said fourth integrator includes a one-half unit delay associated therewith;

a second quantizer, including a second quantizer input connected to an output of said one-half unit delay fourth integrator, and a second quantizer output connected to: an input of said second one-half unit delay feedback block, to an input of said second unit delay feedback block and to said second digital output signal;

a first post-quantization digital input, output from said first quantizer;

a second post-quantization digital input, output from said second quantizer;

wherein said first post-quantization digital input is connected to an input of a post-quantization delay block;

wherein said second post-quantization digital input is multiplied by a constant and is then provided to a first input of a first post-quantization summing node;

wherein an output of said post-quantization delay block is provided to a second input of said first post-quantization summing node and to an input of a first post-quantization D/A converter;

wherein an output of said first post-quantization summing node is connected to an input of a differentiator;

wherein an output of said differentiator is input to a second post-quantization D/A converter;

wherein an output of said post-quantization first D/A converter is provided to a first input of a second post-quantization summing node and an output of said second post-quantization D/A converter is provided to a second input of said second summing node; and

wherein said analog output signal is provided at an output of said second post-quantization summing node.

25. A fourth-order sigma-delta modulator system comprising:

a first second-order sigma-delta modulator having an input and an output;

a second-order sigma-delta modulator having an input and an output;

a post-quantization network having a first network input connected to said output of said first modulator and a second network input connected to said output of said second modulator; and

wherein said first and second modulators each include a first and a second integration stage, wherein each said integration stage includes an integrator with a 1/2 unit delay associated therewith.

26. The fourth-order modulator system of claim 25, wherein said first modulator further comprises a first modulator quantizer, said first

modulator quantizer being connected to an output of said second integration stage in said first modulator, and wherein an output of said first modulator quantizer is connected to said output of said first modulator.

27. The fourth-order modulator system of claim 26, wherein said second modulator further comprises a second modulator quantizer, said second modulator quantizer being connected to an output of said second integration stage in said second modulator, and wherein an output of said second modulator quantizer is connected to said output of said second modulator.

28. The fourth-order modulator system of claim 26, wherein a feedback path having a 1/2 unit delay associated therewith connects between said first modulator output and an input to said second integration stage in said first modulator, wherein a second feedback path, having a unit delay associated therewith, connects between said first modulator output and an input to said first integration stage in said first modulator.

29. The fourth-order modulation system of claim 27, wherein a feedback path having a 1/2 unit delay associated therewith connects between said second modulator output and an input to said second integration stage in said second modulator, wherein a second feedback path, having a unit delay associated therewith, connects between said second modulator output and an input to said first integration stage in said second modulator.

30. A fourth-order modulator system for a A/D converter, comprising:

an analog input signal;

a digital output signal;

a first second-order modulator comprising: a first switched capacitor selectively connected to either a positive or a negative reference voltage, said first switched capacitor also being selectively connected to a first input of a first op amp;

a first feedback capacitor connected between said first op amp first input and an output of said first op amp;

an analog input signal selectively connected to a second switched capacitor, wherein said second switched capacitor is selectively connected also to said first op amp first input;

a third switched capacitor selectively connected to either said positive or said negative reference voltage, said third switched capacitor also being selectively connected to a first input of a second op amp;

a second feedback capacitor connected between said second op amp first input and an output of said second op amp;

a fourth switched capacitor selectively connected to said output of said second op amp and selectively connected to said first input of said second op amp;

a first latching comparator, having a differential output, wherein a first input of said first latching comparator is connected to an output of said second op amp; and

a second second-order modulator, wherein an input of said second modulator is connected to said output of said second op amp.

31. The system of claim 30, wherein a second input of said first and said second op amp is connected to ground.

32. The system of claim 30, wherein said second modulator includes a second latching comparator having a differential output.

33. The system of claim 32, wherein said differential output of said first and said second latching comparators are digital control signals used to control switches which selectively connect said positive and said negative reference voltages to said first and third switching capacitors.

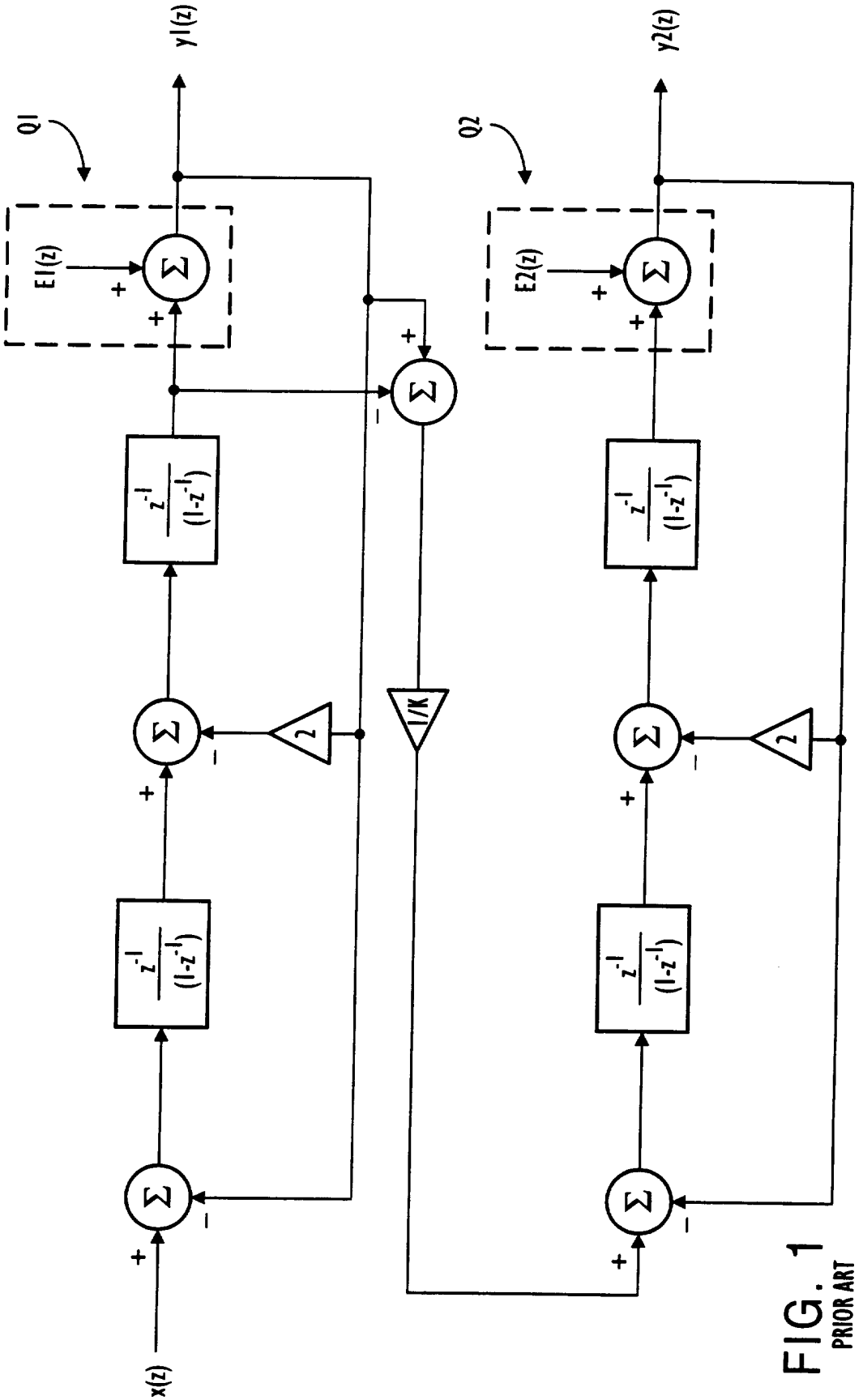


FIG. 1
PRIOR ART

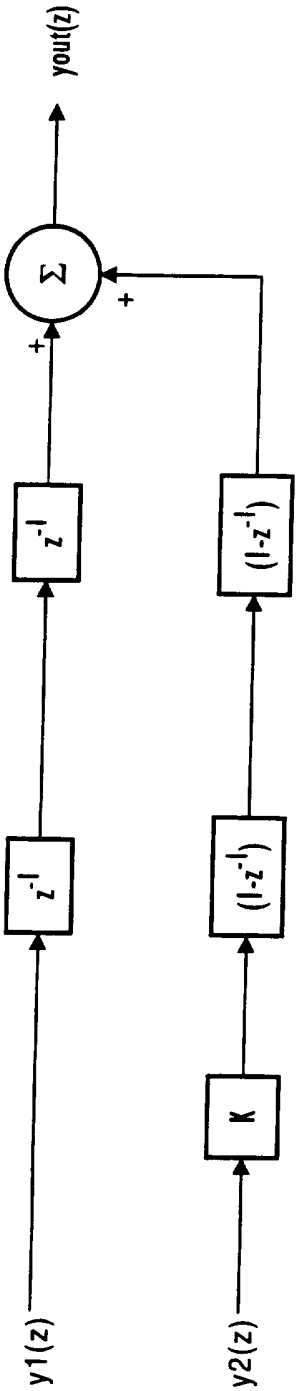


FIG. 2
PRIOR ART

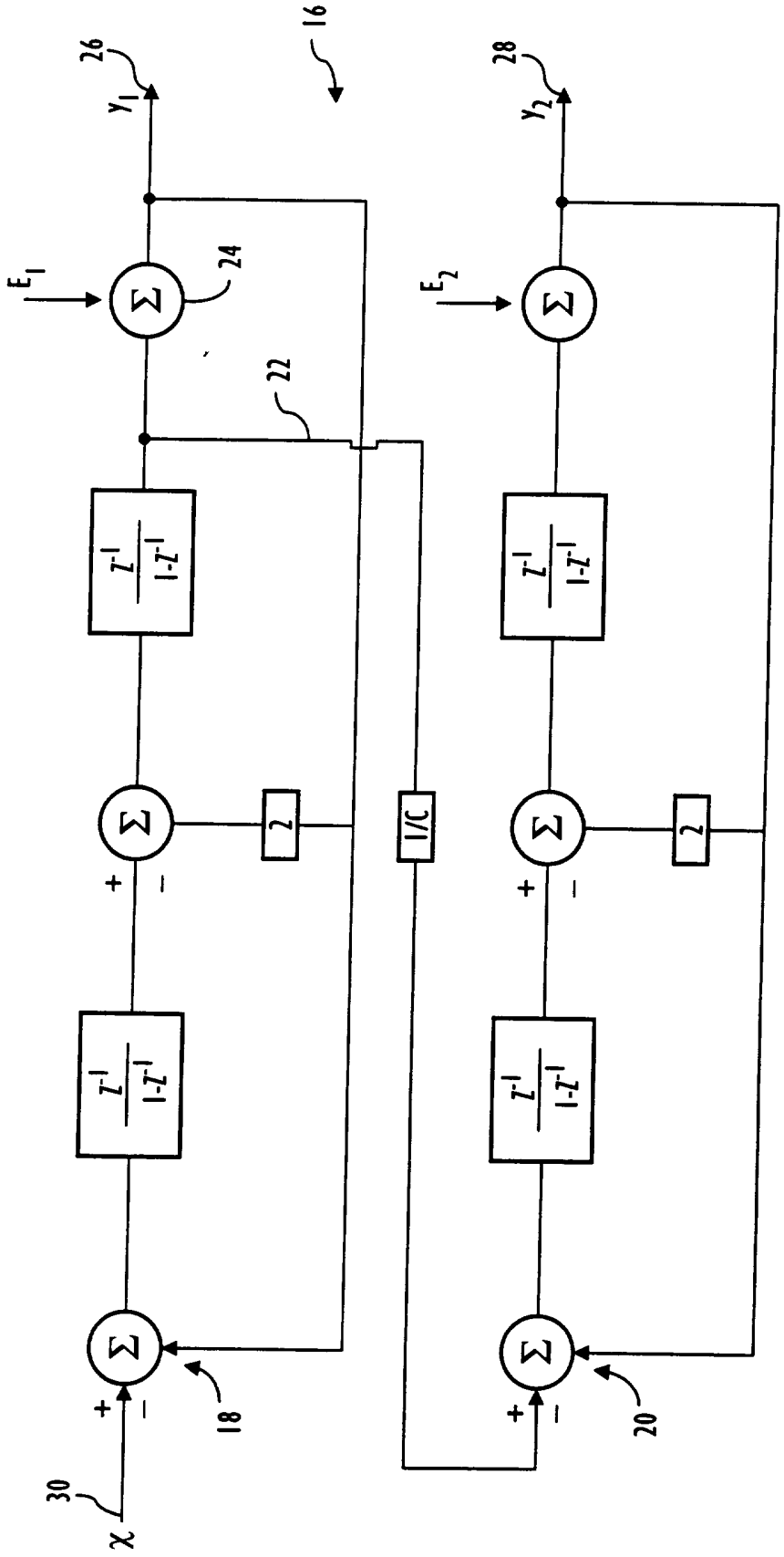


FIG. 3
PRIOR ART

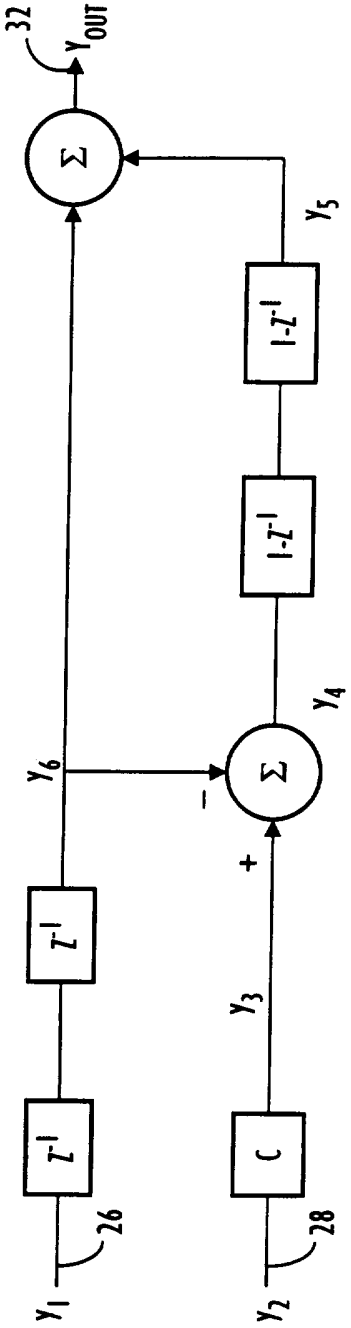


FIG 4
PRIOR ART

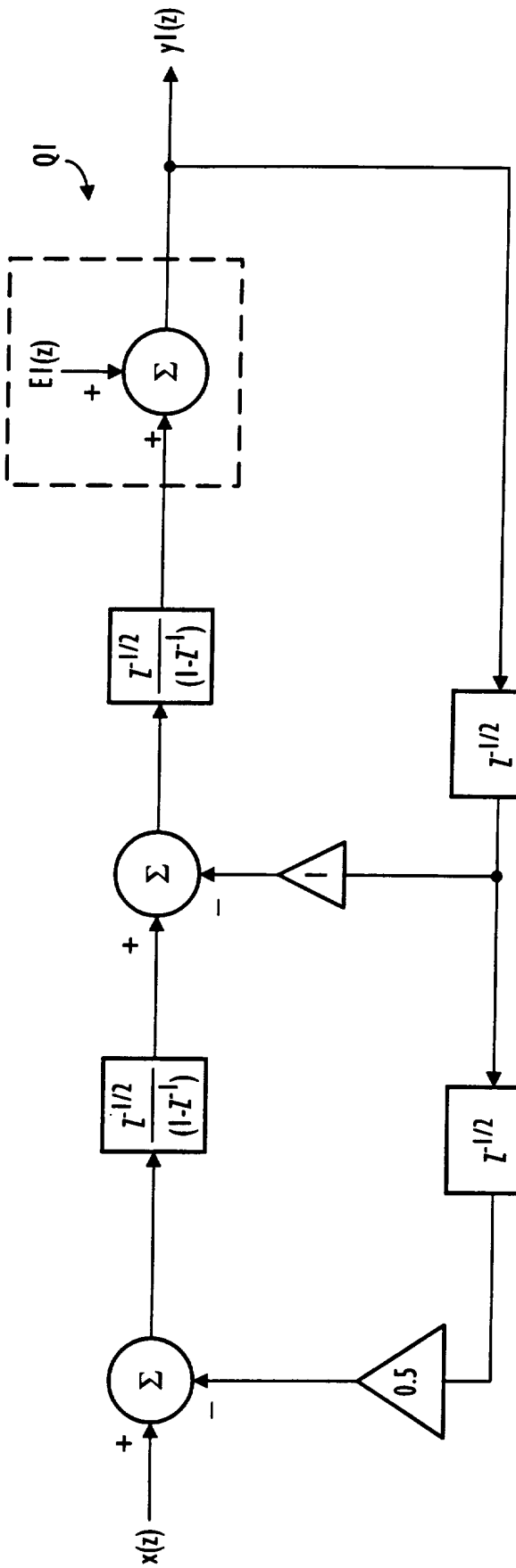


FIG. 5
PRIOR ART

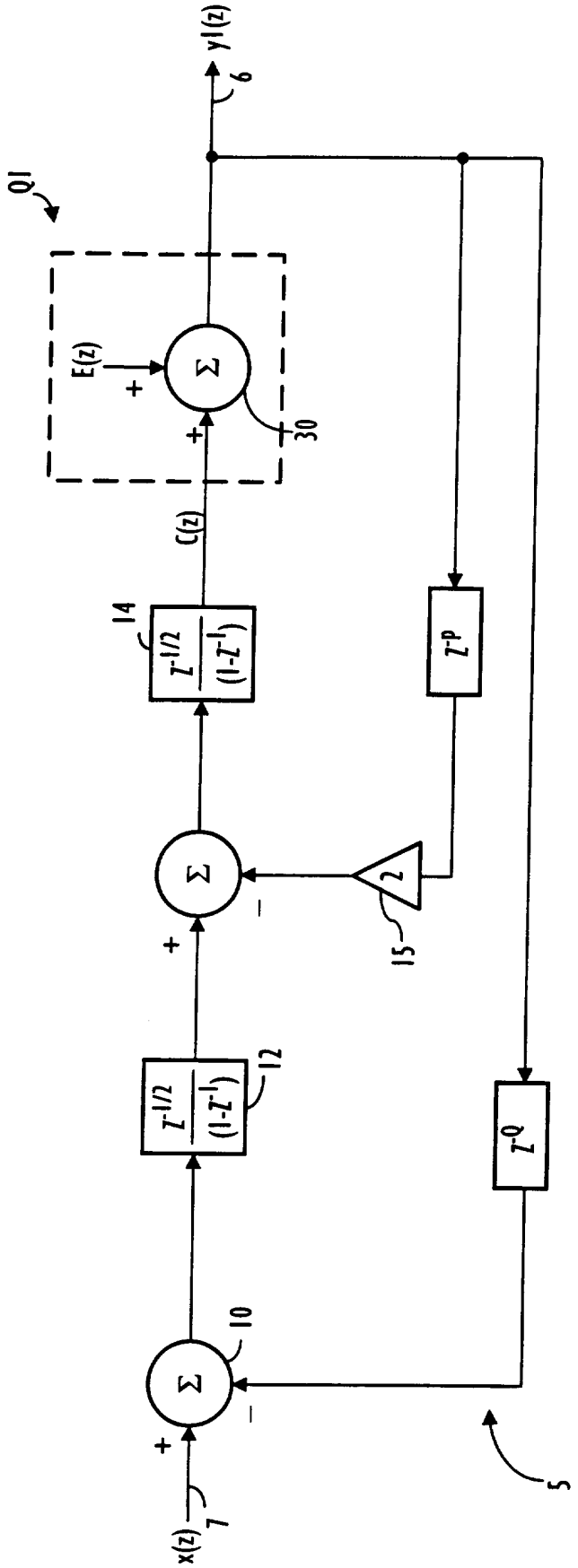


FIG. 6
PRIOR ART

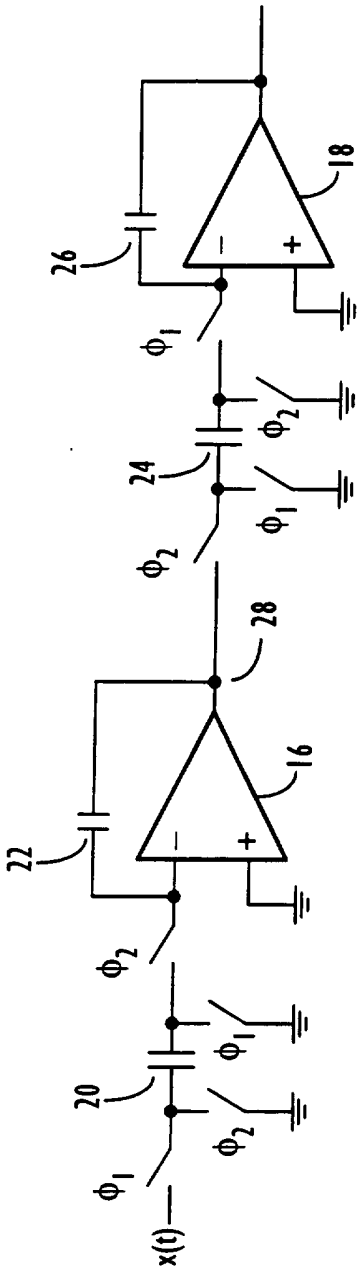

18
26
ϕ_1
ϕ_2
24
ϕ_2
ϕ_1
28
16
22
ϕ_2
ϕ_1
20
ϕ_2
ϕ_1
x(t)

FIG. 7

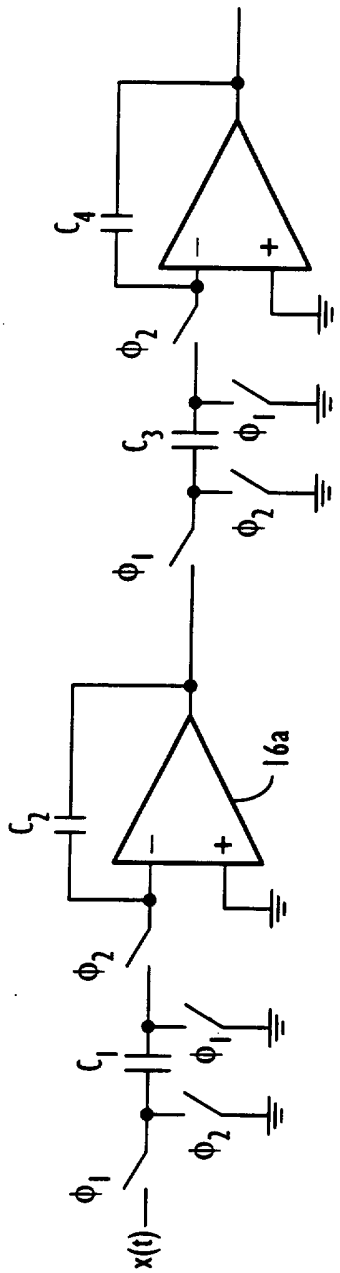

C_4
ϕ_2
C_3
ϕ_1
ϕ_2
ϕ_1
16a
C_2
ϕ_2
C_1
ϕ_1
ϕ_2
ϕ_1
x(t)

FIG. 8

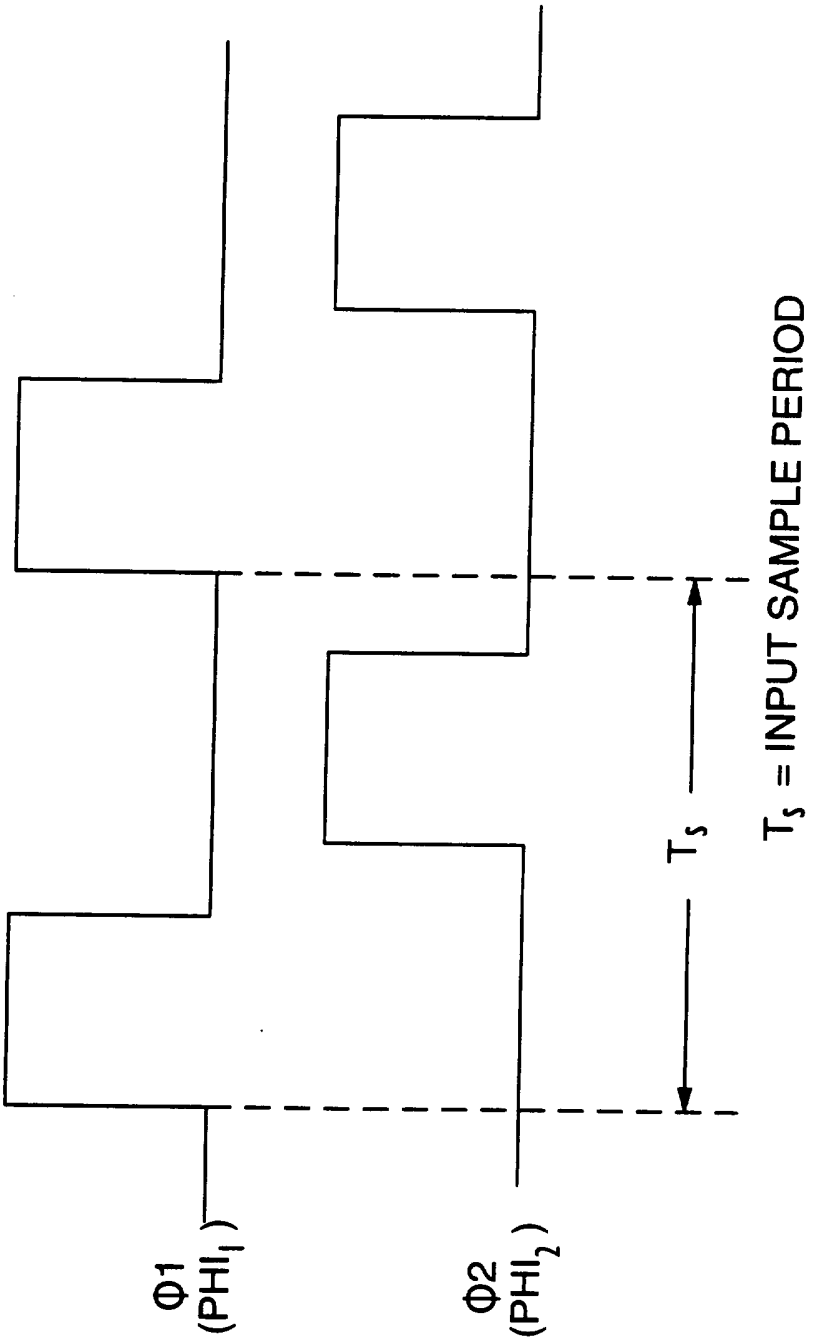


FIG. 9

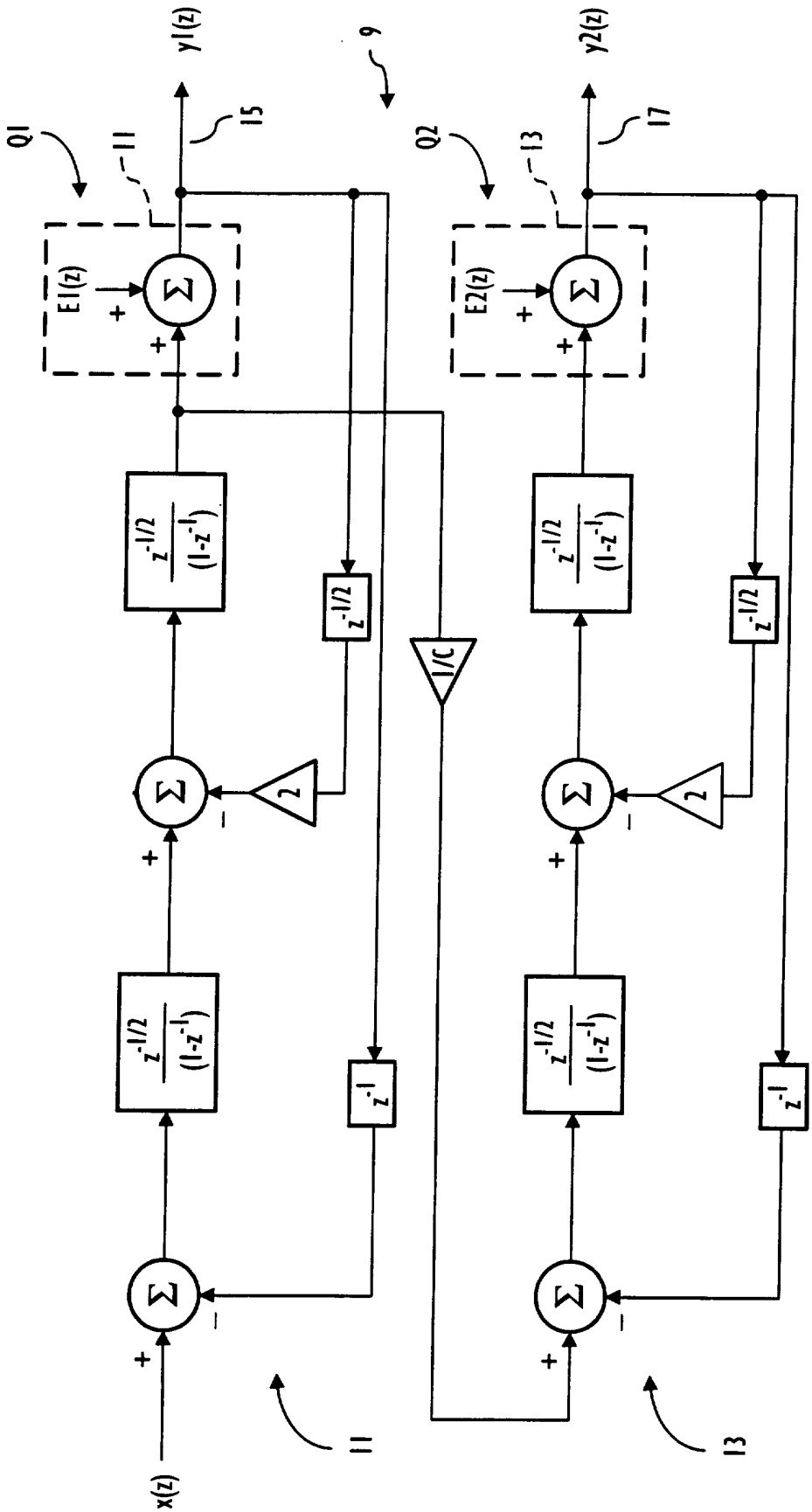


FIG. 10

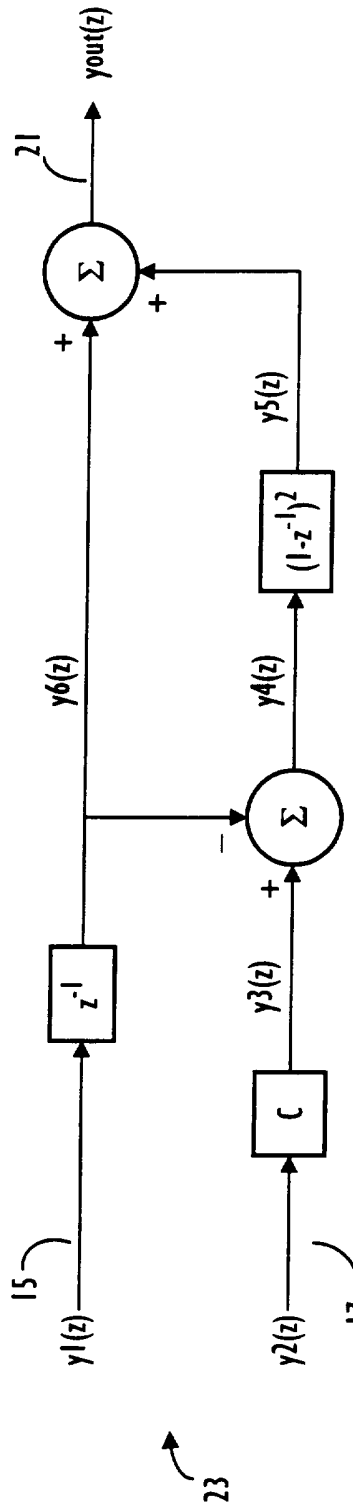


FIG 11

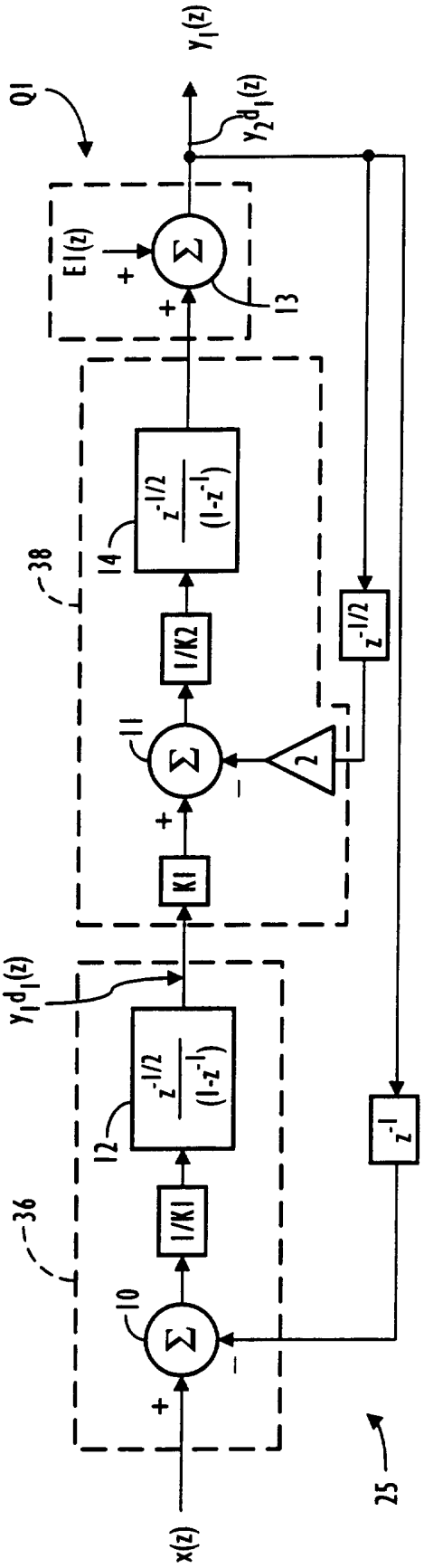

Q1
$Y_1(z)$
$Y_2d_1(z)$
E1(z)
13
14
12
11
10
38
36
25
1/K2
1/K1
K1
2
$z^{-1/2}$
z^{-1}
$\frac{z^{-1/2}}{(1-z^{-1})}$
$Y_1d_1(z)$
x(z)

FIG. 12

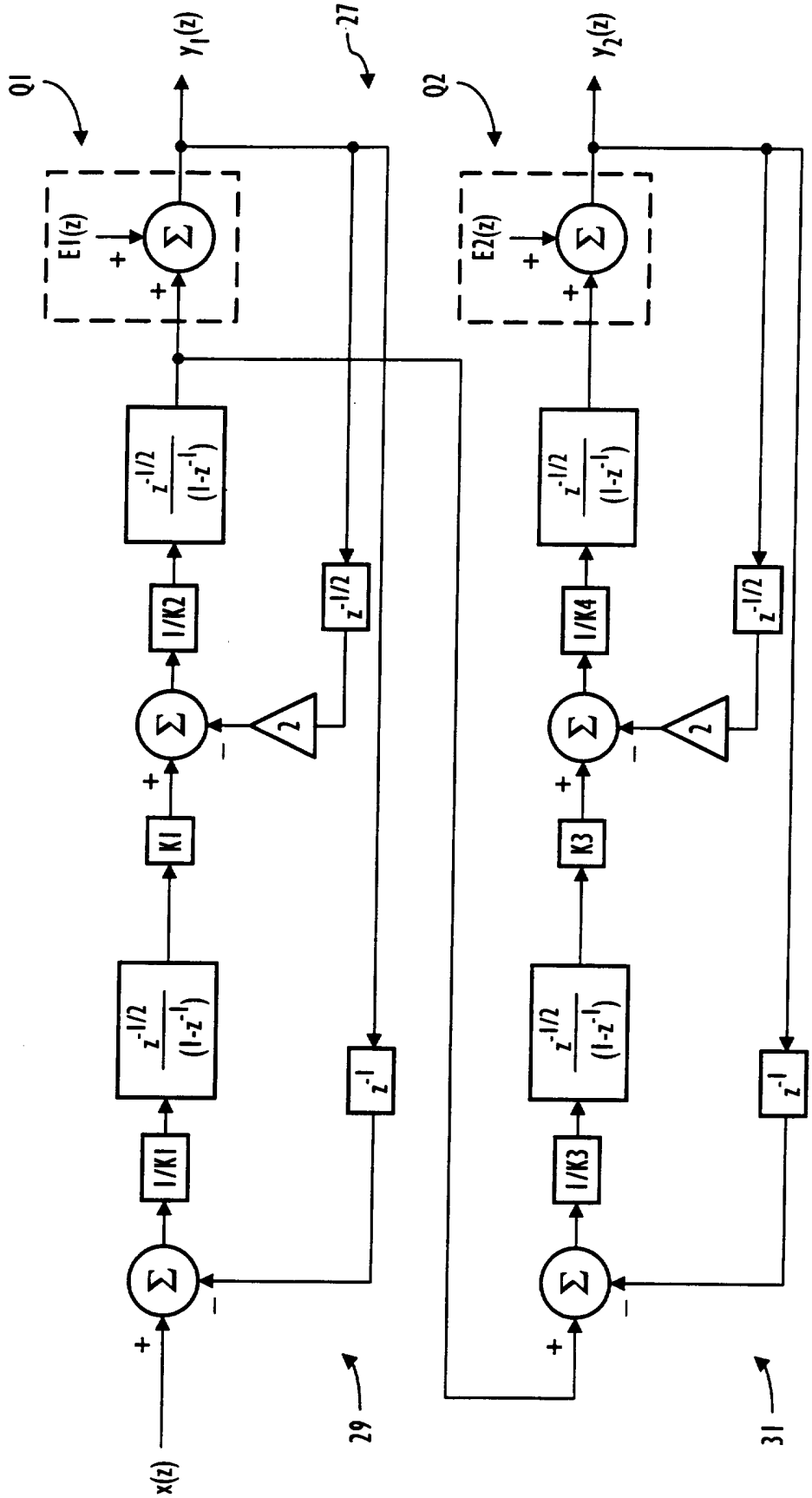

Q1
Q2
Y1(z)
Y2(z)
27
E1(z)
E2(z)
Σ
+
+
$\frac{z^{-1/2}}{(1-z^{-1})}$
1/K2
1/K4
$z^{-1/2}$
2
K1
K3
z^{-1}
1/K1
1/K3
x(z)
29
31

FIG. 13

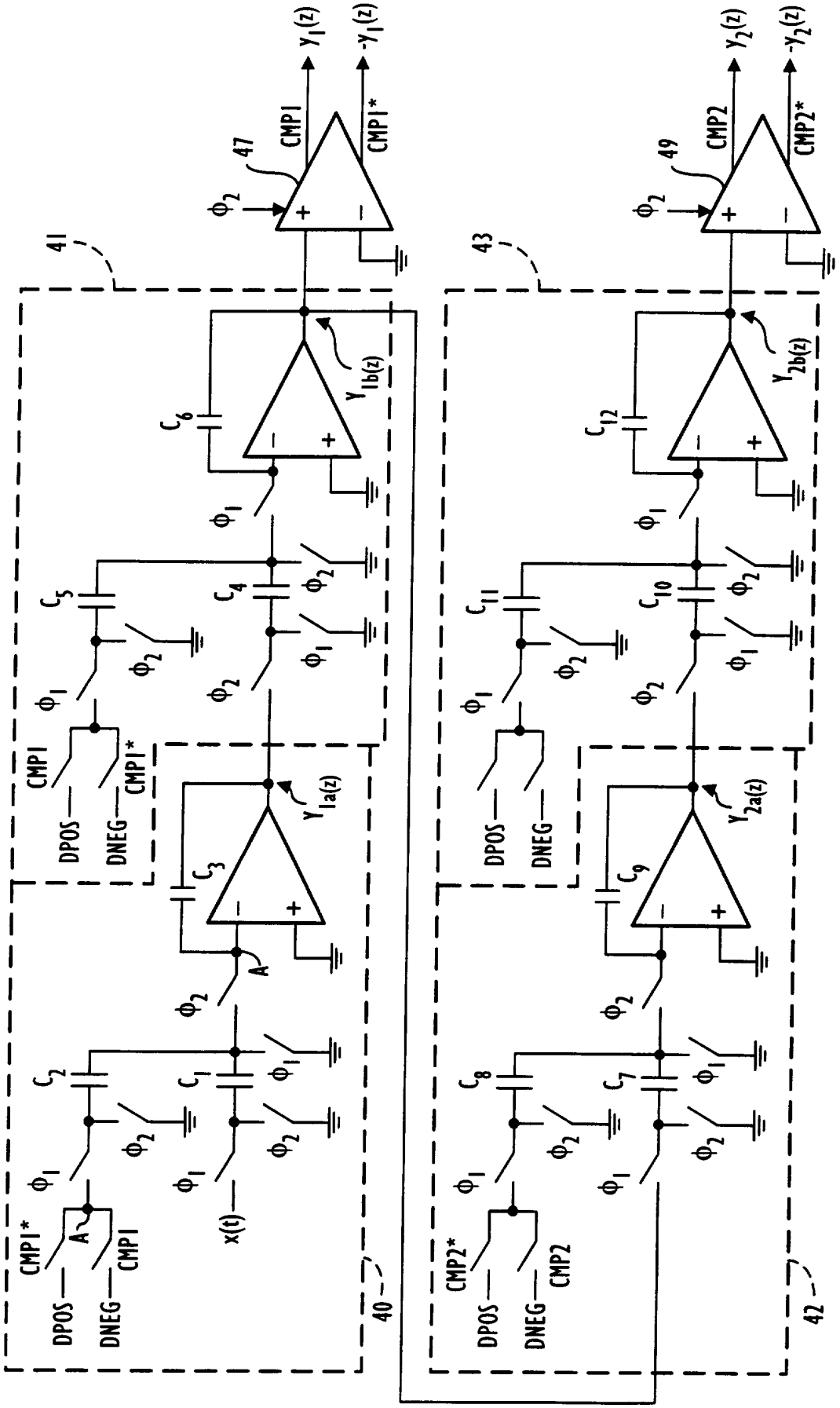

$y_1(z)$
$-y_1(z)$
CMP1
CMP1*
47
ϕ_2
41
$y_{1b(z)}$
C_6
ϕ_1
C_5
C_4
ϕ_2
CMP1
CMP1*
DPOS
DNEG
$y_{1a(z)}$
C_3
A
C_2
C_1
x(t)
CMP1*
CMP1
40
$y_2(z)$
$-y_2(z)$
CMP2
CMP2*
49
43
$y_{2b(z)}$
C_{12}
C_{11}
C_{10}
$y_{2a(z)}$
C_9
C_8
C_7
CMP2*
CMP2
42

FIG. 14

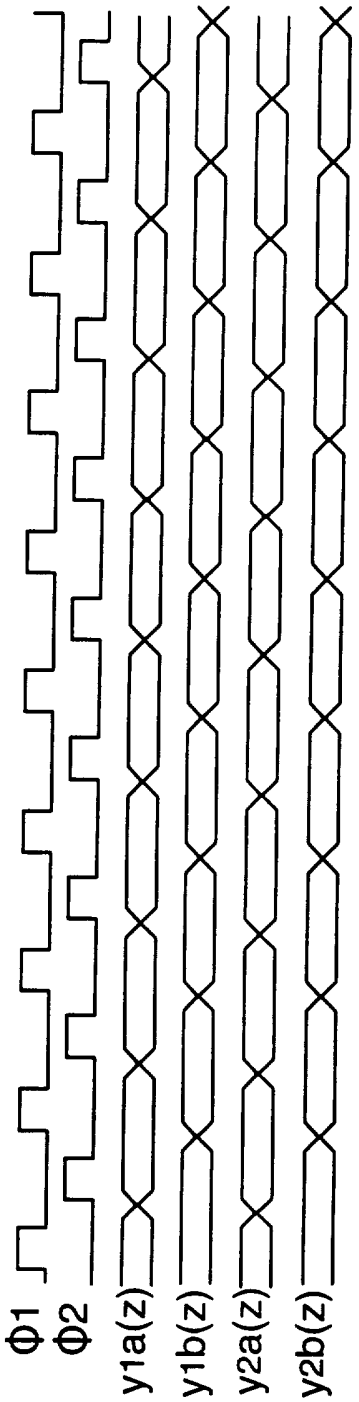


FIG. 15

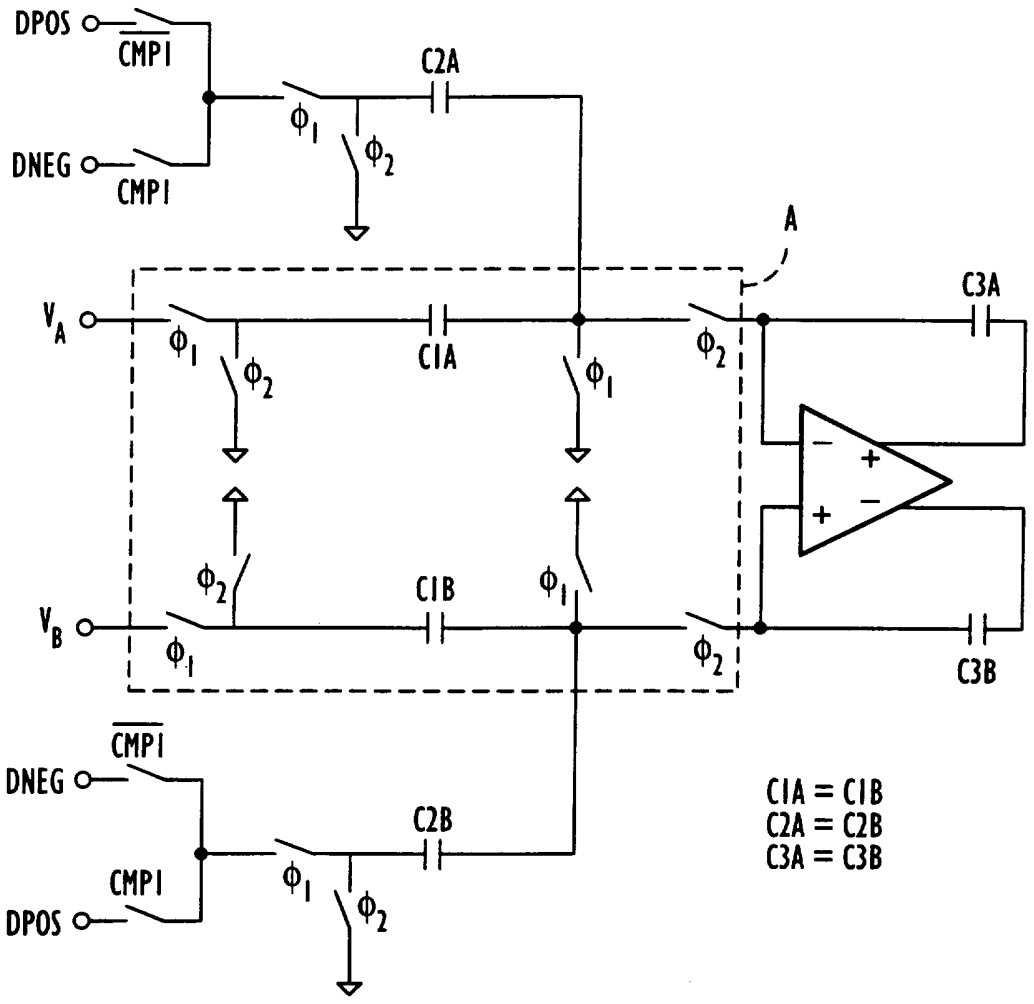

DPOS
CMPI
DNEG
CMPI
C2A
ϕ_1
ϕ_2
A
C3A
V_A
ϕ_1
ϕ_2
C1A
ϕ_1
ϕ_2
ϕ_2
C1B
ϕ_1
V_B
ϕ_1
ϕ_2
C3B
CMPI
DNEG
C2B
CMPI
DPOS
ϕ_1
ϕ_2
C1A = C1B
C2A = C2B
C3A = C3B

FIG. 16

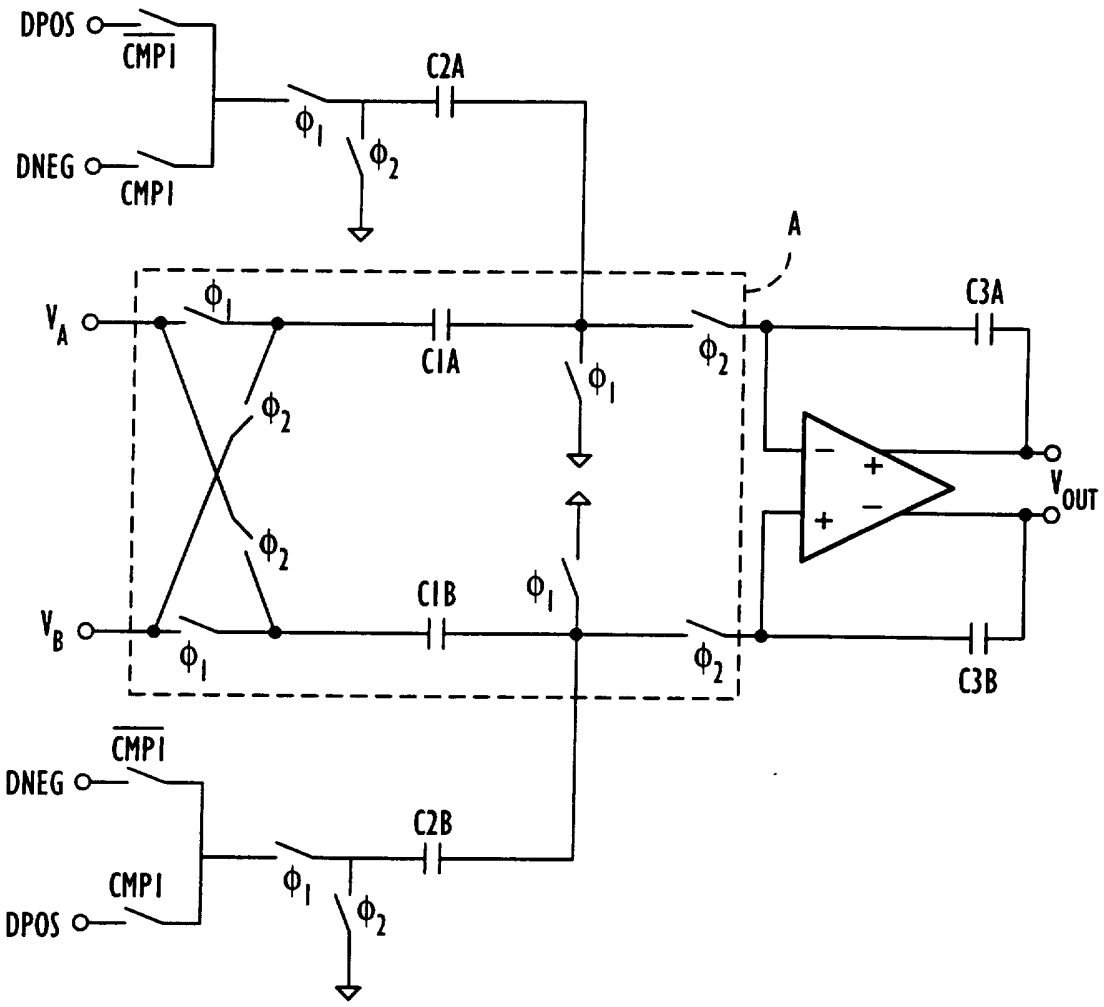

DPOS
CMPI
DNEG
CMPI
C2A
ϕ_1
ϕ_2
A
V_A
ϕ_1
C1A
ϕ_2
ϕ_1
C3A
ϕ_2
ϕ_2
V_{OUT}
ϕ_2
C1B
ϕ_1
V_B
ϕ_1
ϕ_2
C3B
CMPI
DNEG
C2B
CMPI
ϕ_1
ϕ_2
DPOS

FIG. 17

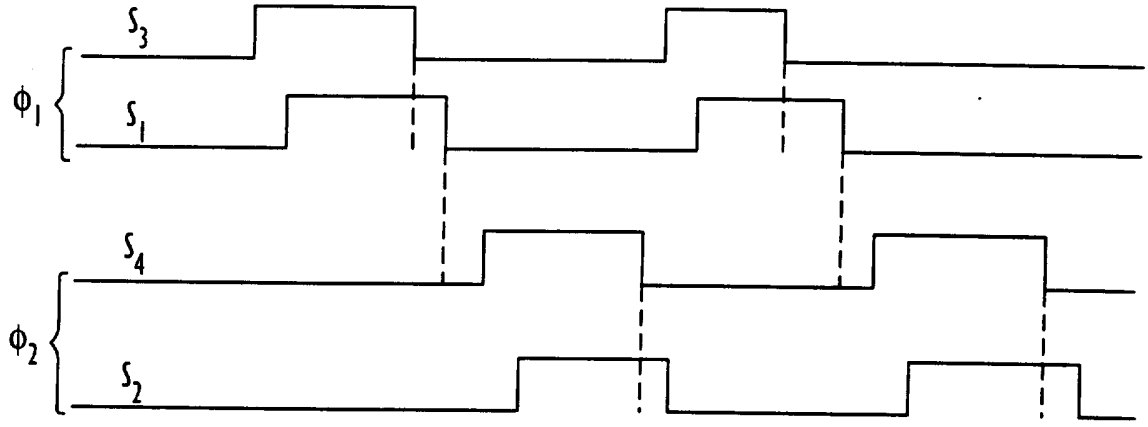


FIG. 18

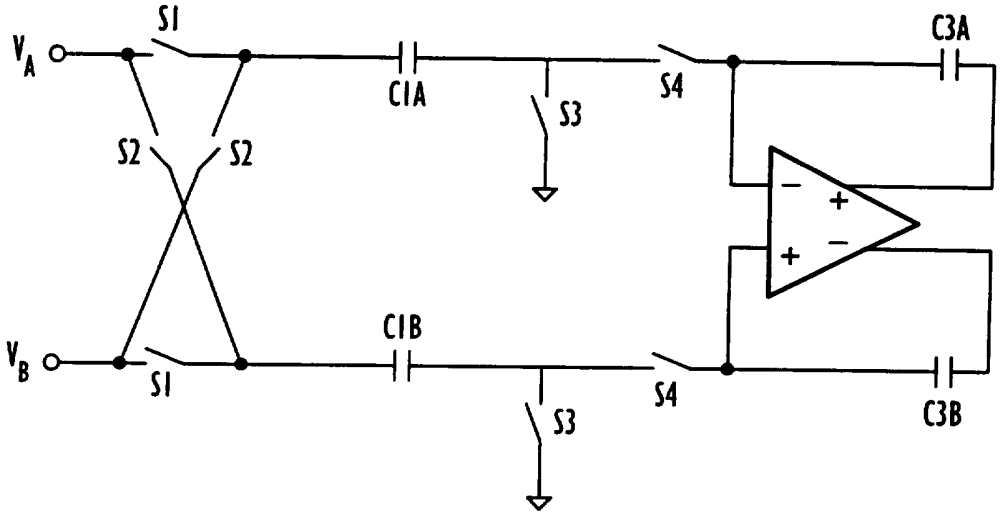


FIG. 19

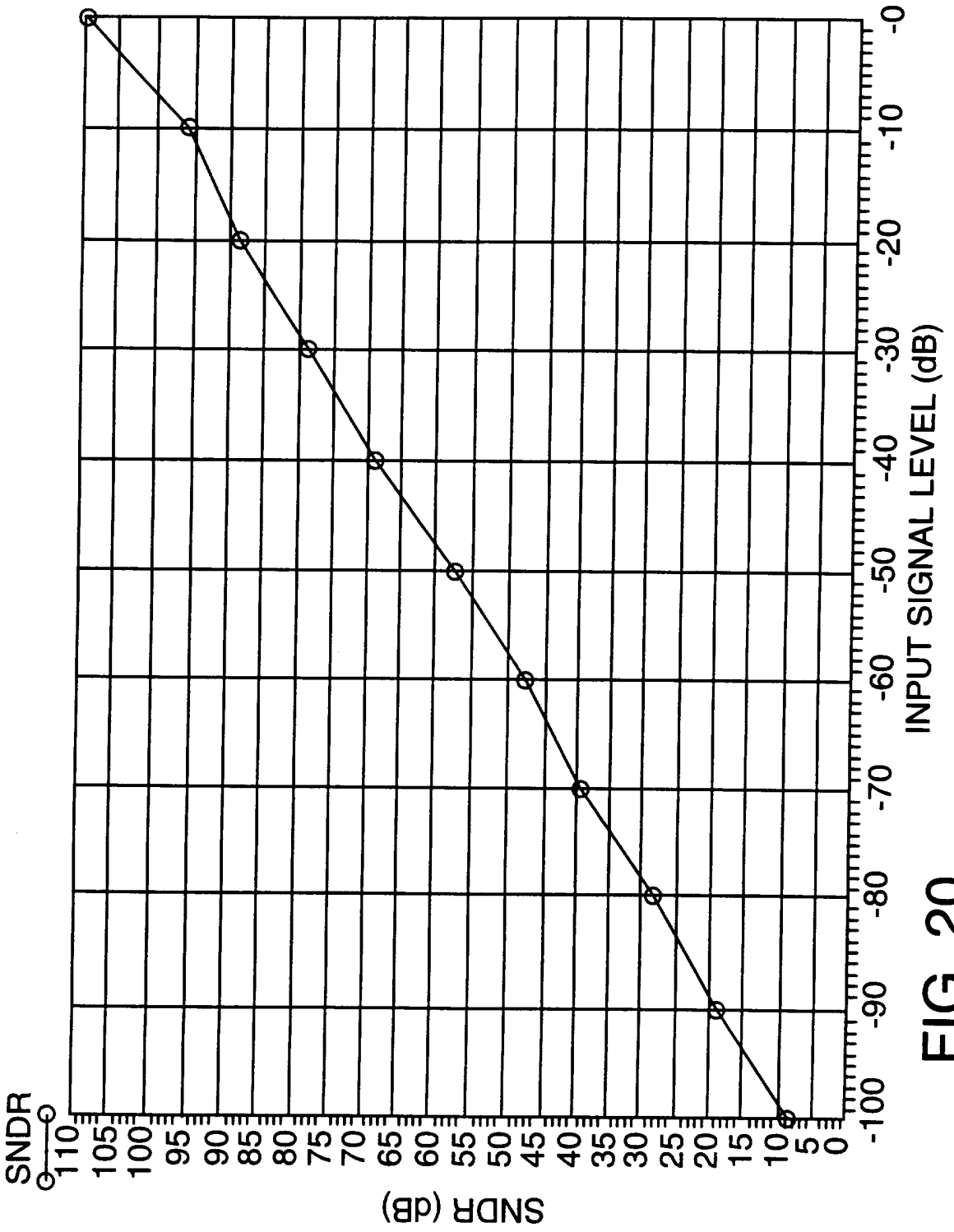

SNDR (dB)
SNDR
110
105
100
95
90
85
80
75
70
65
60
55
50
45
40
35
30
25
20
15
10
5
0
INPUT SIGNAL LEVEL (dB)
-0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100

FIG. 20

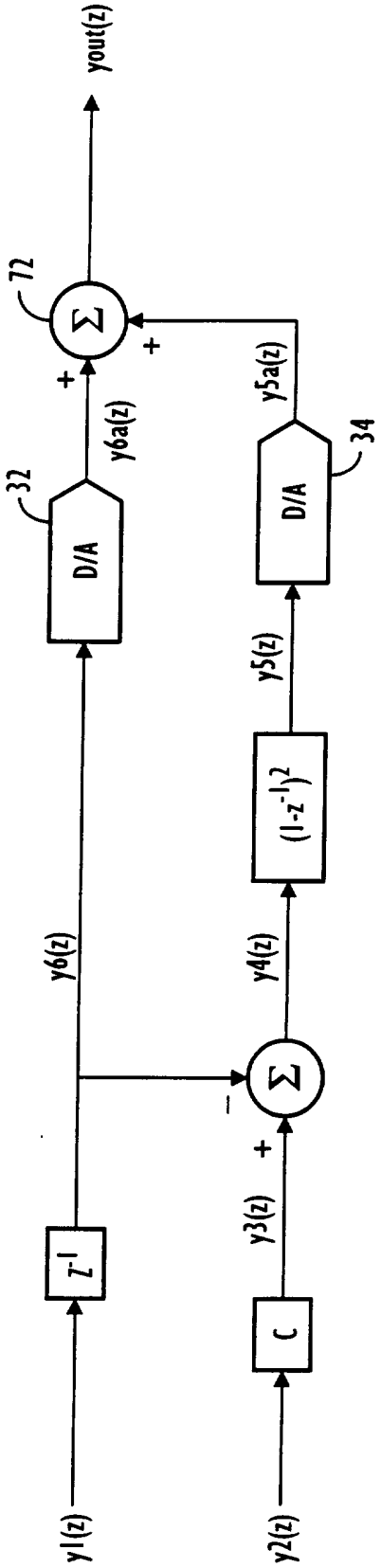

yout(z)
72
Σ
+
+
y6a(z)
y5a(z)
32
D/A
34
D/A
y5(z)
(1-z⁻¹)²
y6(z)
y4(z)
Σ
−
+
y3(z)
z⁻¹
C
y1(z)
y2(z)

FIG. 21

INTERNATIONAL SEARCH REPORT

Interna al Application No
PCT/US 95/14357

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03M3/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 25, no. 4, 1 August 1990 pages 979-986, XP 000149247 FRIEDMAN V ET AL 'THE IMPLEMENTATION OF DIGITAL ECHO CANCELLATION IN CODECS' cited in the application see page 983, right column, last paragraph - page 984, right column, paragraph 1; figures 8,9 ---	1-3
X	EP,A,0 104 988 (SENN PATRICE) 4 April 1984 see page 16, line 28 - page 22, line 16; figure 8	3-5
Y	--- -/--	6,9,25

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
29 March 1996	19. 04. 96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Blaas, D-L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Intern al Application No
PCT/US 95/14357

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 24, no. 2, 1 April 1989 pages 256-266, XP 000122348 NORSWORTHY S R ET AL 'A 14-BIT 80-KHZ SIGMA-DELTA A/D CONVERTER: MODELING, DESIGN AND PERFORMANCE EVALUATION' see figures 3,6	15
A		1,3

X	US,A,5 283 578 (RIBNER DAVID B ET AL) 1 February 1994 see column 6, line 19 - line 32; figure 4	19,21,24
Y		6,9,25
A		13,17,40

A	US,A,4 939 516 (EARLY ADRIAN B) 3 July 1990 see figure 2	11,13,15

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Internal Application No
PCT/US 95/14357

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0104988	04-04-84	FR-A-	2533382	23-03-84
		CA-A-	1224877	28-07-87
		US-A-	4588981	13-05-86
US-A-5283578	01-02-94	NONE		
US-A-4939516	03-07-90	NONE		