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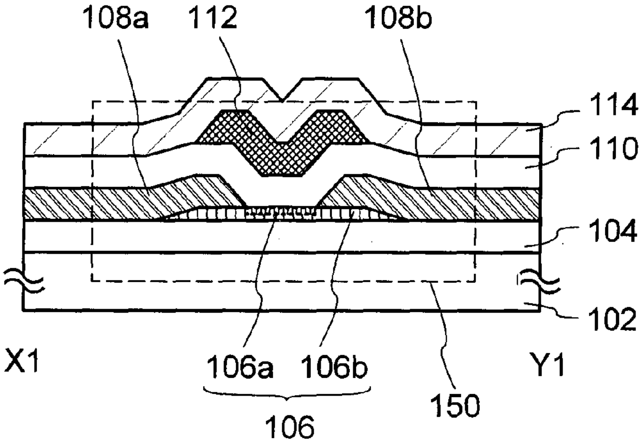
(54) **Title**: SEMICONDUCTOR DEVICE

FIG. 1B



(57) **Abstract**: The concentration of impurity elements included in an oxide semiconductor film in the vicinity of a gate insulating film is reduced. Further, crystallinity of the oxide semiconductor film in the vicinity of the gate insulating film is improved. A semiconductor device includes an oxide semiconductor film over a substrate, a source electrode and a drain electrode over the oxide semiconductor film, a gate insulating film which includes an oxide containing silicon and is formed over the oxide semiconductor film, and a gate electrode over the gate insulating film. The oxide semiconductor film includes a region in which the concentration of silicon is lower than or equal to 1.0 at.%, and at least the region includes a crystal portion.

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DESCRIPTION

SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device.

[0002]

In this specification, a semiconductor device generally means a device which can function by utilizing semiconductor characteristics, and an electrooptic device, a semiconductor circuit, and an electronic device are all semiconductor devices.

BACKGROUND ART

[0003]

A technique for forming transistors using a semiconductor thin film formed over a substrate having an insulating surface has attracted attention. The transistor is applied to a wide range of electronic devices such as an integrated circuit (IC) or an image display device (display device). As a semiconductor thin film applicable to the transistor, a silicon based semiconductor material is widely known for example; moreover, an oxide semiconductor has been attracting attention as another material.

[0004]

For example, a transistor whose active layer includes an amorphous oxide including indium (In), gallium (Ga), and zinc (Zn) is disclosed (see Patent Document 1).

[0005]

Transistors including oxide semiconductors have on-state characteristics (on-state current) superior to those of transistors including amorphous silicon. In order to apply the transistors including oxide semiconductors to high-performance devices, such transistors are required to have further improved characteristics, and thus techniques of crystallization of oxide semiconductors have been developed (see Patent Document 2). In Patent Document 2, a technique in which an oxide semiconductor is crystallized by heat treatment is disclosed.

[Reference]

[Patent Document]

[0006]

[Patent Document 1] Japanese Published Patent Application No. 2006-165528

[Patent Document 2] Japanese Published Patent Application No. 2008-311342

DISCLOSURE OF INVENTION

[0007]

In the case where a top-gate transistor including an oxide semiconductor film is formed, a gate insulating film is formed over the oxide semiconductor film. When the gate insulating film is formed, a constituent element of the gate insulating film may enter the oxide semiconductor film over which the gate insulating film is formed.

[0008]

For example, in the case where a silicon oxide (SiO_x, $x = 2$ or more) film is formed as a gate insulating film by a sputtering method after an oxide semiconductor film is formed, silicon that is a constituent element of the silicon oxide and a rare gas element such as argon used for sputtering are together implanted into the oxide semiconductor film. Such silicon breaks a bond between constituent elements of the oxide semiconductor film (an indium atom and an oxygen atom (In-O bond)) and is included as an impurity element in the oxide semiconductor film. The impurity element may be included at a high concentration particularly in the vicinity of the interface between the oxide semiconductor film and the gate insulating film. In the vicinity of the interface between the oxide semiconductor film and the gate insulating film, a channel formation region is formed; thus, when an impurity element such as silicon is included, the resistance of the oxide semiconductor film is increased. As a result, the on-state current which is one of electric characteristics of a transistor is decreased. As described above, the impurity element left in the oxide semiconductor film becomes a cause which affects electric characteristics of the transistor.

[0009]

Further, in the case where the oxide semiconductor film includes a crystal portion, by entry of the constituent element of the gate insulating film into the oxide semiconductor film, a bond in the crystal portion of the oxide semiconductor film is broken, and accordingly, amorphous regions are more formed in the oxide semiconductor film in the vicinity of the gate insulating film.

[0010]

In view of the above problems, an object is to reduce the concentration of an impurity element included in an oxide semiconductor film in the vicinity of a gate insulating film. Another object is to improve crystallinity of the oxide semiconductor film in the vicinity of the gate insulating film. Further, another object is to provide a semiconductor device with stable electric characteristics by using the oxide semiconductor film.

[0011]

One embodiment of the present invention to be disclosed is a semiconductor device including a base insulating film, an oxide semiconductor film formed over the base insulating film, a source electrode and a drain electrode formed over the oxide semiconductor film, a gate insulating film which includes an oxide containing silicon and is formed over the oxide semiconductor film, the source electrode and the drain electrode, and a gate electrode provided to be in contact with the gate insulating film and overlap with at least the oxide semiconductor film. The oxide semiconductor film includes a region in which a concentration of silicon distributed from an interface with the gate insulating film toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at.%, and at least the region includes a crystal portion.

[0012]

Another embodiment of the present invention to be disclosed is a semiconductor device including a base insulating film, an oxide semiconductor film formed over the base insulating film, a gate insulating film which includes an oxide containing silicon and is formed over the oxide semiconductor film, a gate electrode provided to be in contact with the gate insulating film and overlap with at least the oxide semiconductor film, an interlayer insulating film formed over the gate insulating film and the gate electrode, and a source electrode and a drain electrode provided over the interlayer insulating film to be electrically connected to at least the oxide semiconductor film. The oxide semiconductor film includes a region in which a concentration of silicon distributed from an interface with the gate insulating film toward an inside of the oxide semiconductor film is lower than or equal to 1.0 at.%, and at least the region includes a crystal portion.

[0013]

In each of the above structures, the region is preferably formed to be in contact with the gate insulating film and have a thickness less than or equal to 5 nm. In addition, the oxide semiconductor film other than the region preferably includes a crystal portion. In the crystal portion, c-axes are preferably aligned in a direction perpendicular to the interface between the base insulating film and the oxide semiconductor film.

[0014]

Further, in each of the above structures, the region preferably has a silicon concentration lower than or equal to 0.1 at.%. In addition, the region preferably has a carbon concentration lower than or equal to 1.0×10^{20} atoms/cm^3.

[0015]

When the oxide semiconductor film in the vicinity of the gate insulating film has the above silicon concentration or the above carbon concentration, an increase in resistance of the oxide semiconductor film can be suppressed and crystallinity of the oxide semiconductor film can be improved. As a result, a semiconductor device with stable electric characteristics can be provided.

[0016]

According to one embodiment of the present invention to be disclosed, the concentration of an impurity element included in the oxide semiconductor film in the vicinity of the gate insulating film can be decreased. In addition, crystallinity of the oxide semiconductor film in the vicinity of the gate insulating film can be improved. Further, a semiconductor device with stable electric characteristics can be provided.

BRIEF DESCRIPTION OF DRAWINGS

[0017]

FIGS. 1A and 1B are a plan view and a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 2A to 2D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 3A and 3B are a plan view and a cross-sectional view illustrating one embodiment of a semiconductor device.

FIGS. 4A to 4D are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 5A and 5B are cross-sectional views illustrating an example of a manufacturing process of a semiconductor device.

FIGS. 6A to 6C illustrate one embodiment of a semiconductor device.

FIGS. 7A and 7B illustrate one embodiment of a semiconductor device.

FIGS. 8A and 8B illustrate one embodiment of a semiconductor device.

FIG. 9 illustrates one embodiment of a semiconductor device.

FIG. 10 illustrates one embodiment of a semiconductor device.

FIG. 11 illustrates one embodiment of a semiconductor device.

FIGS. 12A and 12B are model diagrams used for calculation.

FIGS. 13A and 13B are model diagrams used for calculation.

FIG. 14 shows calculation results.

FIGS. 15A and 15B are model diagrams used for calculation.

FIG. 16 shows calculation results.

FIG. 17 shows measurement results according to Example of the present invention.

FIGS. 18A and 18B show measurement results according to Example of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0018]

Hereinafter, embodiments of the invention disclosed in this specification will be described with reference to the accompanying drawings. Note that the present invention is not limited to the following description and it will be readily appreciated by those skilled in the art that modes and details can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the invention should not be construed as being limited to the description in the following embodiments.

[0019]

Note that the position, the size, the range, or the like of each structure illustrated in drawings and the like is not accurately represented in some cases for easy understanding. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like as disclosed in the drawings and the like.

[0020]

In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components, and the terms do not limit the components numerically.

[0021]

Note that in this specification and the like, the term such as "over" or "below" does not necessarily mean that a component is placed "directly on" or "directly under" another component. For example, the expression "a gate electrode over a gate insulating layer" can mean the case where there is an additional component between the gate insulating layer and the gate electrode.

[0022]

In addition, in this specification and the like, the term such as "electrode" or "wiring" does not limit a function of a component. For example, an "electrode" is sometimes used as part of a "wiring", and vice versa. Furthermore, the term "electrode" or "wiring" can include the case where a plurality of "electrodes" or "wirings" are formed in an integrated manner.

[0023]

Functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of opposite polarity is used or when the direction of current flowing is changed in circuit operation, for example. Therefore, the terms "source" and "drain" can be replaced with each other in this specification and the like.

[0024]

Note that in this specification and the like, the term "electrically connected" includes the case where components are connected through an object having any electric function. There is no particular limitation on an object having any electric function as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an "object having any electric function" are a switching element such as a transistor, a resistor, an inductor, a capacitor, and an element with a variety of functions as well as an electrode and a wiring.

[0025]

(Embodiment 1)

In this embodiment, one embodiment of a semiconductor device and one embodiment of a method for manufacturing the semiconductor device will be described with reference to FIGS. 1A and 1B and FIGS. 2A to 2D.

[0026]

<Example of Structure of Semiconductor Device>

As an example of a semiconductor device, a top-gate transistor is illustrated in FIGS. 1A and 1B. FIG. 1A is a plan view and FIG. 1B is a cross-sectional view taken along dashed line X1-Y1 in FIG. 1A. Note that in FIG. 1A, some components of a transistor 150 (e.g., a gate insulating film 110) are omitted for simplicity.

[0027]

The transistor 150 illustrated in FIGS. 1A and 1B includes, over a substrate 102, a base insulating film 104, an oxide semiconductor film 106 which is formed over the base insulating film 104 and includes a region 106a and a region 106b, a source electrode 108a and a drain electrode 108b formed over the base insulating film 104 and the oxide semiconductor film 106, the gate insulating film 110 formed over the oxide semiconductor film 106 and the source electrode 108a and the drain electrode 108b, and a gate electrode 112 provided to be in contact with the gate insulating film 110 and overlap with at least the oxide semiconductor film 106. In addition, an interlayer insulating film 114 is formed over the transistor 150.

[0028]

The thickness of the oxide semiconductor film 106 is greater than 5 nm and less than or equal to 200 nm, preferably greater than or equal to 10 nm and less than or equal to 30 nm. Further, the oxide semiconductor film 106 preferably has a structure with crystallinity (e.g., a single crystal structure, a microcrystalline structure, or the like).

[0029]

As illustrated in FIG. 1B, an end portion of the oxide semiconductor film 106 is preferably tapered at an angle of 20° to 50°. When the oxide semiconductor film 106 has a perpendicular end portion, oxygen is more likely to be released from the end portion of the oxide semiconductor film 106, and accordingly, oxygen vacancies are likely to be generated. When the oxide semiconductor film 106 has a tapered end portion, generation of oxygen vacancies is suppressed, and thus generation of leakage current of the transistor 150 can be reduced.

[0030]

In this embodiment, the oxide semiconductor film 106 is preferably a c-axis aligned crystalline oxide semiconductor (CAAC-OS) film. Note that the CAAC-OS film will be described in detail later in a manufacturing method of the transistor 150.

[0031]

For the gate insulating film 110, an oxide containing silicon, which has a sufficient withstand voltage and sufficient insulating properties, is preferably used. In the case where the gate insulating film 110 has a single-layer structure, an insulating film such as a silicon oxide film may be used, for example.

[0032]

Alternatively, the gate insulating film 110 may have a stacked structure. In the case where the gate insulating film 110 has a stacked structure, an oxide containing silicon may be stacked over a gallium oxide, an aluminum oxide, a silicon nitride, a silicon oxynitride, an aluminum oxynitride, a yttrium oxide, a lanthanum oxide, a silicon nitride oxide, or the like. Alternatively, an oxide containing silicon may be stacked over a high-k material such as hafnium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0$, $y > 0$)), hafnium silicate to which nitrogen is added ($HfSiO_xN_y$ ($x > 0$, $y > 0$)), or hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)).

[0033]

In the case of using an oxide containing silicon as the gate insulating film 110, part of contained oxygen can be released from the insulating film when the insulating film is heated; thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled. In particular, the gate insulating film 110 preferably contains a large amount of oxygen which exceeds at least the stoichiometry thereof. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 110. When such a silicon oxide film is used as the gate insulating film 110, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 150 using the oxide semiconductor film 106 can have favorable transistor characteristics.

[0034]

However, in the case of using a silicon oxide film as the gate insulating film 110, silicon that is a constituent element of the gate insulating film 110 might be taken as an impurity into the oxide semiconductor film 106. Silicon or the like which is a constituent element of the gate insulating film 110 enters the oxide semiconductor film 106 and serves as an impurity, which affects characteristics of the transistor.

[0035]

Further, in the case where the oxide semiconductor film 106 is a CAAC-OS film, silicon or the like, which is a constituent element of the gate insulating film 110, enters the oxide semiconductor film 106, and a bond in the crystal portion in the oxide semiconductor film 106 is broken. Thus, amorphous regions are more formed in the oxide semiconductor film 106 in the vicinity of the gate insulating film 110.

[0036]

In particular, impurities such as silicon are likely to enter the oxide semiconductor film 106 in the vicinity of the gate insulating film 110. A channel formation region of the transistor 150 is formed in the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110; thus, when impurities such as silicon enter the vicinity of the interface between the oxide semiconductor film 106 and the gate insulating film 110, characteristics of the transistor 150 might be changed.

[0037]

Change in structure of the oxide semiconductor film 106 when SiO_2, oxide containing silicon, is added as an impurity was examined by classical molecular dynamics calculation. The results thereof are described with reference to FIGS. 12A and 12B, FIGS. 13A and 13B, and FIG. 14. Note that simulation software "SCIGRESS ME" manufactured by Fujitsu Limited was used for classical molecular dynamics calculation. An empirical potential which characterizes the interaction between atoms is defined in the classical molecular dynamics method, so that force that acts on each atom is estimated. Newton's equation of motion is numerically solved, whereby motion (time-dependent change) of each atom can be deterministically tracked.

[0038]

Hereinafter, calculation models and calculation conditions are described. Note that in this calculation, the Born-Mayer-Huggins potential was used.

[0039]

A single crystal structure of $InGaZnO_4$ including 1680 atoms (see FIG. 12A) and a structure of $InGaZnO_4$ including 1680 atoms in which 20 atoms of each of In, Ga, and Zn are substituted by silicon (Si) atoms (see FIG. 12B) were formed as calculation models. In the model of silicon (Si) substitution shown in FIG. 12B, silicon atoms are included at 3.57 at.% (2.34 wt.%). Further, the density of the model of the single crystal shown in FIG. 12A is 6.36 g/cm^3, and the density of the model of Si substitution shown in FIG. 12B is 6.08 g/cm^3.

[0040]

At 1727 °C which is lower than the melting point of the $InGaZnO_4$ single crystal (about 2000 °C according to estimation by the classical molecular dynamics calculation), structure relaxation was performed on the calculation models shown in FIGS. 12A and 12B by the classical molecular dynamics calculation at a fixed pressure (1 atom) for 150 psec (time step width 0.2 fsec × 750000 steps). The radial distribution functions g(r) of the two structures were calculated. Note that the radial distribution function g(r) is a function representing the probability density of atoms existing at a distance of *r* from one atom. As the correlation between atoms disappears, g(r) becomes closer to 1.

[0041]

FIGS. 13A and 13B show final structures obtained by performing the classical molecular dynamics calculation for 150 psec on the above two calculation models. In addition, FIG. 14 shows the radial distribution function g (r) in each structure.

[0042]

The model of single crystal shown in FIG. 13A is stable and keeps the crystal structure even in the final structure, whereas the model of Si substitution shown in FIG. 13B is unstable, and it can be observed that the crystal structure is distorted with time and changes into an amorphous structure. When the radial distribution functions g(r) of the structural models are compared with each other in FIG. 14, it is found that the single crystal model has peaks even at a long distance and has a long-range order. On the other hand, it is found that in the model of Si substitution, the peak disappears at a distance about 0.6 nm, and the model of Si substitution does not have the long-range order.

[0043]

The above calculation results indicate that when silicon (Si) is included in $InGaZnO_4$, $InGaZnO_4$ is likely to become amorphous. Further, according to the above results, even when $InGaZnO_4$ including silicon (Si) is heated at high temperature, such $InGaZnO_4$ is not crystallized.

[0044]

Next, change in structure of the oxide semiconductor film 106 when carbon atoms (C) are added was examined by classical molecular dynamics calculation. The results thereof are described with reference to FIG. 12A, FIGS. 15A and 15B, and FIG. 16. Note that simulation software "SCIGRESS ME" manufactured by Fujitsu Limited was used for classical molecular dynamics calculation.

[0045]

Calculation models and calculation conditions are as follows. Note that in this calculation, the Born-Mayer-Huggins potential was used. Further, for the interaction between carbon atoms (C), a Lennard-Jones potential was used.

[0046]

A single crystal structure of $InGaZnO_4$ including 1680 atoms (see FIG. 12A) and a structure of $InGaZnO_4$ including 1680 atoms in which 20 atoms of each of In, Ga, and Zn are substituted by carbon atoms (C) and 80 atoms of oxygen (O) are substituted by carbon atoms (C) (see FIG. 15A) were formed as calculation models. In the model of C substitution shown in FIG. 15A, carbon atoms (C) are included at 8.33 at.%. Further, the density of the model of the single crystal shown in FIG. 12A is 6.36 g/cm^3, and the density of the model of C substitution shown in FIG. 15A is 5.89 g/cm^3.

[0047]

At 1727 °C which is lower than the melting point of the $InGaZnO_4$ single crystal (about 2000 °C according to estimation by the classical molecular dynamics calculation), structure relaxation was performed on the calculation models shown in FIG.

12A and FIG. 15A by the classical molecular dynamics calculation at a fixed pressure (1 atom) for 150 psec (time step width 0.2 fsec × 750000 steps). The radial distribution functions g(r) of the two structures were calculated. Note that the radial distribution function g(r) is a function representing the probability density of atoms existing at a distance of *r* from one atom. As the correlation between atoms disappears, g(r) becomes closer to 1.

[0048]

FIG. 13A and FIG. 15B show final structures obtained by performing the classical molecular dynamics calculation for 150 psec on the above two calculation models. The radial distribution function g(r) in each structure is shown in FIG. 16.

[0049]

The model of single crystal shown in FIG. 13A is stable and keeps the crystal structure even in the final structure, whereas the model of C substitution shown in FIG. 15B is unstable, and it can be observed that the crystal structure is distorted with time and changes into an amorphous structure. As seen in FIG. 16, by comparing the radial distribution functions g(r) of the structural models with each other, it is found that the model of single crystal has peaks even at a long distance and the long-range order. On the other hand, it is found that in the model of C substitution, the peak disappears at a distance about 0.7 nm, and the model of C substitution does not have the long-range order.

[0050]

The above calculation results indicate that when carbon (C) is included in $InGaZnO_4$, $InGaZnO_4$ is likely to become amorphous. In addition, according to the above results, even when $InGaZnO_4$ including carbon (C) is heated at high temperature, such $InGaZnO_4$ is not crystallized.

[0051]

Thus, in the semiconductor device described in this embodiment, entry of impurities such as silicon into the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110 is suppressed. As a result, in the oxide semiconductor film 106, a region in which the concentration of silicon distributed from an interface with the gate insulating film 110 toward an inside of the oxide semiconductor film 106 is lower than or equal to 1.0 at.% is formed. Such a region is referred to as a region 106a as illustrated in FIG. 1B. The concentration of silicon included in the region 106a is further preferably lower than or equal to 0.1 at.%. Further, the region 106a is provided to be in contact with the gate insulating film 110 and have a thickness less than or equal to 5 nm.

[0052]

Note that as shown in FIG. 1B, a region in the oxide semiconductor film 106 other than the region 106a is referred to as a region 106b.

[0053]

Further, in the case where impurities such as carbon is included in the gate insulating film 110, such impurities might also enter the oxide semiconductor film 106 and serve as impurities, as in the case of silicon. In that case, the concentration of carbon included in the region 106a is lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0054]

In order to prevent impurities such as silicon from entering the oxide semiconductor film 106, the gate insulating film may be formed in such a manner as not to damage the oxide semiconductor film 106. For example, in the case where a silicon oxide film is formed as the gate insulating film 110 by a sputtering method, the impact caused by silicon (that is a constituent element of the gate insulating film 110) colliding with the oxide semiconductor film 106 may be reduced. For achieving the above, specifically, a method in which the power for deposition of the gate insulating film 110 is low, a method in which the pressure for deposition of the gate insulating film 110 is high, a method in which a distance between a target and a substrate (T-S distance) is increased in deposition of the gate insulating film 110, or the like can be used. However, a formation method of the gate insulating film 110 is not limited to the above. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or the like, which is formed by a PE-CVD method, can be used. A PE-CVD method is preferred to a sputtering method because with use of the PE-CVD method, the oxide semiconductor film 106 serving as a base film is less damaged.

[0055]

As described above, the concentration of impurities such as silicon and carbon entering the region 106a in the oxide semiconductor film 106 is reduced, whereby change in characteristics of the transistor 150 can be suppressed. Further, in the case where the oxide semiconductor film 106 is a CAAC-OS film, a crystal portion can be formed even in the vicinity with the gate insulating film 110. When the transistor 150 is formed using such an oxide semiconductor film 106, a semiconductor device with stable electric characteristics can be provided.

[0056]

Note that the details of the other components of the transistor are described with reference to FIGS. 2A to 2D, in description of a method for manufacturing the transistor 150 below.

[0057]

<Manufacturing Method of Transistor 150>

Hereinafter, an example of a method for manufacturing the transistor 150 illustrated in FIGS. 1A and 1B of this embodiment is described with reference to FIGS. 2A to 2D.

[0058]

First, the substrate 102 is prepared. Although there is no particular limitation on a substrate that can be used as the substrate 102, it is necessary that the substrate have heat resistance to withstand at least a heat treatment performed later. For example, a glass substrate such as a barium borosilicate glass substrate or an aluminoborosilicate glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like can be used. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon or silicon carbide, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like can be used.

[0059]

A flexible substrate may be used as the substrate 102. In the case of using a flexible substrate, a transistor including the oxide semiconductor film 106 may be directly formed over the flexible substrate. Alternatively, a transistor including the oxide semiconductor film 106 may be formed over another substrate, and then, the transistor may be separated and transferred to a flexible substrate. For separation of the transistor from the substrate and transfer to the flexible substrate, a separation layer may be provided between the substrate and the transistor including the oxide semiconductor film 106.

[0060]

Next, the base insulating film 104 is formed over the substrate 102 (see FIG. 2A). The base insulating film 104 has an effect to prevent diffusion of an impurity element such as hydrogen or moisture from the substrate 102, and can be formed with a single-layer structure or a stacked structure using one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0061]

Further, as another effect of the base insulating film 104, oxygen can be supplied to the oxide semiconductor film 106 formed later. For example, in the case where an insulating film including oxide is formed as the base insulating film 104, by heating the base insulating film 104, part of contained oxygen can be released. Thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled accordingly. In particular, the base insulating film 104 preferably contains a large amount of oxygen which exceeds at least the stoichiometry thereof. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the base insulating film 104. When such a silicon oxide film is used as the base insulating film 104, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 150 using the oxide semiconductor film 106 can have favorable transistor characteristics.

[0062]

Before the base insulating film 104 is formed, plasma treatment or the like may be performed on the substrate 102. As plasma treatment, reverse sputtering in which an argon gas is introduced and plasma is generated can be performed. The reverse sputtering refers to a method in which an RF power source is used for application of a voltage to the substrate 102 side in an argon atmosphere so that plasma is generated in the vicinity of the substrate 102 to modify a surface of the substrate. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used. The reverse sputtering can remove particle substances (also referred to as particles or dust) attached to the surface of the substrate

102.

[0063]

Next, the oxide semiconductor film 106 is formed over the base insulating film 104 (see FIG. 2A). The oxide semiconductor film 106 is preferably a CAAC-OS film. Note that the base insulating film 104 and the oxide semiconductor film 106 are preferably formed successively without being exposed to the air.

[0064]

The CAAC-OS film that can be used for the oxide semiconductor film 106 is described in detail below.

[0065]

The CAAC-OS film is not completely single crystal or completely amorphous. The CAAC-OS film is an oxide semiconductor film with a crystal-amorphous mixed phase structure where crystal portions are included in an amorphous phase. Note that in most cases, the crystal portion fits inside a cube whose one side is less than 100 nm. From an observation image obtained with a transmission electron microscope (TEM), a boundary between an amorphous portion and a crystal portion in the CAAC-OS film is not clear. Further, with the TEM, a grain boundary in the CAAC-OS film is not found. Thus, in the CAAC-OS film, a reduction in electron mobility due to the grain boundary is suppressed.

[0066]

In each of the crystal portions included in the CAAC-OS film, a c-axis is aligned in a direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, triangular or hexagonal atomic arrangement which is seen from the direction perpendicular to the a-b plane is formed, and metal atoms are arranged in a layered manner or metal atoms and oxygen atoms are arranged in a layered manner when seen from the direction perpendicular to the c-axis. Note that, among crystal portions, the directions of an a-axis and a b-axis of one crystal portion may be different from those of another crystal portion. In this specification and the like, a simple term "perpendicular" includes a range from 85° to 95°. In addition, a simple term "parallel" includes a range from −5° to 5°.

[0067]

In the CAAC-OS film, distribution of crystal portions is not necessarily uniform. For example, in the formation process of the CAAC-OS film, in the case where crystal growth occurs from a surface side of the oxide semiconductor film, the proportion of crystal portions in the vicinity of the surface of the oxide semiconductor film is higher than that in a vicinity of a surface where the oxide semiconductor film is formed in some cases.

[0068]

Since the c-axes of the crystal portions included in the CAAC-OS film are aligned in the direction parallel to a normal vector of a surface where the CAAC-OS film is formed or a normal vector of a surface of the CAAC-OS film, the directions of the c-axes may be different from each other depending on the shape of the CAAC-OS film (the cross-sectional shape of the surface where the CAAC-OS film is formed or the cross-sectional shape of the surface of the CAAC-OS film). Note that when the CAAC-OS film is formed, the direction of c-axis of the crystal portion is the direction parallel to a normal vector of the surface where the CAAC-OS film is formed or a normal vector of the surface of the CAAC-OS film. The crystal portion is formed by film formation or by performing treatment for crystallization such as heat treatment after film formation.

[0069]

With use of the CAAC-OS film in a transistor, change in electric characteristics of the transistor due to irradiation with visible light or ultraviolet light can be reduced. Change and variation in threshold voltages can be suppressed. Thus, the transistor has high reliability.

[0070]

In an oxide semiconductor having crystallinity (crystalline oxide semiconductor), defects in the bulk can be further reduced. Further, when planarity of the surface of the crystalline oxide semiconductor film is enhanced, a top-gate transistor including such an oxide semiconductor can obtain higher field-effect mobility than a transistor including an amorphous oxide semiconductor. In order to enhance the surface planarity of the oxide semiconductor film, the oxide semiconductor is preferably formed over a flat surface. Specifically, the oxide semiconductor is preferably formed over a surface with an average surface roughness (R_a) less than or equal to 0.15 nm, preferably less than or equal to 0.1 nm.

[0071]

Note that the average surface roughness (R_a) is obtained by expanding, into three dimensions, arithmetic mean surface roughness so as to be able to apply it to a curved surface. R_a can be expressed as an "average value of the absolute values of deviations from a reference surface to a specific surface" and is defined by the following formula.

[0072]

[FORMULA 1]

$$Ra = \frac{1}{S_0} \int_{y_1}^{y_2} \int_{x_1}^{x_2} \left| f(x, y) - Z_0 \right| dxdy$$

[0073]

Here, the specific surface is a surface that is a target of roughness measurement, and is a quadrilateral region specified by four points represented by the coordinates (x_1, y_1, $f(x_1, y_1)$), (x_1, y_2, $f(x_1, y_2)$), (x_2, y_1, $f(x_2, y_1)$), and (x_2, y_2, $f(x_2, y_2)$). Moreover, S_0 represents the area of a rectangle which is obtained by projecting the specific surface on the xy plane, and Z_0 represents the height of the reference surface (the average height of the specific surface). R_a can be measured using an atomic force microscope (AFM).

[0074]

An oxide semiconductor used for the oxide semiconductor film 106 preferably contains at least indium (In) or zinc (Zn). In particular, In and Zn are preferably contained. As a stabilizer for reducing variation in electric characteristics of a transistor using the oxide semiconductor film, gallium (Ga) is preferably additionally contained. Tin (Sn) is preferably contained as a stabilizer. In addition, as a stabilizer, one or more selected from hafnium (Hf), zirconium (Zr), titanium (Ti), scandium (Sc), yttrium (Y), and an lanthanoid element (such as cerium (Ce), neodymium (Nd), or gadolinium (Gd), for example) is preferably contained.

[0075]

As the oxide semiconductor, for example, any of the following can be used: indium oxide, tin oxide, zinc oxide, an In-Zn-based oxide, a Sn-Zn-based oxide, an Al-Zn-based oxide, a Zn-Mg-based oxide, a Sn-Mg-based oxide, an In-Mg-based oxide, an In-Ga-based oxide, an In-Ga-Zn-based oxide (also referred to as IGZO), an In-Al-Zn-based oxide, an In-Sn-Zn-based oxide, a Sn-Ga-Zn-based oxide, an Al-Ga-Zn-based oxide, a Sn-Al-Zn-based oxide, an In-Hf-Zn-based oxide, an In-Zr-Zn-based oxide, an In-Ti-Zn-based oxide, an In-Sc-Zn-based oxide, an In-Y-Zn-based oxide, an In-La-Zn-based oxide, an In-Ce-Zn-based oxide, an In-Pr-Zn-based oxide, an In-Nd-Zn-based oxide, an In-Sm-Zn-based oxide, an In-Eu-Zn-based oxide, an In-Gd-Zn-based oxide, an In-Tb-Zn-based oxide, an In-Dy-Zn-based oxide, an In-Ho-Zn-based oxide, an In-Er-Zn-based oxide, an In-Tm-Zn-based oxide, an In-Yb-Zn-based oxide, an In-Lu-Zn-based oxide, an In-Sn-Ga-Zn-based oxide, an In-Hf-Ga-Zn-based oxide, an In-Al-Ga-Zn-based oxide, an In-Sn-Al-Zn-based oxide, an In-Sn-Hf-Zn-based oxide, or an In-Hf-Al-Zn-based oxide.

[0076]

Here, an "In-Ga-Zn-based oxide" means an oxide containing In, Ga, and Zn as its main components and there is no particular limitation on the ratio of In: Ga: Zn. The In-Ga-Zn-based oxide may contain a metal element other than the In, Ga, and Zn.

[0077]

Alternatively, a material represented by $InMO_3(ZnO)_m$ ($m > 0$ is satisfied, and m is not an integer) may be used as an oxide semiconductor. Note that M represents one or more metal elements selected from Ga, Fe, Mn, and Co, or the above-described element as a stabilizer. Alternatively, as the oxide semiconductor, a material expressed by a chemical formula, $In_2SnO_5(ZnO)_n$ ($n > 0$, n is a natural number) may be used.

[0078]

For example, an In-Ga-Zn-based oxide with an atomic ratio where In: Ga: Zn = 1:1:1, In: Ga: Zn = 3:1:2, or In: Ga: Zn = 2:1:3, or any of oxides whose composition is in the neighborhood of the above compositions can be used.

[0079]

In a formation step of the oxide semiconductor film 106, it is preferable that hydrogen or water be contained in the oxide semiconductor film 106 as little as possible. For example, it is preferable that the substrate 102 on which the base insulating film 104 is already formed be preheated in a preheating chamber of a sputtering apparatus as pretreatment for formation of the oxide semiconductor film 106 so that impurities such as hydrogen and moisture adsorbed to the substrate 102 and the base insulating film 104 are removed and evacuated. Then, the oxide semiconductor film 106 is preferably formed in a deposition chamber from which remaining moisture is removed.

[0080]

In order to remove the moisture in the preheating chamber and the deposition chamber, an entrapment vacuum pump, for example, a cryopump, an ion pump, or a titanium sublimation pump is preferably used. Further, an evacuation unit may be a turbo pump provided with a cold trap. From the preheating chamber and the deposition chamber which is evacuated with a cryopump, a hydrogen atom, a compound containing a hydrogen atom such as water (H_2O) (more preferably, also a compound containing a carbon atom), and the like are removed, whereby the concentration of impurities such as hydrogen or moisture in the oxide semiconductor film 106 that is to be formed can be reduced.

[0081]

Note that in this embodiment, an In-Ga-Zn-based oxide is deposited as the oxide semiconductor film 106 by a sputtering method. The oxide semiconductor film 106 can be formed by a sputtering method in a rare gas (typically argon) atmosphere, an oxygen atmosphere, or a mixed atmosphere of a rare gas and oxygen.

[0082]

As a target used for forming an In-Ga-Zn-based oxide film as the oxide semiconductor film 106 by a sputtering method, for example, a metal oxide target with an atomic ratio where In: Ga: Zn =1:1:1, a metal oxide target with an atomic ratio where In: Ga: Zn =3:1:2, or a metal oxide target with an atomic ratio where In: Ga: Zn =2:1:3 can be used. However, a material and composition of a target used for formation of the oxide semiconductor film 106 is not limited to the above.

[0083]

Further, when the oxide semiconductor film 106 is formed using the above metal oxide target, the composition of the target is different from the composition of a film formed over the substrate in some cases. For example, when the metal oxide target having a molar ratio where In_2O_3: Ga_2O_3: ZnO = 1:1:1 is used, the composition ratio of the thin oxide semiconductor film 106 becomes In_2O_3: Ga_2O_3: ZnO = 1:1:0.6 to 1:1:0.8 [molar ratio] in some cases, though it depends on the film formation conditions. This is because in formation of the oxide semiconductor film 106, ZnO is sublimed, or because a sputtering rate differs between the components of In_2O_3, Ga_2O_3, and ZnO.

[0084]

Accordingly, when a thin film having a preferable composition ratio is formed, a composition ratio of the metal oxide target needs to be adjusted in advance. For example, in order to make the composition ratio of the thin oxide semiconductor film 106 be In_2O_3: Ga_2O_3: ZnO = 1:1:1 [molar ratio], the composition ratio of the metal oxide target is made to be In_2O_3: Ga_2O_3: ZnO = 1:1:1.5 [molar ratio]. In other words, the ZnO content of the metal oxide target is made higher in advance. The composition ratio of the target is not limited to the above value, and can be adjusted as appropriate depending on the film formation conditions or the composition of the thin film to be formed. Further, it is preferable to increase the ZnO content of the metal oxide target because in that case, the crystallinity of the obtained thin film is improved.

[0085]

The relative density of the metal oxide target is 90 % to 100 % inclusive, preferably, 95 % to 99.9 % inclusive. By using the metal oxide target with high relative density, a dense oxide semiconductor film 106 can be formed.

[0086]

As a sputtering gas used for forming the oxide semiconductor film 106, it is preferable to use a high-purity gas from which an impurity such as hydrogen, water, a hydroxyl group, or a hydride is removed.

[0087]

There are three methods for forming a CAAC-OS film when the CAAC-OS film is used as the oxide semiconductor film 106. One of the methods (first method) is to form an oxide semiconductor film at a temperature higher than or equal to 100 °C and lower than or equal to 450 °C to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction parallel to a normal vector of a surface where the oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film. Another method (second method) is to form an oxide semiconductor film with a small thickness and then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction parallel to a normal vector of a surface where the oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film. The other method (third method) is to form a first oxide semiconductor film with a small thickness, then heat it at a temperature higher than or equal to 200 °C and lower than or equal to 700 °C, and form a second oxide semiconductor film, to form, in the oxide semiconductor film, crystal portions in which the c-axes are aligned in the direction parallel to a normal vector of a surface where the oxide semiconductor film is formed or a normal vector of a surface of the oxide semiconductor film.

[0088]

For example, the CAAC-OS film is formed by a sputtering method with a polycrystalline oxide semiconductor sputtering target. When ions collide with the sputtering target, a crystal region included in the sputtering target may be separated from the target along an a-b plane; in other words, a sputtered particle having a plane parallel to an a-b plane (flat-plate-like sputtered particle or pellet-like sputtered particle) may flake off from the sputtering target. In that case, the flat-plate-like sputtered particle reaches a substrate while maintaining their crystal state, whereby the CAAC-OS film can be formed.

[0089]

For formation of the CAAC-OS film, the following conditions are preferably used.

[0090]

By reducing the amount of impurities entering the CAAC-OS film during the deposition, the crystal state can be prevented from being broken by the impurities. For example, the concentration of impurities (e.g., hydrogen, water, carbon dioxide, or nitrogen) which exist in the deposition chamber may be reduced. Furthermore, the concentration of impurities in a deposition gas may be reduced. Specifically, a deposition gas whose dew point is −80 °C or lower, preferably −100 °C or lower is used.

[0091]

By increasing the substrate heating temperature during the deposition, migration of a sputtered particle is likely to occur after the sputtered particle reaches a substrate surface. Specifically, the substrate heating temperature during the deposition is higher than or equal to 100 °C and lower than or equal to 740 °C, preferably higher than or equal to 150 °C and lower than or equal to 500 °C. By increasing the substrate heating temperature during the deposition, when the flat-plate-like sputtered particle reaches the substrate, migration occurs on the substrate surface, so that a flat plane of the flat-plate-like sputtered particle is attached to the substrate.

[0092]

Furthermore, it is preferable that the proportion of oxygen in the deposition gas be increased and the power be optimized in order to reduce plasma damage at the deposition. The proportion of oxygen in the deposition gas is 30 vol.% or higher, preferably 100 vol.%.

[0093]

Note that when a crystalline (single-crystal or microcrystalline) oxide semiconductor film other than a CAAC-OS film is formed as the oxide semiconductor film 106, there is no particular limitation on the deposition temperature.

[0094]

Next, a conductive film used for a source electrode and a drain electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the base insulating film 104 and the oxide semiconductor film 106. As the conductive film used for the source electrode and the drain electrode, for example, a metal film containing an element selected from aluminum, chromium, copper, tantalum, titanium, molybdenum, or tungsten, or a metal nitride film containing any of the above elements as its component (e.g., a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) can be used. Alternatively, the conductive film may have a structure in which a film of a high-melting-point metal such as titanium, molybdenum, or tungsten, or a nitride film of any of these metals (a titanium nitride film, a molybdenum nitride film, or a tungsten nitride film) is stacked on either or both of the bottom surface and the top surface of a metal film of aluminum, copper, or the like. Further, the conductive film used for the source electrode and the drain electrode may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium tin oxide (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), or indium zinc oxide (In_2O_3-ZnO) can be used. The conductive film used for the source electrode and the drain electrode can be formed using any of the above materials to have a single layer or a stacked structure. There is no particular limitation on the method for forming the conductive film, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, and a spin coating method can be employed.

[0095]

Next, a resist mask is formed over the conductive film through a photolithography step and selective etching is performed, so that the source electrode 108a and the drain electrode 108b are formed. Then, the resist mask is removed (see FIG. 2B). For the light exposure for forming the resist mask in this photolithography step, ultraviolet, KrF laser, or ArF laser can be used.

[0096]

In this step, a channel length L of the transistor 150 that is to be completed in a later step is determined by a distance between a lower end of the source electrode 108a and a lower end of the drain electrode 108b that are adjacent to each other over the oxide semiconductor film 106. When light exposure is performed for a channel length L smaller than 25 nm, the light exposure for forming the resist mask in the photolithography step may be performed using extreme ultraviolet light having an extremely short wavelength of several nanometers to several tens of nanometers, for example. In the light exposure by extreme ultraviolet light, the resolution is high and the focus depth is large. Thus, the channel length L of the transistor 150 formed later can be reduced, whereby the operation speed of a circuit can be increased.

[0097]

In order to reduce the number of photomasks used in a photolithography step and reduce the number of photolithography steps, an etching step may be performed with use of a multi-tone mask which is a light-exposure mask through which light is transmitted to have a plurality of intensities. A resist mask formed with use of a multi-tone mask has a plurality of thicknesses and further can be changed in shape by etching; therefore, the resist mask can be used in a plurality of etching steps for processing into different patterns. Therefore, a resist mask corresponding to at least two kinds or more of different patterns can be formed by one multi-tone mask. Thus, the number of light-exposure masks can be reduced and the number of corresponding photolithography steps can be also reduced, whereby simplification of a process can be achieved.

[0098]

Note that it is preferable that etching conditions be optimized so as not to etch and divide the oxide semiconductor film 106 when the conductive film is etched. However, it is difficult to obtain etching conditions in which only the conductive film is etched and the oxide semiconductor film 106 is not etched at all. In some cases, only part of the oxide semiconductor film 106, e.g., 5 % to 50 % in thickness of the oxide semiconductor film 106, is etched, so that the oxide semiconductor film 106 has a groove portion (a recessed portion) when the conductive film is etched.

[0099]

Next, the gate insulating film 110 is formed to cover the oxide semiconductor film 106 and the source electrode 108a and the drain electrode 108b. The gate insulating film 110 can have a thickness greater than or equal to 1 nm and less than or equal to 500 nm. There is no particular limitation on the formation method of the gate insulating film 110; for example, a sputtering method, an MBE method, a CVD method, a pulsed laser deposition method, an ALD method, or the like can be used as appropriate for formation of the gate insulating film 110.

[0100]

For the gate insulating film 110, an oxide insulating film having a sufficient withstand voltage and sufficient insulating properties is preferably used. In the case where the gate insulating film 110 has a single-layer structure, an oxide containing silicon such as a silicon oxide film may be used.

[0101]

Further, when the gate insulating film 110 is formed, impurities such as silicon are taken to the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110. As a result, in the oxide semiconductor film 106, the region 106a is formed in the vicinity of the interface with the gate insulating film 110, and a region in the oxide semiconductor film 106 other than the region 106a is the region 106b.

[0102]

Note that the concentration of silicon included in the region 106a is lower than or equal to 1.0 at.%, preferably lower than or equal to 0.1 at.%. The region 106a is provided to be in contact with the gate insulating film 110 to have a thickness less than or equal to 5 nm.

[0103]

Further, in the case where impurities such as carbon is included in the gate insulating film 110, such impurities also enter the region 106a in the oxide semiconductor film 106 and serve as impurities, as in the case of silicon. In that case, the concentration of carbon included in the region 106a is lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0104]

Alternatively, the gate insulating film 110 may have a stacked structure. In the case where the gate insulating film 110 has a stacked structure, for example, gallium oxide, aluminum oxide, silicon nitride, silicon oxynitride, aluminum oxynitride, yttrium oxide, lanthanum oxide, silicon nitride oxide, or the like may be stacked over oxide containing silicon. Alternatively, a high-k material such as hafnium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)), hafnium silicate to which nitrogen is added ($HfSiO_xN_y$ ($x > 0, y > 0$)), or hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)) may be stacked over an oxide containing silicon.

[0105]

When an oxide containing silicon is used as the gate insulating film 110, part of oxygen contained in the insulating film can be released by performing heat treatment described later; thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled. In particular, the gate insulating film 110 preferably contains a large amount of oxygen which exceeds at least the stoichiometry. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 110. When such a silicon oxide film is used as the gate insulating film 110, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 150 using the oxide semiconductor film 106 can have favorable transistor characteristics.

[0106]

In order to prevent impurities such as silicon from entering the oxide semiconductor film 106, the gate insulating film 110 is formed in such a manner as not to damage the oxide semiconductor film 106. For example, in the case where a silicon oxide film is formed as the gate insulating film 110 by a sputtering method, the impact of silicon (that is a constituent element of the gate insulating film 110) colliding with the oxide semiconductor film 106 may be reduced. For achieving the above, specifically, a method in which the power for deposition of the gate insulating film 110 is low, a method in which the pressure for deposition of the gate insulating film 110 is high, a method in which a distance between a target and a substrate (T-S distance) is increased in deposition of the gate insulating film 110, or the like can be used. However, a formation method of the gate insulating film 110 is not limited to the above. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or the like, which is formed by a PE-CVD method, can be used. A PE-CVD method is preferred to a sputtering method because with use of the PE-CVD method, the oxide semiconductor film 106 serving as a base film is less damaged.

[0107]

Next, a conductive film used for formation of a gate electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the gate insulating film 110. The conductive film used for the gate electrode can be formed using, for example, a metal material such as molybdenum, titanium, tantalum, tungsten, aluminum, copper, neodymium, or scandium, or an alloy material including any of these materials as a main component. Alternatively, the conductive film used for the gate electrode may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), indium tin oxide (In_2O_3-SnO_2, which is abbreviated to ITO in some cases), indium zinc oxide (In_2O_3-ZnO), or any of these metal oxide materials in which silicon or silicon oxide is included can be used. The gate electrode can be formed to have a single layer or a stacked structure using any of the above materials. There is no particular limitation on the method for forming the conductive film, and a variety of film formation methods such as an evaporation method, a CVD method, a sputtering method, and a spin coating method can be employed.

[0108]

Next, a resist mask is formed over the conductive film through a photolithography step and selective etching is performed, so that the gate electrode 112 is formed. Then, the resist mask is removed (see FIG. 2C). The resist mask used for forming the gate electrode 112 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced. For etching the gate electrode 112, wet etching, dry etching, or both of them may be employed. Note that when the gate electrode 112 is formed, the transistor 150 is formed.

[0109]

Next, the interlayer insulating film 114 is formed over the gate insulating film 110 and the gate electrode 112 (see FIG. 2D).

[0110]

The interlayer insulating film 114 is preferably formed using an inorganic insulating film to have a single layer or a stacked layer of any of oxide insulating films such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, and a hafnium oxide film. Further, over the above oxide insulating film, a single layer or a stacked layer of any of nitride insulating films such as a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, and an aluminum nitride oxide film may be formed. For example, as a stacked layer, a silicon oxide film and an aluminum oxide film are deposited in this order over the gate electrode 112.

[0111]

After the formation of the interlayer insulating film 114, heat treatment is preferably performed on the oxide semiconductor film 106. The temperature of the heat treatment is higher than or equal to 300 °C and lower than or equal to 700 °C, or lower than the strain point of a substrate.

[0112]

The heat treatment may be performed in an atmosphere of nitrogen, oxygen, ultra-dry air (air in which the moisture content is less than or equal to 20 ppm, preferably less than or equal to 1 ppm, further preferably less than or equal to 10 ppb), or a rare gas (such as argon or helium). Note that it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen, oxygen, ultra-dry air, a rare gas, or the like. It is also preferable that the purity of nitrogen, oxygen, or the rare gas which is introduced into a heat treatment apparatus be set to higher than or equal to 6N (99.9999 %), preferably higher than or equal to 7N (99.99999 %) (that is, the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

[0113]

In the case of performing heat treatment after formation of the oxide semiconductor film, oxygen that is one of main component materials included in the oxide semiconductor might be reduced. However, during the heat treatment in this step, oxygen can be supplied to the oxide semiconductor film 106 from the base insulating film 104 or the gate insulating film 110 which is formed using an oxide containing silicon; thus, oxygen vacancies in the oxide semiconductor film 106 can be filled.

[0114]

By performing the heat treatment as described above, the oxide semiconductor film 106 can be highly purified so as not to contain impurities other than main components as little as possible. The highly purified oxide semiconductor film 106 contains extremely few (close to zero) carriers derived from a donor, and the carrier concentration thereof is lower than 1×10^{14} /cm^3, preferably lower than 1×10^{12} /cm^3, further preferably lower than 1×10^{11} /cm^3. In such a manner, the oxide semiconductor film 106 that becomes an i-type (intrinsic) oxide semiconductor can be formed.

[0115]

Through the above steps, the transistor 150 is formed. In the transistor 150, the concentration of impurities such as silicon taken into the region 106a of the oxide semiconductor film 106 is small. Further, in the case where the oxide semiconductor film is a CAAC-OS film, a crystal portion can be formed even in the vicinity of the interface between the oxide semiconductor film and the gate insulating film 110. Thus, the transistor 150 can have stable electric characteristics.

[0116]

Over the interlayer insulating film 114, a planarization insulating film may be further provided. The planarization insulating film can be formed using an organic material having heat resistance, such as, an acrylic resin, a polyimide resin, a benzocyclobutene-based resin, a polyamide resin, or an epoxy resin can be used. Other than such organic materials, a low-dielectric constant material (a low-k material) or a siloxane-based resin can be used. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed of any of these materials.

[0117]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0118]

(Embodiment 2)

In this embodiment, modification examples of the semiconductor device and the method for manufacturing the semiconductor device of Embodiment 1, which are illustrated in FIGS. 1A and 1B and FIGS. 2A to 2D, will be described with reference to FIGS. 3A and 3B, FIGS. 4A to 4D, FIGS. 5A and 5B. Note that portions similar to those in FIGS. 1A and 1B and FIGS. 2A to 2D are denoted by the same reference numerals, and description thereof is skipped.

[0119]

<Example of Structure of Semiconductor Device (Modification Example)>

In FIGS. 3A and 3B, a top-gate transistor is illustrated as an example of a semiconductor device. FIG. 3A is a plan view, and FIG. 3B is a cross-sectional view taken along dashed line X2-Y2 in FIG. 3A. Note that in FIG. 3A, some components of a transistor 160 (e.g., a gate insulating film 110) are omitted for simplicity.

[0120]

The transistor 160 illustrated in FIGS. 3A and 3B includes, over a substrate 102, a base insulating film 104, an oxide semiconductor film 106 which is formed over the base insulating film 104 and includes a region 106c, a region 106d, a region 106e, and a region 106f, the gate insulating film 110 formed over the oxide semiconductor film 106, a gate electrode 112 provided to be in contact with the gate insulating film 110 and overlap with at least the oxide semiconductor film 106, an interlayer insulating film 114 formed over the gate insulating film 110 and the gate electrode 112, and a source electrode 108a and a drain electrode 108b which are provided over the interlayer insulating film 114 and electrically connected to the oxide semiconductor film 106.

[0121]

The oxide semiconductor film 106 includes the region 106c and the region 106d, which function as a channel formation region, and the region 106e and the region 106f which function as a pair of low resistance regions provided so that the channel formation region is sandwiched therebetween.

[0122]

Further, as illustrated in FIG. 3B, an end portion of the oxide semiconductor film 106 is preferably tapered at an angle of 20° to 50°. When the oxide semiconductor film 106 has a perpendicular end portion, oxygen is more likely to be released from the end portion of the oxide semiconductor film 106, and accordingly, oxygen vacancies are likely to be generated. When the oxide semiconductor film 106 has a tapered end portion, generation of oxygen vacancies is suppressed, and thus generation of leakage current of the transistor 160 can be reduced.

[0123]

For the gate insulating film 110, an oxide insulating film having a sufficient withstand voltage and sufficient insulating properties is preferably used. In the case where the gate insulating film 110 has a single-layer structure, an oxide containing silicon, such as a silicon oxide film, may be used, for example.

[0124]

When an oxide containing silicon is used as the gate insulating film 110, part of oxygen contained in the insulating film can be released by performing heat treatment; thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled. In particular, the gate insulating film 110 preferably contains a large amount of oxygen which exceeds at least the stoichiometry. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 110. When such a silicon oxide film is used as the gate insulating film 110, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 160 using the oxide semiconductor film

106 can have favorable transistor characteristics.

[0125]

However, in the case of using a silicon oxide film as the gate insulating film 110, silicon that is a constituent element of the gate insulating film 110 might be taken as an impurity into the oxide semiconductor film 106. Silicon which is a constituent element of the gate insulating film 110 or the like enters the oxide semiconductor film 106 and serves as an impurity, which affects characteristics of the transistor. Further, in the case where the oxide semiconductor film 106 is a CAAC-OS film, a constituent element of the gate insulating film 110 enters the oxide semiconductor film 106, and a bond in the crystal portion in the oxide semiconductor film 106 is broken. Thus, amorphous regions are more formed in the oxide semiconductor film 106 in the vicinity of the gate insulating film 110.

[0126]

In particular, impurities such as silicon are likely to enter the oxide semiconductor film 106 in the vicinity of the gate insulating film 110. A channel formation region of the transistor 160 is formed in the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110; thus, when impurities such as silicon enter the vicinity of the interface between the oxide semiconductor film 106 and the gate insulating film 110, characteristics of the transistor 150 might be changed.

[0127]

Thus, in the semiconductor device described in this embodiment, entry of impurities such as silicon into the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110 is suppressed. As a result, in the oxide semiconductor film 106, a region in which the concentration of silicon distributed from an interface with the gate insulating film 110 toward an inside of the oxide semiconductor film 106 is lower than or equal to 1.0 at.% is formed. Such a region is referred to as the region 106c and the region 106e in FIG. 3B. The concentrations of silicon included in the region 106c and the region 106e are further preferably lower than or equal to 0.1 at.%. Further, the region 106c and the region 106e are provided to be in contact with the gate insulating film 110 and have a thickness less than or equal to 5 nm.

[0128]

Note that in FIG. 3B, in the oxide semiconductor film 106, regions on the base insulating film 104 side are the region 106d and the region 106f, and regions on the gate insulating film 110 side are the region 106c and the region 106e.

[0129]

Further, in the case where impurities such as carbon is included in the gate insulating film 110, such impurities might also enter the oxide semiconductor film 106 and serve as impurities, as in the case of silicon. In that case, the concentrations of carbon included in the region 106c and the region 106e are lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0130]

In order to prevent impurities such as silicon from entering the oxide semiconductor film 106, the gate insulating film 110 may be formed in such a manner as not to damage the oxide semiconductor film 106. For example, in the case where a silicon oxide film is formed as the gate insulating film 110 by a sputtering method, the impact caused by silicon (that is a constituent element of the gate insulating film 110) colliding with the oxide semiconductor film 106 may be reduced. For achieving the above, specifically, a method in which the power for deposition of the gate insulating film 110 is low, a method in which the pressure for deposition of the gate insulating film 110 is high, a method in which a distance between a target and a substrate (T-S distance) is increased in deposition of the gate insulating film 110, or the like can be used. However, a formation method of the gate insulating film 110 is not limited to the above. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or the like, which is formed by a PE-CVD method, can be used. A PE-CVD method is preferred to a sputtering method because with use of the PE-CVD method, the oxide semiconductor film 106 serving as a base film is less damaged.

[0131]

As described above, the concentrations of impurities such as silicon and carbon entering the region 106c and the region 106e in the oxide semiconductor film 106 are reduced, whereby change in characteristics of the transistor 160 can be suppressed. Further, in the case where the oxide semiconductor film 106 is a CAAC-OS film, a crystal portion can be formed even in the vicinity with the gate insulating film 110.

When the transistor 160 is formed using such an oxide semiconductor film 106, a semiconductor device with stable electric characteristics can be provided.

[0132]

Note that the details of the other components of the transistor are described with reference to FIGS. 4A to 4D and FIGS. 5A and 5B, in description of a method for manufacturing the transistor 160 below.

[0133]

<Manufacturing Method of Transistor 160>

Hereinafter, an example of a method for manufacturing the transistor 160 illustrated in FIGS. 3A and 3B of this embodiment is described with reference to FIGS. 4A to 4D and FIGS. 5A and 5B.

[0134]

First, the substrate 102 is prepared. A substrate having a structure similar to that described in Embodiment 1 can be used as the substrate 102.

[0135]

Next, the base insulating film 104 is formed over the substrate 102 (see FIG. 4A). The base insulating film 104 has a function of preventing diffusion of an impurity element such as hydrogen or moisture from the substrate 102, and can be formed with a single-layer structure or a stacked structure using one or more of a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and a silicon oxynitride film.

[0136]

In addition, the base insulating film 104 has another function of supplying oxygen to the oxide semiconductor film 106 formed later. For example, in the case where an insulating film containing an oxide is formed as the base insulating film 104, by heating the base insulating film 104, part of contained oxygen can be released. Thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled accordingly. In particular, the base insulating film 104 preferably contains a large amount of oxygen which exceeds at least the stoichiometry thereof. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the base insulating film 104. When such a silicon oxide film is used as the base insulating film 104, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 160 using the oxide semiconductor film 106 can have favorable transistor characteristics.

[0137]

Before the base insulating film 104 is formed, plasma treatment or the like may be performed on the substrate 102. As plasma treatment, reverse sputtering in which an argon gas is introduced and plasma is generated can be performed. As plasma treatment, reverse sputtering in which an argon gas is introduced and plasma is generated can be performed. The reverse sputtering refers to a method in which an RF power source is used for application of a voltage to the substrate 102 side in an argon atmosphere so that plasma is generated in the vicinity of the substrate 102 to modify a surface of the substrate. Note that instead of an argon atmosphere, a nitrogen atmosphere, a helium atmosphere, an oxygen atmosphere, or the like may be used. The reverse sputtering can remove particle substances (also referred to as particles or dust) attached to the surface of the substrate 102.

[0138]

Next, the oxide semiconductor film 106 is formed over the base insulating film 104 (see FIG. 4A). The oxide semiconductor film 106 is preferably a CAAC-OS film. Note that the base insulating film 104 and the oxide semiconductor film 106 are preferably formed successively without being exposed to the air.

[0139]

The oxide semiconductor film 106 can have a structure similar to that described in Embodiment 1.

[0140]

Next, the gate insulating film 110 is formed to cover the oxide semiconductor film 106 (see FIG. 4B). The thickness of the gate insulating film 110 can be greater than or equal to 1 nm and less than or equal to 500 nm. There is no particular limitation on the formation method of the gate insulating film 110; for example, a sputtering method, an MBE method, a CVD method, a pulsed laser deposition method, an ALD method, or the like can be used as appropriate for formation of the gate insulating film 110.

[0141]

For the gate insulating film 110, an oxide insulating film having a sufficient withstand voltage and sufficient insulating properties is preferably used. In the case where the gate insulating film 110 has a single-layer structure, an oxide containing silicon film such as a silicon oxide film, may be used, for example.

[0142]

Further, when the gate insulating film 110 is formed, impurities such as silicon enter the oxide semiconductor film 106 in the vicinity of the interface with the gate insulating film 110. As a result, in the oxide semiconductor film 106, a region 106g is formed in the vicinity of the interface with the gate insulating film 110, and a region in the oxide semiconductor film 106 other than the region 106g is a region 106h. Note that the region 106g becomes the region 106c and the region 106e in a later step, and the region 106h becomes the region 106d and the region 106f in the later step.

[0143]

The concentration of silicon included in the region 106g is lower than or equal to 1.0 at.%, preferably lower than or equal to 0.1 at.%. Further, the region 106g is provided to be in contact with the gate insulating film 110 to have a thickness less than or equal to 5 nm.

[0144]

Further, in the case where impurities such as carbon is included in the gate insulating film 110, such impurities also enter the region 106g of the oxide semiconductor film 106 and serve as impurities, as in the case of silicon. In that case, the concentration of carbon included in the region 106g is lower than or equal to 1.0×10^{20} atoms/cm^3, preferably lower than or equal to 1.0×10^{19} atoms/cm^3.

[0145]

The gate insulating film 110 may have a stacked structure. In the case where the gate insulating film 110 has a stacked structure, for example, gallium oxide, aluminum oxide, silicon nitride, silicon oxynitride, aluminum oxynitride, yttrium oxide, lanthanum oxide, silicon nitride oxide, or the like may be stacked over oxide containing silicon. Alternatively, a high-k material such as hafnium oxide, hafnium silicate ($HfSi_xO_y$ ($x > 0, y > 0$)), hafnium silicate to which nitrogen is added ($HfSiO_xN_y$ ($x > 0, y > 0$)), or hafnium aluminate ($HfAl_xO_y$ ($x > 0, y > 0$)) may be stacked over an oxide containing silicon.

[0146]

When an oxide containing silicon is used as the gate insulating film 110, part of oxygen contained in the insulating film can be released by performing heat treatment; thus, oxygen can be supplied to the oxide semiconductor film 106, and oxygen vacancies in the oxide semiconductor film 106 can be filled. In particular, the gate insulating film 110 preferably contains a large amount of oxygen which exceeds at least the stoichiometry. For example, a film of silicon oxide represented by the formula $SiO_{2+\alpha}$ ($\alpha > 0$) is preferably used as the gate insulating film 110. When such a silicon oxide film is used as the gate insulating film 110, oxygen can be supplied to the oxide semiconductor film 106, so that the transistor 160 using the oxide semiconductor film 106 can have favorable transistor characteristics.

[0147]

In order to prevent impurities such as silicon from entering the oxide semiconductor film 106, the gate insulating film 110 is formed in such a manner as not to damage the oxide semiconductor film 106. For example, in the case where a silicon oxide film is formed as the gate insulating film 110 by a sputtering method, the impact of silicon (that is a constituent element of the gate insulating film 110) colliding with the oxide semiconductor film 106 may be reduced. For achieving the above, specifically, a method in which the power for deposition of the gate insulating film 110 is low, a method in which the pressure for deposition of the gate insulating film 110 is high, a method in which a distance between a target and a substrate (T-S distance) is increased in deposition of the gate insulating film 110, or the like can be used. However, a formation method of the gate insulating film 110 is not limited to the above. For example, a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, or the like, which is formed by a PE-CVD method, can be used. A PE-CVD method is preferred to a sputtering method because with use of the PE-CVD method, the oxide semiconductor film 106 serving as a base film is less damaged.

[0148]

Next, a conductive film used for formation of a gate electrode (as well as a wiring formed in the same layer as the gate electrode) is formed over the gate insulating film 110. The conductive film used for the gate electrode may have a structure similar to that of a material and the like described in Embodiment 1.

[0149]

Next, a resist mask is formed over the conductive film through a photolithography step and selective etching is performed, so that the gate electrode 112 is formed. Then, the resist mask is removed (see FIG. 4C). The resist mask used for forming the gate electrode 112 may be formed by an inkjet method. Formation of the resist mask by an inkjet method needs no photomask; thus, manufacturing cost can be reduced. For etching the gate electrode 112, wet etching, dry etching, or both of them may be employed.

[0150]

Next, dopant 181 is introduced into the oxide semiconductor film 106 with use of the gate electrode 112 as a mask, so that a pair of low resistance regions 106e and a pair of low resistance regions 106f are formed (see FIG. 4D).

[0151]

The dopant 181 is an impurity by which the electrical conductivity of the oxide semiconductor film 106 is changed. One or more selected from the following can be used as the dopant 181: Group 15 elements (typical examples thereof are phosphorus (P), arsenic (As), and antimony (Sb)), boron (B), aluminum (Al), nitrogen (N), argon (Ar), helium (He), neon (Ne), indium (In), fluorine (F), chlorine (Cl), titanium (Ti), and zinc (Zn).

[0152]

The dopant 181 can be introduced into the oxide semiconductor film 106 through another film (e.g., the gate insulating film 110) by an implantation method. As a method for introducing the dopant 181, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, or the like can be used. In the case where the above method is used, it is preferable to use a single ion of the dopant 181, a fluoride ion, or a chloride ion.

[0153]

The introduction of the dopant 181 may be controlled by setting the implantation conditions such as the accelerated voltage and the dosage, or the thickness of the films through which the dopant passes as appropriate. In this embodiment, phosphorus is used as the dopant 181, whose ion is added by an ion implantation method. The dosage of the dopant 181 can be set to be greater than or equal to 1 ×

10^{13} ions/cm^2 and less than or equal to 5×10^{16} ions/cm^2.

[0154]

The concentration of the dopant 181 in the low-resistance regions is preferably higher than or equal to 5×10^{18} /cm^3 and lower than or equal to 1×10^{22} /cm^3.

[0155]

The substrate 102 may be heated while the dopant 181 is introduced.

[0156]

The introduction of the dopant 181 into the oxide semiconductor film 106 may be performed plural times, and the number of kinds of dopant may be plural.

[0157]

After the dopant 181 is introduced, heat treatment may be performed. The heat treatment is preferably performed at a temperature higher than or equal to 300 °C and lower than or equal to 700 °C, preferably higher than or equal to 300 °C and lower than or equal to 450 °C for one hour in an oxygen atmosphere. The heat treatment may be performed in a nitrogen atmosphere, reduced pressure, or the air (ultra-dry air).

[0158]

In the case where the oxide semiconductor film 106 is a crystalline oxide semiconductor film or a CAAC-OS film, part of the oxide semiconductor film may be amorphous by introduction of the dopant 181. In that case, the crystallinity of the oxide semiconductor film 106 can be recovered by performing heat treatment thereon after the introduction of the dopant 181.

[0159]

Through the above steps, the region 106e and the region 106f between which the region 106c and the region 106d functioning as a channel formation region are sandwiched are formed in the oxide semiconductor film 106.

[0160]

Next, the interlayer insulating film 114 is formed over the gate insulating film 110 and the gate electrode 112 (see FIG. 5A).

[0161]

As the interlayer insulating film 114, an inorganic insulating film is preferable; a single layer or a stacked layer of any of oxide insulating films of a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a hafnium oxide film, and the like. Further, over the above oxide insulating film, a single layer or a stacked layer of any of nitride insulating films of a silicon nitride film, a silicon nitride oxide film, an aluminum nitride film, an aluminum nitride oxide film, and the like may be formed. For example, a silicon oxide film and an aluminum oxide film are stacked in this order on the gate electrode 112 side by a sputtering method.

[0162]

In the case where an aluminum oxide film is used as the interlayer insulating film, during or after the manufacturing process, the aluminum oxide film can serve to prevent impurities such as hydrogen or moisture, which causes a change in electric characteristics of the transistor 160, from entering the oxide semiconductor film 106. In addition, during or after the manufacturing process, the aluminum oxide film can serve to prevent oxygen which is a main component of an oxide semiconductor from being released from the oxide semiconductor film 106.

[0163]

After the interlayer insulating film 114 is formed, it is preferable to perform heat treatment on the oxide semiconductor film 106. The temperature of the heat treatment is higher than or equal to 300 °C and lower than or equal to 700 °C, or lower than the strain point of a substrate.

[0164]

The heat treatment may be performed in an atmosphere of nitrogen, oxygen, ultra-dry air (air in which the moisture content is less than or equal to 20 ppm, preferably less than or equal to 1 ppm, further preferably less than or equal to 10 ppb), or a rare gas (such as argon or helium). Note that it is preferable that water, hydrogen, and the like be not contained in the atmosphere of nitrogen, oxygen, ultra-dry air, a rare gas, or the like. It is also preferable that the purity of nitrogen, oxygen, or the rare gas which is introduced into a heat treatment apparatus be set to higher than or equal to 6N (99.9999 %), preferably higher than or equal to 7N (99.99999 %) (that is, the impurity concentration is lower than or equal to 1 ppm, preferably lower than or equal to 0.1 ppm).

[0165]

In the case of performing heat treatment after formation of the oxide semiconductor film, oxygen which is one of main components of the oxide semiconductor might be reduced. However, during the heat treatment in this step, oxygen can be supplied to the oxide semiconductor film 106 from the base insulating film 104 or the gate insulating film 110 which is formed using an oxide containing silicon; thus, oxygen vacancies in the oxide semiconductor film 106 can be filled.

[0166]

By performing the heat treatment as described above, the oxide semiconductor film 106 can be highly purified so as not to contain impurities other than main components as little as possible. The highly purified oxide semiconductor film 106 includes extremely few (close to zero) carriers derived from a donor, and the carrier concentration thereof is lower than 1×10^{14} /cm^3, preferably lower than 1×10^{12} /cm^3, further preferably lower than 1×10^{11} /cm^3. In such a manner, the oxide semiconductor film 106 that becomes an i-type (intrinsic) oxide semiconductor can be formed.

[0167]

Next, an opening portion reaching the oxide semiconductor film 106 (the region 106e or the region 106f) is formed in the gate insulating film 110 and the interlayer insulating film 114, and a conductive film used for the source electrode and the drain electrode (as well as a wiring formed in the same layer as the gate electrode) is formed in the opening portion. The conductive film used for the source electrode and the drain electrode may be formed using a material and a structure similar to those described in Embodiment 1.

[0168]

Next, a resist mask is formed over the conductive film through a photolithography step and selective etching is performed, so that the source electrode 108a and the drain electrode 108b are formed. Then, the resist mask is removed (see FIG. 5B).

[0169]

Through the above-described process, the transistor 160 is formed (see FIG.

5B). In the transistor 160, the concentration of silicon entering the region 106c and the region 106e in the oxide semiconductor film 106 is reduced. Further, in the case where the oxide semiconductor film 106 is a CAAC-OS film, a crystal portion can be formed even in the vicinity of the interface with the gate insulating film 110. Thus, the transistor 160 can have stable electric characteristics.

[0170]

Furthermore, a planarization insulating film may be provided over the transistor 160. The planarization insulating film can be formed using an organic material having heat resistance, such as an acrylic resin, a polyimide resin, a benzocyclobutene-based resin, a polyamide-based resin, or an epoxy-based resin. Other than such organic materials, a low-dielectric constant material (a low-k material) or a siloxane-based resin can be used. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed of any of these materials.

[0171]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0172]

(Embodiment 3)

In this embodiment, an example of a semiconductor device which includes the transistor described in this specification, which can hold stored data even when not powered, and which does not have a limitation on the number of write cycles, will be described with reference to drawings.

[0173]

FIGS. 6A to 6C illustrate one example of a structure of the semiconductor device. FIG. 6A is a cross-sectional view of the semiconductor device, FIG. 6B is a plan view of the semiconductor device, and FIG. 6C is a circuit diagram of the semiconductor device. FIG. 6A is a cross-sectional view taken along line C1-C2 and line D1-D2 in FIG. 6B.

[0174]

The semiconductor device illustrated in FIGS. 6A and 6B includes a transistor 260 including a first semiconductor material in a lower portion, and a transistor 150 including a second semiconductor material in an upper portion. A transistor having the structure described in Embodiment 1 can be employed for the transistor 150. The transistor 150 has a structure in which a source electrode 108a and a drain electrode 108b are provided to be in contact with an oxide semiconductor film 106. Note that although there is no description, the transistor described in Embodiment 2 can also be employed in this embodiment.

[0175]

Here, the first semiconductor material and the second semiconductor material are preferably materials having different band gaps. For example, the first semiconductor material may be a semiconductor material other than an oxide semiconductor (e.g., single crystal silicon) and the second semiconductor material may be an oxide semiconductor. A transistor including single crystal silicon as a material other than an oxide semiconductor can operate at high speed. On the other hand, a transistor including an oxide semiconductor enables holding of charge for a long time owing to its characteristics.

[0176]

Although all the transistors are n-channel transistors here, it is needless to say that p-channel transistors can be used. Although an oxide semiconductor in the transistor 150 described in Embodiment 1 is used so that data can be held, it is not necessary to limit a specific structure of the semiconductor device, such as a material of the semiconductor device or a structure of the semiconductor device, to the structure described here.

[0177]

The transistor 260 illustrated in FIG. 6A includes a channel formation region 216 provided in a substrate 200 including a semiconductor material (e.g., silicon), impurity regions 220 with the channel formation region 216 provided therebetween, intermetallic compound regions 224 in contact with the impurity regions 220, a gate insulating film 208 provided over the channel formation region 216, and the gate electrode 210 provided over the gate insulating film 208. Note that a transistor whose source electrode and drain electrode are not illustrated in a drawing may be referred to as a transistor for the sake of convenience. Further, in such a case, in description of a connection of a transistor, a source region and a source electrode are collectively referred to as a "source electrode," and a drain region and a drain electrode are collectively referred to as a "drain electrode". That is, in this specification, the term "source electrode" may include a source region.

[0178]

An element isolation insulating film 206 is provided over the substrate 200 so as to surround the transistor 260, and an insulating film 228 and an insulating film 230 are provided to cover the transistor 260. Note that for high integration, it is preferable that, as illustrated in FIG. 6A, the transistor 260 does not have a sidewall insulating film. On the other hand, when the characteristics of the transistor 260 have priority, the sidewall insulating film may be formed on a side surface of the gate electrode 210 and the impurity regions 220 may include a region having different impurity concentrations.

[0179]

The transistor 260 formed using a single crystal semiconductor substrate can operate at high speed. Thus, when the transistor is used as a reading transistor, data can be read at a high speed. Two insulating films are formed so as to cover the transistor 260. As treatment prior to formation of the transistor 150 and a capacitor 264, CMP treatment is performed on the two insulating films, whereby an insulating film 228 and an insulating film 230 which are planarized are formed and, at the same time, an upper surface of the gate electrode 210 is exposed.

[0180]

As each of the insulating film 228 and the insulating film 230, typically, it is possible to use an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, an aluminum oxynitride film, a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum nitride oxide film. The insulating film 228 and the insulating film 230 can be formed by a plasma CVD method, a sputtering method, or the like.

[0181]

As the planarization insulating film, an organic material such as a polyimide-based resin, an acrylic-based resin, or a benzocyclobutene-based resin can be used. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material) or the like. In the case of using an organic material, the insulating film 228 and the insulating film 230 may be formed by a wet method such as a spin coating method or a printing method.

[0182]

Note that in this embodiment, a silicon nitride film is used as the insulating film 228, and a silicon oxide film is used as the insulating film 230.

[0183]

An oxide semiconductor film 106 is formed over the insulating film 230 which is sufficiently planarized by polishing treatment (such as CMP treatment). Note that the average plane roughness of a surface of the insulating film 230 is preferably less than or equal to 0.15 nm.

[0184]

The transistor 150 illustrated in FIG. 6A uses an oxide semiconductor in the channel formation region. Here, the oxide semiconductor film 106 included in the transistor 150 is preferably highly purified. With use of a highly purified oxide semiconductor, the transistor 150 which has extremely favorable off-state characteristics can be obtained.

[0185]

Since the off-state current of the transistor 150 is small, stored data can be held for a long time owing to such a transistor. In other words, power consumption can be sufficiently reduced because a semiconductor memory device in which refresh operation is unnecessary or the frequency of refresh operation is extremely low can be provided.

[0186]

An insulating film 180 having a single-layer structure or a stacked structure is provided over the transistor 150. In this embodiment, the insulating film 180 has a stacked structure in which an aluminum oxide film and a silicon oxide film are stacked in this order on a gate electrode 112 side. Note that when the aluminum oxide film has high density (e.g., a film density higher than or equal to 3.2 g/cm^3, preferably higher than or equal to 3.6 g/cm^3), the transistor 150 can have stable electric characteristics.

[0187]

Further, a conductive film 182 is provided in a region which overlaps with the source electrode 108a of the transistor 150 with the gate insulating film 110 and the insulating film 180 interposed therebetween. A capacitor 264 is formed with the source electrode 108a, the gate insulating film 110, the insulating film 180, and the conductive film 182. That is, the source electrode 108a of the transistor 150 functions as one electrode of the capacitor 264, and the conductive film 182 functions as the other electrode of the capacitor 264. Note that in the case where a capacitor is not needed, the capacitor 264 may be omitted. Alternatively, the capacitor 264 may be separately provided above the transistor 150.

[0188]

An insulating film 184 is provided over the transistor 150 and the capacitor 264. In addition, a wiring 186 for connecting the transistor 150 to another transistor is provided over the insulating film 184. Although not illustrated in FIG. 6A, the wiring 186 is electrically connected to the drain electrode 108b with an electrode formed in an opening that is formed in the insulating film 180, the gate insulating film 110, and the like. Here, the electrode is preferably provided so as to partly overlap with at least the oxide semiconductor film 106 of the transistor 150.

[0189]

In FIGS. 6A and 6B, the transistor 260 and 150 are provided so as to at least partly overlap with each other, and the source region or the drain region of the transistor 260 is preferably provided to partly overlap with the oxide semiconductor film 106. Further, the transistor 150 and the capacitor 264 are provided so as to overlap with at least part of the transistor 260. For example, the conductive film 182 of the capacitor 264 is provided so as to at least partly overlap with the gate electrode 210 of the transistor 260. With such a planar layout, the area occupied by the semiconductor device can be reduced; thus, higher integration can be achieved.

[0190]

Note that the electrical connection between the drain electrode 108b and the wiring 186 may be established by direct contact of the drain electrode 108b and the wiring 186 with each other or through an electrode provided in an insulating layer lying therebetween. Alternatively, the electrical connection may be established through a plurality of electrodes.

[0191]

Next, an example of a circuit configuration corresponding to FIGS. 6A and 6B is shown in FIG. 6C.

[0192]

In FIG. 6C, a first wiring (1st Line) is electrically connected to one of the source electrode and the drain electrode of the transistor 260, and a second wiring (2nd Line) is electrically connected to the other of the source electrode and the drain electrode of the transistor 260. A third wiring (3rd line) and one of the source electrode and the drain electrode of the transistor 150 are electrically connected to each other, and a fourth wiring (4th line) and the gate electrode of the transistor 150 are electrically connected to each other. A gate electrode of the transistor 260 and the other of the source electrode and the drain electrode of the transistor 150 are electrically connected to one electrode of the capacitor 264. A fifth wiring (5th Line) and the other electrode of the capacitor 264 are electrically connected to each other.

[0193]

The semiconductor device in FIG. 6C can write, hold, and read data as described below, utilizing a characteristic in which the potential of the gate electrode of the transistor 260 can be held.

[0194]

Writing and holding of data will be described. First, the potential of the fourth wiring is set to a potential at which the transistor 150 is turned on, so that the transistor 150 is turned on. Thus, the potential of the third wiring is applied to the gate electrode of the transistor 260 and the capacitor 264. In other words, a predetermined charge is supplied to the gate electrode of the transistor 260 (i.e., writing of data). Here, charge for supply of a potential level or charge for supply of a different potential level (hereinafter referred to as Low level charge and High level charge) is given. After that, the potential of the fourth wiring is set to a potential at which the transistor 150 is turned off, so that the transistor 150 is turned off. Thus, the charge given to the gate electrode of the transistor 260 is held (holding).

[0195]

Since the amount of off-state current of the transistor 150 is significantly small, the charge of the gate electrode of the transistor 260 is held for a long time.

[0196]

Next, reading of data is described. By supplying an appropriate potential (reading potential) to the fifth wiring while a predetermined potential (constant potential) is supplied to the first wiring, the potential of the second wiring fluctuates depending on the amount of charge retained in the gate electrode of the transistor 260. This is because in general, when the transistor 260 is an n-channel transistor, an apparent threshold voltage $V_{\mathrm{th\_H}}$ in the case where High level charge is given to the gate electrode of the transistor 260 is lower than an apparent threshold voltage $V_{\mathrm{th\_L}}$ in the case where Low level charge is given to the gate electrode of the transistor 260. Here, an apparent threshold voltage refers to the potential of the fifth wiring, which is needed to turn on the transistor 260. Thus, the potential of the fifth wiring is set to a potential V_0 existing between $V_{\mathrm{th\_H}}$ and $V_{\mathrm{th\_L}}$, whereby charge given to the gate electrode of the transistor 260 can be determined. For example, in the case where High level charge is given in writing, when the potential of the fifth wiring is set to V_0 ($> V_{\mathrm{th\_H}}$), the transistor 260 is turned on. In the case where a low level charge is given in writing, even when the potential of the fifth wiring is set to V_0 ($< V_{\mathrm{th\_L}}$), the transistor 260 remains in an off state. Therefore, the stored data can be read by the potential of the second line.

[0197]

Note that in the case where memory cells are arrayed to be used, only data of desired memory cells needs to be read. In the case where data is not read out, a potential at which the transistor 260 is turned off regardless of the state of the gate electrode, that is, a potential lower than $V_{\mathrm{th\_H}}$ may be supplied to the fifth wiring. Alternatively, a potential at which the transistor 260 is turned on, that is, a potential higher than $V_{\mathrm{th\_L}}$ may be given to the fifth wiring regardless of the state of the gate electrode of the transistor 260.

[0198]

When a transistor having a channel formation region formed using an oxide semiconductor and having an extremely small amount of off-state current is applied to the semiconductor device in this embodiment, the semiconductor device can store data for an extremely long period. In other words, power consumption can be adequately reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be held for a long period even when power is not supplied (note that a potential is preferably fixed).

[0199]

Further, in the semiconductor device described in this embodiment, high voltage is not needed for writing data and there is no problem of deterioration of elements. For example, unlike a conventional non-volatile memory, it is not necessary to inject and extract electrons into and from a floating gate, and thus a problem of deterioration of a gate insulating layer does not occur at all. In other words, the semiconductor device according to one embodiment of the present invention does not have a limit on the number of times of writing which is a problem in a conventional nonvolatile memory, and reliability thereof is drastically improved. Furthermore, data is written depending on the on state and the off state of the transistor, whereby high-speed operation can be easily realized.

[0200]

Further, in the transistor 150, the concentration of impurities such as silicon entering the region 106a of the oxide semiconductor film 106 is reduced. In the case where the oxide semiconductor film 106 is a CAAC-OS film, a crystal portion can be formed even in the vicinity of the interface with the gate insulating film 110. As a result, the transistor 150 can have stable electric characteristics.

[0201]

Therefore, a semiconductor device in which miniaturization and high integration are achieved and which have excellent electric characteristics can be provided.

[0202]

The methods and structures described in this embodiment can be combined as appropriate with any of the methods and structures described in the other embodiments.

[0203]

(Embodiment 4)

In this embodiment, a semiconductor device which includes the transistor described in Embodiment 1 or 2, which can hold stored data even when not powered, and which does not have a limitation on the number of write cycles, and which has a structure different from the structure described in Embodiment 3 will be described with reference to FIGS. 7A and 7B.

[0204]

FIG. 7A is an example of a circuit configuration of a semiconductor device, and

FIG. 7B is a conceptual diagram illustrating an example of a semiconductor device. First, the semiconductor device illustrated in FIG. 7A will be described, and then, the semiconductor device illustrated in FIG. 7B will be described.

[0205]

In the semiconductor device illustrated in FIG. 7A, a bit line BL is electrically connected to a source electrode or a drain electrode of the transistor 150, a word line WL is electrically connected to a gate electrode of the transistor 150, and the source electrode or the drain electrode of the transistor 150 is electrically connected to a first terminal of a capacitor 354.

[0206]

Here, the off-state current of the transistor 150 using an oxide semiconductor is extremely small. For that reason, a potential of the first terminal of the capacitor 354 (or a charge accumulated in the capacitor 354) can be held for an extremely long period in the state where the transistor 150 is off.

[0207]

Next, writing and holding of data in the semiconductor device (a memory cell 350) illustrated in FIG. 7A will be described.

[0208]

First, the potential of the word line WL is set to a potential at which the transistor 150 is turned on, and the transistor 150 is turned on. Accordingly, the potential of the bit line BL is supplied to the first terminal of the capacitor 354 (writing). After that, the potential of the word line WL is set to a potential at which the transistor 150 is turned off, so that the transistor 150 is turned off. Thus, the potential of the first terminal of the capacitor 354 is held (holding).

[0209]

Because the off-state current of the transistor 150 is extremely small, the potential of the first terminal of the capacitor 354 (or the charge accumulated in the capacitor) can be held for a long time.

[0210]

Next, reading of data will be described. When the transistor 150 is turned on, the bit line BL which is in a floating state and the capacitor 354 are electrically connected to each other, and the charge is redistributed between the bit line BL and the capacitor 354. As a result, the potential of the bit line BL is changed. The amount of change in potential of the bit line BL fluctuates depending on the potential of the first terminal of the capacitor 354 (or the charge accumulated in the capacitor 354).

[0211]

For example, the potential of the bit line BL after charge redistribution is $(C_B \times V_{B0} + C \times V)/(C_B + C)$, where V is the potential of the first terminal of the capacitor 354, C is the capacitance of the capacitor 354, C_B is the capacitance of the bit line BL (hereinafter also referred to as bit line capacitance), and V_{B0} is the potential of the bit line BL before the charge redistribution. Therefore, it can be found that assuming that the memory cell 350 is in either of two states in which the potentials of the first terminal of the capacitor 354 are V_1 and V_0 ($V_1 > V_0$), the potential of the bit line BL in the case of holding the potential V_1 ($=(C_B \times V_{B0} + C \times V_1)/(C_B + C)$) is higher than the potential of the bit line BL in the case of holding the potential V_0 ($=(C_B \times V_{B0} + C \times V_0)/(C_B + C)$).

[0212]

Then, by comparing the potential of the bit line BL with a predetermined potential, data can be read.

[0213]

As described above, the semiconductor device illustrated in FIG. 7A can hold charge that is accumulated in the capacitor 354 for a long time because the off-state current of the transistor 150 is extremely small. In other words, power consumption can be adequately reduced because refresh operation becomes unnecessary or the frequency of refresh operation can be extremely low. Moreover, stored data can be held for a long time even when power is not supplied.

[0214]

Next, the semiconductor device illustrated in FIG. 7B is described.

[0215]

The semiconductor device illustrated in FIG. 7B includes memory cell arrays 351a and 351b including a plurality of memory cells 350 illustrated in FIG. 7A as a memory circuit in an upper portion, and a peripheral circuit 353 in a lower portion which is necessary for operation of the memory cell array 351 (the memory cell arrays 351a and 351b). Note that the peripheral circuit 353 is electrically connected to the memory cell array 351.

[0216]

In the structure illustrated in FIG. 7B, the peripheral circuit 353 can be provided directly below the memory cell array 351 (the memory cell arrays 351a and 351b). Thus, the size of the semiconductor device can be decreased.

[0217]

It is preferable that a semiconductor material of a transistor provided in the peripheral circuit 353 be different from that of the transistor 150. For example, silicon, germanium, silicon germanium, silicon carbide, gallium arsenide, or the like can be used, and a single crystal semiconductor is preferably used. Alternatively, an organic semiconductor material or the like may be used. A transistor including such a semiconductor material can operate at sufficiently high speed. Therefore, a variety of circuits (e.g., a logic circuit or a driver circuit) which needs to operate at high speed can be favorably realized by the transistor.

[0218]

Note that FIG. 7B illustrates, as an example, the semiconductor device in which two memory cell arrays 351 (the memory cell arrays 351a and 351b) are stacked; however, the number of memory cell arrays to be stacked is not limited thereto. Three or more memory cell arrays may be stacked.

[0219]

A semiconductor device having a novel feature can be obtained by being provided with both a peripheral circuit including the transistor including a material other than an oxide semiconductor (in other words, a transistor capable of operating at sufficiently high speed) and a memory circuit including the transistor including an oxide semiconductor (in a broader sense, a transistor whose off-state current is sufficiently small). In addition, with a structure where the peripheral circuit and the memory circuit are stacked, the degree of integration of the semiconductor device can be increased.

[0220]

This embodiment can be implemented in appropriate combination with the structures described in the other embodiments.

[0221]

(Embodiment 5)

In this embodiment, examples of application of the semiconductor device described in any of the above embodiments to portable devices such as mobile phones, smartphones, or electronic books will be described with reference to FIGS. 8A and 8B, FIG. 9, FIG. 10, and FIG. 11.

[0222]

In portable electronic devices such as a mobile phone, a smart phone, and an e-book reader, an SRAM or a DRAM is used so as to store image data temporarily. This is because response speed of a flash memory is low and thus a flash memory is not suitable for image processing. On the other hand, an SRAM or a DRAM has the following characteristics when used for temporary storage of image data.

[0223]

In an ordinary SRAM, as shown in FIG. 8A, one memory cell includes six transistors, that is, transistors 801 to 806, which are driven with an X decoder 807 and a Y decoder 808. The transistors 803 and 805 and the transistors 804 and 806 each serve as an inverter, and high-speed driving can be performed therewith. However, an SRAM has a disadvantage of large cell area because one memory cell includes six transistors. Provided that the minimum feature size of a design rule is F, the area of a memory cell in an SRAM is generally 100 F^2 to 150 F^2. Therefore, a price per bit of an SRAM is the most expensive among a variety of memory devices.

[0224]

In a DRAM, as shown in FIG. 8B, a memory cell includes a transistor 811 and a storage capacitor 812, which are driven with an X decoder 813 and a Y decoder 814. One cell includes one transistor and one capacitor and thus the area of a memory cell is small. The area of a memory cell of a DRAM is generally less than or equal to 10 F^2. Note that in the case of a DRAM, a refresh operation is always necessary and power is consumed even when a rewriting operation is not performed.

[0225]

However, the area of the memory cell of the semiconductor device described in the above embodiments is about 10 F^2 and frequent refreshing is not needed. Therefore, the area of the memory cell is reduced, and the power consumption can be reduced.

[0226]

Next, FIG. 9 is a block diagram of a portable device. The portable device illustrated in FIG. 9 includes an RF circuit 901, an analog baseband circuit 902, a digital baseband circuit 903, a battery 904, a power supply circuit 905, an application processor 906, a flash memory 910, a display controller 911, a memory circuit 912, a display 913, a touch sensor 919, an audio circuit 917, a keyboard 918, and the like. The display 913 includes a display portion 914, a source driver 915, and a gate driver 916. The application processor 906 includes a CPU 907, a DSP 908, and an interface 909 (IF 909). In general, the memory circuit 912 includes an SRAM or a DRAM; by employing the semiconductor device described in any of the above embodiments for the memory circuit 912, writing and reading of data can be performed at high speed, data can be held for a long time, and power consumption can be sufficiently reduced.

[0227]

FIG. 10 illustrates an example of using the semiconductor device described in any of the above embodiments in a memory circuit 950 for a display. The memory circuit 950 illustrated in FIG. 10 includes a memory 952, a memory 953, a switch 954, a switch 955, and a memory controller 951. Further, the memory circuit is connected to a display controller 956 which reads and controls image data (input image data) input through a signal line and data stored in the memories 952 and 953 (stored image data), and is also connected to a display 957 which displays an image based on a signal from the display controller 956.

[0228]

First, image data (input image data A) is formed by an application processor (not shown). The input image data A is held in the memory 952 though the switch 954. The image data (stored image data A) held in the memory 952 is transmitted to the display 957 through the switch 955 and the display controller 956 and displayed.

[0229]

In the case where the input image data A is not changed, the stored image data A is read from the memory 952 through the switch 955 by the display controller 956 normally with a frequency of 30 Hz to 60 Hz.

[0230]

Next, for example, when data displayed on the screen is rewritten by a user (that is, in the case where the input image data A is changed), new image data (input image data B) is formed by the application processor. The input image data B is held in the memory 953 through the switch 954. The stored image data A is read periodically from the memory 952 through the switch 955 even during that time. After the completion of storing the new image data (the stored image data B) in the memory 953, from the next frame for the display 957, the stored image data B starts to be read, transmitted to the display 957 through the switch 955 and the display controller 956, and displayed on the display 957. This reading operation is continued until another new image data is held in the memory 952.

[0231]

Accordingly, image data is alternately written and read in the memories 952 and 953, so that the image data is displayed on the display 957. The memories 952 and 953 are not necessarily different memories, and a memory region included in one memory may be divided to be used. By employing the semiconductor device described in any of the above embodiments for the memory 952 and the memory 953, data can be written and read at high speed and held for a long time, and power consumption can be sufficiently reduced.

[0232]

FIG. 11 is a block diagram of an e-book reader. FIG. 11 includes a battery 1001, a power supply circuit 1002, a microprocessor 1003, a flash memory 1004, an audio circuit 1005, a keyboard 1006, a memory circuit 1007, a touch panel 1008, a display 1009, and a display controller 1010.

[0233]

Here, the semiconductor device described in any of the above embodiments can be used for the memory circuit 1007 in FIG. 11. The memory circuit 1007 has a function of temporarily storing the contents of a book. For example, users use a highlight function in some cases. When users read an e-book reader, they sometimes want to mark a specified place. This marking refers to a highlight function, and users can make difference from other places by, for example, changing the color of a letter displayed, underlining a word, making a letter bold, or changing the font type of a letter. That is, this is a function of storing and holding data of a place specified by users. In order to save data for a long time, the data may be copied into the flash memory 1004.

Even in such a case, by employing the semiconductor device described in any of the above embodiments, writing and reading of data can be performed at high speed, data can be held for a long time, and power consumption can be sufficiently reduced.

[0234]

As described above, the semiconductor device in any of the above embodiments is mounted on each of the portable devices described in this embodiment. Therefore, a portable device in which writing and reading of data are performed at high speed, data is held for a long time, and power consumption is sufficiently reduced, can be obtained.

[0235]

The structures, methods, and the like described in this embodiment can be combined as appropriate with any of the other structures, methods, and the like described in the other embodiments.

[Example]

[0236]

In this example, the characteristics of an oxide semiconductor film to which silicon (Si) was intentionally added were evaluated. The evaluation method will be described in detail below.

[0237]

First, the oxide semiconductor film was formed with a sputtering apparatus. Thus, Si was intentionally added to a metal oxide target used for sputtering. As a metal oxide target, a target in which SiO_2 was added to an In-Ga-Zn-based oxide (hereinafter, IGZO) was formed. In other words, an In-Ga-Zn-Si-based oxide target was formed.

[0238]

In this example, three IGZO targets were formed: Target A in which SiO_2 was added at 2 wt.% to a target with a composition ratio where In: Ga: Zn = 1:1:1 [atomic ratio]; Target B in which SiO_2 was added at 5 wt.% to a target with a composition ratio where In: Ga: Zn = 1:1:1 [atomic ratio]; and Target C (In: Ga: Zn = 1:1:1 [atomic ratio]) to which SiO_2 was not added.

[0239]

Note that in some cases, a thin film formed using Target A is referred to as IGZO-SiO$_x$ (2 wt.%), a thin film formed using Target B is referred to as IGZO-SiO$_x$ (5 wt.%), and a thin film formed using Target C is referred to as IGZO.

[0240]

Next, thin oxide semiconductor films were formed using Target A, Target B, and Target C, and their characteristics were evaluated. For evaluation, sheet resistance, composition, and crystallinity of the obtained thin films were measured and analyzed.

[0241]

(Sheet Resistance Measurement)

Samples 1 to 6 were manufactured. Sample 1 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target C by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 10/5 sccm (O_2 = 33 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 2 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target C by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 3 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 10/5 sccm (O_2 = 33 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 4 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour;

and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 5 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 10/5 sccm (O_2 = 33 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 6 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour.

[0242]

Each thickness of the oxide semiconductor films in Samples 1 to 6 was 100 nm. The deposition conditions of manufactured samples, structures thereof, and the like are shown in Table 1.

[0243]

[Table 1]

	Target	Deposition Condition	Sample Structure	Heat Treatment
Sample 1	Target C	Ar/O_2=10/5sccm (O_2=33%)	Glass\IGZO=100nm	450°C
Sample 2	Target C	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO=100nm	450°C
Sample 3	Target A	Ar/O_2=10/5sccm (O_2=33%)	Glass\IGZO-SiO_x(2wt%)= 100nm	450°C
Sample 4	Target A	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(2wt%)= 100nm	450°C
Sample 5	Target B	Ar/O_2=10/5sccm (O_2=33%)	Glass\IGZO-SiO_x(5wt%)= 100nm	450°C
Sample 6	Target B	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(5wt%)= 100nm	450°C

[0244]

Next, sheet resistance of Samples 1 to 6 was measured. Note that for sheet resistance measurement, a sheet resistance measurement system was used. FIG. 17 shows measurement results of sheet resistance of Samples 1 to 6. In FIG. 17, the horizontal axis indicates objects (formed thin films), and the vertical axis indicates sheet resistance.

[0245]

As can be seen from FIG. 17, sheet resistance of thin films is increased by adding Si to IGZO. In particular, the sheet resistance of Sample 5 exceeded the measurement upper limit (5×10^5 Ω/cm^2) of the measurement system and thus it was impossible to measure the sheet resistance value. Note that although the sheet resistance of Sample 6 also exceeded the measurement upper limit of the measurement system, the value around the upper limit of the measurement system was calculated in principle. However, the value of the upper limit of the measurement system is not always measured accurately.

[0246]

(Composition Analysis)

Samples 7 and 8 were manufactured. Sample 7 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %). Sample 8 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %).

[0247]

Each thickness of the oxide semiconductor films in Samples 7 and 8 was 100 nm.

[0248]

Next, composition analysis was performed on Samples 7 and 8. For composition analysis, X-ray photoelectron spectroscopy (XPS) was used. XPS is a measurement method by which photoelectron energy generated by irradiating a surface of sample with X-ray is measured, so that a constituent element of the sample and the electron state thereof can be analyzed. Table 2 shows deposition conditions, structures, and composition analysis of Samples 7 and 8.

[0249]

[Table 2]

	Target	Deposition Condition	Sample Structure	Composition Analysis Result [unit: at.%]				
				In	Ga	Zn	O	Si
Sample 7	Target A	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(2 wt%)=100nm	18.0	15.3	4.6	61.0	1.1
Sample 8	Target B	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(5 wt%)=100nm	16.7	14.4	4.3	62.0	2.6

[0250]

According to Table 2, Sample 7 formed with use of Target A has such composition that In = 18.0 (at.%), Ga = 15.3 (at.%), Zn = 4.6 (at.%), O = 61.0 (at.%), and Si = 1.1 (at.%); Sample 8 formed with use of Target B has such composition that In = 16.7 (at.%), Ga = 14.4 (at.%), Zn = 4.3 (at.%), O = 62.0 (at.%), and Si = 2.6 (at.%).

[0251]

(Crystallinity Analysis)

Samples 9 to 14 were manufactured. Sample 9 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %). Sample 10 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 11 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target A by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 650 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 650 °C was conducted in an oxygen atmosphere for one hour. Sample 12 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %). Sample 13 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 450 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 450 °C was conducted in an oxygen atmosphere for one hour. Sample 14 was formed in the following manner: an oxide semiconductor film was formed over a glass substrate with use of Target B by a sputtering method under conditions that power = 100 W, pressure = 0.4 Pa, substrate temperature = 200 °C, and Ar/O_2 = 0/15 sccm (O_2 = 100 %); heat treatment at 650 °C was conducted on the oxide semiconductor film in a nitrogen atmosphere for one hour; and then heat treatment at 650 °C was conducted in an oxygen atmosphere for one hour.

[0252]

Each thickness of the oxide semiconductor films in Samples 9 to 14 was 100 nm. Table 3 shows deposition conditions of the manufactured samples, structures thereof, and the like. Note that Samples 9 to 11 are oxide semiconductor films each of which has composition similar to that of Sample 7, and Samples 12 to 14 are oxide semiconductor films each of which has composition similar to that of Sample 8.

[0253]

[Table 3]

	Target	Deposition Condition	Sample Structure	Heat Treatment
Sample 9	Target A	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(2wt%)= 100nm	No
Sample 10	Target A	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(2wt%)= 100nm	450°C
Sample 11	Target A	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(2wt%)= 100nm	650°C
Sample 12	Target B	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(5wt%)= 100nm	No
Sample 13	Target B	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(5wt%)= 100nm	450°C
Sample 14	Target B	Ar/O_2=0/15sccm (O_2=100%)	Glass\IGZO-SiO_x(5wt%)= 100nm	650°C

[0254]

Next, crystallinity of Samples 9 to 14 was analyzed. For analysis of crystallinity, X-ray diffraction (XRD) was used. XRD is a phenomenon in which a X-ray is diffracted at a crystal lattice, so that crystallinity of samples for measurement can be measured. FIG. 18A shows crystallinity analysis results of Samples 9 to 11, and FIG. 18B shows crystallinity analysis results of Samples 12 to 14.

[0255]

As can be seen from FIG. 18A showing analysis results of Samples 9 to 11 formed with use of Target A, Sample 9 on which heat treatment was not performed and Sample 10 on which heat treatment at 450 °C was performed have no diffraction peak showing definite crystallinity. On the other hand, in the case of Sample 11 on which heat treatment at 650 °C was performed, a diffraction peak showing crystallinity is observed around at $2\theta = 31°$.

[0256]

Further, as can be seen from FIG. 18B showing analysis results of Samples 12 to 14 formed with use of Target B, a diffraction peak showing definite crystallinity is not observed in any of Sample 12 on which heat treatment was not performed, Sample 13 on which heat treatment at 450 °C was performed, and Sample 14 on which heat treatment at 650 °C was performed.

[0257]

According to the above results, in each of Samples 9 to 11 formed with use of Target A, the concentration of silicon (Si) in the oxide semiconductor film is 1.1 at.%; in each of Samples 12 to 14 formed with use of Target B, the concentration of silicon (Si) in the oxide semiconductor film is 2.6 at.%. As a result, it is found that crystallinity of the oxide semiconductor film is inhibited when the concentration of Si in the oxide semiconductor film is high.

EXPLANATION OF REFERENCE

[0258]

102: substrate, 104: base insulating film, 106: oxide semiconductor film, 106a: region, 106b: region, 106c: region, 106d: region, 106e: region, 106f: region, 106g: region, 106h: region, 108a: source electrode, 108b: drain electrode, 110: gate insulating film, 112: gate electrode, 113: oxide semiconductor film, 114: interlayer insulating film, 150: transistor, 160: transistor, 180: insulating film, 181: dopant, 182: conductive film, 184: insulating film, 186: wiring, 200: substrate, 206: element isolation insulating film, 208: gate insulating film, 210: gate electrode, 216: channel formation region, 220: impurity region, 224: intermetallic compound region, 228: insulating film, 230: insulating film, 254: capacitor, 260: transistor, 264: capacitor, 350: memory cell, 351: memory cell array, 351a: memory cell array, 351b: memory cell array, 353: peripheral circuit, 354: capacitor, 801: transistor, 803: transistor, 804: transistor, 805: transistor, 806: transistor, 807: X decoder, 808: Y decoder, 811: transistor, 812: storage capacitor, 813: X decoder, 814: Y decoder, 901: RF circuit, 902: analog baseband circuit, 903: digital baseband circuit, 904: battery, 905: power supply circuit, 906: application processor, 907: CPU, 908: DSP, 909: interface, 910: flash memory, 911: display controller, 912: memory circuit, 913: display, 914: display portion, 915: source driver, 916: gate driver, 917:

audio circuit, 918: keyboard, 919: touch sensor, 950: memory circuit, 951: memory controller, 952: memory, 953: memory, 954: switch, 955: switch, 956: display controller, 957: display, 1001: battery, 1002: power supply circuit, 1003: microprocessor, 1004: flash memory, 1005: audio circuit, 1006: keyboard, 1007: memory circuit, 1008: touch panel, 1009: display, 1010: display controller

This application is based on Japanese Patent Application serial no. 2011-227022 filed with Japan Patent Office on October 14, 2011, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising:

an oxide semiconductor film over a substrate;

a source electrode and a drain electrode over the oxide semiconductor film;

a gate insulating film over the oxide semiconductor film, wherein the gate insulating film comprises an oxide containing silicon; and

a gate electrode over the gate insulating film,

wherein the oxide semiconductor film comprises a region in which a concentration of silicon is lower than or equal to 1.0 at.%,

wherein the region is located at an interface between the oxide semiconductor film and the gate insulating film and in contact with the gate insulating film, and

wherein the region comprises a crystal portion.

2. The semiconductor device according to claim 1, wherein an end portion of the oxide semiconductor film is tapered at an angle of 20° to 50°.

3. The semiconductor device according to claim 1, wherein the oxide semiconductor film except the region comprises a second crystal portion.

4. The semiconductor device according to claim 1, further comprising a base insulating film between the substrate and the oxide semiconductor film,

wherein in the crystal portion, a c-axis is aligned in a direction perpendicular to an interface between the base insulating film and the oxide semiconductor film.

5. The semiconductor device according to claim 1, wherein the concentration of silicon in the region is lower than or equal to 0.1 at.%.

6. The semiconductor device according to claim 1, further comprising an interlayer insulating film over the gate insulating film and the gate electrode.

7. A semiconductor device comprising:

an oxide semiconductor film over a substrate;

a source electrode and a drain electrode over the oxide semiconductor film;

a gate insulating film over the oxide semiconductor film, wherein the gate insulating film comprises an oxide containing silicon; and

a gate electrode over the gate insulating film,

wherein the oxide semiconductor film comprises a region in which a concentration of silicon is lower than or equal to 1.0 at.% and a concentration of carbon is lower than or equal to 1.0×10^{20} atoms/cm^3,

wherein the region is located at an interface between the oxide semiconductor film and the gate insulating film and in contact with the gate insulating film, and

wherein the region comprises a crystal portion.

8. The semiconductor device according to claim 7, wherein an end portion of the oxide semiconductor film is tapered at an angle of 20° to 50°.

9. The semiconductor device according to claim 7, wherein the oxide semiconductor film except the region comprises a second crystal portion.

10. The semiconductor device according to claim 7, further comprising a base insulating film between the substrate and the oxide semiconductor film,

wherein in the crystal portion, a c-axis is aligned in a direction perpendicular to an interface between the base insulating film and the oxide semiconductor film.

11. The semiconductor device according to claim 7, wherein the concentration of silicon in the region is lower than or equal to 0.1 at.%.

12. The semiconductor device according to claim 7, further comprising an interlayer insulating film over the gate insulating film and the gate electrode.

13. A semiconductor device comprising:

an oxide semiconductor film over a substrate;

a source electrode and a drain electrode over the oxide semiconductor film;

a gate insulating film over the oxide semiconductor film, wherein the gate insulating film comprises an oxide containing silicon; and

a gate electrode over the gate insulating film,

wherein the oxide semiconductor film comprises a region in which a concentration of silicon is lower than or equal to 1.0 at.% and a concentration of carbon is lower than or equal to 1.0×10^{20} atoms/cm^3,

wherein the region is located at an interface between the oxide semiconductor film and the gate insulating film and in contact with the gate insulating film,

wherein the region comprises a crystal portion, and

wherein the region has a thickness less than or equal to 5 nm.

14. The semiconductor device according to claim 13, wherein an end portion of the oxide semiconductor film is tapered at an angle of 20° to 50°.

15. The semiconductor device according to claim 13, wherein the oxide semiconductor film except the region comprises a second crystal portion.

16. The semiconductor device according to claim 13, further comprising a base insulating film between the substrate and the oxide semiconductor film,

wherein in the crystal portion, a c-axis is aligned in a direction perpendicular to an interface between the base insulating film and the oxide semiconductor film.

17. The semiconductor device according to claim 13, wherein the concentration of silicon in the region is lower than or equal to 0.1 at.%.

18. The semiconductor device according to claim 13, further comprising an interlayer insulating film over the gate insulating film and the gate electrode.

FIG. 1A

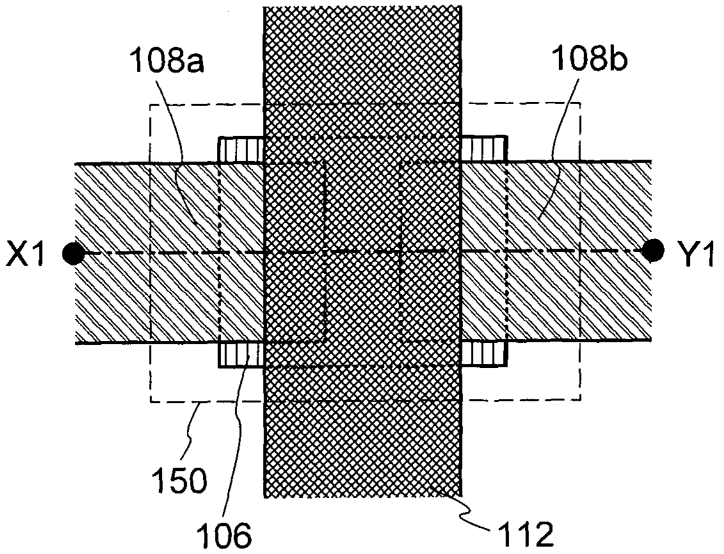
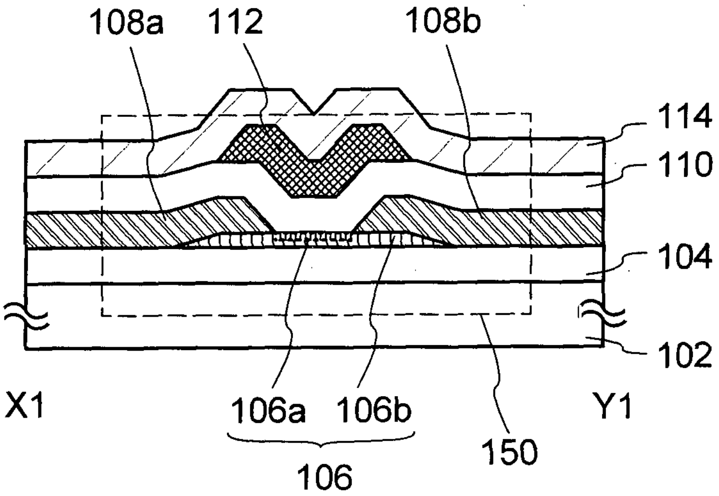

108a
108b
X1
Y1
150
106
112

FIG. 1B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112
108b
114
110
104
102
X1
106a
106b
106
150
Y1

FIG. 2A

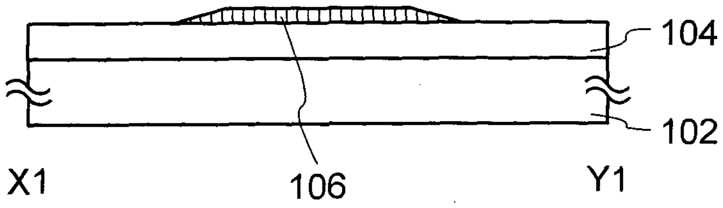


FIG. 2B

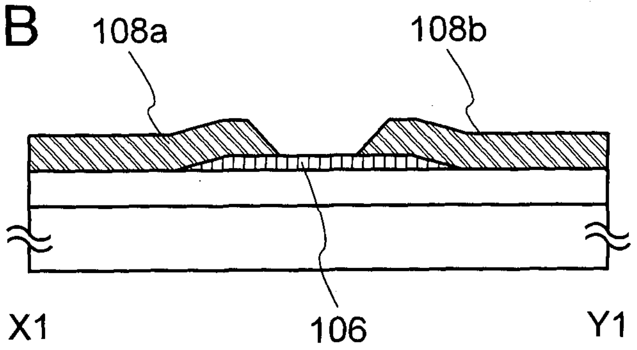


FIG. 2C

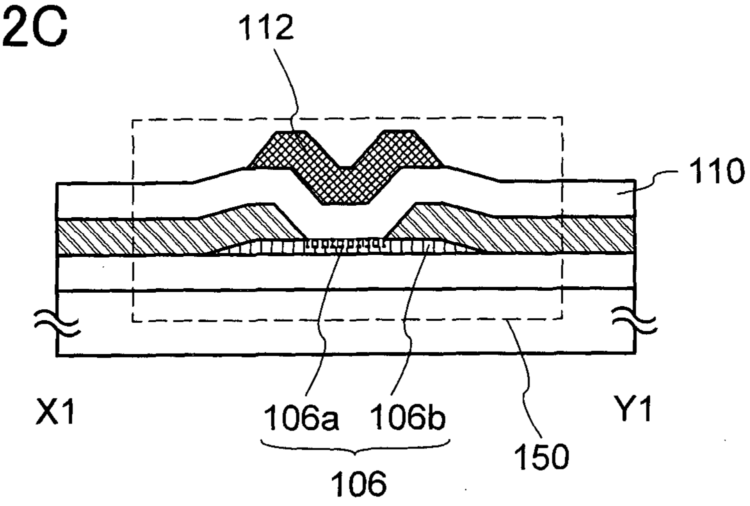


FIG. 2D

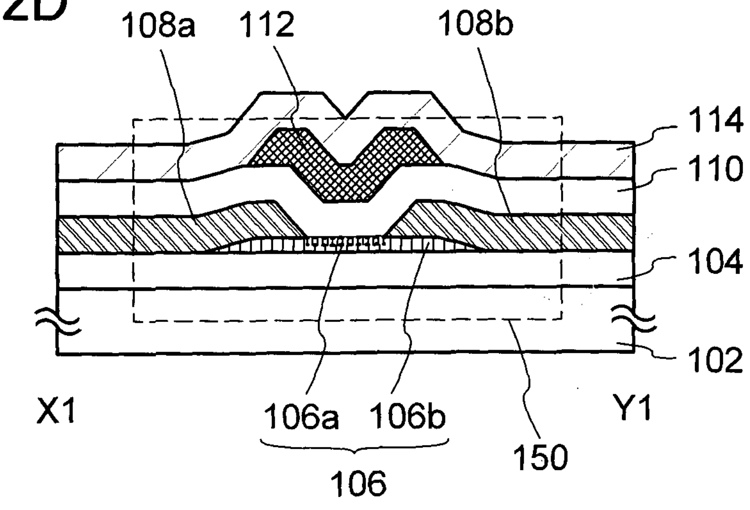


FIG. 3A

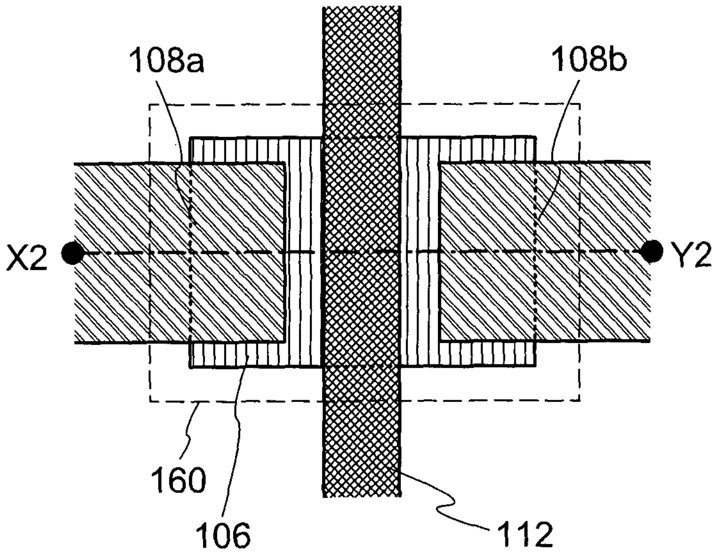

108a
108b
X2
Y2
160
106
112

FIG. 3B

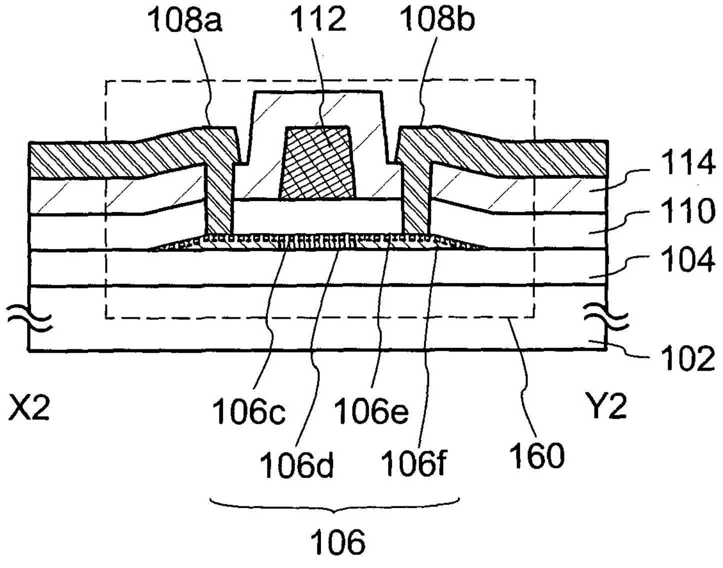

108a
112
108b
114
110
104
102
X2
106c
106e
Y2
106d
106f
160
106

FIG. 4A

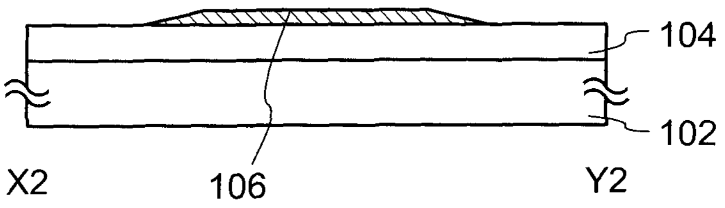


FIG. 4B

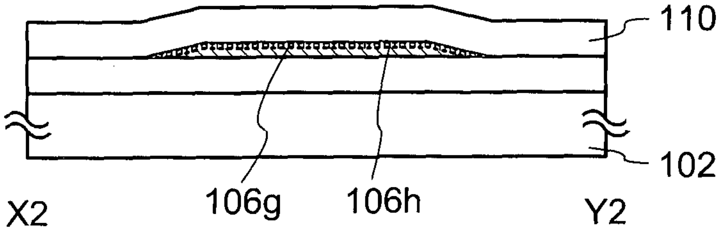


FIG. 4C

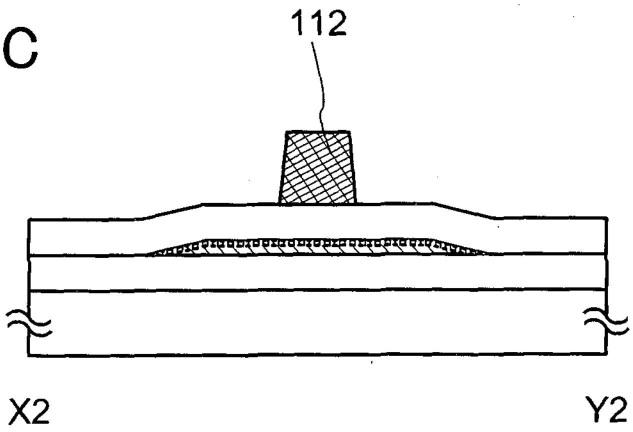


FIG. 4D

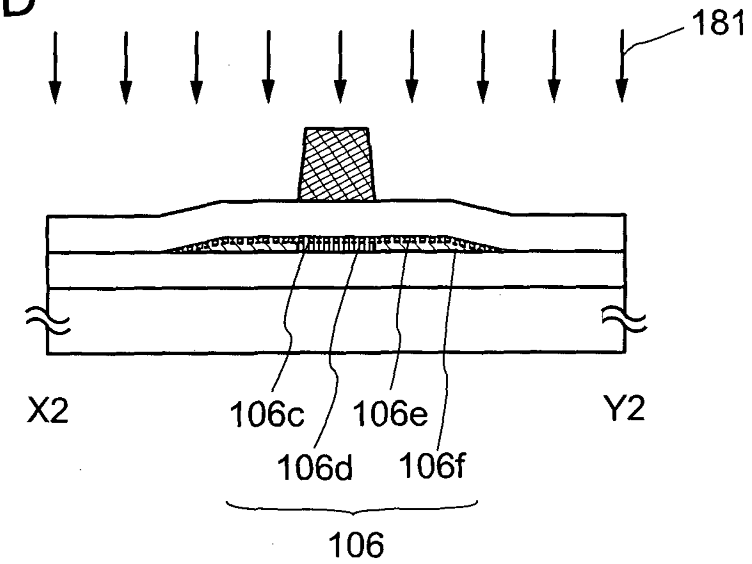


FIG. 5A

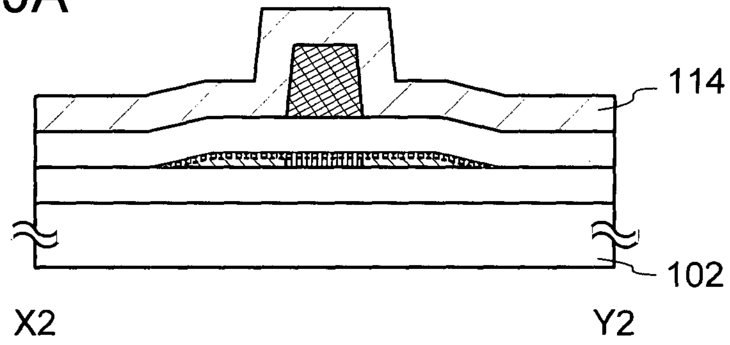

114
102
X2
Y2

FIG. 5B

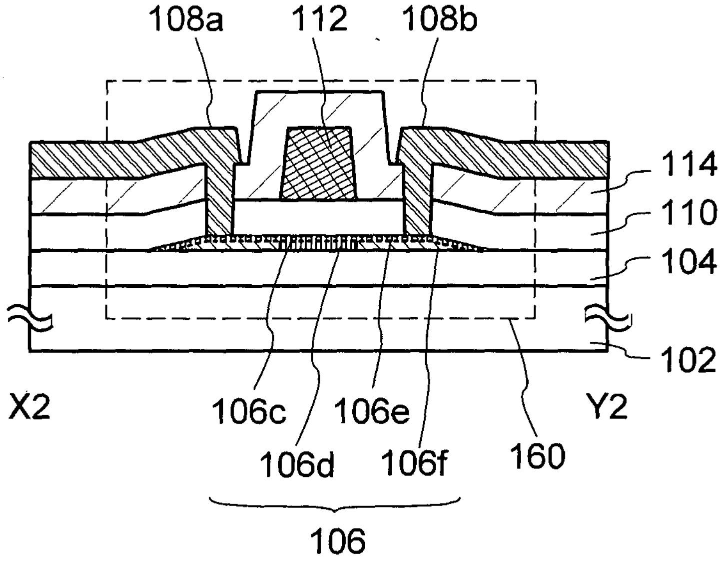

108a
112
108b
114
110
104
102
X2
Y2
106c
106e
106d
106f
160
106

FIG. 6A

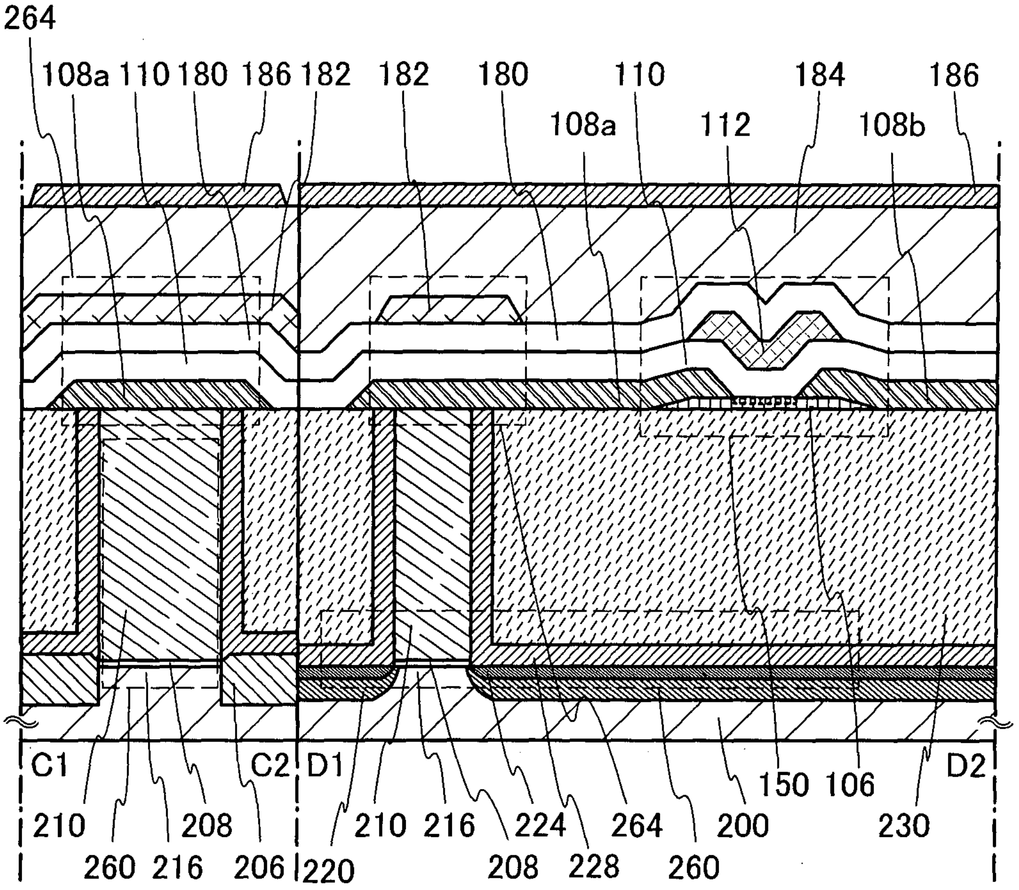


FIG. 6B

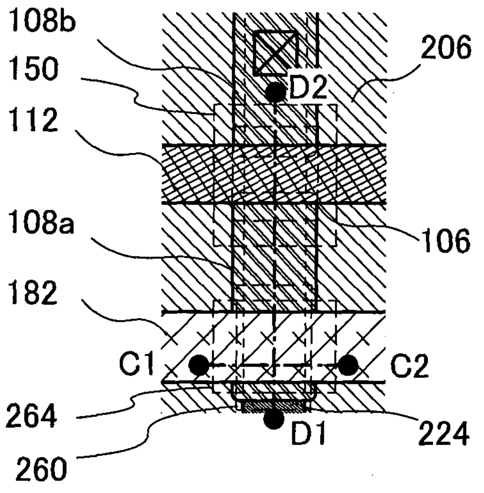


FIG. 6C

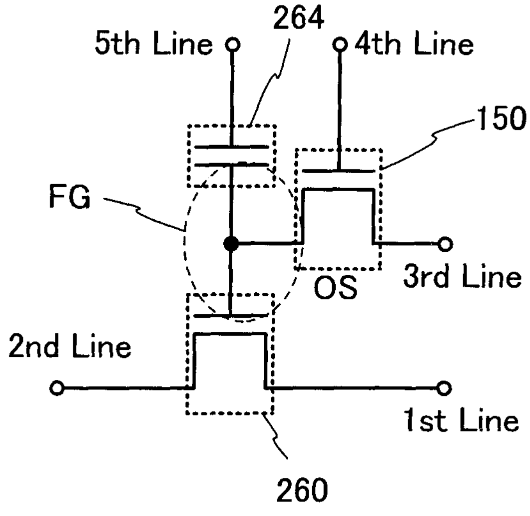


FIG. 7A

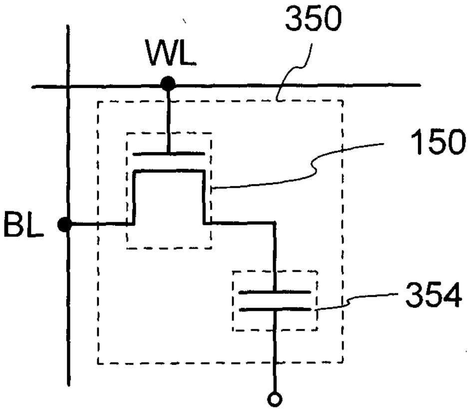


FIG. 7B

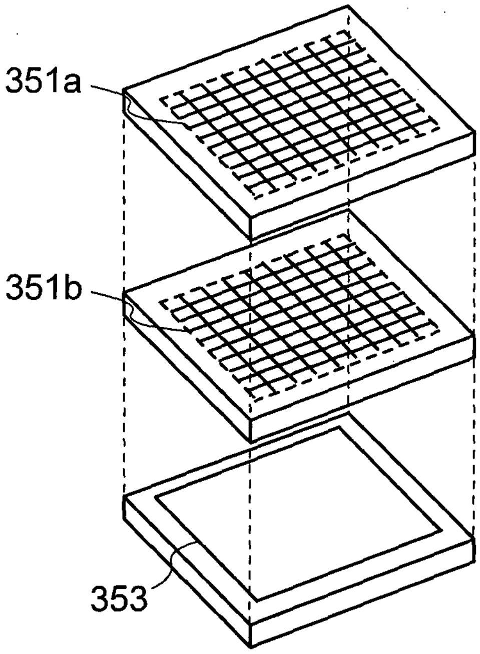


FIG. 8A

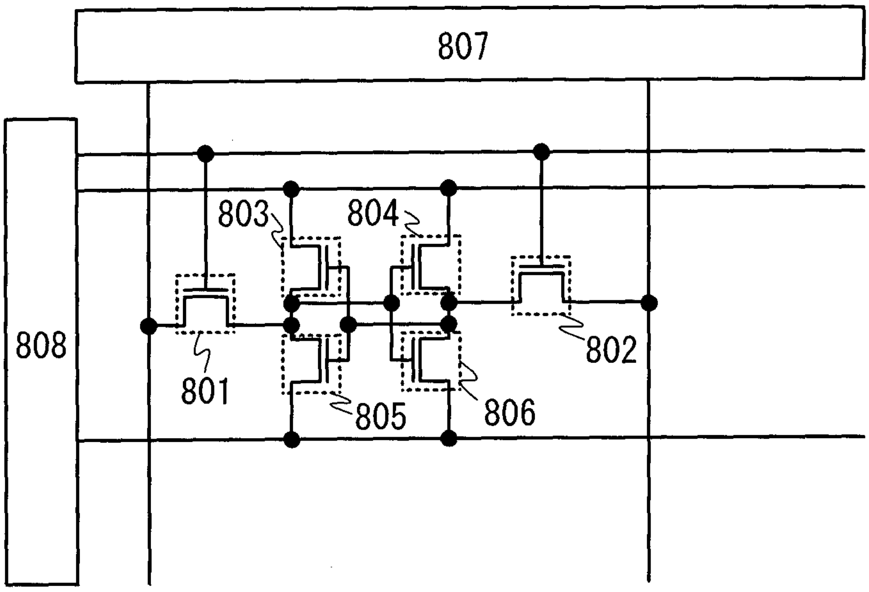


FIG. 8B

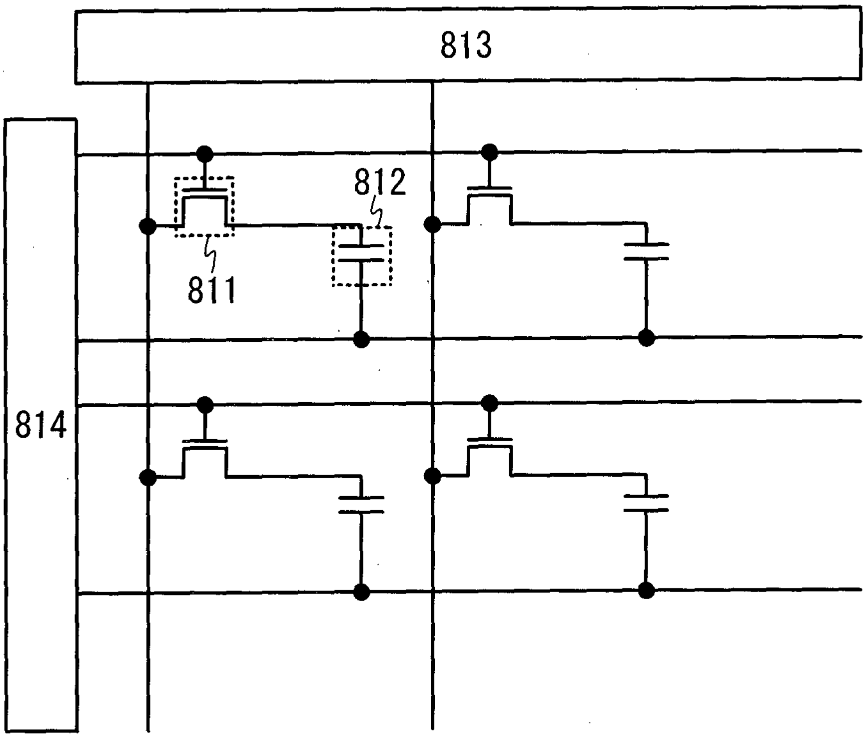


FIG. 9

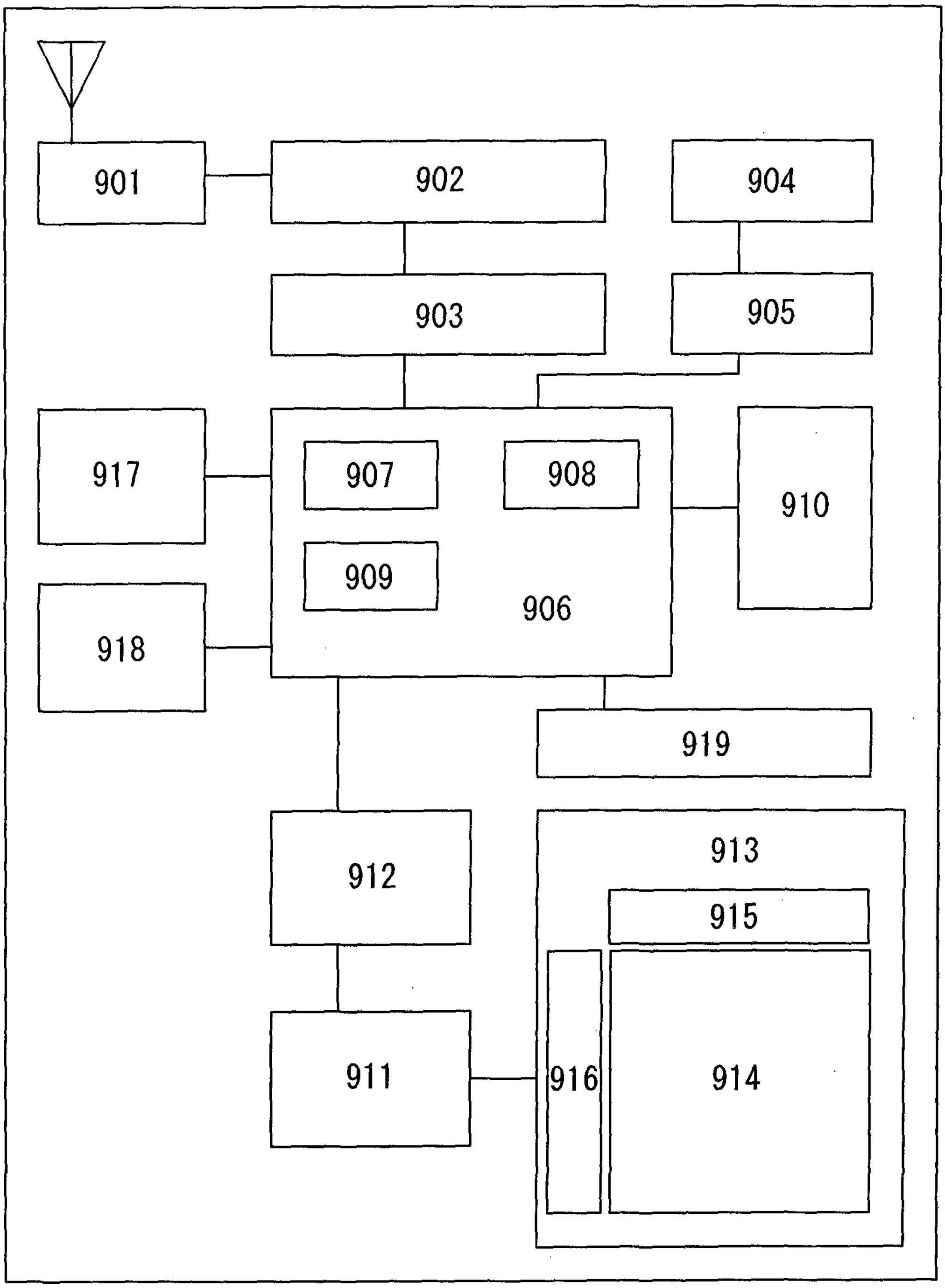

901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919

FIG. 10

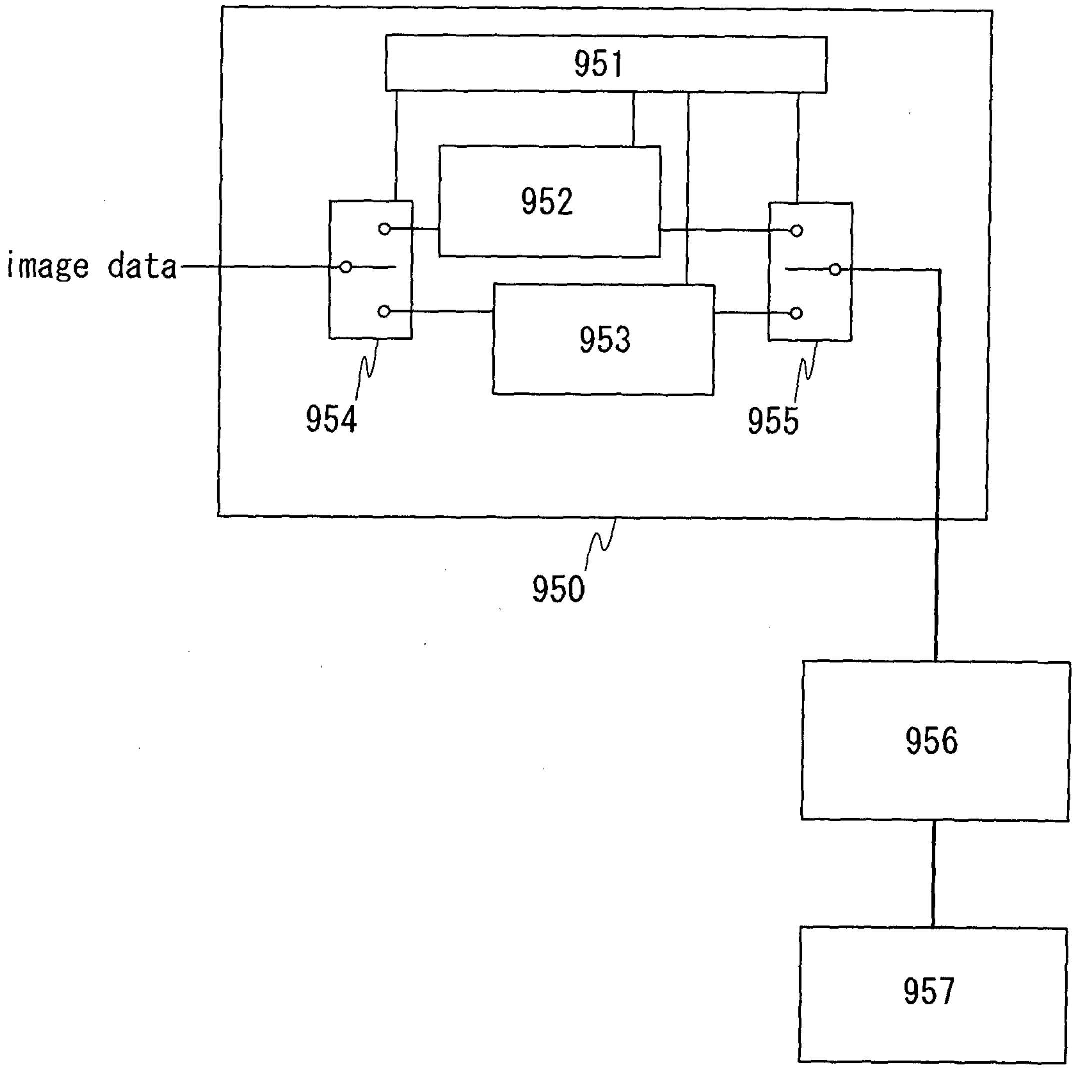


FIG. 11

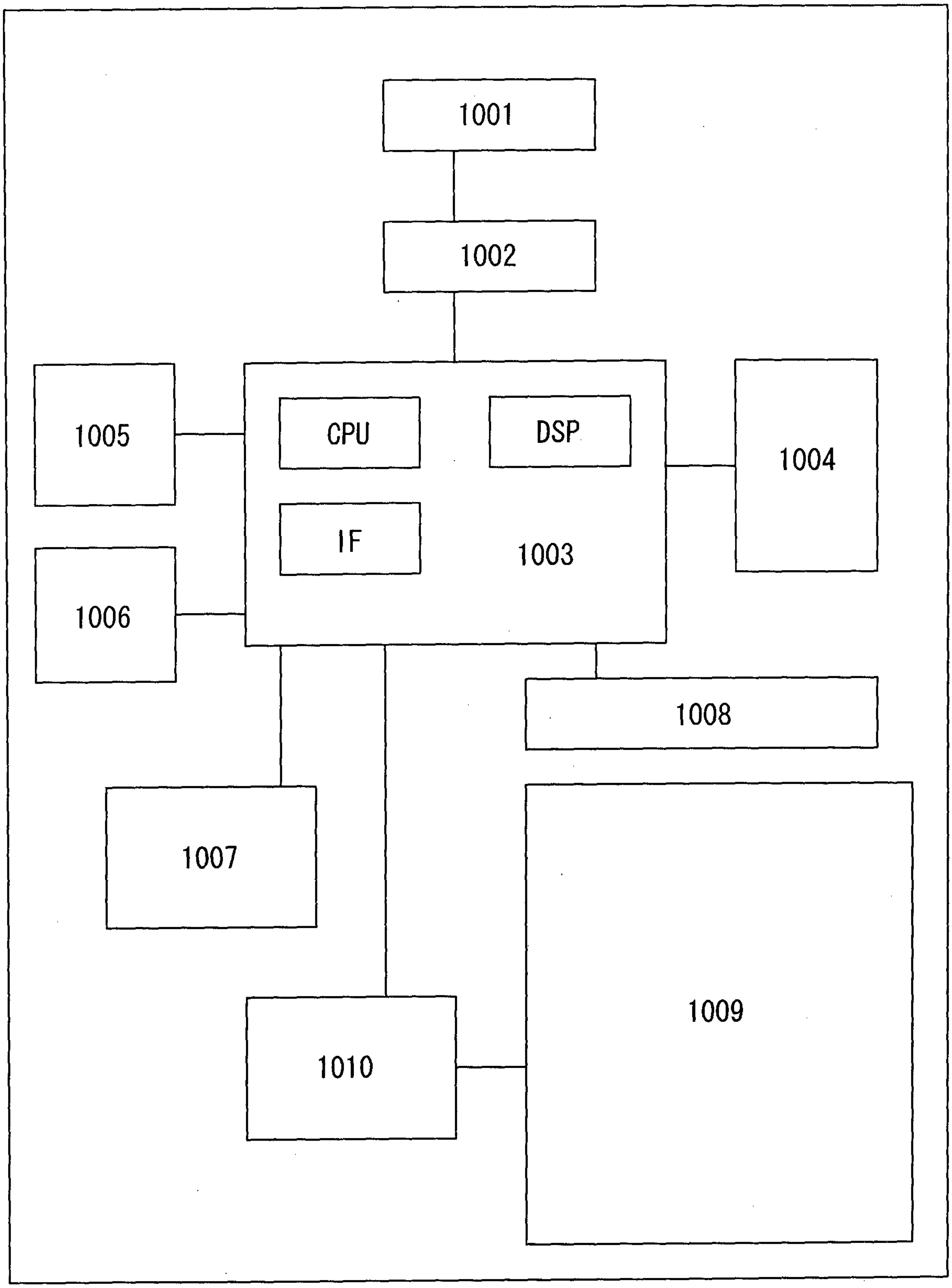


FIG. 12A

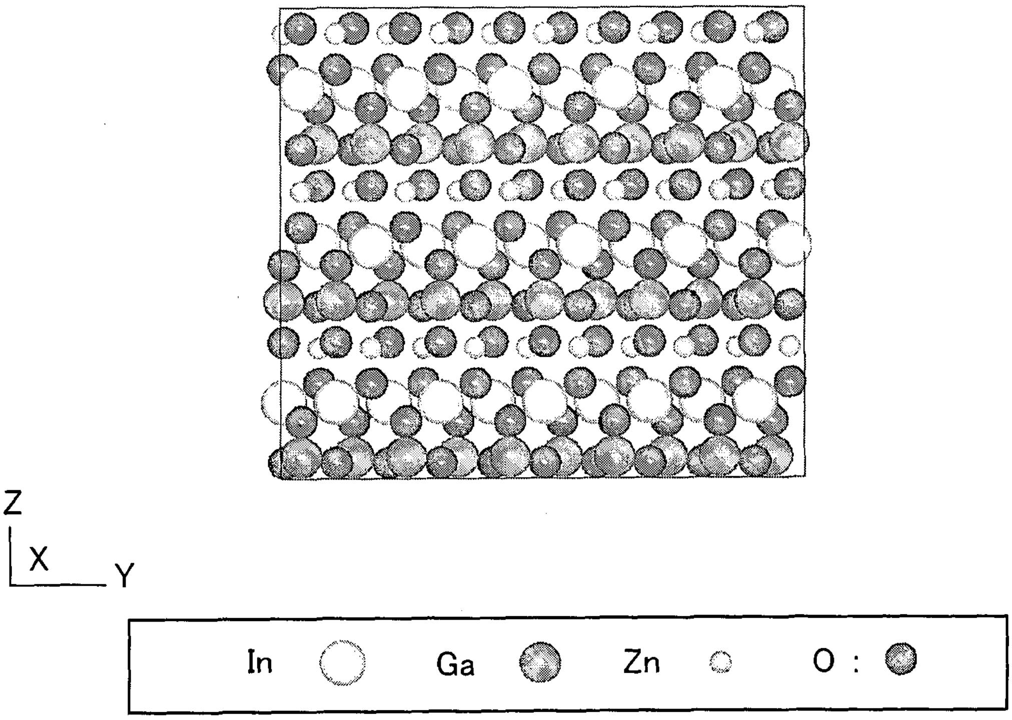


FIG. 12B

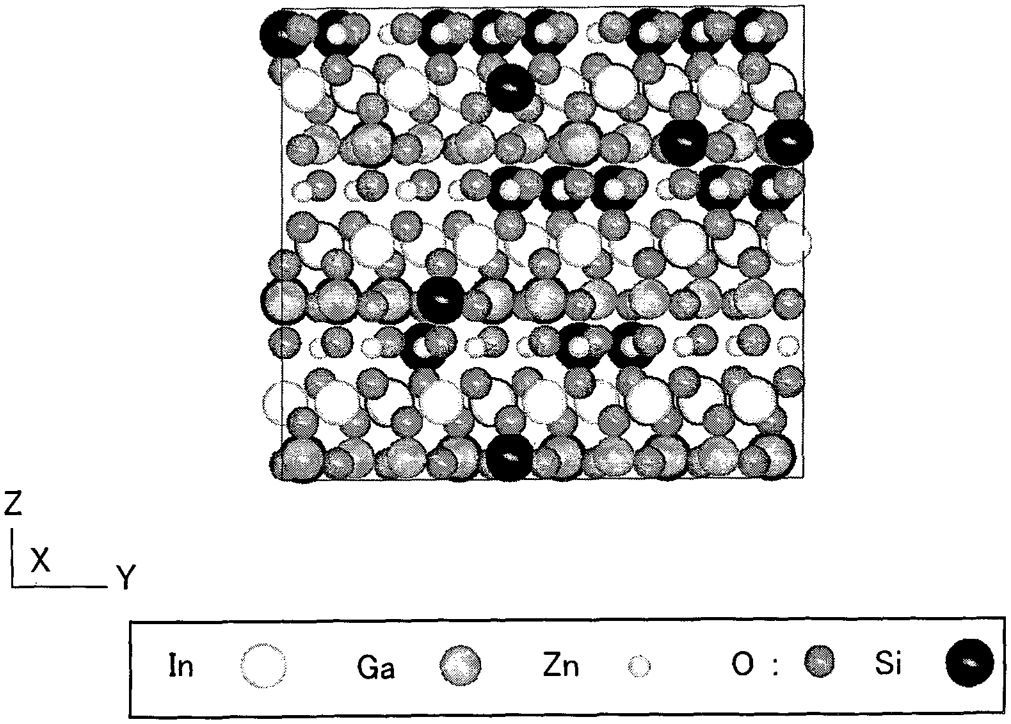


FIG. 13A

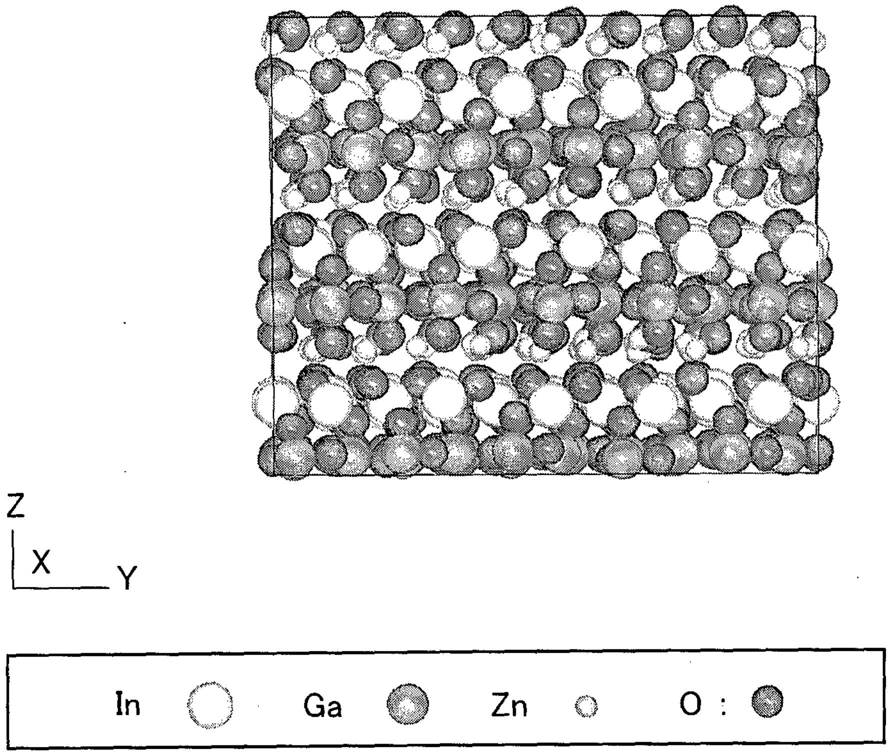


FIG. 13B

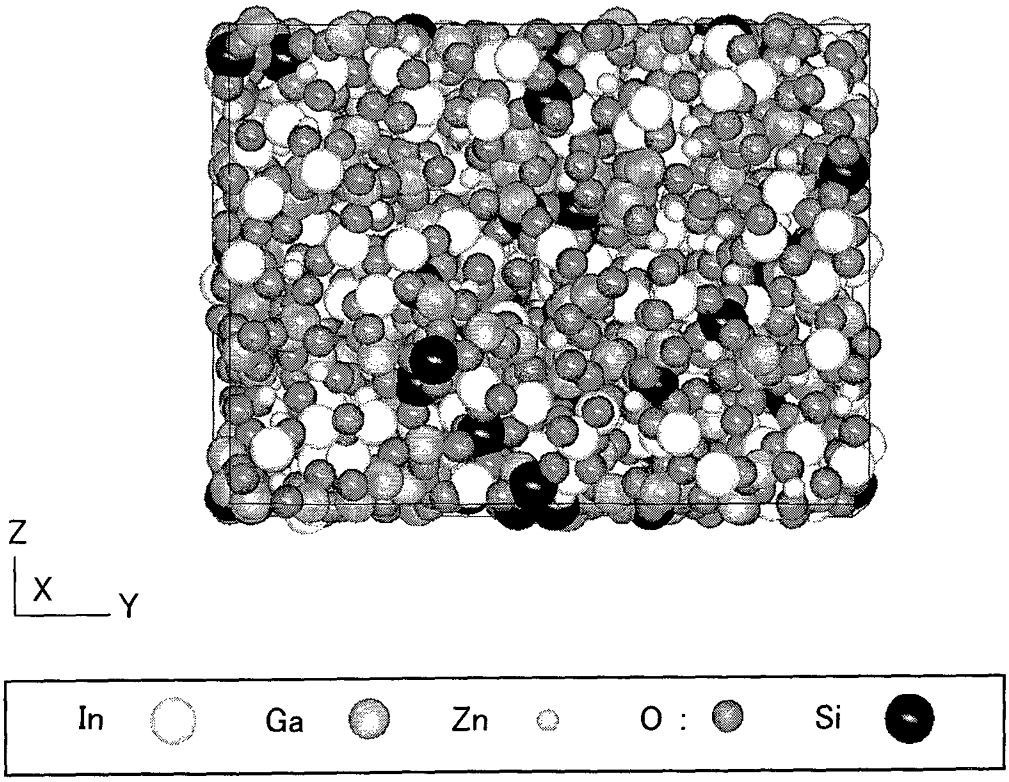


FIG. 14

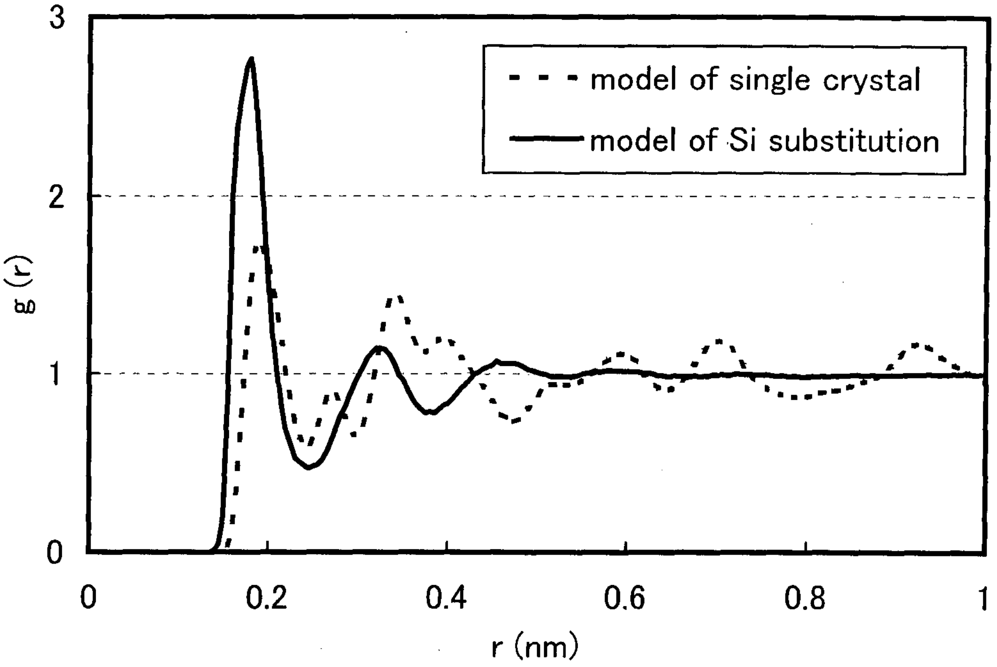

model of single crystal
model of Si substitution
g (r)
r (nm)
0
1
2
3
0
0.2
0.4
0.6
0.8
1

FIG. 15A

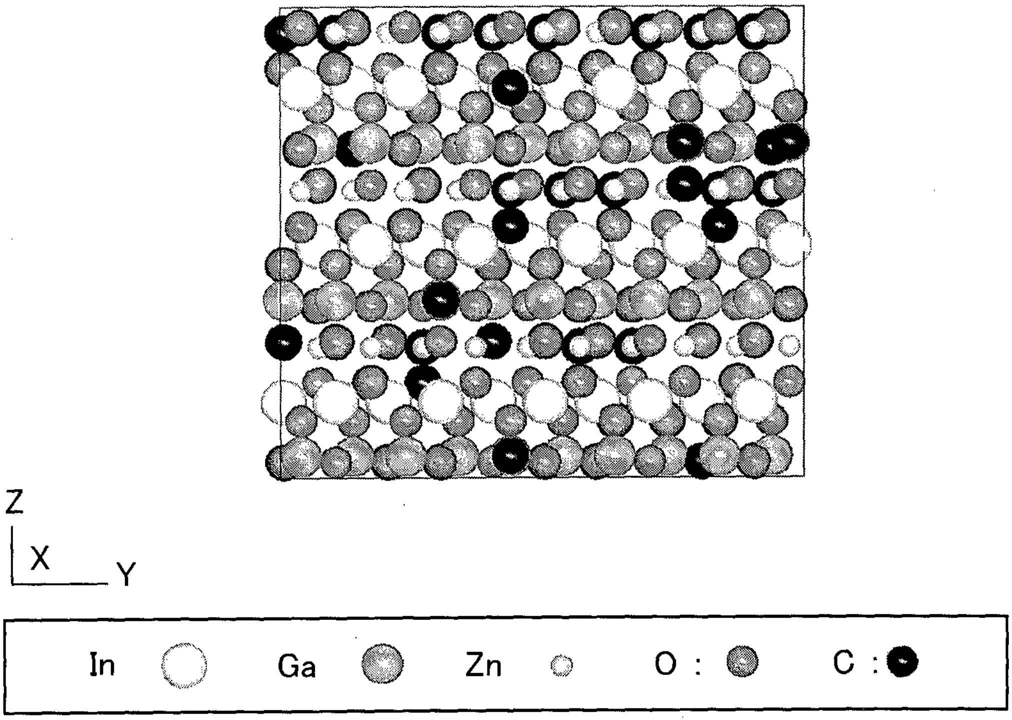


FIG. 15B

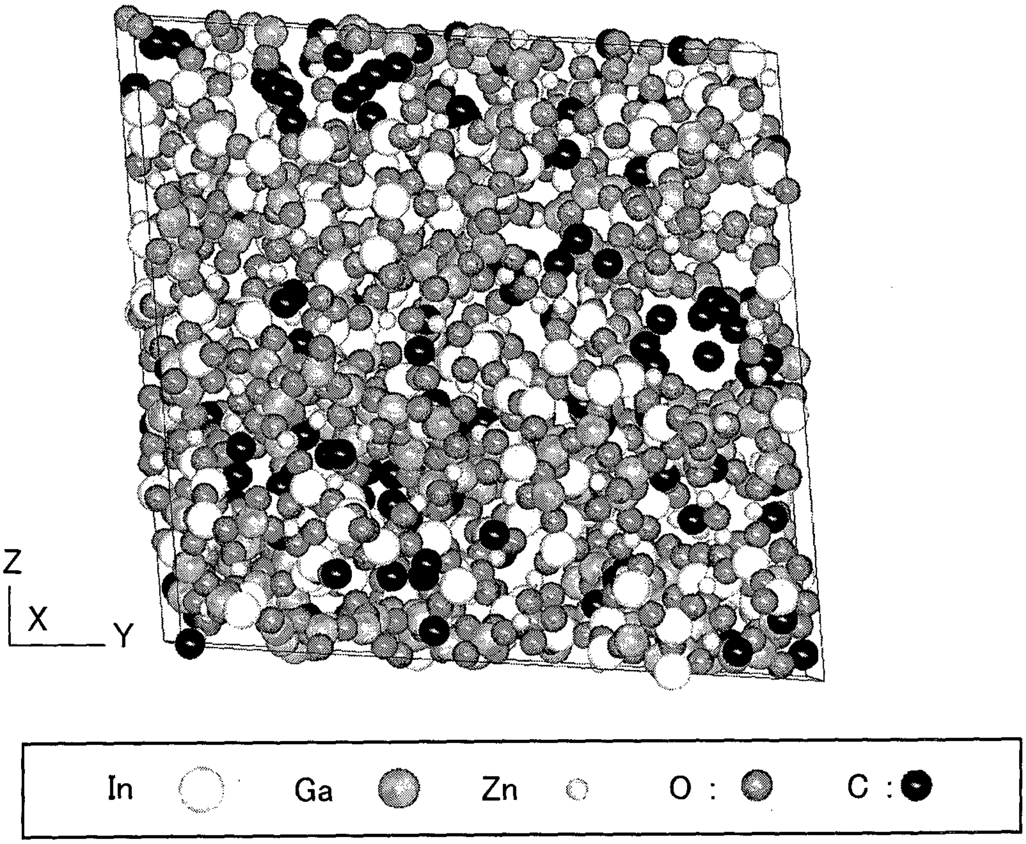


FIG. 16

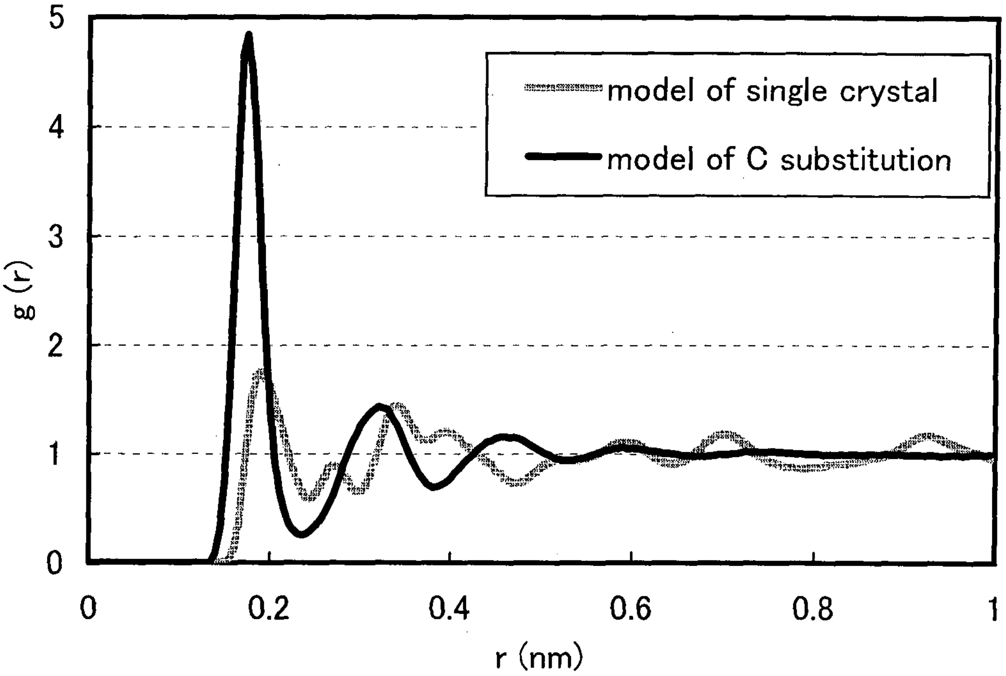

5
4
3
2
1
0
g (r)
0
0.2
0.4
0.6
0.8
1
r (nm)
model of single crystal
model of C substitution

FIG. 17

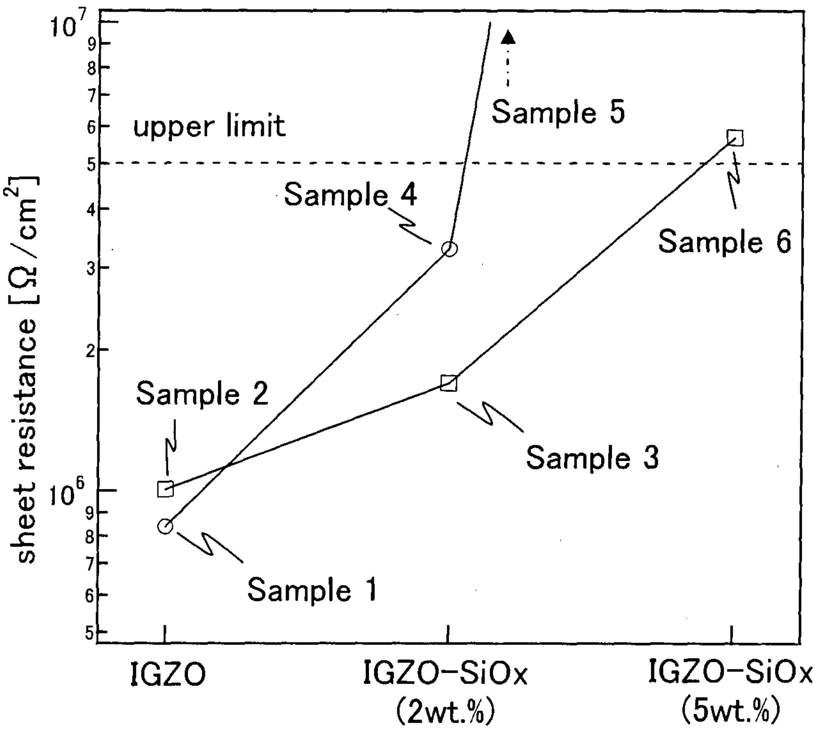

sheet resistance [Ω/cm^2]
10^7
9
8
7
6
5
4
3
2
10^6
9
8
7
6
5
upper limit
Sample 5
Sample 4
Sample 6
Sample 2
Sample 3
Sample 1
IGZO
IGZO-SiOx
(2wt.%)
IGZO-SiOx
(5wt.%)

FIG. 18A

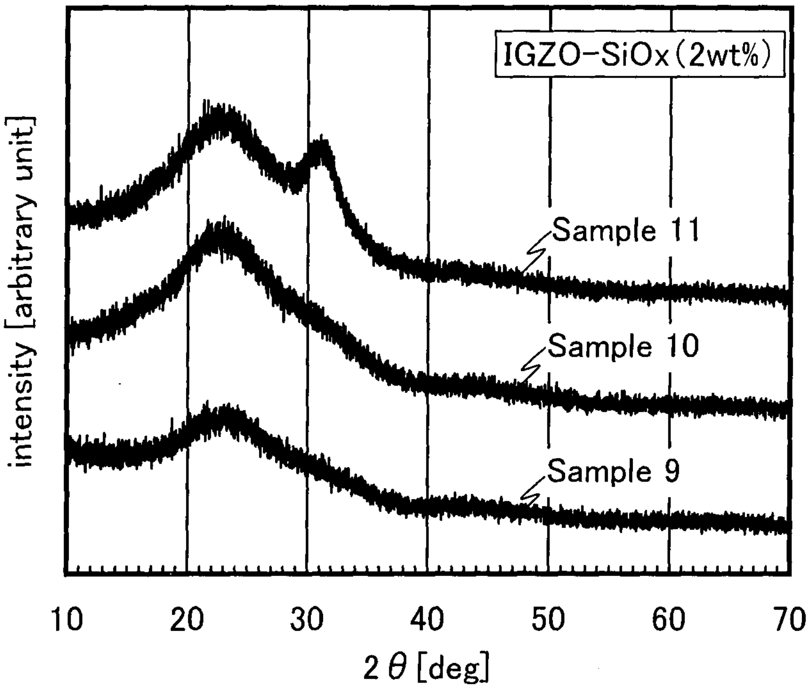
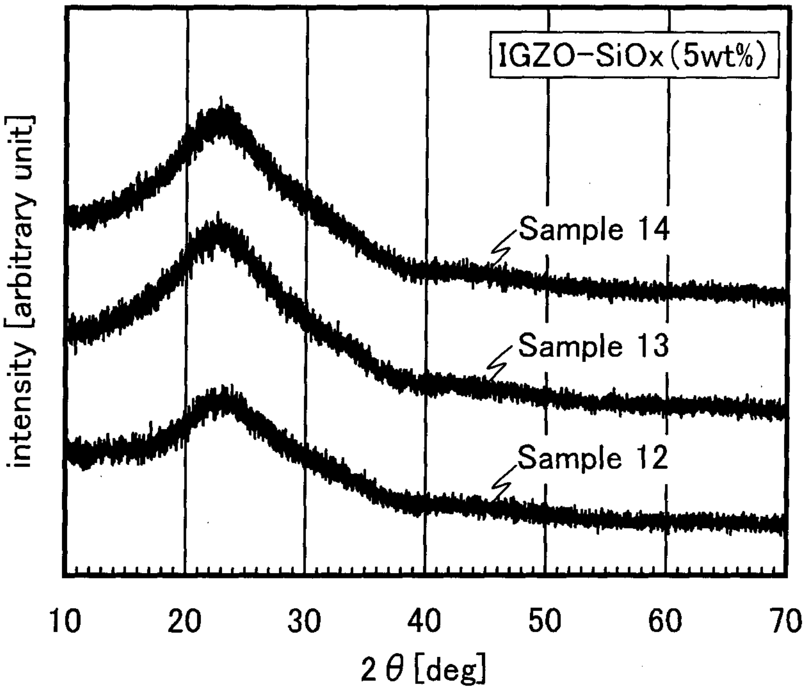


FIG. 18B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2012/076563

A. CLASSIFICATION OF SUBJECT MATTER

Int.Cl. See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Int.Cl. H01L29/786, H01L21/336, H01L21/477, H01L21/8242, H01L21/8244, H01L27/108, H01L27/11, H01L29/788, H01L29/792

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Published examined utility model applications of Japan 1922-1996
Published unexamined utility model applications of Japan 1971-2012
Registered utility model specifications of Japan 1996-2012
Published registered utility model applications of Japan 1994-2012

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI, JSTPlus(JDreamII)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2010-186994 A (SEMICONDUCTOR ENERGY LAVORATORY CO., LTD) 2010.08.26, Par. Nos. [0013], [0063] to [0065], [0175] to [0186], Fig. 17 & US 2010/0181565 A1 & CN 101794820 A & KR 10-2010-0084466 A & TW 201114040 A	1-18
A	JP 2011-205017 A (DAI NIPPON PRINTING CO., LTD.) 2011.10.13, Par. Nos. [0008] to [0013] (No Family)	1-18
A	JP 2011-142315 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.07.21, Par. Nos. [0007], [0041] to [0043], Figs. 1 and 2 & US 2011/0140098 A1 & WO 2011/070887 A1	1-18

☑ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
“A” document defining the general state of the art which is not considered to be of particular relevance
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“O” document referring to an oral disclosure, use, exhibition or other means
“P” document published prior to the international filing date but later than the priority date claimed
“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
“&” document member of the same patent family

Date of the actual completion of the international search 31.10.2012	Date of mailing of the international search report 13.11.2012
Name and mailing address of the ISA/JP **Japan Patent Office** 3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan	Authorized officer 5O 3864 Soichiro Suzuki Telephone No. +81-3-3581-1101 Ext. 3559

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2011-96884 A (STANLEY ELECTRIC CO., LTD.) 2011.05.12, Par. Nos. [0042] to [0050] (No Family)	1-18
A	JP 2009-81413 A (CANON INC.) 2009.04.16, Par. Nos. [0051] to [0078], [0108] & US 2010/0258794 A1 & EP 2193547 A & WO 2009/031634 A1 & KR 10-2010-0061511 A & CN 101796644 A	1-18
A	JP 2008-311342 A (IDEMITSU KOSAN CO., LTD.) 2008.12.25, Par. Nos. [0053] to [0072] (No Family)	1-18

CLASSIFICATION OF SUBJECT MATTER

H01L29/786(2006.01)i, H01L21/336(2006.01)i, H01L21/477(2006.01)i, H01L21/8242(2006.01)i, H01L21/8244(2006.01)i, H01L27/108(2006.01)i, H01L27/11(2006.01)i, H01L29/788(2006.01)i, H01L29/792(2006.01)i