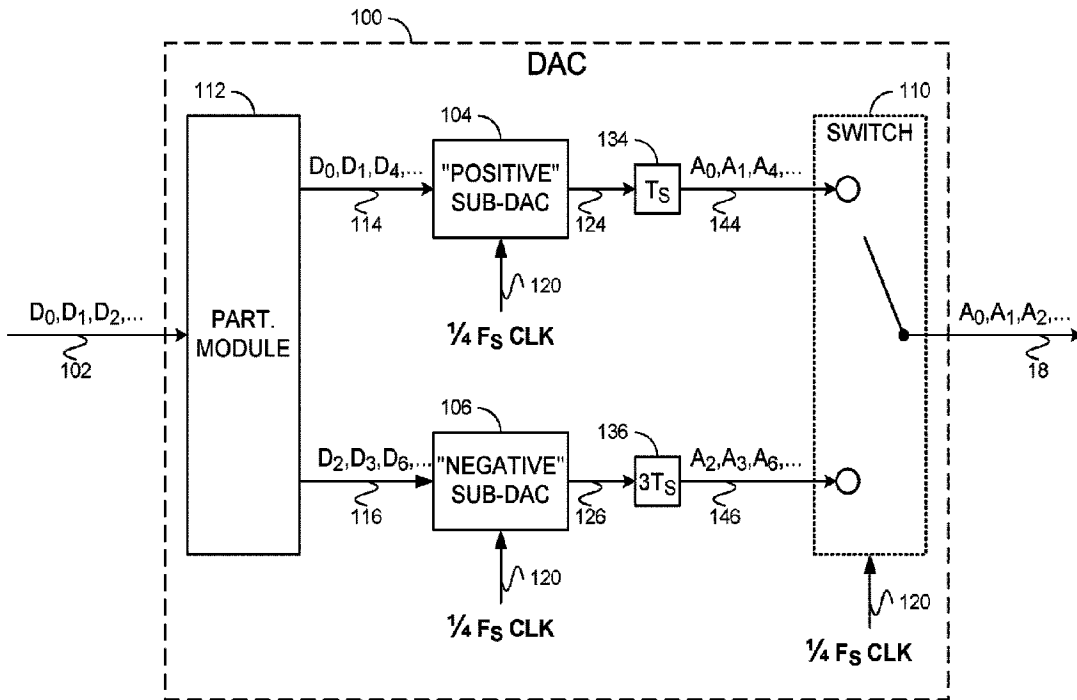




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(57) **Abrégé/Abstract:**

A controlled switch having N inputs and a single output ( $N \geq 2$ ) is switchable between N states. In each state a respective one of the inputs is connected to the single output. There are N sources of sub-streams of analog samples, each sub-stream composed of pairs of adjacent analog samples. Each source is coupled to a respective one of the inputs. In operation, the controlled switch is controlled by a control signal to switch between the N states. While the controlled switch is in any one of the states, a data transition occurs between two adjacent analog samples in the sub-stream whose source is coupled to the input that is connected to the single output. The single output yields a high-bandwidth analog signal. Any pair of adjacent analog samples in any one of the sub-streams substantially determines a corresponding pair of adjacent analog samples in the high-bandwidth analog signal.

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(54) **Title:** DIGITAL-TO-ANALOG CONVERTER AND GENERATION OF HIGH-BANDWIDTH ANALOG SIGNALS

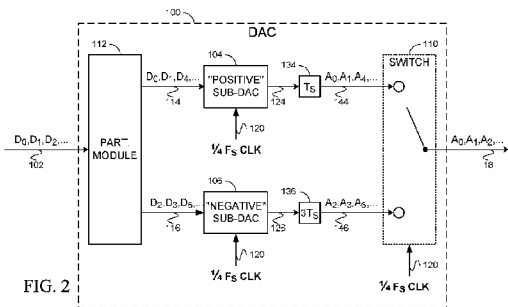


FIG. 2

(57) **Abstract:** A controlled switch having  $N$  inputs and a single output ( $N \geq 2$ ) is switchable between  $N$  states. In each state a respective one of the inputs is connected to the single output. There are  $N$  sources of sub-streams of analog samples, each sub-stream composed of pairs of adjacent analog samples. Each source is coupled to a respective one of the inputs. In operation, the controlled switch is controlled by a control signal to switch between the  $N$  states. While the controlled switch is in any one of the states, a data transition occurs between two adjacent analog samples in the sub-stream whose source is coupled to the input that is connected to the single output. The single output yields a high-bandwidth analog signal. Any pair of adjacent analog samples in any one of the sub-streams substantially determines a corresponding pair of adjacent analog samples in the high-bandwidth analog signal.

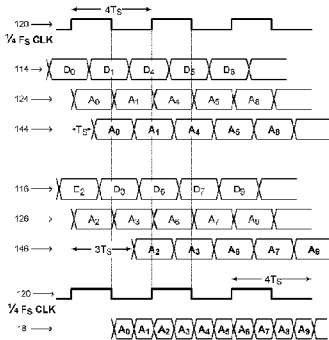


FIG. 3



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## Digital-to-Analog Converter and Generation of High-Bandwidth Analog Signals

### TECHNICAL FIELD

[0001] This disclosure is related to the technical field of generating analog signals and digital-to-analog conversion.

### BACKGROUND

[0002] “Ultra-Wideband Digital-to-Analog Conversion Technologies for Tbit/s channel transmission” by Yamazaki et al, presented at ECOC 2017, notes that “high-speed electronic digital-to-analog converters (DACs) are of key importance in modern optical transmission systems” and “in multilevel optical transmitters, the analog bandwidth of the DACs is one of the factors limiting the transmitter’s bandwidth”. Yamazaki et al. describes a digital-preprocessed analog-multiplexed DAC (DP-AM-DAC) that uses a digital pre-processor, two sub-DACs, and an analog multiplexer (AMUX). “With sub-DACs with a bandwidth of  $\sim\frac{1}{2}f_B$ , we can generate signals with a bandwidth of  $\sim f_B$  as the output from the AMUX.” The AMUX is a heterojunction bipolar transistor (HBT) analog multiplexer (mux). Figure 2 of Yamazaki et al. shows an interleaving method (type I) and a preprocessed spectrum method (type II) that reduces the switching frequency of the analog mux by a factor of two. However, type II is very sensitive to imperfections of the matching of the analog characteristics of the two inputs of the analog mux, as very large signal components need to be almost-perfectly cancelled.

[0003] “An 8-bit 100-GS/s Distributed DAC in 28-nm CMOS for Optical Communications” by Huang et al., *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4 (April 2015), discloses a distributed structure to interleave together the outputs from two DACs. Huang et al. uses two interleaved NRZ (non-return-to-zero) DACs sampled at 90 degrees out of phase with respect to each other and summed up at the output stage. The interleaving is structured to invert one of the image spectra so that they are cancelled when summed. Again, there are very strong interference terms that are suppressed only with precise matching of the two halves of the analog circuit.

[0004] US Patent No. 8,693,876 discloses the combining of two half-band signals from two DACs into a full-band signal, by shifting up the frequency of one of the half-band signals with a bipolar mixer. It is desirable to have the circuit implemented using lower energy technologies such as complementary metal-oxide-semiconductor (CMOS).

[0005] Packet and burst switches are known, where typically 1500 bytes received from one tributary are sent in sequence out of one optical or electrical output.

### SUMMARY

[0006] An apparatus comprises a controlled switch having  $N$  inputs and a single output ( $N \geq 2$ ), where the controlled switch is switchable between  $N$  states. In each state a respective one of the inputs is connected to the single output. There are  $N$  sources of sub-streams of analog samples, each sub-stream composed of pairs of adjacent analog samples. Each source is coupled to a respective one of the inputs. In operation, the controlled switch is controlled by a control signal to switch between the  $N$  states. While the controlled switch is in any one of the states, a data transition occurs between two adjacent analog samples in the sub-stream whose source is coupled to the input that is connected to the single output. The single output yields the high-bandwidth analog signal. Any pair of adjacent analog samples in any one of the sub-streams substantially determines a corresponding pair of adjacent analog samples in the high-bandwidth analog signal. The apparatus may be a digital-to-analog converter (DAC), where each source is a sub-DAC. The sub-DACs may employ techniques that increase resilience to distortions as well as to time mismatches between sub-DACs.

### BRIEF DESCRIPTION OF THE DRAWINGS

- [0007] **FIG. 1** illustrates a mechanism that relies on data transitions to get an effective sampling rate that is twice the number of sub-streams;
- [0008] **FIG. 2** illustrates an example DAC that uses the mechanism illustrated in FIG. 1;
- [0009] **FIG. 3** is a timing diagram of clock signals and data signals in the DAC of FIG. 2;
- [0010] **FIG. 4** illustrates an example DAC that is a variant of the DAC of FIG. 2;
- [0011] **FIG. 5** is a timing diagram of clock signals and data signals in the DAC of FIG. 4;
- [0012] **FIG. 6** illustrates another example DAC that uses the mechanism illustrated in FIG. 1;
- [0013] **FIG. 7** is a timing diagram of clock signals and data signals in the DAC of FIG. 6;
- [0014] **FIG. 8** illustrates an example DAC that is a variant of the DAC of FIG. 6;
- [0015] **FIG. 9** is a timing diagram of clock signals and data signals in the DAC of FIG. 8;
- [0016] **FIG. 10** illustrates an example "positive" sub-DAC for use in the example DACs of FIG. 2 and FIG. 4;
- [0017] **FIG. 11** is a timing diagram of clock signals and data signals in the sub-DAC of FIG. 10;
- [0018] **FIG. 12** illustrates an example "negative" sub-DAC for use in the example DACs of FIG. 2 and FIG. 4;
- [0019] **FIG. 13** is a timing diagram of clock signals and data signals in the sub-DAC of FIG. 12; and
- [0020] **FIG. 14** is a block diagram illustration of an example transmitter.

### DETAILED DESCRIPTION

[0001] **FIG. 1** illustrates a mechanism for creating a high-bandwidth analog signal.

[0002] A controlled switch 10 has  $N$  inputs and a single output, where the number  $N$  of inputs is an integer greater than or equal to two ( $N \geq 2$ ).  $N$  sub-streams of analog samples are provided as input to the controlled switch 10, each sub-stream to a respective one of the inputs. A first sub-stream 12, a second sub-stream 14 and an  $N$ -th sub-stream 16 are illustrated in FIG. 1.

[0003] The controlled switch 10 is operative to produce a high-bandwidth analog signal at a sample rate of  $F_S$ . The high-bandwidth analog signal comprises an output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$  that contains one analog sample in each time period of duration  $\sim T_S$ . The symbol “ $\sim$ ” is shorthand for the word “approximately”. The index  $i$  of each analog sample  $A_i$  represents an order of the analog samples in the output stream 18. A pair of samples is deemed “adjacent” if the index of the second sample in the pair is one greater than the index of the first sample in the pair.

[0004] The controlled switch 10 has  $N$  different states. In the first state, the first sub-stream 12 is connected to the output of the controlled switch 10 and thus contributes to the output stream 18. In the second state, the second sub-stream 14 is connected to the output of the controlled switch 10 and thus contributes to the output stream 18. In the  $N$ -th state, the  $N$ -th sub-stream 16 is connected to the output of the controlled switch 10 and thus contributes to the output stream 18.

[0005] A control signal 20 having a period of  $\sim 2N T_S$  controls the controlled switch 10 to switch between the  $N$  different states. For example, the control signal 20 is a clock signal operating at a frequency of  $\frac{1}{2N} F_S$ , and the controlled switch 10 is controlled by rising edges and falling edges of the  $\frac{1}{2N} F_S$  clock signal 20.

[0006] The first sub-stream 12 is intentionally composed of pairs of adjacent analog samples such as  $\{A_0, A_1\}$  and  $\{A_{2N}, A_{2N+1}\}$ . The timing of the control signal 20 is intentionally arranged so that a data transition occurs between two adjacent analog samples

in the first sub-stream 12 while the controlled switch 10 is in the first state. For example, the analog samples  $A_0$  and  $A_1$  contribute one after the other to the output stream 18 while the controlled switch 10 is in the first state.

[0007] The second sub-stream 14 is intentionally composed of pairs of adjacent analog samples such as  $\{A_2, A_3\}$  and  $\{A_{2N+2}, A_{2N+3}\}$ . The timing of the control signal 20 is intentionally arranged so that a data transition occurs between two adjacent analog samples in the second sub-stream 14 while the controlled switch 10 is in the second state. For example, the analog samples  $A_2$  and  $A_3$  contribute one after the other to the output stream 18 while the controlled switch 10 is in the second state.

[0008] The  $N$ -th sub-stream 16 is intentionally composed of pairs of adjacent analog samples such as  $\{A_{2N-2}, A_{2N-1}\}$  and  $\{A_{4N-2}, A_{4N-1}\}$ . The timing of the control signal 20 is intentionally arranged so that a data transition occurs between two adjacent analog samples in the  $N$ -th sub-stream 16 while the controlled switch 10 is in the  $N$ -th state. For example, the analog samples  $A_{2N-2}$  and  $A_{2N-1}$  contribute one after the other to the output stream 18 while the controlled switch 10 is in the  $N$ -th state.

[0009] Two adjacent analog samples in the output stream 18 are substantially determined by a corresponding two adjacent analog samples in one of the sub-streams. For example, the output stream 18 has the analog samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$ , and the samples  $\{A_0, A_1\}$  in the output stream 18 are substantially determined by the corresponding samples  $\{A_0, A_1\}$  in the first sub-stream 12, and the samples  $\{A_2, A_3\}$  in the output stream 18 are substantially determined by the corresponding samples  $\{A_2, A_3\}$  in the second sub-stream 14. The term “substantially determined” is used to express the fact that the samples in the output stream 18 may not be identical to the samples in the sub-streams. Imperfect circuits may contribute distortion and/or noise. Analog filtering, peaking, hysteresis, reconstruction filtering, and parasitic circuit elements can cause inter-symbol interference (ISI) so that one output sample is a function of more than one input sample, while still being substantially determined by one input sample.

[0030] The “capture” of a data transition between two adjacent analog samples in a sub-stream, with both of the adjacent analog samples contributing, one after the other, to the output stream 18, results in an effective sampling rate of twice the number of sub-streams. Stated differently, the mechanism described with respect to FIG. 1 achieves twice the throughput as expected for the number of sub-streams.

[0031] It is unconventional, unexpected, and unintuitive to intentionally “capture” a data transition from one analog sample to an adjacent analog sample, because samples are unstable during the data transition, for example, due to the inter-symbol interference (ISI). Usual design practice is to resample the data in the center of the data interval, to avoid the effects of timing jitter, timing offset, and the complicated and potentially asymmetric dynamics of the data transition.

[0032] It is a challenge to generate a high-speed clock and to bring the high-speed clock to an analog multiplexer component. Furthermore, an analog multiplexer component controlled by a high-speed clock consumes power that is directly proportional to the clock speed.

[0033] One potential benefit of the mechanism described with respect to FIG. 1 is that for a desired sample rate of  $F_S$ , it is sufficient to generate and bring to the controlled switch 10 a control signal 20 having a period of  $\sim 2N T_S$ . For example, if there are precisely two sub-streams, then a clock signal 20 operating at  $\sim \frac{1}{4}F_S$  is sufficient to achieve the desired sample rate of  $F_S$ . In another example, if there are precisely four sub-streams, then a clock signal 20 operating at  $\sim \frac{1}{8}F_S$  is sufficient to achieve the desired sample rate of  $F_S$ . It is much easier for the controlled switch 10 to switch when controlled by a slower clock signal than when controlled by a fast clock signal, and the controlled switch 10 will consume less heat when controlled by the slower clock signal than when controlled by the fast clock signal.

[0034] The source of the first sub-stream 12 of analog samples provided as input to the controlled switch 10 is shown conceptually in FIG. 1 as an arbitrary source 22. The source of the second sub-stream 14 of analog samples provided as input to the controlled switch 10 is shown conceptually in FIG. 1 as an arbitrary source 24. The source of the  $N$ -th sub-stream 16

of analog samples provided as input to the controlled switch 10 is shown conceptually in FIG. 1 as an arbitrary source 26.

[0035] Another potential benefit of the mechanism described with respect to FIG. 1 is that it involves a single control signal 20 to drive the arbitrary sources 22, 24, 26 and to drive the controlled switch 10. No other control signals or clock signals are required.

[0036] Each one of the  $N$  sub-streams of analog samples provided as input to the controlled switch 10 may be converted from a respective sub-stream of digital samples (not shown). Various example digital-to-analog converters that employ the mechanism described with respect to FIG. 1 are illustrated in FIG. 2, FIG. 4, FIG. 6, and FIG. 8 and are described hereinbelow. In those example digital-to-analog converters, the arbitrary sources 22, 24, 26 of the  $N$  sub-streams of analog samples are sub-DACs controlled by a clock signal operating at a frequency of  $\frac{1}{2N} F_S$ .

[0037] Linear digital filtering of the sub-streams of digital samples may adapt the signals in each sub-stream to obtain a cleaner output from the controlled switch 10. This may become more important when the controlled switch 10 is physically further away from the sources of the sub-streams. The linear digital filtering may be calibrated in the factory. Alternatively, local or remote feedback may be used to dynamically control the linear digital filtering.

[0038] Nonlinear compensation may be included in the generation of the sub-streams, for example, as described in US Patent No. 6781537 to Taraschuk et al., without memory, or with memory (time delays) in the response. This nonlinear compensation may compensate for nonlinearity in the component DACs, the controlled switch, or downstream elements.

[0039] The arrangement of the timing of the control signal 20 relative to the occurrence of data transitions between two adjacent analog samples in the sub-streams may result from delays introduced in the sub-streams. This is the case, for example, in the DACs illustrated in FIG. 2 and FIG. 6.

[0040] The arrangement of the timing of the control signal 20 relative to the occurrence of data transitions between two adjacent analog samples in the sub-streams may result from a phase offset between the control signal 20 and clocks used to generate the sub-streams. This is the case, for example, in the DACs illustrated in FIG. 4 and FIG. 8. Phase shifting may be

used to obtain precision control of the clock phases. This may be calibrated in the factory. Alternatively, local or remote feedback may be used to dynamically control the phase.

[0041] Depending on the implementation, it may be simpler to produce clock signals having zero relative phase offset (as used in the DACs illustrated in FIG. 2 and FIG. 6) than to produce clock signals having a non-zero relative phase offset (as used in the DACs illustrated in FIG. 4 and FIG. 8).

[0042] Depending on the implementation, it may be simpler to produce clock signals having non-zero relative phase offset (as used in the DACs illustrated in FIG. 4 and FIG. 8) than to delay analog signals (as used in the DACs illustrated in FIG. 2 and FIG. 6).

[0043] FIG. 2 illustrates an example digital-to-analog converter (DAC) 100 that is operative to convert an input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$  at a sampling rate of  $F_S$ .

[0044] FIG. 3 is a timing diagram of clock signals and data signals in the DAC 100.

[0045] The DAC 100 comprises a “positive” sub-DAC component 104, a “negative” sub-DAC component 106, and a controlled switch 110. The controlled switch 110 has two inputs (coupled to the outputs of the sub-DAC components 104, 106) and a single output (the output stream 18). (The controlled switch 110 is a specific example of the controlled switch 10 described with respect to FIG. 1, where the number of sub-streams is precisely two ( $N=2$ )).

[0046] The positive sub-DAC component 104 receives as input a first sub-stream 114 of digital samples  $\{D_0, D_1, D_4, D_5, \dots\}$ , and the negative sub-DAC component 106 receives as input a second sub-stream 116 of digital samples  $\{D_2, D_3, D_6, D_7, \dots\}$ . The first sub-stream 114 is composed of pairs of adjacent digital samples such as  $\{D_0, D_1\}$ ,  $\{D_4, D_5\}$ , and  $\{D_8, D_9\}$ , and the second sub-stream 116 is composed of pairs of adjacent digital samples such as  $\{D_2, D_3\}$ ,  $\{D_6, D_7\}$ , and  $\{D_{10}, D_{11}\}$ . A partitioning module 112 comprised in the DAC 100 is operative to partition the input stream 102 of digital samples into the first sub-stream 114 and the second sub-stream 116, using any suitable technique. For example, the partitioning module 112 could reorder every four consecutive samples in the input stream 102 as  $\{D_0, D_2,$

$D_1, D_3, D_4, D_6, D_5, D_7, \dots$ . To obtain the first sub-stream 114 of digital samples  $\{D_0, D_1, D_4, D_5, \dots\}$ , the partitioning module 112 could apply a decimate-by-two function to the reordered samples. To obtain the second sub-stream 116 of digital samples  $\{D_2, D_3, D_6, D_7, \dots\}$ , the partitioning module 112 could delay a copy of the reordered samples by a delay of duration  $\sim T_S$ , and then apply a decimate-by-two function.

[0047] A clock signal 120 operating at  $\sim \frac{1}{4}F_S$  (and therefore having a period of  $\sim 4T_S$ ) is provided to the sub-DAC components 104, 106. The positive sub-DAC component 104 samples the first sub-stream 114 at rising edges and falling edges of the  $\sim \frac{1}{4}F_S$  clock signal 120, thus converting the first sub-stream 114 into a first sub-stream 124 of analog samples  $\{A_0, A_1, A_4, A_5, \dots\}$ . The negative sub-DAC component 106 samples the second sub-stream 116 at rising edges and falling edges of the  $\sim \frac{1}{4}F_S$  clock signal 120, thus converting the second sub-stream 116 into a second sub-stream 126 of analog samples  $\{A_2, A_3, A_6, A_7, \dots\}$ . An analog delay line 134 is operative to delay the first sub-stream 124 by a delay of duration  $\sim T_S$ , yielding a first sub-stream 144 of delayed analog samples  $\{A_0, A_1, A_4, A_5, \dots\}$ . An analog delay line 136 is operative to delay the second sub-stream 126 by a delay of duration  $\sim 3T_S$ , yielding a second sub-stream 146 of delayed analog samples  $\{A_2, A_3, A_6, A_7, \dots\}$ . (The first sub-stream 144 is a specific example of the first sub-stream 12 described with respect to FIG. 1, and the second sub-stream 146 is a specific example of the second sub-stream 14 described with respect to FIG. 1.)

[0048] The  $\sim \frac{1}{4}F_S$  clock signal 120 is provided, with zero phase offset, to the controlled switch 110. The controlled switch 110 is controlled by rising edges and falling edges of the  $\sim \frac{1}{4}F_S$  clock signal 120, switching between a “positive” state in which the first sub-stream 144 of delayed analog samples  $\{A_0, A_1, A_4, A_5, \dots\}$  contributes to the output stream 18 and a “negative” state in which the second sub-stream 146 of delayed analog samples  $\{A_2, A_3, A_6, A_7, \dots\}$  contributes to the output stream 18. The resulting output stream 18 of analog

samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$  contains one analog sample in each time period of duration  $\sim T_s$ .

[0049] As mentioned, the analog delay line 134 and the analog delay line 136 are operative to introduce delays in the sub-streams of analog samples. These delays result in the arrangement of the timing of the “positive” states and “negative” states of the controlled switch 110 relative to the occurrence of data transitions between two adjacent analog samples in the first sub-stream 144 and in the second sub-stream 146.

[0050] While the controlled switch 110 is in the “positive” state, the data transition in the first sub-stream 144 from one analog sample to an adjacent analog sample is captured. While the controlled switch 110 is in the “negative” state, the data transition in the second sub-stream 146 from one analog sample to an adjacent analog sample is captured. For example, the analog samples  $A_0$  and  $A_1$  contribute one after the other to the output stream 18 during a single half-period of duration  $\sim 2T_s$  of the  $\sim \frac{1}{4}F_s$  clock signal 120, and then the analog samples  $A_2$  and  $A_3$  contribute one after the other to the output stream 18 during a next single half-period of duration  $\sim 2T_s$  of the  $\sim \frac{1}{4}F_s$  clock signal 120.

[0051] The following time-table is helpful for understanding the operation of the DAC 100 and the timing diagram illustrated in FIG. 3.

Time/ $T_s$	[0,1)	[1,2)	[2,3)	[3,4)	[4,5)	[5,6)	[6,7)	[7,8)
sub-stream 144	$A_0$	$A_1$	$A_4$	$A_5$	$A_8$			
sub-stream 146		$A_2$	$A_3$	$A_6$	$A_7$			
switch 110 state	“positive”		“negative”		“positive”		“negative”	
output 18	$A_0$	$A_1$	$A_2$	$A_3$	$A_4$	$A_5$	$A_6$	$A_7$

**Table 1**

[0052] By employing the mechanism described above with respect to FIG. 1, the DAC 100 produces the output stream 18 at the rate of  $\sim F_s$  using clock signals operating solely at  $\sim \frac{1}{4}F_s$ .

[0053] FIG. 4 illustrates an example digital-to-analog converter (DAC) 150 that is operative to convert the input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$  at the sampling rate of  $F_s$ .

[0054] FIG. 5 is a timing diagram of clock signals and data signals in the DAC 150.

[0055] The DAC 150 is a variant of the DAC 100 illustrated in FIG. 2. In contrast to the DAC 100, there are no analog delay lines in the DAC 150. (The first sub-stream 124 is a specific example of the first sub-stream 12 described with respect to FIG. 1, and the second sub-stream 126 is a specific example of the second sub-stream 14 described with respect to FIG. 1.)

[0056] In the DAC 150, the  $\sim\frac{1}{4}F_S$  clock signal 120 provided to the controlled switch 110 has a  $90^\circ$  phase offset relative to the  $\sim\frac{1}{4}F_S$  clock signal 120 that is provided to the sub-DAC components 104, 106. The controlled switch 110 is controlled by rising edges and falling edges of the  $90^\circ$  phase offset  $\sim\frac{1}{4}F_S$  clock signal 120, switching between a “positive” state in which the first sub-stream 124 of analog samples  $\{A_0, A_1, A_4, A_5, \dots\}$  contributes to the output stream 18 and a “negative” state in which the second sub-stream 126 of analog samples  $\{A_2, A_3, A_6, A_7, \dots\}$  contributes to the output stream 18. The resulting output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$  contains one analog sample in each time period of duration  $\sim T_S$ .

[0057] As illustrated, in the DAC 150, the  $\sim\frac{1}{4}F_S$  clock signal 120 provided to the controlled switch 110 has a  $90^\circ$  phase offset relative to the  $\sim\frac{1}{4}F_S$  clock signal 120 that is provided to the sub-DAC components 104, 106. This  $90^\circ$  phase offset results in the arrangement of the timing of the “positive” states and “negative” states of the controlled switch 110 relative to the occurrence of data transitions between two adjacent analog samples in the first sub-stream 124 and in the second sub-stream 126.

[0058] While the controlled switch 110 is in the “positive” state, the data transition in the first sub-stream 124 from one analog sample to an adjacent analog sample is captured. While the controlled switch 110 is in the “negative” state, the data transition in the second sub-stream 126 from one analog sample to an adjacent analog sample is captured. For example, the analog samples  $A_0$  and  $A_1$  contribute one after the other to the output stream 18 during a single half-period of duration  $\sim 2T_S$  of the  $90^\circ$  phase offset  $\sim\frac{1}{4}F_S$  clock signal 120, and then

the analog samples  $A_2$  and  $A_3$  contribute one after the other to the output stream 18 during a next single half-period of duration  $\sim 2T_S$  of the  $90^\circ$  phase offset  $\sim 1/4F_S$  clock signal 120.

[0059] By employing the mechanism described above with respect to FIG. 1, the DAC 150 produces the output stream 18 at the rate of  $\sim F_S$  using clock signals operating solely at  $\sim 1/4F_S$ .

[0060] FIG. 6 illustrates an example digital-to-analog converter (DAC) 200 that is operative to convert the input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$  at the sampling rate of  $F_S$ .

[0061] FIG. 7 is a timing diagram of clock signals and data signals in the DAC 200.

[0062] The DAC 200 comprises a “positive” sub-DAC component 204, a “zero” sub-DAC component 206, a “negative” sub-DAC component 208, and a controlled switch 210. The controlled switch 210 has three inputs (coupled to the outputs of the sub-DAC components 204, 206, 208) and a single output (the output stream 18). (The controlled switch 210 is a specific example of the controlled switch 10 described with respect to FIG. 1, where the number of sub-streams is precisely three ( $N=3$ ).)

[0063] The positive sub-DAC component 204 receives as input a first sub-stream 214 of digital samples  $\{D_0, D_1, D_6, D_7, \dots\}$ , the zero sub-DAC component 206 receives as input a second sub-stream 216 of digital samples  $\{D_2, D_3, D_8, D_9, \dots\}$ , and the negative sub-DAC component 208 receives as input a third sub-stream 218 of digital samples  $\{D_4, D_5, D_{10}, D_{11}, \dots\}$ . The first sub-stream 214 is composed of pairs of adjacent samples such as  $\{D_0, D_1\}$ ,  $\{D_6, D_7\}$ , and  $\{D_{12}, D_{13}\}$ , the second sub-stream 216 is composed of pairs of adjacent samples such as  $\{D_2, D_3\}$ ,  $\{D_8, D_9\}$ , and  $\{D_{14}, D_{15}\}$ , and the third sub-stream 218 is composed of pairs of adjacent samples such as  $\{D_4, D_5\}$ ,  $\{D_{10}, D_{11}\}$ , and  $\{D_{16}, D_{17}\}$ . A partitioning module 212 comprised in the DAC 200 is operative to partition the input stream 102 of digital samples into the first sub-stream 214, the second sub-stream 216, and the third sub-stream 218, using any suitable technique.

[0064] A clock signal 220 operating at  $\sim\frac{1}{6}F_S$  (and therefore having a period of  $\sim 6T_S$ ) is provided to the sub-DAC components 204, 206, 208. The positive sub-DAC component 204 samples the first sub-stream 214 at rising edges and falling edges of the  $\sim\frac{1}{6}F_S$  clock signal 220, thus converting the first sub-stream 214 into a first sub-stream 224 of analog samples  $\{A_0, A_1, A_6, A_7, \dots\}$ . The zero sub-DAC component 206 samples the second sub-stream 216 at rising edges and falling edges of the  $\sim\frac{1}{6}F_S$  clock signal 220, thus converting the second sub-stream 216 into a second sub-stream 226 of analog samples  $\{A_2, A_3, A_8, A_9, \dots\}$ . The negative sub-DAC component 208 samples the third sub-stream 218 at rising edges and falling edges of the  $\sim\frac{1}{6}F_S$  clock signal 220, thus converting the third sub-stream 218 into a third sub-stream 228 of analog samples  $\{A_4, A_5, A_{10}, A_{11}, \dots\}$ .

[0065] An analog delay line 234 is operative to delay the first sub-stream 224 by a delay of duration  $\sim T_S$ , yielding a first sub-stream 244 of delayed analog samples  $\{A_0, A_1, A_6, A_7, \dots\}$ . An analog delay line 236 is operative to delay the second sub-stream 226 by a delay of duration  $\sim 3T_S$ , yielding a second sub-stream 246 of delayed analog samples  $\{A_2, A_3, A_8, A_9, \dots\}$ . An analog delay line 238 is operative to delay the third sub-stream 228 by a delay of duration  $\sim 5T_S$ , yielding a third sub-stream 248 of delayed analog samples  $\{A_4, A_5, A_{10}, A_{11}, \dots\}$ .

[0066] A three-state control signal 240 having a period of  $\sim 6T_S$  is provided to the controlled switch 210. The controlled switch 210 is controlled by transitions of the three-state control signal 240, switching between a “positive” state in which the first sub-stream 244 of delayed analog samples  $\{A_0, A_1, A_6, A_7, \dots\}$  contributes to the output stream 18, a “zero” state in which the second sub-stream 246 of delayed analog samples  $\{A_2, A_3, A_8, A_9, \dots\}$  contributes to the output stream 18, and a “negative” state in which the third sub-stream 248 of delayed analog samples  $\{A_4, A_5, A_{10}, A_{11}, \dots\}$  contributes to the output stream 18. The

resulting output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$  contains one analog sample in each time period of duration  $\sim T_s$ .

[0067] As illustrated, the three-state control signal 240 has a zero-phase offset relative to the  $\sim 1/6 F_s$  clock signal 220 provided to the sub-DAC components 204, 206, 208. The delays introduced by the analog delay lines 234, 236, and 238 result in the arrangement of the timing of the “positive”, “zero” and “negative” states of the controlled switch 210, respectively, relative to the occurrence of data transitions between two adjacent analog samples in the first sub-stream 244, the second sub-stream 246 and the third sub-stream 248.

[0068] While the controlled switch 210 is in the “positive” state, the data transition in the first sub-stream 244 from one analog sample to an adjacent analog sample is captured. While the controlled switch 210 is in the “zero” state, the data transition in the second sub-stream 246 from one analog sample to an adjacent analog sample is captured. While the controlled switch 210 is in the “negative” state, the data transition in the third sub-stream 248 from one analog sample to an adjacent analog sample is captured. For example, the analog samples  $A_0$  and  $A_1$  contribute one after the other to the output stream 18 during a single third-period of duration  $\sim 2T_s$  of the control signal 240, and then the analog samples  $A_2$  and  $A_3$  contribute one after the other to the output stream 18 during a next single third-period of duration  $\sim 2T_s$  of the control signal 240, and then the analog samples  $A_4$  and  $A_5$  contribute one after the other to the output stream 18 during a next single third-period of duration  $\sim 2T_s$  of the control signal 240.

[0069] The following time-table is helpful for understanding the operation of the DAC 200 and the timing diagram illustrated in FIG. 7.

Time/ $T_s$	[0,1)	[1,2)	[2,3)	[3,4)	[4,5)	[5,6)	[6,7)	[7,8)
sub-stream 244	$A_0$	$A_1$		$A_6$			$A_7$	
sub-stream 246	$A_2$			$A_3$			$A_8$	
sub-stream 248				$A_4$			$A_5$	
switch 210 state	“positive”		“zero”		“negative”		“positive”	
output 18	$A_0$	$A_1$	$A_2$	$A_3$	$A_4$	$A_5$	$A_6$	$A_7$

Table 2

[0070] By employing the mechanism described above with respect to FIG. 1, the DAC 200 produces the output stream at the rate of  $\sim F_S$  using clock signals operating solely at  $\sim \frac{1}{6}F_S$ .

[0071] FIG. 8 illustrates an example digital-to-analog converter (DAC) 250 that is operative to convert the input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$  at the sampling rate of  $F_S$ .

[0072] FIG. 9 is a timing diagram of clock signals and data signals in the DAC 250.

[0073] The DAC 250 is a variant of the DAC 200 illustrated in FIG. 5. In contrast to the DAC 200, there are no analog delay lines in the DAC 250.

[0074] In the DAC 250, a three-state control signal 260 having a period of  $\sim 6T_S$  is provided to the controlled switch 210. The controlled switch 210 is controlled by transitions of the three-state control signal 260, switching between a “positive” state in which the first sub-stream 224 of analog samples  $\{A_0, A_1, A_6, A_7, \dots\}$  contributes to the output stream 18, a “zero” state in which the second sub-stream 226 of analog samples  $\{A_2, A_3, A_8, A_9, \dots\}$  contributes to the output stream 18, and a “negative” state in which the third sub-stream 228 of analog samples  $\{A_4, A_5, A_{10}, A_{11}, \dots\}$  contributes to the output stream 18. The resulting output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, \dots\}$  contains one analog sample in each time period of duration  $\sim T_S$ .

[0075] As illustrated, the three-state control signal 260 has a  $60^\circ$  phase offset relative to the  $\sim \frac{1}{6}F_S$  clock signal 220. This  $60^\circ$  phase offset results in the arrangement of the timing of the “positive”, “zero” and “negative” states of the controlled switch 210 relative to the occurrence of data transitions between two adjacent analog samples in the first sub-stream 224, the second sub-stream 226 and the third sub-stream 228.

[0076] While the controlled switch 210 is in the “positive” state, the data transition in the first sub-stream 224 from one analog sample to an adjacent analog sample is captured. While the controlled switch 210 is in the “zero” state, the data transition in the second sub-stream 226 from one analog sample to an adjacent analog sample is captured. While the controlled

switch 210 is in the “negative” state, the data transition in the third sub-stream 228 from one analog sample to an adjacent analog sample is captured. For example, the analog samples  $A_0$  and  $A_1$  contribute one after the other to the output stream 18 during a single third-period of duration  $\sim 2T_S$  of the three-state control signal 260, and then the analog samples  $A_2$  and  $A_3$  contribute one after the other to the output stream 18 during a next single third-period of duration  $\sim 2T_S$  of the three-state control signal 260, and then the analog samples  $A_4$  and  $A_5$  contribute one after the other to the output stream 18 during a next single third-period of duration  $\sim 2T_S$  of the three-state control signal 260.

[0077] By employing the mechanism described above with respect to FIG. 1, the DAC 250 produces the output stream 18 at the rate of  $\sim F_S$  using clock signals operating solely at  $\sim \frac{1}{6}F_S$ .

[0078] FIG. 10 illustrates an example sub-DAC 300 that is operative to convert digital samples into analog samples. The sub-DAC 300 may optionally be used as the “positive” sub-DAC 104 in DAC 100 or DAC 150 to convert the first sub-stream 114 of digital samples  $\{D_0, D_1, D_4, D_5, \dots\}$  into the first sub-stream 124 of analog samples  $\{A_0, A_1, A_4, A_5, \dots\}$  at a sampling rate of  $\frac{1}{2}F_S$ .

[0079] FIG. 11 is a timing diagram of clock signals and data signals in the sub-DAC 300.

[0080] The sub-DAC 300 comprises an “even” sub-sub-DAC component 304, an “odd” sub-DAC component 306, and an analog multiplexer (AMUX) component 310. The AMUX component 310 has two inputs (coupled to the outputs of the sub-sub-DAC components 304, 306) and a single output (the first sub-stream 124).

[0081] The even sub-sub-DAC component 304 receives as input a first sub-sub-stream 314 of digital samples  $\{D_0, D_4, D_8, \dots\}$ , and the odd sub-sub-DAC component 306 receives as input a second sub-sub-stream 316 of digital samples  $\{D_1, D_5, D_9, \dots\}$ . A partitioning module 312 is operative to partition the first sub-stream 114 of digital samples into the first sub-sub-stream 314 and the second sub-sub-stream 316, using any suitable technique. For example, the first sub-stream 114 could be duplicated, a delay buffer (not shown) could delay

one copy of the first sub-stream 114 by a duration of  $\sim T_S$ , and decimator elements (not shown) could remove every other sample from the copies of the first sub-stream 114.

[0082] A clock signal 320 operating at  $\sim \frac{1}{8}F_S$  (and therefore having a period of  $\sim 8T_S$ ) is provided to the sub-sub-DAC components 304, 306. The  $\sim \frac{1}{8}F_S$  clock signal 320 provided to the odd sub-sub-DAC component 306 has a  $90^\circ$  phase offset relative to the  $\sim \frac{1}{8}F_S$  clock signal 320 provided to the even sub-sub-DAC component 304. The even sub-sub-DAC component 304 samples the first sub-sub-stream 314 at rising edges and falling edges of the  $\sim \frac{1}{8}F_S$  clock signal 320, thus converting the first sub-sub-stream 314 into a first sub-sub-stream 324 of analog samples  $\{A_0, A_4, A_8, \dots\}$ . The odd sub-DAC component 306 samples the second sub-sub-stream 316 at rising edges and falling edges of the  $90^\circ$  phase offset  $\sim \frac{1}{8}F_S$  clock signal 320, thus converting the second sub-sub-stream 316 into a second sub-sub-stream 326 of analog samples  $\{A_1, A_5, A_9, \dots\}$ .

[0083] The  $\sim \frac{1}{4}F_S$  clock signal 120 is provided to the AMUX component 310. The AMUX component 310 is controlled by rising edges and falling edges of the  $\sim \frac{1}{4}F_S$  clock signal 120, switching between an “even” state in which the first sub-sub-stream 324 of analog samples  $\{A_0, A_4, A_8, \dots\}$  contributes a single analog sample to the first sub-stream 124 and an “odd” state in which the second sub-sub-stream 326 of analog samples  $\{A_1, A_5, A_9, \dots\}$  contributes a single analog sample to the first sub-stream 124. The resulting first sub-stream 124 of analog samples  $\{A_0, A_1, A_4, A_5, A_8, A_9, \dots\}$  contains one analog sample in each time period of duration  $\sim 2T_S$ .

[0084] The  $\sim \frac{1}{4}F_S$  clock signal 120 is offset by approximately  $90^\circ$  phase from double the  $\sim \frac{1}{8}F_S$  clock signal 320. The  $\sim \frac{1}{4}F_S$  clock signal 120 is intentionally timed so that no data transition occurs between analog samples in the first sub-sub-stream 324 while the AMUX component 310 is in the “even” state, and no data transition occurs between analog samples in the second sub-sub-stream 326 while the AMUX component 310 is in the “odd” state.

Stated differently, all samples in the first sub-stream 124 are captured from stable portions of the sub-sub-streams 324 and 326.

[0085] FIG. 12 illustrates an example sub-DAC 350 that is operative to convert digital samples into analog samples. The sub-DAC 350 may optionally be used as the “negative” sub-DAC 106 in DAC 100 or DAC 150 to convert the second sub-stream 116 of digital samples  $\{D_2, D_3, D_6, D_7, \dots\}$  into the second sub-stream 126 of analog samples  $\{A_2, A_3, A_6, A_7, \dots\}$  at a sampling rate of  $\frac{1}{2}F_S$ .

[0086] FIG. 13 is a timing diagram of clock signals and data signals in the sub-DAC 350.

[0087] The sub-DAC 350 comprises an “even” sub-sub-DAC component 354, an “odd” sub-sub-DAC component 356, and an analog multiplexer (AMUX) component 360. The AMUX component 360 has two inputs (coupled to the outputs of the sub-sub-DAC components 354, 356) and a single output (the second sub-stream 126).

[0088] The even sub-sub-DAC component 354 receives as input a first sub-sub-stream 364 of digital samples  $\{D_2, D_6, D_{10}, \dots\}$ , and the odd sub-sub-DAC component 356 receives as input a second sub-sub-stream 366 of digital samples  $\{D_3, D_7, D_{11}, \dots\}$ . A partitioning module 362 is operative to partition the second sub-stream 116 of digital samples into the first sub-sub-stream 364 and the second sub-sub-stream 366, using any suitable technique. For example, the second sub-stream 116 could be duplicated, a delay buffer (not shown) could delay one copy of the second sub-stream 116 by a duration of  $\sim T_S$ , and decimator elements (not shown) could remove every other sample from the copies of the second sub-stream 116.

[0089] The  $\sim \frac{1}{8}F_S$  clock signal 320 is provided to the sub-sub-DAC components 354, 356. The  $\sim \frac{1}{8}F_S$  clock signal 320 provided to the odd sub-sub-DAC component 356 has a  $90^\circ$  phase offset relative to the  $\sim \frac{1}{8}F_S$  clock signal 320 provided to the even sub-sub-DAC component 354. The even sub-sub-DAC component 354 samples the first sub-sub-stream 364 at rising edges and falling edges of the  $90^\circ$  phase offset  $\sim \frac{1}{8}F_S$  clock signal 320, thus converting the first sub-sub-stream 364 into a first sub-sub-stream 374 of analog samples

{A<sub>2</sub>, A<sub>6</sub>, A<sub>10</sub>, ...}. The odd sub-DAC component 356 samples the second sub-sub-stream 366 at rising edges and falling edges of the  $\sim\frac{1}{8}F_S$  clock signal 320, thus converting the second sub-sub-stream 366 into a second sub-sub-stream 376 of analog samples {A<sub>3</sub>, A<sub>7</sub>, A<sub>11</sub>, ...}.

[0090] The  $\sim\frac{1}{4}F_S$  clock signal 120 is provided to the AMUX component 360. The AMUX component 360 is controlled by rising edges and falling edges of the  $\sim\frac{1}{4}F_S$  clock signal 120, switching between an “even” state in which the first sub-sub-stream 374 of analog samples {A<sub>2</sub>, A<sub>6</sub>, A<sub>10</sub>, ...} contributes a single analog sample to the second sub-stream 126 and an “odd” state in which the second sub-sub-stream 376 of analog samples {A<sub>3</sub>, A<sub>7</sub>, A<sub>11</sub>, ...} contributes a single analog sample to the second sub-stream 126. The resulting second sub-stream 126 of analog samples {A<sub>2</sub>, A<sub>3</sub>, A<sub>6</sub>, A<sub>7</sub>, A<sub>10</sub>, A<sub>11</sub>, ...} contains one analog sample in each time period of duration  $\sim 2T_S$ .

[0091] The  $\sim\frac{1}{4}F_S$  clock signal 120 is offset by approximately 90° phase from double the  $\sim\frac{1}{8}F_S$  clock signal 320. The  $\sim\frac{1}{4}F_S$  clock signal 120 is intentionally timed so that no data transition occurs between analog samples in the first sub-sub-stream 374 while the AMUX component 360 is in the “even” state, and no data transition occurs between analog samples in the second sub-sub-stream 376 while the AMUX component 360 is in the “odd” state. Stated differently, all samples in the second sub-stream 126 are captured from stable portions of the sub-sub-streams 374 and 376.

[0092] Use of the sub-DACs 300 and 350 in the DAC 100 or in the DAC 150 will increase resilience to distortions as well as to time mismatches between sub-DACs, at a cost of increased complexity. The increased complexity involves providing a clock signal at approximately one quarter of the sampling rate ( $\sim\frac{1}{4}F_S$ ), and the increased complexity may be deemed acceptable.

[0093] The following time-table is helpful for understanding use of the sub-DACs 300 and 350 in the operation of the DAC 100.

Time/Ts	[0,1)	[1,2)	[2,3)	[3,4)	[4,5)	[5,6)	[6,7)	[7,8)
sub-sub-stream 324	A <sub>0</sub>		A <sub>4</sub>			A <sub>8</sub>		
sub-sub-stream 326	A <sub>1</sub>				A <sub>5</sub>			
AMUX 310 state	“even”	“odd”		“even”		“odd”		“even”
sub-stream 124	A <sub>0</sub>	A <sub>1</sub>		A <sub>4</sub>		A <sub>5</sub>		A <sub>8</sub>
sub-sub-stream 374	A <sub>2</sub>		A <sub>6</sub>			A <sub>10</sub>		
sub-sub-stream 376	A <sub>3</sub>				A <sub>7</sub>			
AMUX 360 state	“even”	“odd”		“even”		“odd”		“even”
sub-stream 126	A <sub>2</sub>	A <sub>3</sub>		A <sub>6</sub>		A <sub>7</sub>		A <sub>10</sub>
sub-stream 144 (delayed by Ts relative to sub-stream 124)	A <sub>0</sub>		A <sub>1</sub>		A <sub>4</sub>		A <sub>5</sub>	
sub-stream 146 (delayed by 3Ts relative to sub-stream 126)			A <sub>2</sub>		A <sub>3</sub>		A <sub>6</sub>	
switch 110 state			“positive”		“negative”		“positive”	
output 18			A <sub>0</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	A <sub>4</sub>	A <sub>5</sub>
							A <sub>6</sub>	

Table 3

[0094] Sub-DACs similar to the sub-DACs 300 and 350 could be used as the “positive” sub-DAC, “zero” sub-DAC, and “negative” sub-DAC in the DAC 200 or in the DAC 250.

[0095] FIG. 14 is a block diagram illustration of an example transmitter 400 that employs polarization-division multiplexing (PDM). A laser 402 is operative to generate a continuous wave (CW) optical carrier 404. A polarizing beam splitter 406 is operative to split the CW optical carrier 404 into orthogonally-polarized components 408, 410 (nominally referred to as the “X-polarization” component and the “Y-polarization” component) that are modulated by respective electrical-to-optical modulators 412, 414 to produce modulated polarized optical signals 416, 418 that are combined by a beam combiner 420, thus yielding an optical signal 422.

[0096] A symbol source 424 is operative to generate a stream of symbols representing data to be transmitted in the optical signal 422. A digital signal processor (DSP) 426 is operative to process the symbols output from the symbol source 424, for example, performing one or

more of pulse shaping, subcarrier multiplexing, chromatic dispersion pre-compensation, and distortion pre-compensation on the symbols. The DSP 426 is operative to generate I and Q digital drive signals 432 for the X-polarization to be converted by a DAC 434 into I and Q analog drive signals 436 for the X-polarization that, after amplification by amplifiers 438, are used to drive the electrical-to-optical modulator 412. The DSP 426 is operative to generate I and Q digital drive signals 442 for the Y-polarization to be converted by a DAC 444 into I and Q analog drive signals 446 for the Y-polarization that, after amplification by amplifiers 448, are used to drive the electrical-to-optical modulator 414.

[0097] The DACs described in this document could be used as the DAC 434 and the DAC 444. For example, the I and Q digital drive signals 432 for the X-polarization may be the input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  and the I and Q analog drive signals 436 for the X-polarization may be the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$ . For example, the I and Q digital drive signals 442 for the Y-polarization may be the input stream 102 of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  and the I and Q analog drive signals 446 for the Y-polarization may be the output stream 18 of analog samples  $\{A_0, A_1, A_2, A_3, \dots\}$ .

[0098] Stated differently, each of the DAC 434, 444 may comprise two or more sub-DACs, and the streams of analog samples that are output from the two or more sub-DACs may be provided as inputs to a controlled switch that is a specific example of the controlled switch 10 described with respect to FIG. 1. In some implementations, a sub-DAC may employ the architecture described with respect to FIG. 10 or FIG. 12.

[0099] In some implementations, the DSP 426 and the DACs 434, 444 are comprised in a CMOS module, and the amplifiers 438, 448 are comprised in a BiCMOS module.

[0100] In other implementations, when the interconnect between blocks does not support the full bandwidth, the controlled switches of the DACs 434, 444 may be separate from the CMOS module that comprises the DSP 426 and the other components (including the sub-DACs) of the DACs 434, 444. For example, the controlled switches may be comprised in another CMOS module, or a BiCMOS module, or HBT. For example, the controlled switches may be co-packaged with the electrical-to-optical modulator 412, 414 or the driver.

[0101] For simplicity of explanation, perfect analog switches were used in the examples, with a square clock. At high frequencies, the clock will generally consist of a fundamental along with one or two harmonics. The controlled switch may be implemented with nonlinear electrical, electro-optic, or optical elements, such as CMOS field effect transistors (FETs) or diodes, bipolar transistors or diodes, heterojunction bipolar transistors (HBTs), electro-absorption (EA) modulators, phase modulators, or semiconductor optical amplifier (SOA) structures. The switching function may be substantially a multiplication by the clock voltage or may include strong nonlinear functional terms.

[0102] The techniques described in this document may be used to convert integer sub-streams into a voltage stream, in CMOS. However, other instantiations may be used. For example, current sub-streams may be converted to an optical E-Field stream, as was described in US Patent No. 7277603 to Roberts et al. An integer sub-stream may be combined with a voltage sub-stream to produce a voltage stream. The analog characteristic of the stream that is being created may be an optical or electrical phase, or other modulation of an input analog signal.

[0103] A series of integer values that represent a time-series signal may be instantiated in parallel circuits or any other pre-determined pattern.

[0104] The scope of the claims should not be limited by the details set forth in the examples, but should be given the broadest interpretation consistent with the description as a whole.

**What is claimed is:**

## 1. A method comprising:

partitioning an input stream of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into  $N$  sub-streams, wherein  $N$  is an integer greater than or equal to two, such that the first sub-stream includes a first pair of adjacent digital samples  $\{D_0, D_1\}$  from the input stream and each subsequent  $N$ th pair of adjacent digital samples  $\{D_{2N}, D_{2N+1}\}$  from the input stream, and the second sub-stream includes a second pair of adjacent digital samples  $\{D_2, D_3\}$  from the input stream and each subsequent  $N$ th pair of adjacent digital samples  $\{D_{2N+2}, D_{2N+3}\}$  from the input stream;

for each of the  $N$  sub-streams

converting the sub-stream of digital samples into a respective sub-stream of analog samples such that each analog sample in the sub-stream of analog samples is captured from a stable portion of a corresponding digital sample in the sub-stream of digital samples, and where the sub-stream of analog samples contains one analog sample in each time period of duration  $\sim 2T_s$ ; and

providing the sub-stream of analog samples to a respective one of  $N$  inputs of a controlled switch, the controlled switch having a single output; and

controlling with a control signal the controlled switch to switch between  $N$  different states, the control signal having a period of  $\sim 2N T_s$ , where in each state a respective one of the  $N$  inputs is connected to the single output,

wherein while the controlled switch is in any one of the  $N$  different states, a data transition occurs between two adjacent analog samples in the sub-stream that is provided to the one of the  $N$  inputs that is connected to the single output, and

wherein the single output yields a high-bandwidth analog signal that contains one analog sample  $\{A_0, A_1, A_2, A_3, \dots\}$  in each time period of duration approximately  $T_s$ , and any pair of adjacent analog samples in any one of the  $N$  sub-streams substantially determines a corresponding pair of adjacent analog samples in the high-bandwidth signal.

2. The method as recited in claim 1, wherein  $N$  is equal to two.
3. The method as recited in claim 1, wherein  $N$  is equal to three.
4. The method as recited in claim 1, wherein  $N$  is equal to four.
5. The method as recited in any one of claims 1 to 4, wherein an order of the digital samples in the input stream is identical to an order of the analog samples in the high-bandwidth analog signal.
6. The method as recited in any one of claims 1 to 5, wherein converting the sub-stream of digital samples into a respective sub-stream of analog samples comprises:
  - partitioning the sub-stream of digital samples into a first sub-sub-stream of digital samples and a second sub-sub-stream of digital samples, the first sub-sub-stream consisting of the first digital sample of each of the pairs of adjacent digital samples in that sub-stream, and the second sub-sub-stream consisting of the second digital sample of each of the pairs of adjacent digital samples in that sub-stream;
  - converting the first sub-sub-stream of digital samples into a first sub-sub-stream of analog samples and providing the first sub-sub-stream of analog samples to a first input of an analog multiplexer component;
  - converting the second sub-sub-stream of digital samples into a second sub-sub-stream of analog samples and providing the second sub-sub-stream of analog samples to a second input of the analog multiplexer component; and
  - controlling the analog multiplexer component to produce one of the  $N$  sub-streams of analog samples by switching between a first state in which the first input is connected to a single output of the analog multiplexer component and a second state in which the second input is connected to the single output of the analog multiplexer component,
  - wherein no data transition occurs between analog samples in the first sub-sub-stream while the analog multiplexer component is in the first state, and no data transition occurs

between analog samples in the second sub-sub-stream while the analog multiplexer component is in the second state.

7. A digital-to-analog converter (DAC) apparatus comprising:

a partitioning module operative to partition an input stream of digital samples  $\{D_0, D_1, D_2, D_3, \dots\}$  into  $N$  sub-streams of digital samples, wherein  $N$  is an integer greater than or equal to two, such that the first sub-stream includes a first pair of adjacent digital samples  $\{D_0, D_1\}$  from the input stream and each subsequent  $N$ th pair of adjacent digital samples  $\{D_{2N}, D_{2N+1}\}$  from the input stream, and the second sub-stream includes a second pair of adjacent digital samples  $\{D_2, D_3\}$  from the input stream and each subsequent  $N$ th pair of adjacent digital samples  $\{D_{2N+2}, D_{2N+3}\}$  from the input stream;

$N$  sub-DACs each operative to convert a respective one of the  $N$  sub-streams of digital samples into a respective sub-stream of analog samples such that each analog sample in the sub-stream of analog samples is captured from a stable portion of a corresponding digital sample in the sub-stream of digital samples, and where the sub-stream of analog samples contains one analog sample in each time period of duration  $\sim 2T_s$ ; and

a controlled switch having  $N$  inputs and a single output, each of the  $N$  inputs coupled to an output of a respective one of the  $N$  sub-DACs to receive the sub-stream of analog samples produced by that sub-DAC, the controlled switch being switchable between  $N$  different states, where in each state a respective one of the  $N$  inputs is connected to the single output,

where, in operation, the controlled switch is controlled by a control signal having a period of  $\sim 2N T_s$  to switch between the  $N$  different states so that while the controlled switch is in any one of the  $N$  different states, a data transition occurs between two adjacent analog samples in the sub-stream of analog samples from the sub-DAC whose output is coupled to the input that is connected to the single output,

wherein the single output yields a high-bandwidth analog signal that contains one analog sample  $\{A_0, A_1, A_2, A_3, \dots\}$  in each time period of duration approximately  $T_s$ , and any pair of adjacent analog samples in any one of the  $N$  sub-streams substantially determines a corresponding pair of adjacent analog samples in the high-bandwidth analog signal.

8. The DAC apparatus as recited in claim 7, wherein  $N$  is equal to two.
9. The DAC apparatus as recited in claim 7, wherein  $N$  is equal to three.
10. The DAC apparatus as recited in claim 7, wherein  $N$  is equal to four.
11. The DAC apparatus as recited in any one of claims 7 to 10, wherein each of the  $N$  sub-DACs is driven by a clock at a rate identical to a rate of the control signal.
12. The DAC apparatus as recited in any one of claims 7 to 11, wherein each one of the  $N$  sub-DACs is driven by the control signal.
13. The DAC apparatus as recited in any one of claims 7 to 12, wherein the controlled switch comprises nonlinear electrical elements.
14. The DAC apparatus as recited in any one of claims 7 to 12, wherein the controlled switch comprises electro-optical elements.
15. The DAC apparatus as recited in any one of claims 7 to 12, wherein the controlled switch comprises optical elements.
16. The DAC apparatus as recited in any one of claims 7 to 15, wherein the input stream of digital samples comprises multi-bit digital values of in-phase and quadrature components of a target optical e-field modulation.
17. The DAC apparatus as recited in claim 16, wherein the high-bandwidth analog signal is suitable to control an effective length of a control region of an optical modulator.
18. The DAC apparatus as recited in any one of claims 7 to 17, wherein the partitioning module, the  $N$  sub-DACs, and the controlled switch are comprised in a single complementary metal-oxide-semiconductor (CMOS) module.

19. The DAC apparatus as recited in any one of claims 7 to 17, wherein the partitioning module and the  $N$  sub-DACs are comprised in a complementary metal-oxide-semiconductor (CMOS) module and the controlled switch is not comprised in the CMOS module.

20. The DAC apparatus as recited in claim 19, wherein the controlled switch is comprised in a separate CMOS module.

21. The DAC apparatus as recited in claim 19, wherein the controlled switch is comprised in a bipolar-CMOS (BiCMOS) module.

22. The DAC apparatus as recited in claim 19, wherein the controlled switch is comprised in a heterojunction bipolar transistor (HBT) module.

23. The DAC apparatus as recited in any one of claims 7 to 22, further comprising a linear digital filter to adapt the  $N$  sub-streams of digital samples.

24. The DAC apparatus as recited in any one of claims 7 to 23, wherein the partitioning module is operative to perform nonlinear compensation when generating the  $N$  sub-streams of digital samples.

25. The DAC apparatus as recited in any one of claims 7 to 24, further comprising an analog delay line operative to delay at least one of the  $N$  sub-streams of digital samples relative to at least another one of the  $N$  sub-streams of digital samples.

26. The apparatus as recited in any one of claims 7 to 25, wherein each of the  $N$  sub-DACs comprises:

a module to partition the respective one of the  $N$  sub-streams of digital samples into a first sub-sub-stream of digital samples and a second sub-sub-stream of digital samples, the first sub-sub-stream consisting of the first digital sample of each of the pairs of adjacent digital

samples in that sub-stream, and the second sub-sub-stream consisting of the second digital sample of each of the pairs of adjacent digital samples in that sub-stream;

an analog multiplexer component having a first input, a second input, and a single output;

a first sub-sub-DAC coupled to the first input, the first sub-sub-DAC operative to convert the first sub-sub-stream of digital samples into a first sub-sub-stream of analog samples; and

a second sub-sub-DAC coupled to the second input, the second sub-sub-DAC operative to convert the second sub-sub-stream of digital samples into a second sub-sub-stream of analog samples,

where, in operation, the analog multiplexer component is controlled to switch between a first state in which the first input is connected to the single output of the analog multiplexer component and a second state in which the second input is connected to the single output analog multiplexer component, and

wherein no data transition occurs between analog samples in the first sub-sub-stream while the analog multiplexer component is in the first state and no data transition occurs between analog samples in the second sub-sub-stream while the analog multiplexer component is in the second state.

27. The DAC apparatus as recited in claim 7, wherein  $N$  is equal to two and wherein the partitioning module is operative:

to reorder every four consecutive digital samples in the input stream as  $\{D_0, D_2, D_1, D_3, D_4, D_6, D_5, D_7, \dots\}$ ;

to apply a decimate-by-two function to the reordered samples to obtain the first sub-stream of digital samples  $\{D_0, D_1, D_4, D_5, \dots\}$ ; and

to delay a copy of the reordered samples by a delay of duration  $\sim T_S$  and then apply a decimate-by-two function to the delayed copy of the reordered samples to obtain the second sub-stream of digital samples  $\{D_2, D_3, D_6, D_7, \dots\}$ .

28. A transmitter comprising:

a symbol source operative to generate a stream of symbols representing data to be transmitted in an optical signal;

a digital signal processor (DSP) operative to process the symbols output from the symbol source and to generate first digital drive signals and second digital drive signals;

a first digital-to-analog converter (DAC) apparatus according to any one of claims 7 to 27, the first DAC apparatus operative to convert the first digital drive signals to first analog drive signals;

a second DAC apparatus according to any one of claims 7 to 27, the second DAC apparatus operative to convert the second digital drive signals to second analog drive signals;

a laser operative to generate an optical carrier;

a polarizing beam splitter operative to split the optical carrier into orthogonally-polarized components;

a first electrical-to-optical modulator operative to modulate one of the orthogonally-polarized components according to the first analog drive signals to produce a first modulated polarized optical signal;

a second electrical-to-optical modulator operative to modulate another of the orthogonally-polarized components according to the second analog drive signals to produce a second modulated polarized optical signal; and

a beam combiner operative to combine the first modulated polarized optical signal and the second polarized optical signal into the optical signal.

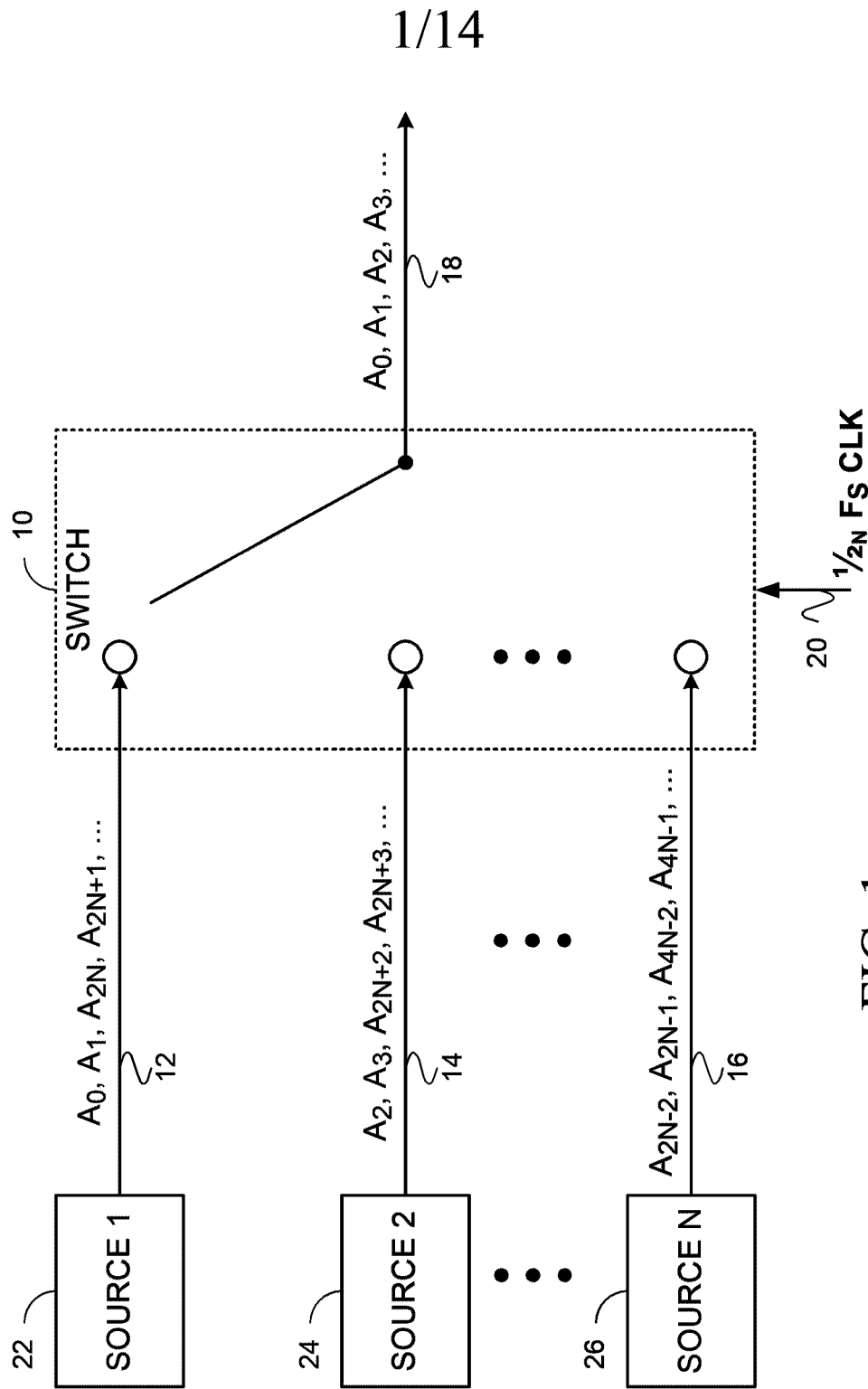


FIG. 1

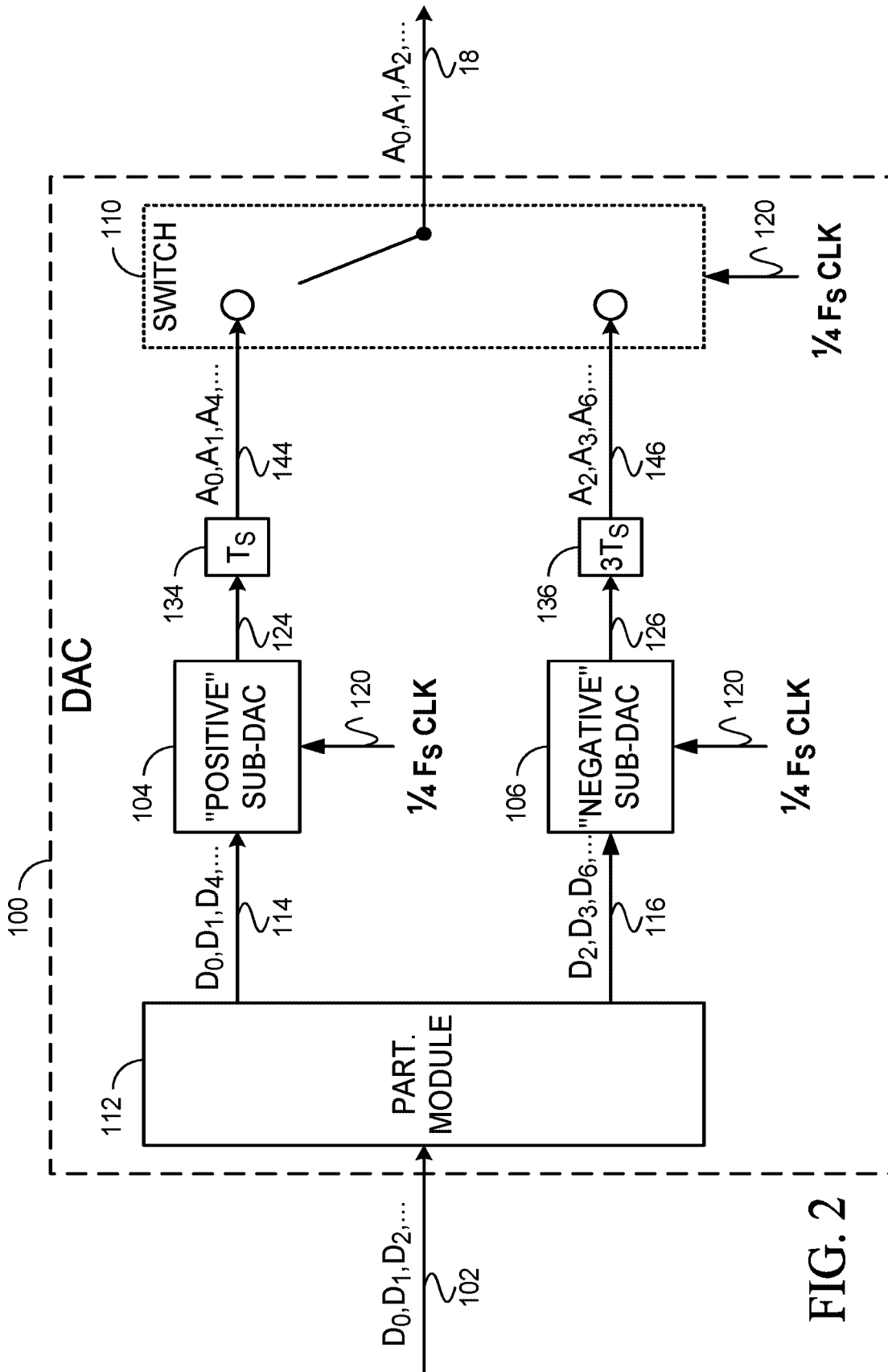


FIG. 2

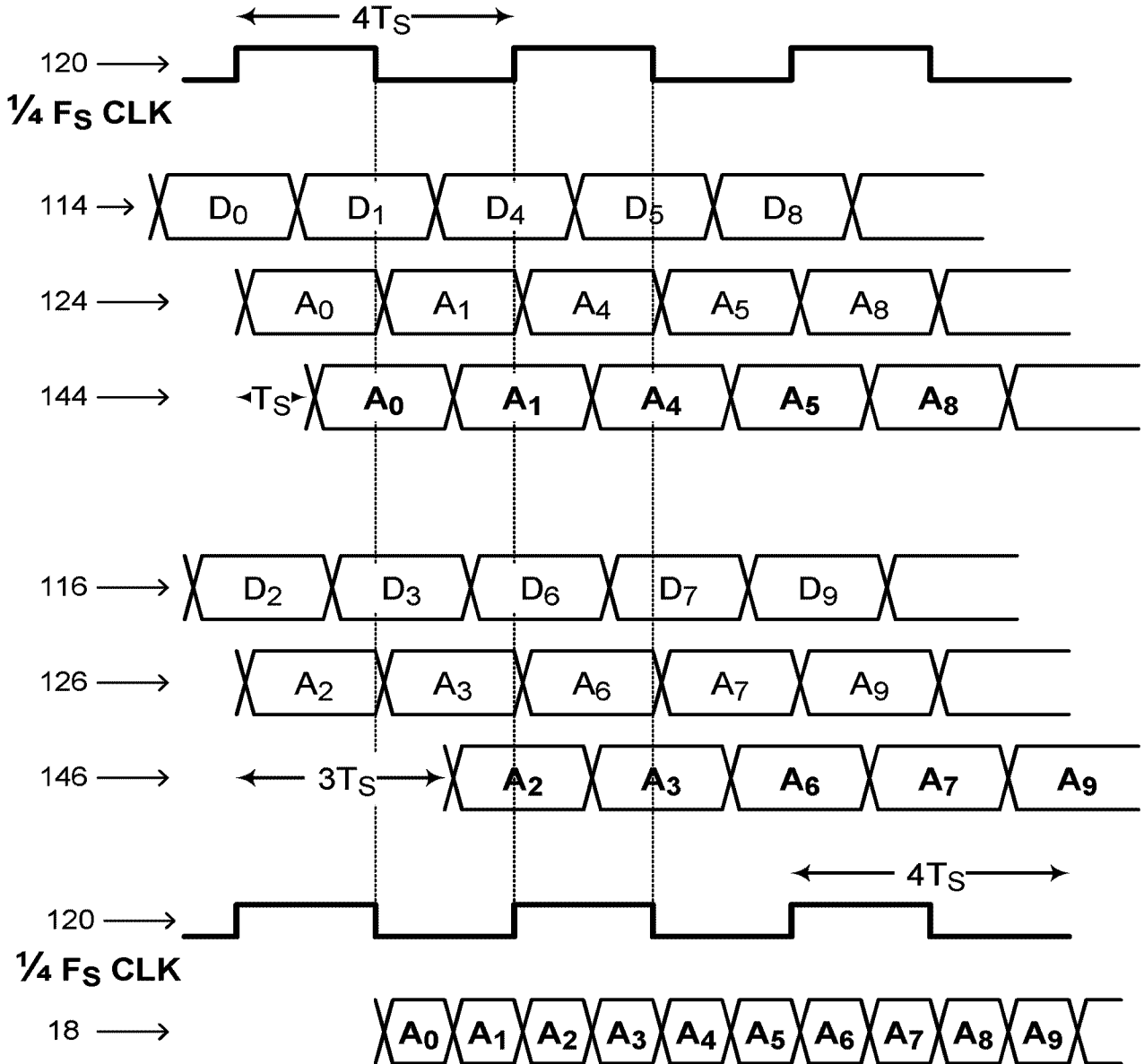


FIG. 3

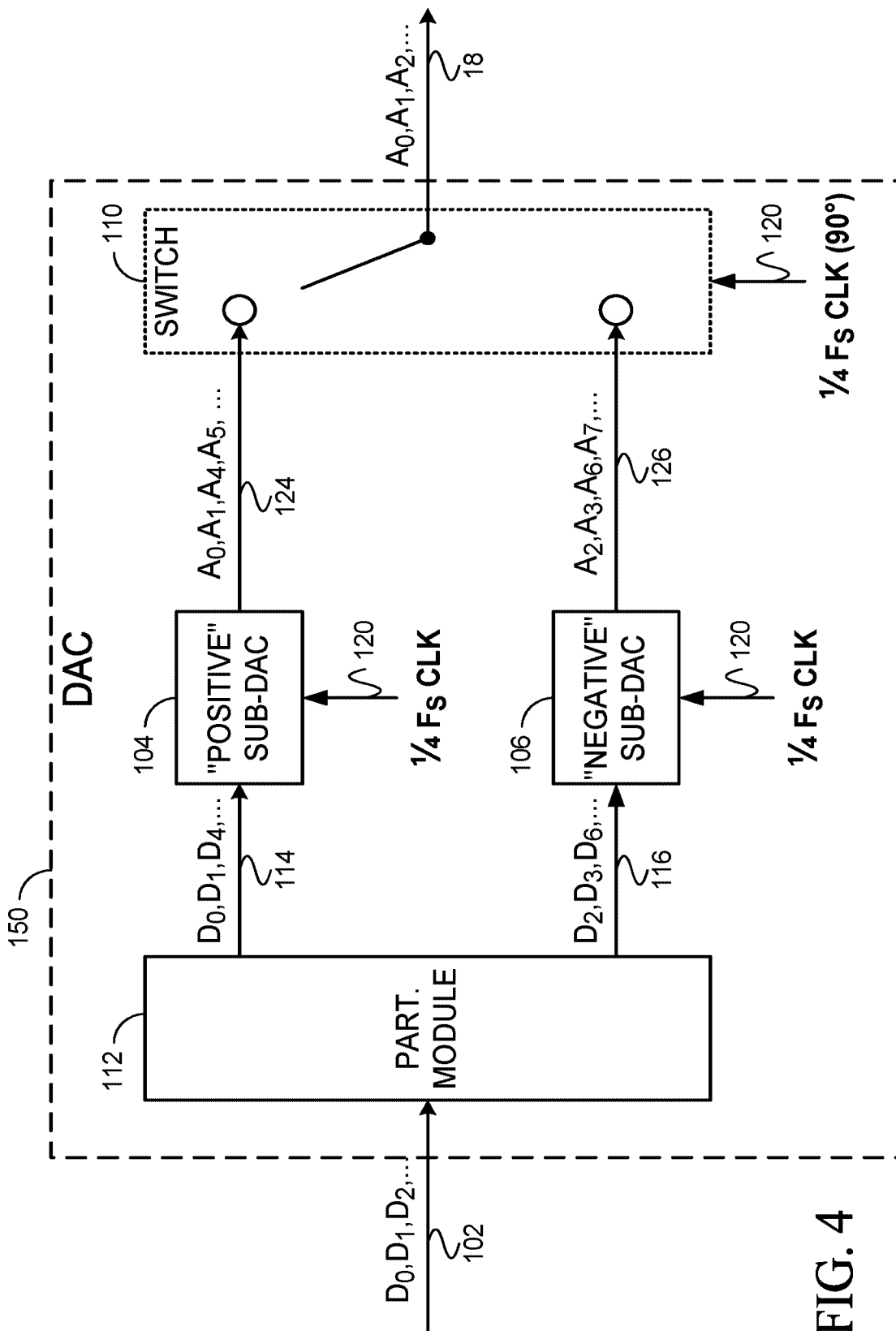


FIG. 4

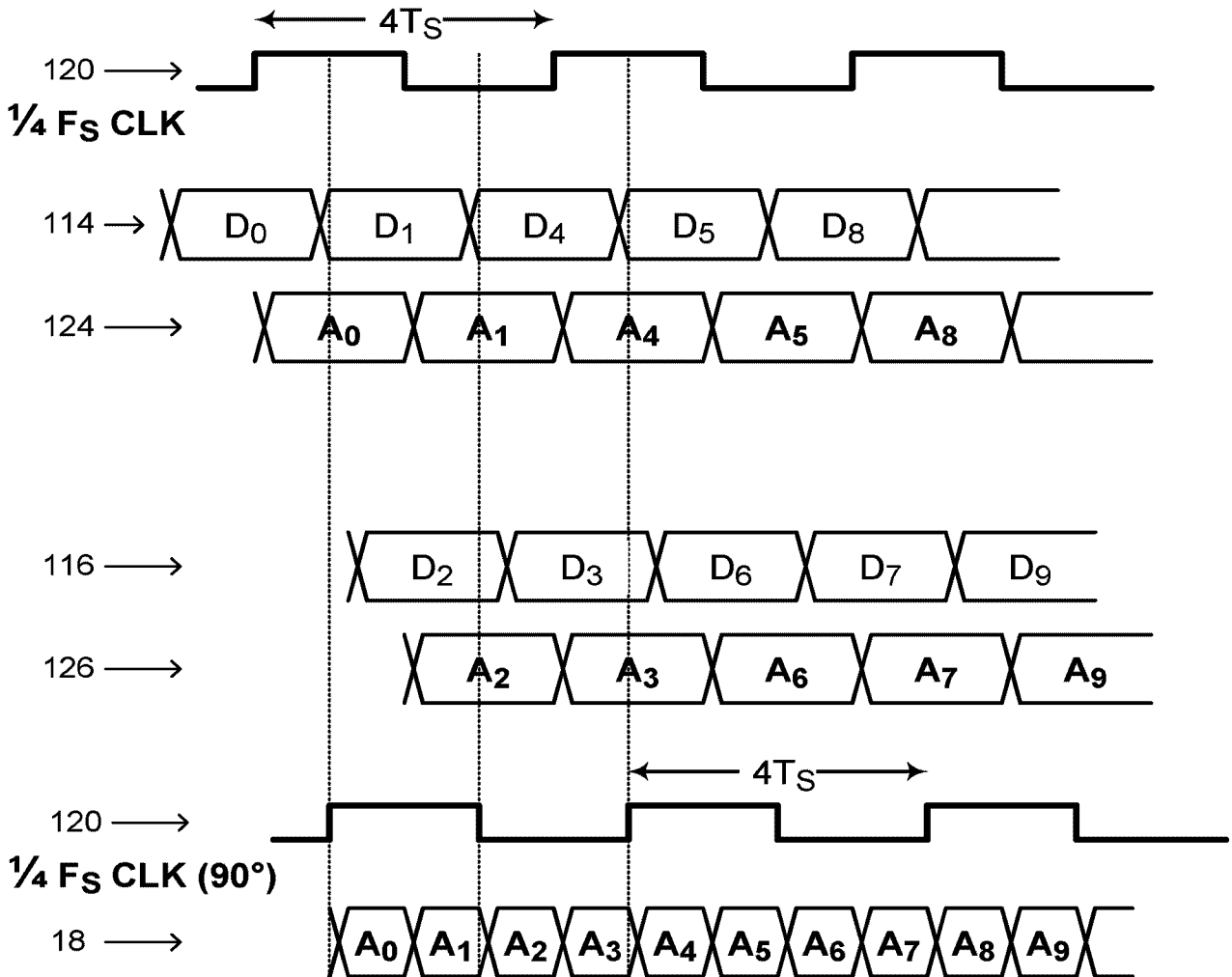


FIG. 5

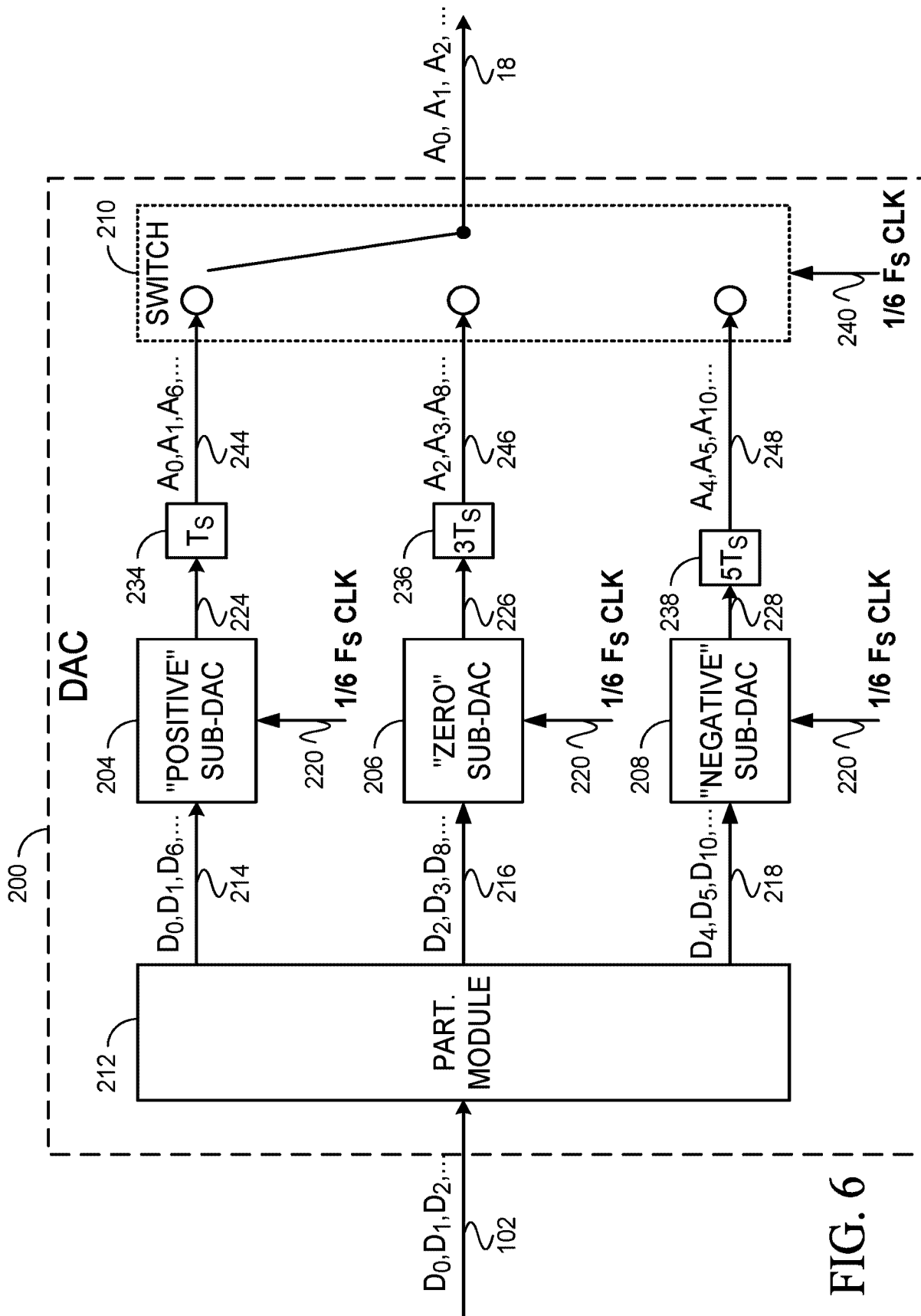


FIG. 6

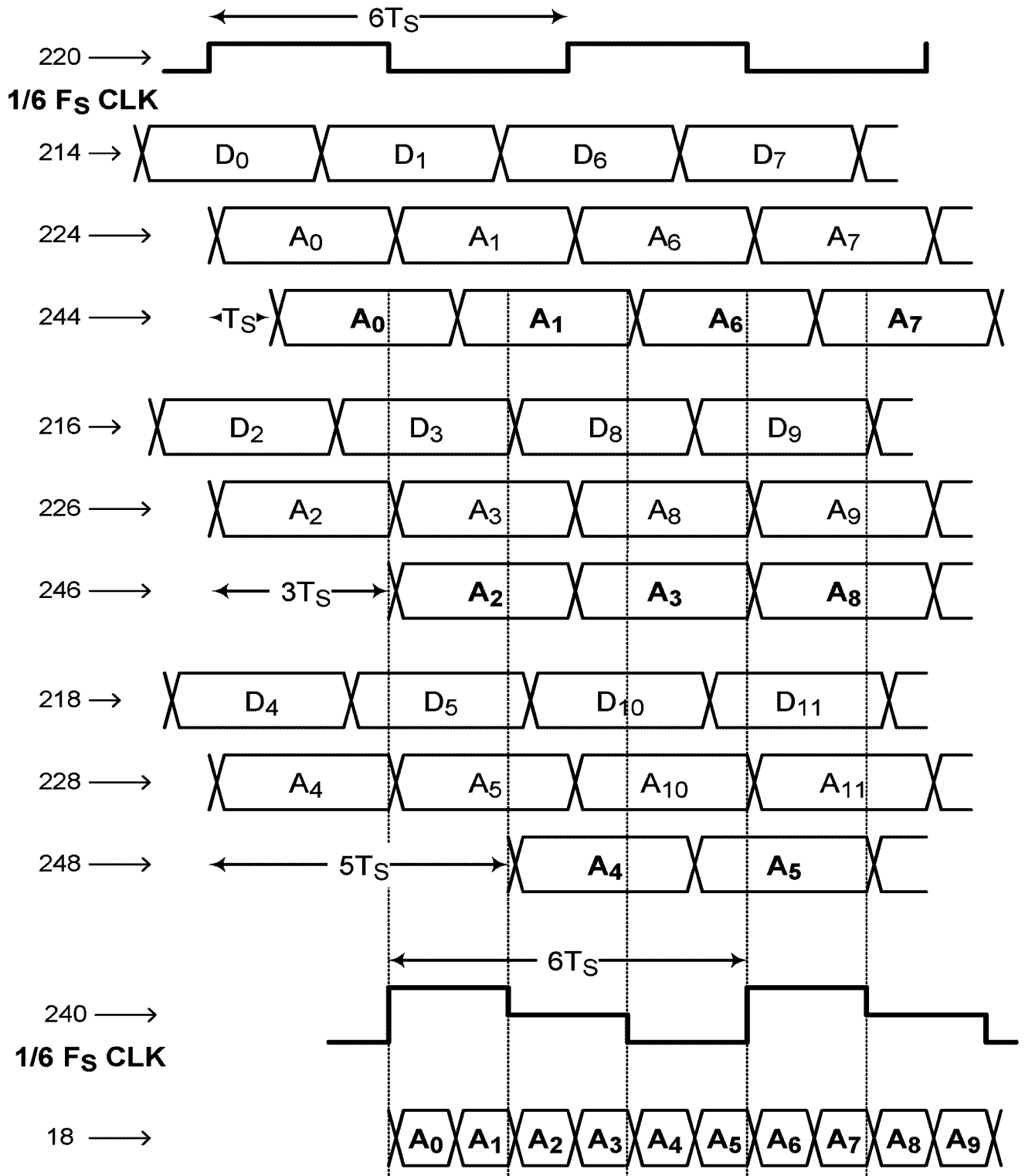


FIG. 7

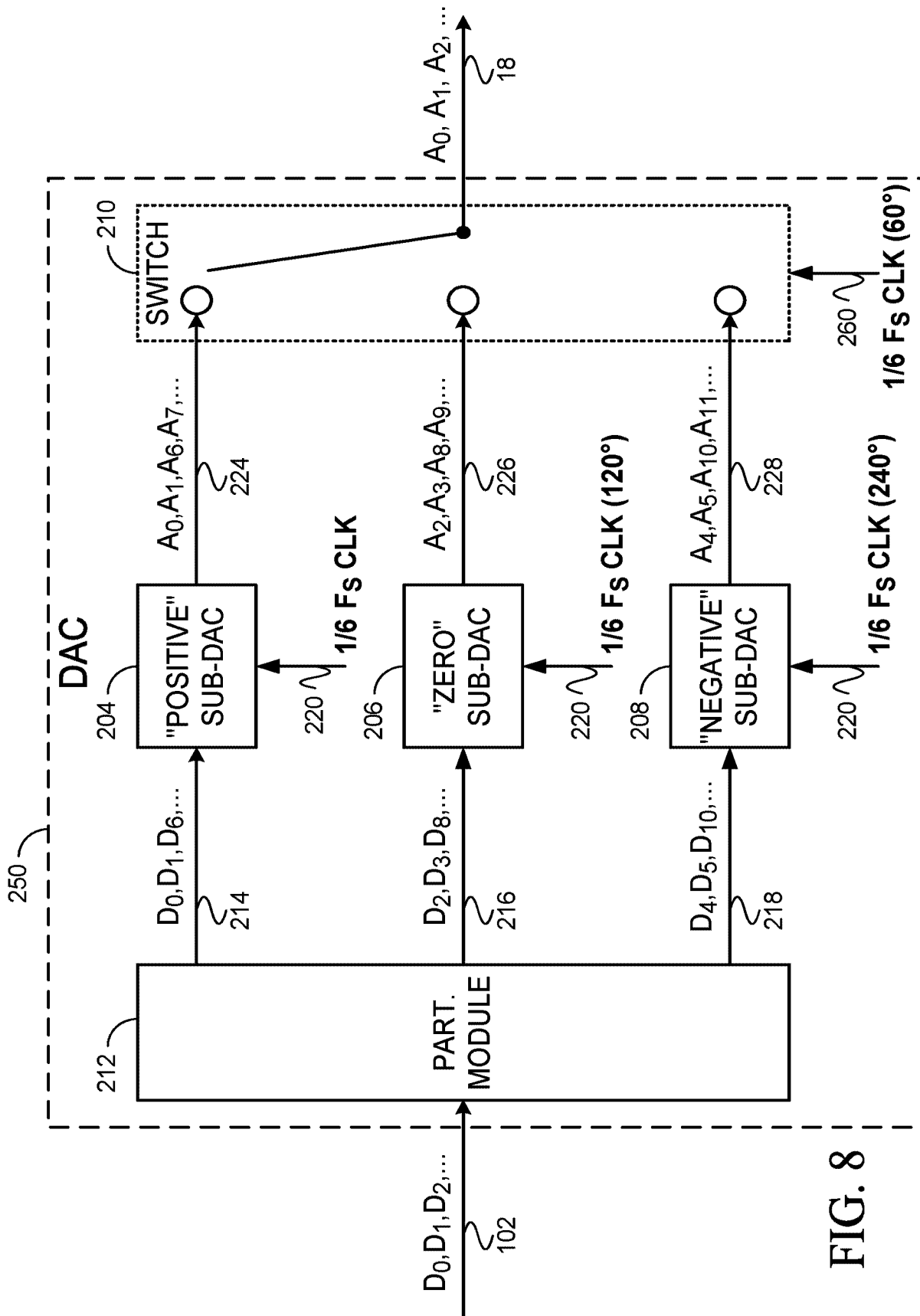


FIG. 8

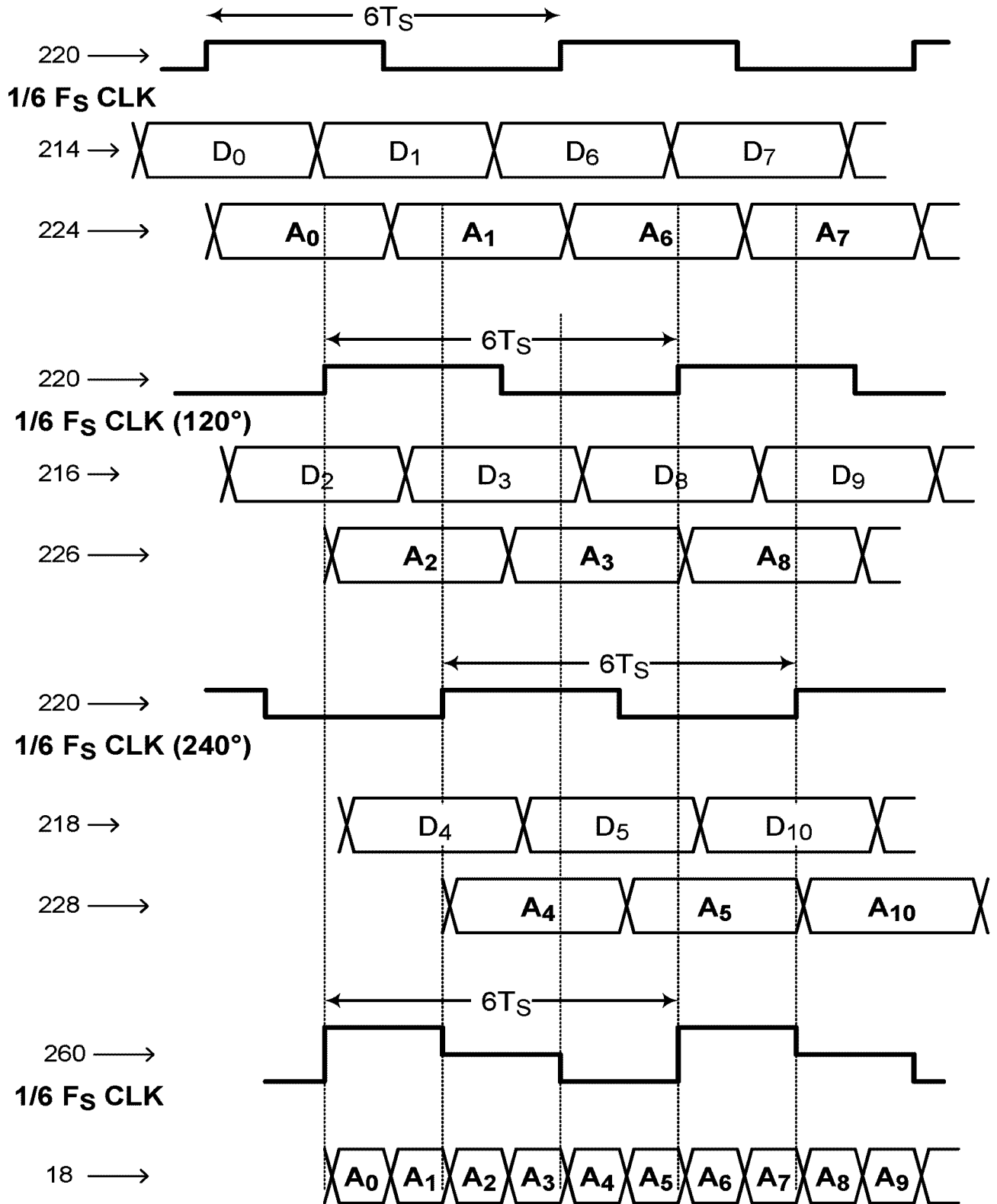


FIG. 9

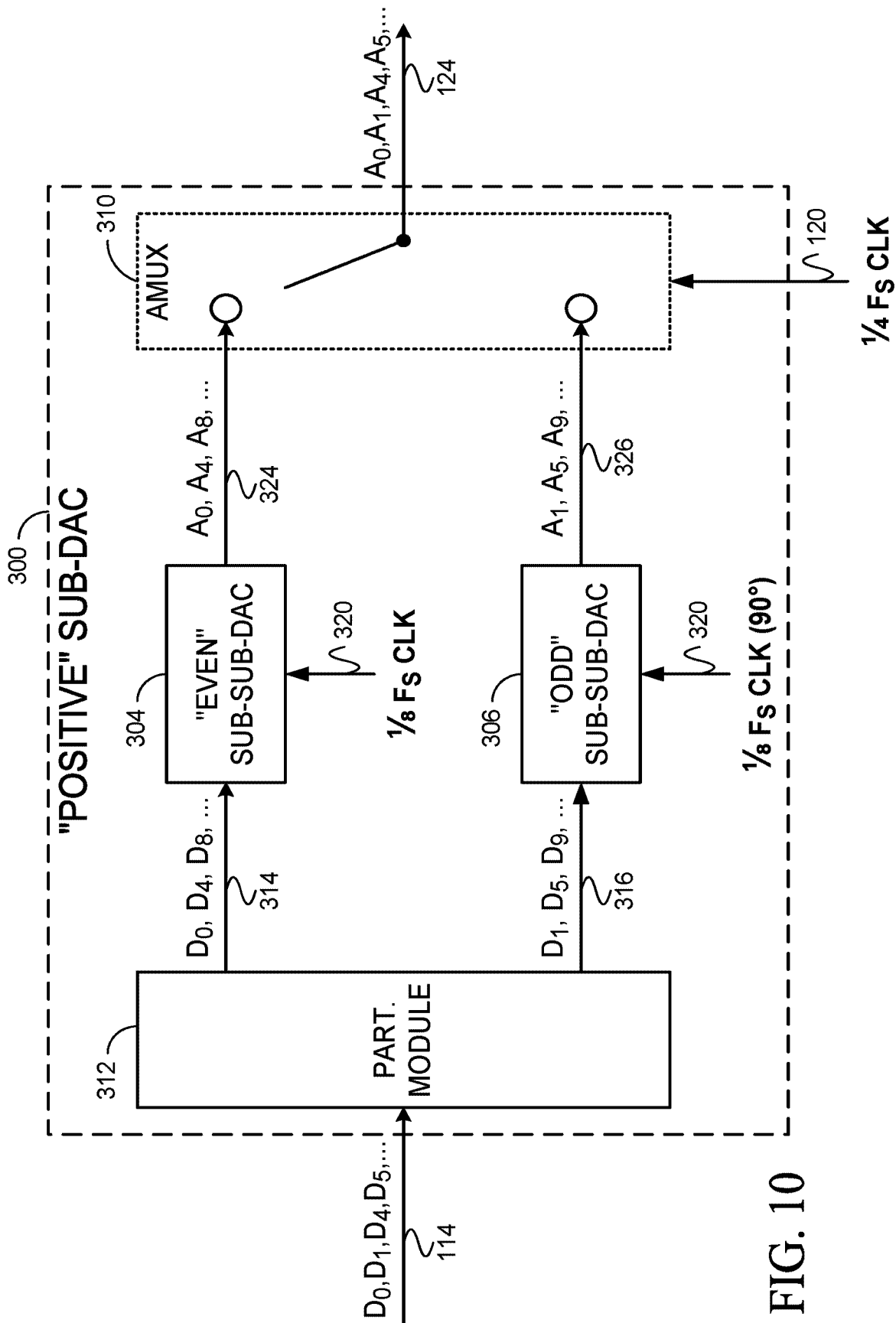


FIG. 10

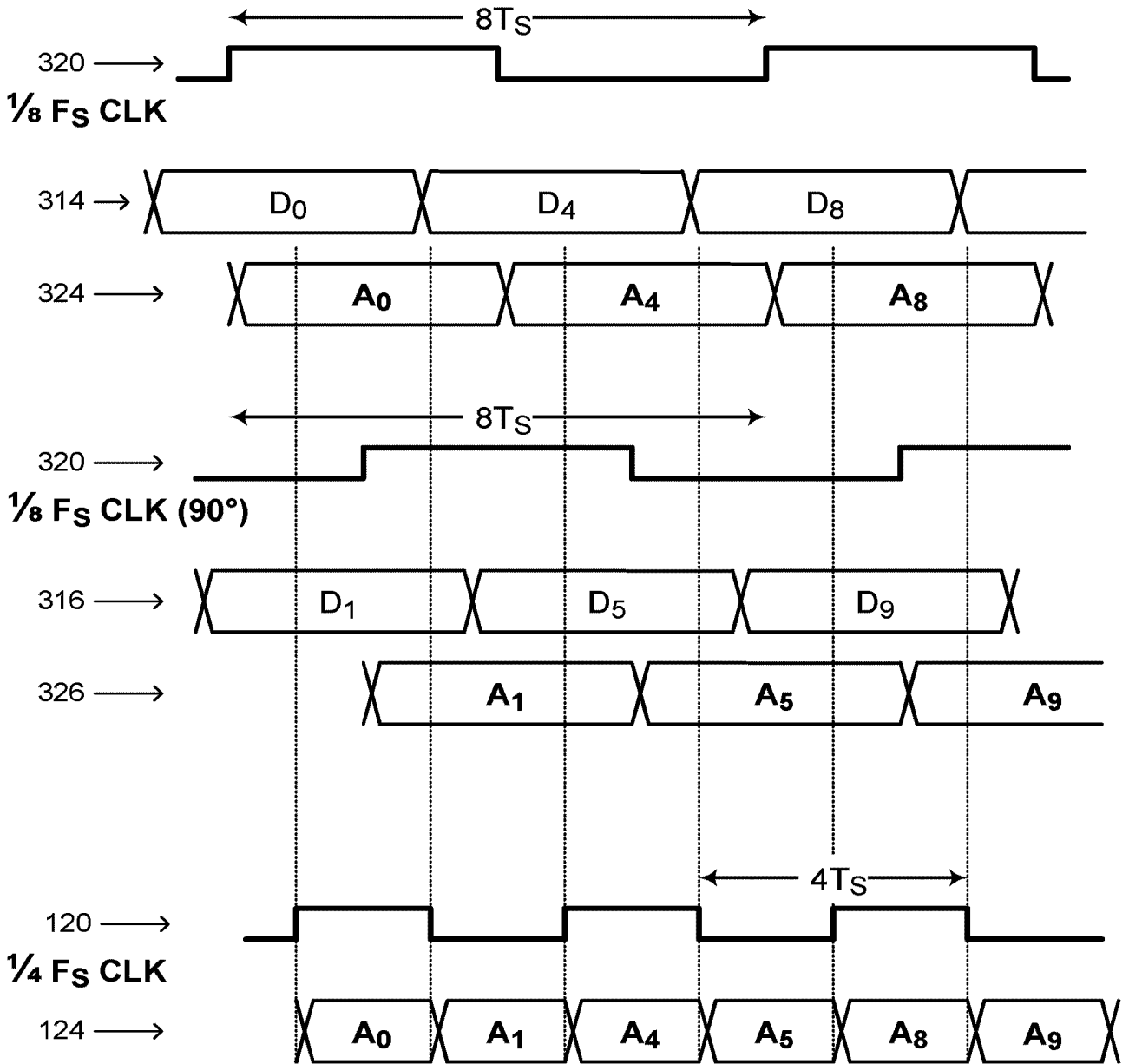


FIG. 11

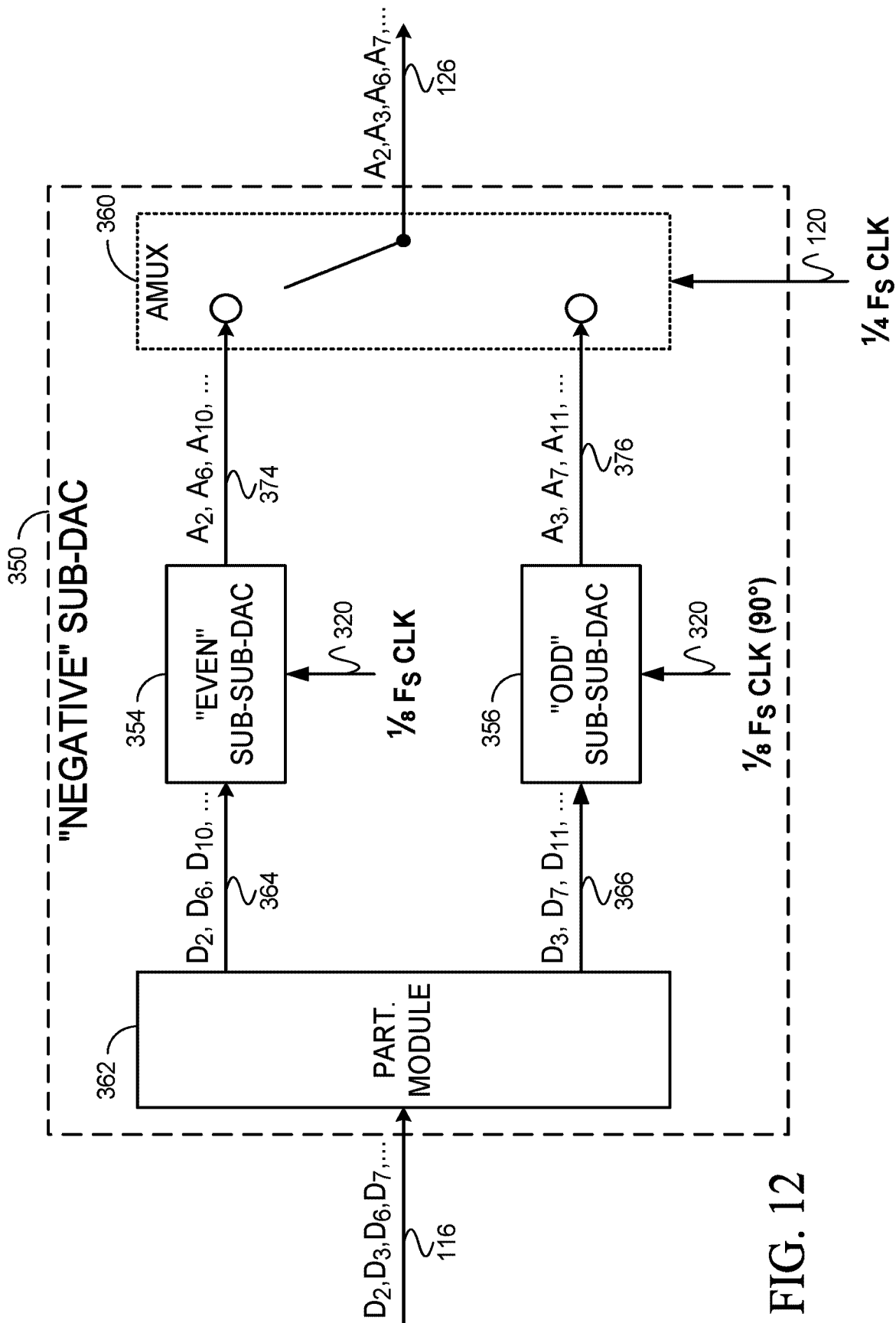


FIG. 12

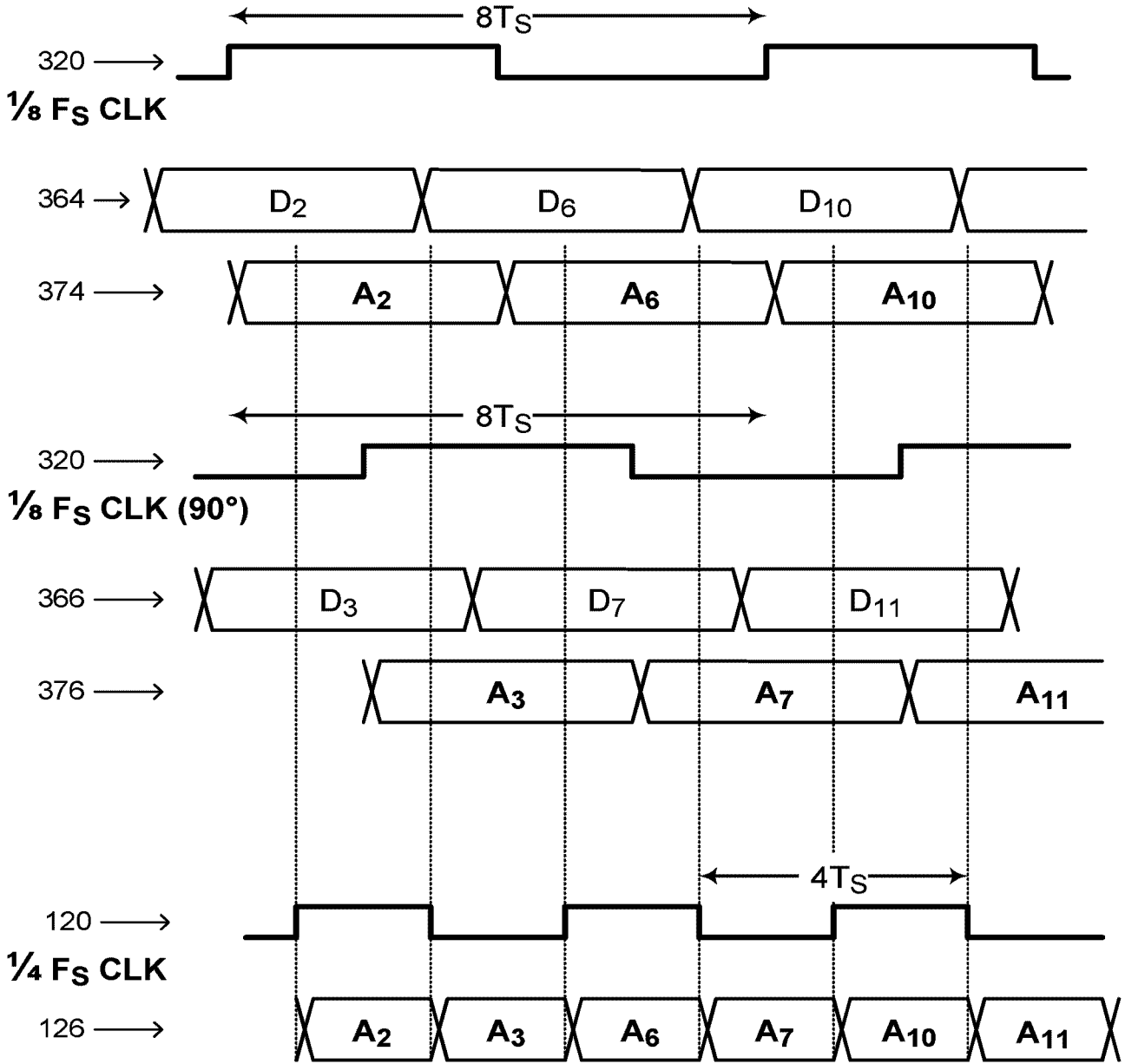


FIG. 13

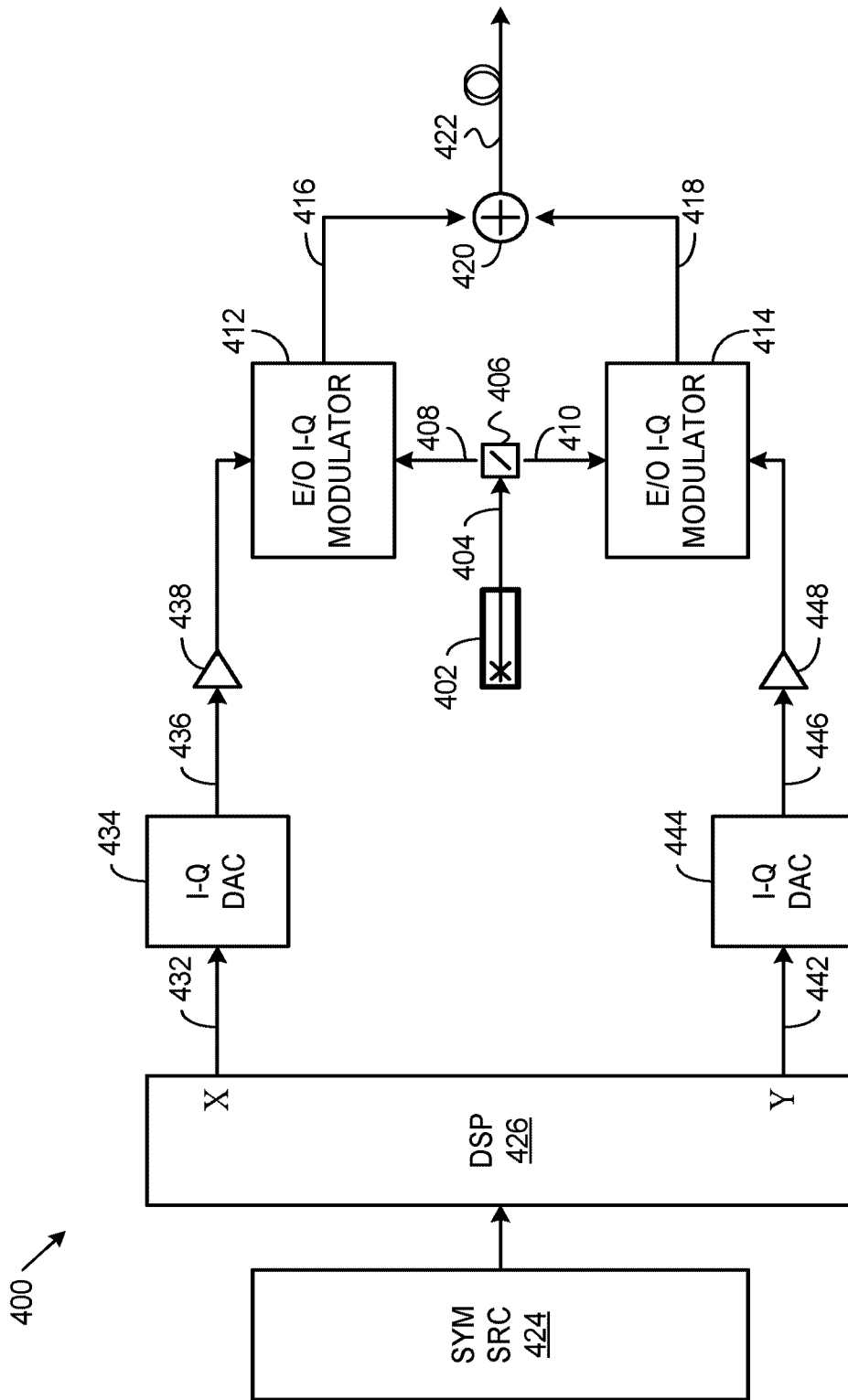


FIG. 14

