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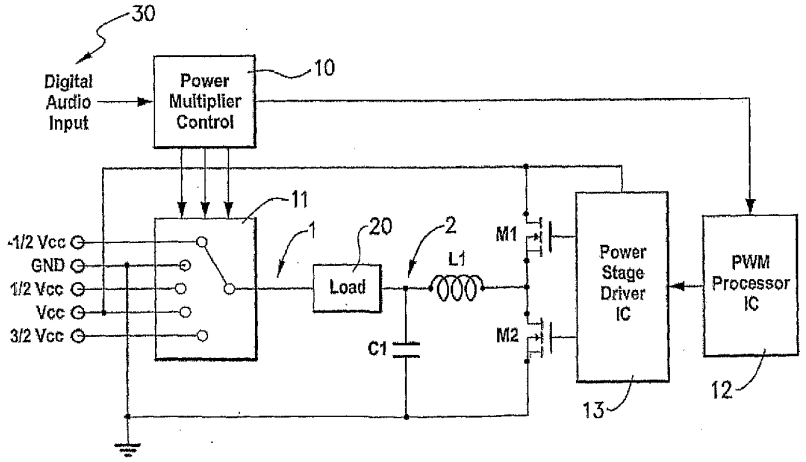
(54) **Title:** A POWER MULTIPLIER APPARATUS AND METHOD



(57) **Abstract:** A power multiplier apparatus for an amplifier comprises a power multiplier control stage (10), an amplifier stage (13) and a first switching stage (11) connectable to the power multiplier control stage (10). The amplifier stage (13) is connectable to the power multiplier control stage (10). The power multiplier apparatus has a first output terminal (1) and a second output terminal (2), the amplifier stage (13) is connectable to the second output terminal (2) for driving a load (20) connectable between the first 1 and second (2) output terminals. The first switching stage (11) is connectable to the first output terminal (1) to apply a switchable DC voltage level to the first output terminal (1). There is also disclosed a method of amplifying the power output of an amplifier apparatus.

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A POWER MULTIPLIER APPARATUS AND METHOD

The present invention relates to a power multiplier apparatus and method, and in particular such an apparatus for use in Class D digital amplifiers.

Currently, the typical maximum output power that can be derived from a conventional Class D digital amplifier is about 100 Watts to 200 Watts into a 4 Ohms load. There is a limitation on this maximum output power due to the semiconductors used in the amplifiers. It is desirable to keep the size of the integrated circuits used to make the amplifiers small to facilitate compact product design, but at the same time, there is also a demand for higher output power, which is especially desirable for Class D digital amplifiers due to their high efficiency.

In general, the invention provides a power multiplier apparatus and method in which the power of the apparatus is increased by restricting the range of the signal applied to a pulse width modulator stage, applying the output of a first switching stage to an output terminal of the apparatus and applying a switched potential to a further output of the apparatus to create a substantially undistorted output signal.

In accordance with one aspect of the present invention there is provided a power multiplier apparatus to which an input signal having an input signal amplitude is receivable, the power multiplier apparatus comprising: an amplifier stage having a peak amplitude input associable therewith, the peak amplitude input being associable with linear working range of the amplifier stage; a power multiplier control stage coupled to the amplifier stage, the power multiplier control stage receiving the input signal which input signal amplitude is multiplied and verified thereat, the input signal amplitude being multiplied to produce a multiplied amplitude which is verified in a manner so as to determine whether it exceeds the peak amplitude input, the multiplied amplitude being receivable at the amplifier stage; and a first switching stage connectable to said power

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multiplier control stage, the first switching stage being configured to reduce the multiplied amplitude when it exceeds the peak amplitude input, wherein the multiplied amplitude is reduced such that the multiplied amplitude does not exceed the peak amplitude input, thereby remaining within the linear working range of the amplifier stage.

In accordance with another aspect of the present invention there is provided a method of amplifying power output from a digital amplifier system having a first output terminal and a second output terminal, the method comprising the steps of: applying an input signal having an input signal amplitude to a power multiplier control stage within which one or more signals are producable; controlling an amplifier stage using one or more of said one or more signals, the amplifier stage having a peak amplitude input associable therewith, the peak amplitude input being associable with linear working range of the amplifier stage; multiplying the input signal amplitude at the power multiplier control stage to produce a multiplied amplitude; verifying the multiplied amplitude at the power multiplier control stage in a manner so as to determine whether it exceeds the peak amplitude input; and controlling a first switching stage using one or more signals from said power multiplier control stage in a manner so as to reduce the multiplied amplitude when it exceeds the peak amplitude input, wherein the multiplied amplitude is reduced such that the multiplied amplitude does not exceed the peak amplitude input, thereby remaining within the linear working range of the amplifier stage.

In one example, there is provided a power multiplier apparatus for an amplifier comprising:

a power multiplier control stage;

an amplifier stage; and

a first switch stage connectable to said power multiplier control stage; said amplifier stage being connectable to said power multiplier control stage; wherein said power multiplier apparatus has a first output terminal and a second output terminal, said amplifier stage being connectable to said second output

terminal for driving a load connectable between said first and second output terminals; and

wherein said first switching stage is connectable to said first output terminal to apply a switchable DC voltage level to said first output terminal.

In another example, there is provided a method of amplifying power output from a digital amplifier system having a first output terminal and a second output terminal, the method comprising the steps of:

applying an input signal to a power multiplier control stage;

producing one or more signals in said power multiplier control stage;

controlling an amplifier stage using one or more of said one or more signals;

driving said second output terminal via said amplifier stage;

controlling a first switching stage using one or more signals from said power multiplier control stage; and

selecting in said first switching stage one or more switchable DC voltage levels from a plurality of voltage levels; and

applying said one or more selected voltage levels to said first output terminal for producing a substantially undistorted waveform across a load connectable between said first and second output terminals.

The invention is described, by way of non-limiting example only, with reference to the accompanying drawings in which:

Figure 1 is a schematic block diagram of a conventional Class D digital amplifier configuration;

Figure 2 is a schematic circuit diagram of an amplifier according to an example;

Figure 3 is a waveform of an output signal at node 2 in the circuit of Figure 2;

Figure 4 is a waveform of a signal at node 1 in the circuit of Figure 2;

Figure 5 is a waveform of a signal present across the load in the circuit of Figure 2 and a waveform of a signal from a conventional bridge-tied load (BTL) amplifier;

Figure 6 is a representation of the waveforms across the load, at node 2 and at node 1 in the circuit of Figure 2;

Figure 7 is a schematic circuit diagram of an amplifier according to a further example;

Figure 8 is a waveform of an output signal at node 2 in the circuit of Figure 7;

Figure 9 is a waveform of a signal at node 1 in the circuit of Figure 7;

Figure 10 is a representation of the waveforms across the load, at node 2 and at node 1 in the circuit of Figure 7;

Figure 11 is a schematic circuit diagram of an amplifier according to another example;

Figure 12 is a schematic representation of the pulse width modulated signal for DC modulated voltages from the pulse width modulator in the circuit of Figure 11;

Figure 13 is a schematic circuit diagram of an amplifier according to another example;

Figure 14 schematic representation of the pulse width modulated signal for DC modulated voltages from the pulse width modulator in the circuit of Figure 13;

Figure 15 is a schematic circuit diagram of an amplifier according to yet another example; and

Figure 16 is a schematic circuit diagram of another further example operating in analogue mode.

Figure 1 shows a block diagram of a conventional Class D digital amplifier system driving a speaker load, in a single channel within a BTL configuration.

The system comprises a pulse width modulator integrated circuit 4, a power stage driver integrated circuit 5, and a MOSFET H-bridge stage 6 driving a load 7. The digital audio input signal is fed to the pulse width modulator circuit 4 and

the pulse width modulated signal output from the pulse width modulator circuit 4 is applied to the power stage driver 5. The output of the power stage driver 5 drives the MOSFET H-bridge stage 6 which in turn drives the load 7.

The peak amplitude of the digital input signal in the system of Figure 1 to produce the maximum undistorted output to the load 7 (V_{cc} volts peak-to-peak) may be denoted as A. In this configuration, the main limitation on the output power is due to the power handling capability of the power stage driver IC 5.

Figure 2 illustrates a system according to a first example and comprises a power multiplier control stage 10, a switching stage 11, a pulse width modulator stage 12, a power driver stage 13, two power MOSFETs M1, M2, an inductor L1, a capacitor C1, and a load 20. The pulse width modulator stage 12, the power driver stage 13, and the two power MOSFETs M1 and M2 form an amplifier stage.

In the system of Figure 2, the digital audio input signal 30 is applied to the power multiplier control stage 10 which multiplies the signal amplitude by, for example, 3 and checks the level of the signal. If the signal is below A, which is the peak amplitude of the digital input signal in a conventional Class D amplifier which will produce the maximum peak-to-peak undistorted output for a supply voltage V_{cc}, the switching stage 11 which is preferably a multiway switch will select the voltage 1/2 V_{cc}.

If the level of the signal exceeds A, the multiway switch 11 will switch to ground (GND) and a level A will be subtracted from the result of the input signal multiplied by 3. If the level exceeds 2A, the switch 11 will select the voltage -1/2 V_{cc} and a level 2A will be subtracted from the result of the signal multiplied by 3. In both cases, this result will be sent to the pulse width modulator stage 12 which is preferably a PWM processor IC. Thus the amplitude of the input to the PWM processor IC 12 is always kept below A so that no overflow will occur and the signal remains within the linear working range of the system.

The multiplied signal is applied to the pulse width modulator 12 to produce a train of width-modulated pulses which are then applied to the power driver stage 13.

Similarly, for the negative peak of the input signal 30, if the level of the signal exceeds –A or -2A, the Multiway Switch 11 will switch to V_{cc} or 3/2 V_{cc} respectively. Also, -A or -2A will be subtracted from the result of the signal multiplied by 3 and this result will be sent to the PWM processor IC 12.

The power driver stage 13 drives the two MOSFETs M1 and M2 which are coupled in series across a power supply V_{cc}. The junction of the two MOSFETs M1 and M2 is connected to a first end of the inductor L1. The output of L1 is coupled to one side of the capacitor C1 at a node 2 and also to one terminal of the load 20. The other side of the capacitor C1 is connected to ground. The digital outputs from the power multiplier control 10 are applied to the switching stage 11 which is also coupled to a range of voltage sources V_{cc}, $3/2V_{cc}$, $1/2V_{cc}$, ground and $-1/2V_{cc}$.

The switching stage 11 selects one of the voltage sources as determined by the power multiplier control unit 10 and the selected voltage level is applied to the second side of the load 20 at a node 1. The inductor L1 and the capacitor C1 form a low pass filter.

Figure 3 shows a plot of the signal at node 2 of the circuit of Figure 2 if a sinusoidal input signal of amplitude A is applied as the audio input signal 30.

Figure 4 shows a plot of the corresponding signal at Node 1. Figure 5 shows a plot of the corresponding overall signal across the load 20 in the system of Figure 2 and a waveform of a signal from a conventional bridge-tied load (BTL) amplifier. Figure 6 shows the signal at node 1, node 2 and across the load 20 in one plot using the system of Figure 2.

As shown in Figure 5, using the system of Figure 2, a peak amplitude of $1.5V_{cc}$ is achieved as compared to a conventional system of the type shown in Figure 1 in which a peak amplitude of V_{cc} is achieved, using the same integrated circuits in both cases. In terms of power, by using the system of Figure 2, the output power may be increased by, for example, 2.25 times the power from a conventional system of the type shown in Figure 1, and this is shown in the calculations below.

Original Output Power, $P_O = \frac{V_0^2}{R}$

Power Multiplier Output Power, $P_X = \frac{V_X^2}{R}$

$$= \frac{(\frac{3}{2}V_0)^2}{R}$$

$$= \frac{9V_0^2}{4R}$$

$$= 2.25P_0$$

As the power multiplier control stage 10 may be implemented using a digital signal processor, the system of Figure 2 may be implemented readily by use of an appropriate algorithm. It may also be possible and desirable to include the power multiplier control stage 10 within the PWM processor 12 as this will reduce the number of integrated circuits required.

Although the input signal 30 has been described and illustrated as being a pure sine wave, any form of input signal may be used.

An alternative example of a system is shown in Figure 7. The circuit of Figure 7 is identical to that shown in Figure 2 with the exception that the number of switched voltages has been reduced to 3, that is, to $-1/2\ V_{cc}$, $1/2\ V_{cc}$ and $3/2\ V_{cc}$.

In the embodiment of Figure 7, the power multiplier control stage 10 multiplies the input signal by 5 and checks the level of the signal. If the signal is below A, the multiway switch 11 will select the voltage 1/2 V_{cc} to be applied to a first side of the load 20. If the level of the signal exceeds A, the multiway switch 11 will switch to -1/2 V_{cc}. At the same time, 2A is subtracted from the result of the signal multiplied by 5 and this result will be sent to the PWM processor IC 12.

Similarly, for the negative side, if the level exceeds –A, the multiway switch 11 will select the voltage 3/2 V_{cc} and -2A will be subtracted from the result of the signal multiplied by 5 and this result will be sent to the PWM processor IC 12.

Figure 8 shows a plot of the signal at node 2 of the system of Figure 7 if a sinusoidal input signal of amplitude A is applied as the digital audio input signal 30.

Figure 9 shows a plot of the corresponding signal at Node 1 in the system of Figure 7 and Figure 10 shows the signal at node 1, node 2 and across the load 20 of the system of figure 7 in one plot.

Figure 11 shows a further preferred example which differs from the embodiments of Figures 2 and 7 in that the MOSFET drive involves a full bridge, whereas for the first described embodiment shown in Figure 2, it can be seen that only half an H-Bridge is used. The embodiment of Figure 11 also has fewer steps of switching voltages, than the embodiment of Figure 2.

In the system of Figure 11, the digital input signal 30 is applied to the power multiplier control stage 10 where it is multiplied and sampled. As in the system of Figure 2, the amplitude of the signal level is checked and adjusted as required to keep the level within the working range of the PWM processor 12. The multiplied output signal is applied to the PWM processor 12, the width modulated pulses from which are then applied to the input of the power driver

stage 13. The outputs from this stage 13, as well as being applied to the MOSFETS M1 and M2, are also applied to two further MOSFETs M3 and M4. M1 and M2 are connected in series across the power supply Vcc to ground, the junction being taken to inductor L1, the second terminal of which is connected to a first terminal of capacitor C1 and a first terminal of the load 20 at node 2. The MOSFETs M3 and M4 are connected in series across the supply V_{cc} to ground. The junction between M3 and M4 is connected to a first terminal of an inductor L2, the second terminal of which is connected to capacitor C2. The other terminals of the capacitors C1 and C2 are connected to ground. The second terminal of L2 is further connected to an input of the switching unit 14 at node 3. The other voltage inputs to the switching unit 14 are $-1/2V_{cc}$ and $3/2V_{cc}$. The switching operation is controlled by the power multiplier stage 10.

In the system of Figure 11, the working principles are the same as the embodiment of Figure 2, but in the configuration of Figure 11 the DC voltages of GND, 1/2 V_{cc} and V_{cc} are provided to Node 1 of the load to the side of the H-Bridge connected to the 3-way switch 14. The DC voltages are applied through the 3-way switch 14 by controlling the width of the pulse width-modulated (PWM) signal applied from the power driver stage 13 to M3 and M4 through the low pass filter formed by L2 and C2. The PWM signals for producing these DC voltages are shown in Figure 12.

A further alternative example is shown in Figure 13. In this embodiment, the input signal 30 is applied to the power multiplier control 10 the output of which is applied to the pulse width modulator 12. The pulse width modulated pulses therefrom are applied to the power driver stage 13 and the outputs of this stage control MOSFETs M1 and M2 connected in series across the supply. The junction of the MOSFETs M1 and M2 is connected to the first terminal of an inductor L1, the second terminal of which is connected to a first terminal of a load 20 and a first terminal of a capacitor C1 to form node 2. The control outputs from the power multiplier control stage 10 are applied to a pulse width modulated signal generator stage 15 which provides

outputs to drive a further pair of MOSFETs M3 and M4 which are connected in series between supplies $3/2V_{cc}$ and $-1/2\ V_{cc}$. The junction of the MOSFETs M3 and M4 is connected to a first terminal of an inductor L2, the second terminal of which is coupled to a first terminal of a capacitor C2 and a second terminal of a load 20 to form node 1. The second terminals of C1 and C2 are both connected to ground.

In the embodiment of Figure 13, the switching among the DC voltages -1/2 Vcc, GND, 1/2 Vcc, Vcc and 3/2 Vcc to Node 1 are provided by a PWM Signal

Generator 15 through the low pass filter formed by L2 and C2, by controlling the width of the PWM signal, which is as shown below in Figure 14.

Figure 14 shows the pulse width modulated signals applied to M3 and M4 respectively the system of Figure 13 for the various switching voltages.

To obtain the switching voltage of $-1/2V_{cc}$, the upper transistor M3 is turned off and the lower transistor M4 is turned on.

To obtain the ground condition, the upper transistor M3 is turned on for 1/3 of the cycle whilst the lower transistor M4 is turned off and then M3 is turned off whilst M4 is turned on for the remaining 2/3 of the cycle.

To obtain the switching voltage $1/2V_{cc}$, M3 is switched on for half of the cycle whilst M4 is switched off and then for the remaining half of the cycle M3 is turned off whilst M4 is turned on.

To obtain the switching voltage V_{cc}, M3 is turned on for 2/3 of the cycle whilst M4 is turned off and M4 is then turned on for the remaining 1/3 of the cycle whilst M3 is turned off.

To obtain the switching voltage $3/2V_{cc}$, M3 is turned on and M4 is turned off for the duration of the cycle.

A further example is shown in Figure 15. A Switching Mode Power Supply is used for switching among the DC voltages. As in the system of Figure 2, the amplitude of the signal level is checked and adjusted as required to keep the level within the working range of the PWM processor 12. The digital audio input signal 30 is applied to a power multiplier control stage 10 where it is multiplied and the multiplied output is then applied to the pulse width modulator stage 12. The pulse width modulated pulses from the pulse width modulator stage 12 are applied to a power driver stage 13 which drives a pair of MOSFET transistors M1 and M2 connected in series across the supply. The junction of the MOSFET transistors M1 and M2 is connected to a first terminal of an inductor L1 and the second terminal of the inductor L1 is connected to a first terminal of a capacitor C1 and a first terminal of a load 20 to form node 2.

The switching outputs of the power multiplier control stage 10 are applied to a switching mode power supply 16 to switch the output voltages thereof between $-1/2V_{cc}$, ground, $1/2V_{cc}$ and $3/2V_{cc}$.

The output voltages of the switching mode power supply 16 are applied to the second terminal of the load 20 to form node 1 and the second terminal of the capacitor C1 is connected to ground. Further outputs voltages V1, V2 and V3 from the switching mode power supply 16 shown in Figure 15 are other voltages supplied to other devices within the equipment, for example, a microcontroller.

As the power multiplier control stage 10 may be implemented using a digital signal processor, the systems of Figures 2, 7, 11, 13, and 15 may be implemented readily by use of an appropriate conventional control algorithm.

Figure 16 illustrates a further preferred example working in the analogue mode which is in contrast to the embodiments of Figures 2, 7, 11, 13 and 15 which work in the digital mode. The system of Figure 16 includes a Class D analogue amplifier 23 having a first (positive) input and a second (negative) input, a switching stage 24, a comparator stage 25, a further interface stage 26, a load 27 and a resistive potential divider network formed of resistors R9 and R10 having a division ratio equivalent to the inverse of the gain of the amplifier 23. The comparator stage 25 and the further interface stage 26 form a power multiplier control stage.

In the system of Figure 16, the analogue input signal 19 is applied to the negative input of the Class D analogue amplifier 23 which has a gain of Gv. The analogue input signal 19 is also applied to the comparator stage 25 wherein it is compared with a plurality of DC voltages obtained from a positive voltage supply Vref and a negative voltage supply –Vref. Within the comparator stage 25 a serially connected chain of six resistors R1 to R6 is connected between Vref and –Vref to provide the plurality of DC voltages. The junction of resistors R3 and R4 is connected to ground. Also within the comparator stage 25 are four comparators. The analogue input signal 19 is applied to one input of each comparator and the other input of each comparator is connected to a junction in the chain of resistors R1 to R6, the junctions being between R1 and R2, R2 and R3, R4 and R5 and R5 and R6. Preferably, resistors R1 to R6 are equal in resistive value. Thus the signal is compared with voltages ± 1/3Vref and ± 2/3Vref.

The outputs of the comparators are coupled to the further stage 26 which may comprise a control circuit to control The switching stage 24. The outputs of the stage 26 are coupled to the switching stage 24.

The output of the switching stage 24 is coupled to a first (positive) terminal of the load 27 and also to resistor R9 of the potential divider formed by resistors R9 and R10. The junction between R9 and R10 is coupled to a first (positive)

terminal of the Class D analogue amplifier 23. The other terminal of R10 is connected to ground. The output of the second (negative) terminal of the load 27 is connected to the output of the Class D analogue amplifier 23.

In the system of Figure 16, the supply voltage to the Class D amplifier 23 need only be one third of the total output voltage swing. If, therefore, the total undistorted output voltage is ± Vcc, then Vref is chosen such that an input swing of ± Vref will give an undistorted output of ± Vcc.

If the positive excursion of the incoming signal 19 exceeds the level 1/3 Vref, then the comparator connected at the junction of R2 and R3 will give an output which, via the stage 26, sets the switching stage 24 to give an output Vcc1 which corresponds to 1/3Vcc.

If the positive excursion exceeds 2/3 Vref, then the comparator connected to the junction of R1 and R2 produces an output which sets the switching stage 24 to give an output of Vcc2 which is equal to 2/3 Vcc.

If the negative excursion of the incoming signal 19 exceeds the level -1/3 Vref, then the comparator connected at the junction of R4 and R5 will give an output which the stage 26 will use to set the switching stage 24 to give an output of -Vcc1 which corresponds to -1/3Vcc.

If the negative excursion exceeds -2/3 Vref, then the comparator connected to the junction of R5 and R6 produces an output which sets the switching stage 24 to give an output of -Vcc2 which is equal to -2Vcc1.

The waveforms at the first (positive) and second (negative) terminals of the load 27 are also shown in Figure 16. In the embodiment of Figure 16, the Class D amplifier 23 can achieve a higher output power than the amplifier alone was designed to produce. As in the embodiments of Figures 2 to 15, it is possible to produce higher output power than conventional amplifier designs without

increasing the voltage applied to the amplifier or to produce the same output power at a lower supply voltage.

As the junction between resistors R9 and R10 is connected to the positive terminal of the Class D analogue amplifier 23, the signal level at this junction is subtracted from the input signal level so that the resulting level of the signal output from the amplifier 23 is within the linear working range of the amplifier 23.

Various modifications to the embodiments of the present invention described above may be made. For example, other components and method steps can be added or substituted for those above. Thus, although the invention has been described above using particular embodiments, many variations are possible within the scope of the claims, as will be clear to the skilled reader, without departing from the spirit and scope of the invention.

The reference in this specification to any prior publication (or information derived from it), or to any matter which is known, is not, and should not be taken as an acknowledgment or admission or any form of suggestion that that prior publication (or information derived from it) or known matter forms part of the common general knowledge in the field of endeavour to which this specification relates.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises" and "comprising", will be understood to imply the inclusion of a stated integer or step or group of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A power multiplier apparatus to which an input signal having an input signal amplitude is receivable, the power multiplier apparatus comprising:

an amplifier stage having a peak amplitude input associable therewith, the peak amplitude input being associable with linear working range of the amplifier stage;

a power multiplier control stage coupled to the amplifier stage, the power multiplier control stage receiving the input signal which input signal amplitude is multiplied and verified thereat, the input signal amplitude being multiplied to produce a multiplied amplitude which is verified in a manner so as to determine whether it exceeds the peak amplitude input, the multiplied amplitude being receivable at the amplifier stage; and

a first switching stage connectable to said power multiplier control stage, the first switching stage being configured to reduce the multiplied amplitude when it exceeds the peak amplitude input,

wherein the multiplied amplitude is reduced such that the multiplied amplitude does not exceed the peak amplitude input, thereby remaining within the linear working range of the amplifier stage.

2. A power multiplier apparatus according to claim 1, wherein said amplifier stage comprises:

a pulse width modulator stage connectable to said power multiplier control stage,

a power driver stage connectable to said pulse width modulator stage; and

a second switching stage connectable to said power driver stage.

3. A power multiplier apparatus according to claim 2, further comprising a low pass filter connectable between said second switching stage and ground.

4. A power multiplier apparatus according to claim 2 or claim 3, wherein said second switching stage comprises at least two MOSFETs connectable in series.

5. A power multiplier apparatus according to claim 1, wherein when the multiplied amplitude exceeds the peak amplitude input, said first switching stage reduces the multiplied amplitude by a level corresponding to a level by which the multiplied amplitude exceeds the peak amplitude input.

6. A power multiplier apparatus according to claim 5, wherein said first switching stage comprises a selector for selecting one or more of a number of predetermined DC voltage levels, the selection of which is based on whether the multiplied amplitude exceeds the peak amplitude input and the level by which the multiplied amplitude exceeds the peak amplitude input.

7. A power multiplier apparatus according to claim 1, wherein said first switching stage comprises a pulse width modulated signal generator.

8. A power multiplier apparatus according to claim 1, wherein said first switching stage comprises a switching mode power supply.

9. A power multiplier apparatus according to any one of the preceding claims, wherein said amplifier stage comprises a Class D analogue amplifier having a first input and a second input and a gain.

10. A power multiplier apparatus according to claim 9, wherein said power multiplier control stage comprises a comparator stage and an interface stage.

11. A power multiplier apparatus according to claim 9 or claim 10, further comprising a potential divider connectable to said class D analogue

amplifier, and having a division ratio corresponding to the inverse of said gain of said class D analogue amplifier.

12. A method of amplifying power output from a digital amplifier system having a first output terminal and a second output terminal, the method comprising the steps of:

applying an input signal having an input signal amplitude to a power multiplier control stage within which one or more signals are producable;

controlling an amplifier stage using one or more of said one or more signals, the amplifier stage having a peak amplitude input associable therewith, the peak amplitude input being associable with linear working range of the amplifier stage;

multiplying the input signal amplitude at the power multiplier control stage to produce a multiplied amplitude;

verifying the multiplied amplitude at the power multiplier control stage in a manner so as to determine whether it exceeds the peak amplitude input; and

controlling a first switching stage using one or more signals from said power multiplier control stage in a manner so as to reduce the multiplied amplitude when it exceeds the peak amplitude input,

wherein the multiplied amplitude is reduced such that the multiplied amplitude does not exceed the peak amplitude input, thereby remaining within the linear working range of the amplifier stage.

13. A method according to claim 12, wherein the step of controlling the amplifier stage comprises

controlling a pulse width modulating stage using one or more of said one or more signals to produce a train of width modulated pulses; and

driving said second output terminal via said amplifier stage,

wherein the step of driving said second output terminal comprises driving said second output terminal via a second switching stage using said train of width modulated pulses.

14. A method according to claim 13, further comprising filtering in a low pass filter said train of width modulated pulse from said first switching stage prior to applying said train of pulses to said first output terminal.

15. A method according to claim 13 or claim 14, wherein the step of driving said second output terminal in said second switching stage comprises driving at least two MOSFETs connectable in series.

16. A method according to claim 13, further comprising providing a number of switchable DC voltage levels to said first output terminal through the first switching stage using a third switching stage connectable to said power driver stage and said first switching stage.

17. A method according to claim 16, wherein said step of providing a number of said levels comprises using at least two MOSFETs connectable in series.

18. A method according to claim 12, wherein reducing the multiplied amplitude comprises reducing the multiplied amplitude by a level corresponding to a level by which the multiplied amplitude exceeds the peak amplitude input.

19. A method according to claim 13, wherein said step of driving said second output terminal comprises applying said input signal to a negative input of said amplifier stage, applying a DC voltage from the output of the switching stage via a potential divider to the positive input of the amplifier stage such that the output of the amplifier stage remains within a linear working range of said amplifier.

20. A method according to claim 19, wherein said amplifier stage has a gain and the potential divider has a division ratio corresponding to the

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inverse of the gain.

21. A power multiplier apparatus substantially as hereinbefore described with reference to the drawings and/or Examples.

22. A method of amplifying power output from a digital amplifier system substantially as hereinbefore described with reference to the drawings and/or Examples.

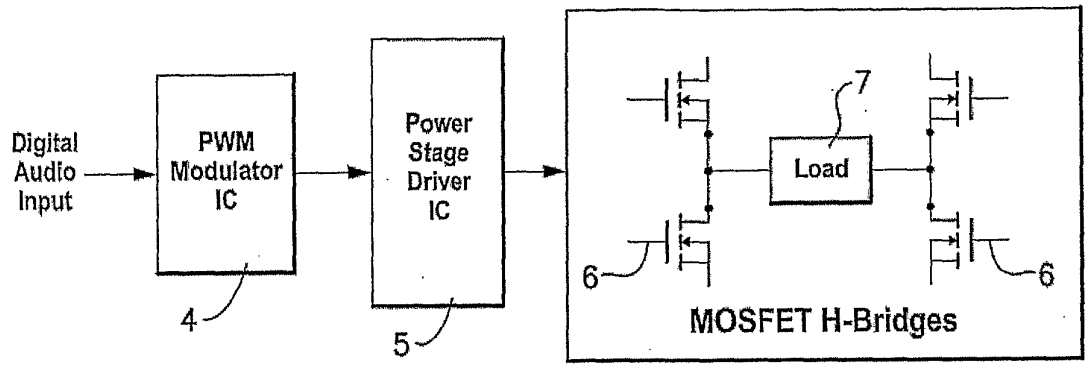

Fig. 1 Prior Art

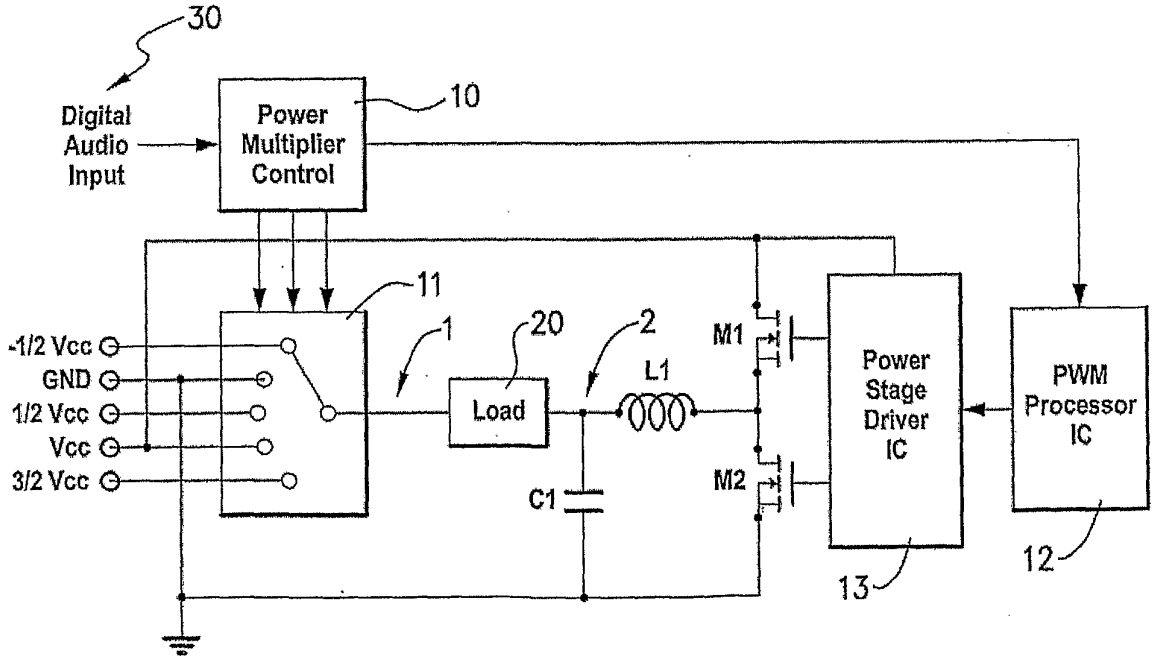

Fig. 2

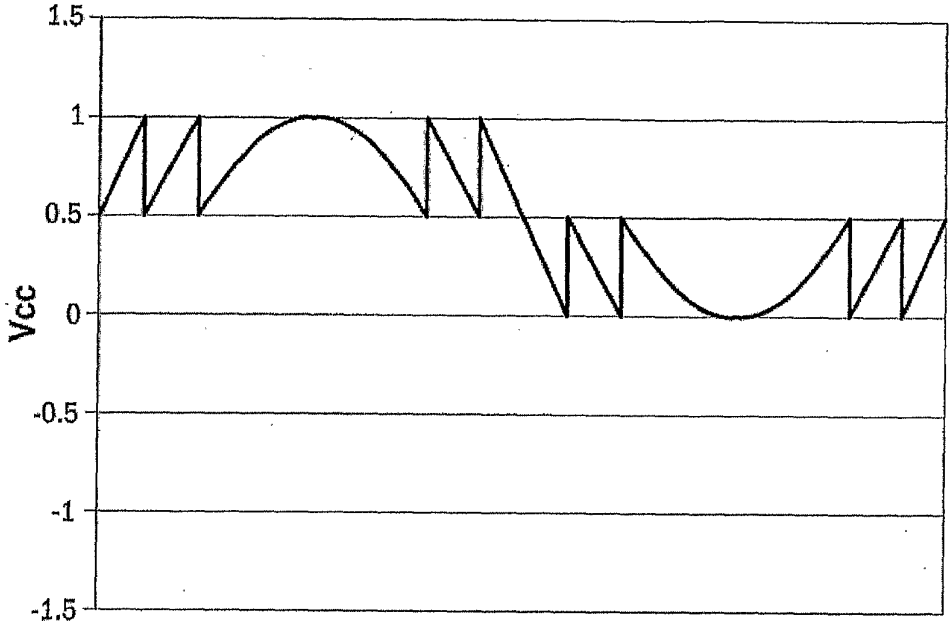

Fig. 3

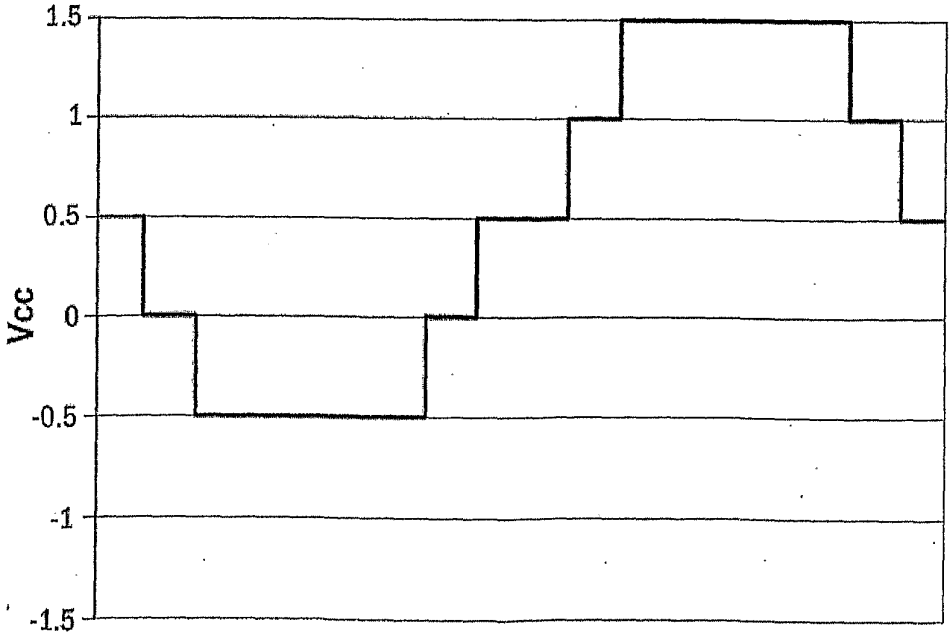

Fig. 4

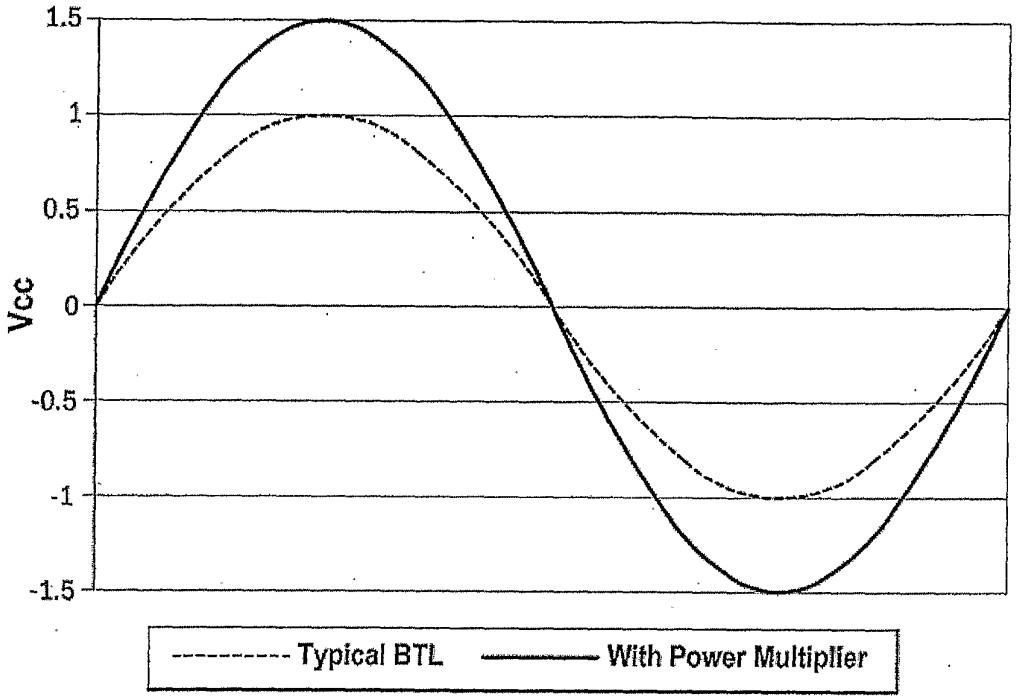
1.5
1
0.5
0
-0.5
-1
-1.5
Vcc
Typical BTL
With Power Multiplier

Fig. 5

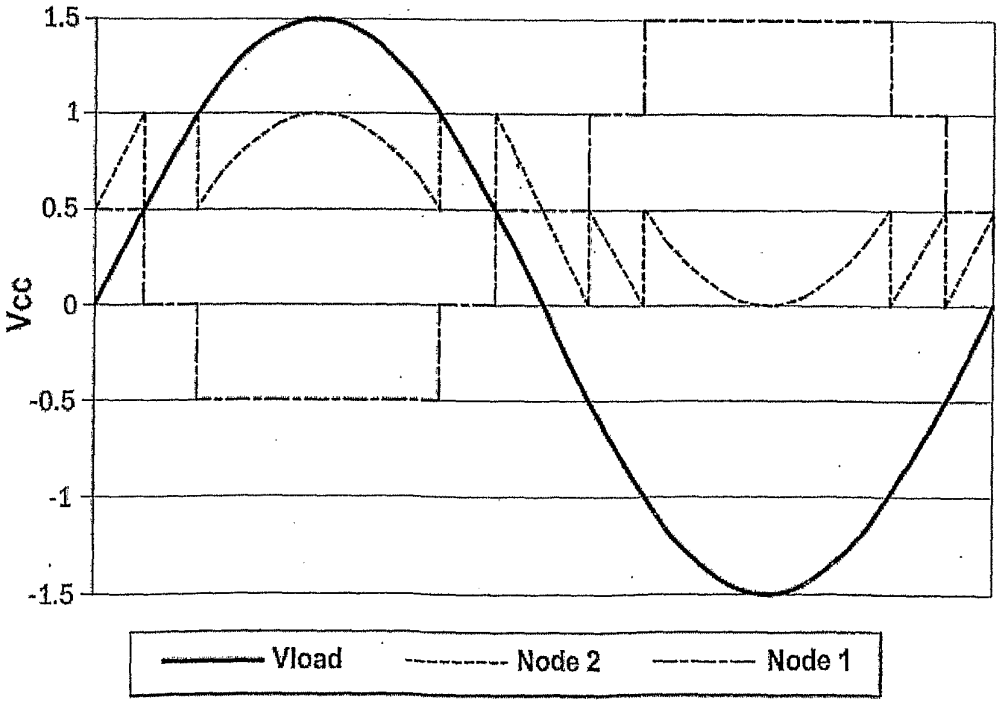
1.5
1
0.5
0
-0.5
-1
-1.5
Vcc
Vload
Node 2
Node 1

Fig. 6

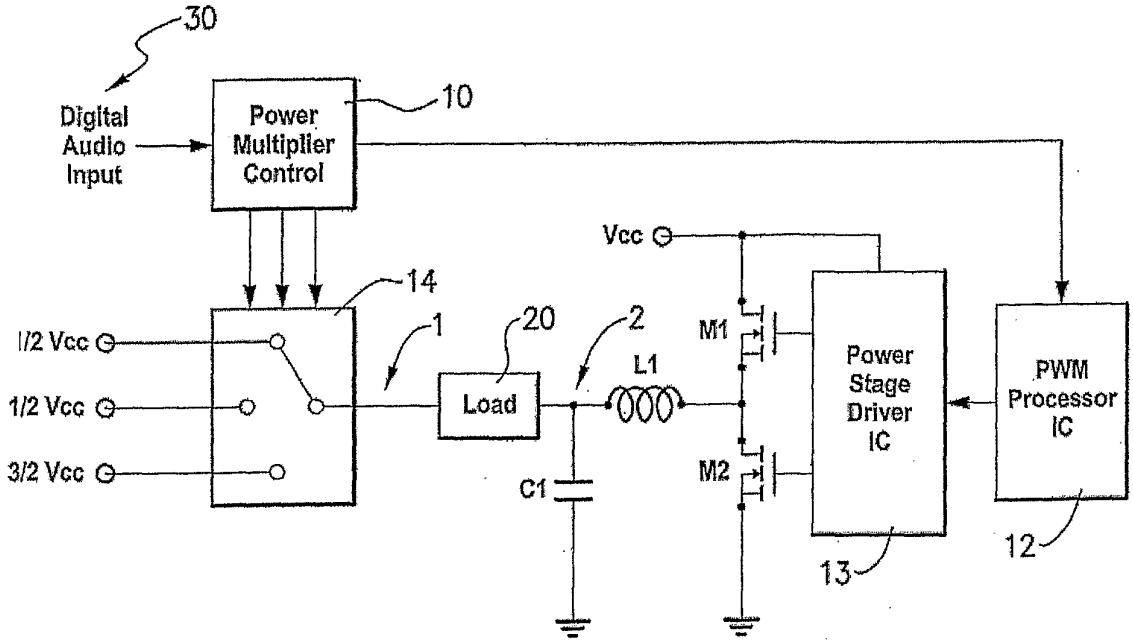
30
Digital Audio Input
Power Multiplier Control
10
Vcc
14
1/2 Vcc
1/2 Vcc
3/2 Vcc
1
20
2
Load
L1
M1
M2
C1
Power Stage Driver IC
PWM Processor IC
13
12

Fig. 7

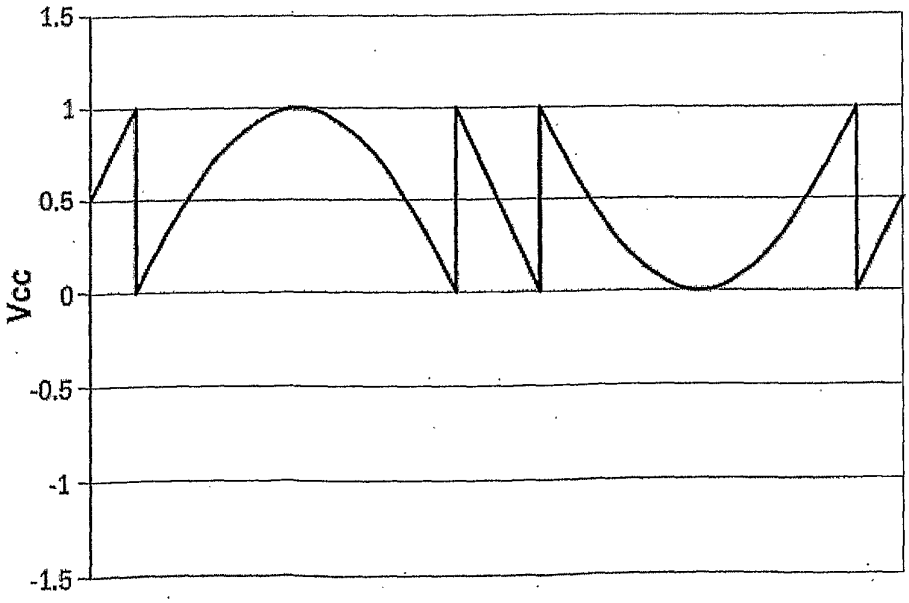
1.5
1
0.5
0
-0.5
-1
-1.5
Vcc

Fig. 8

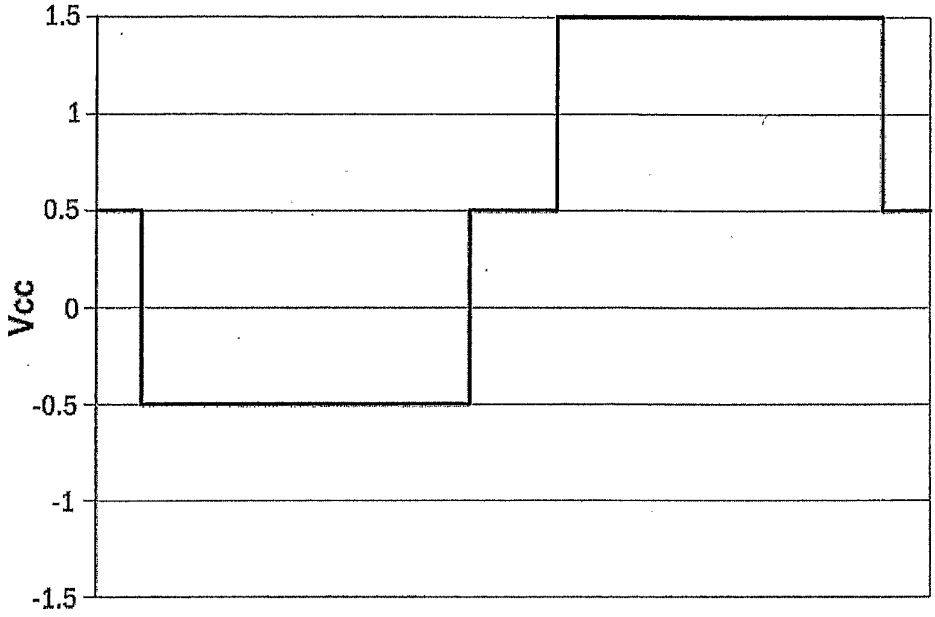

Fig. 9

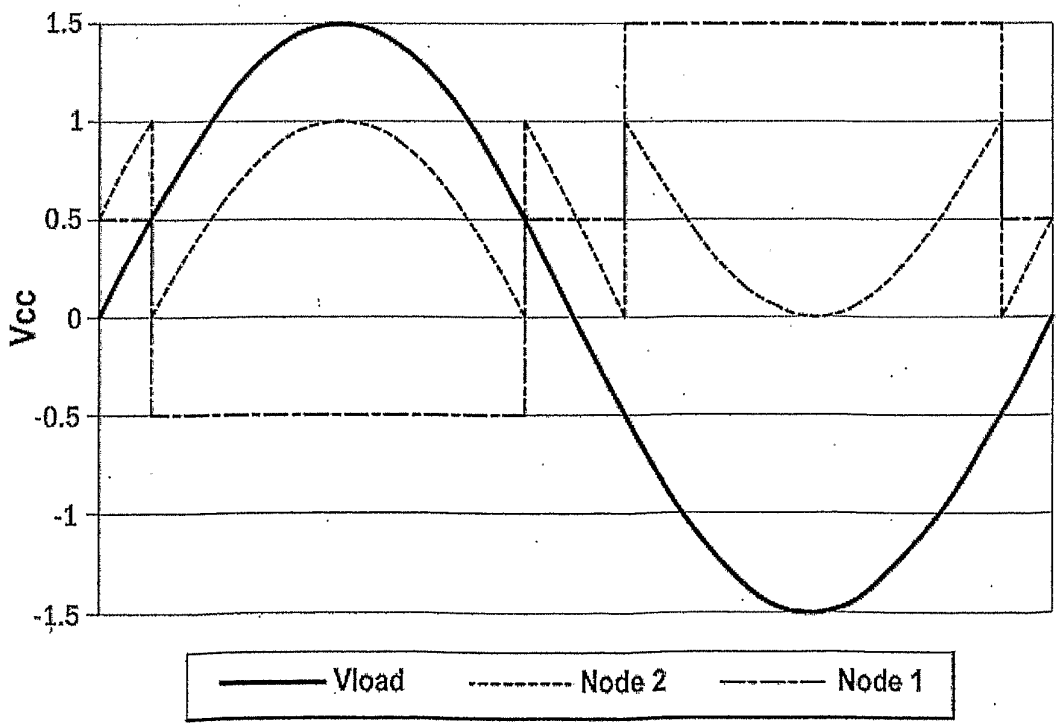

Fig. 10

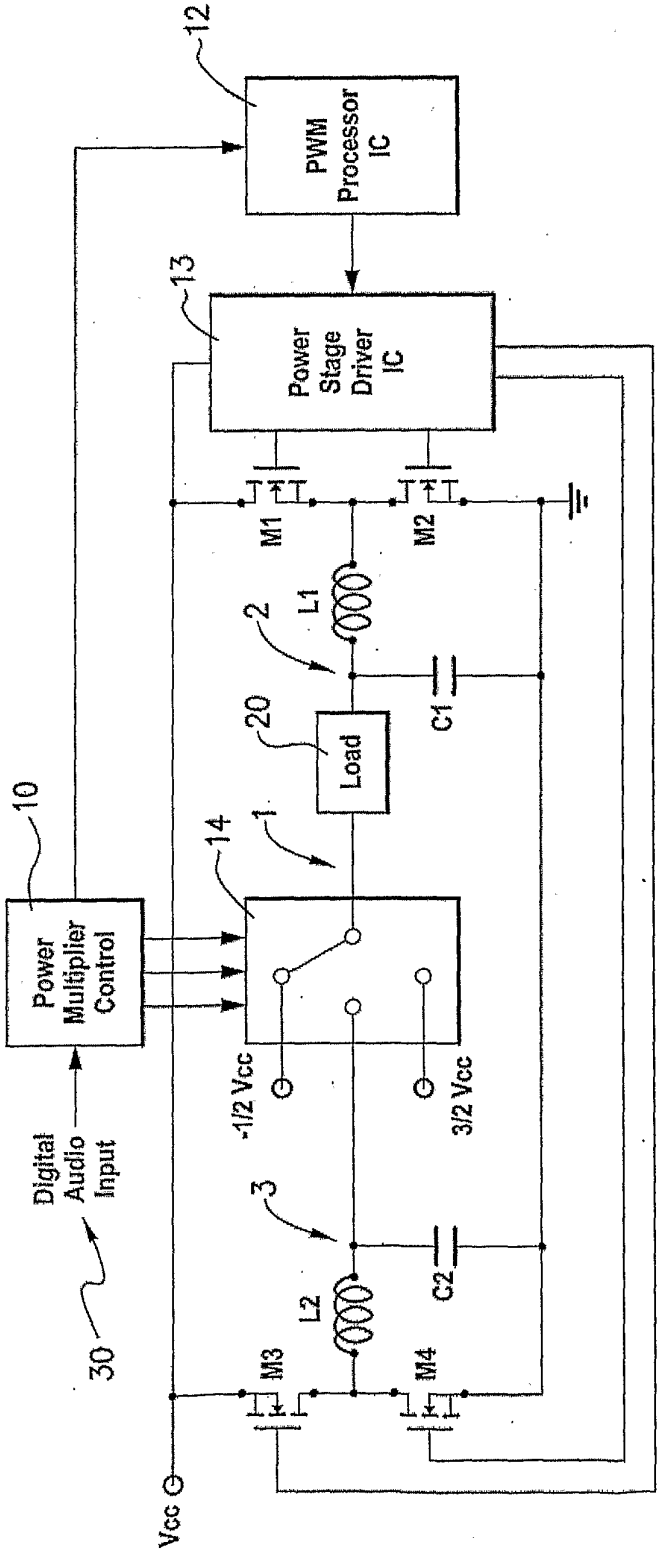
12
PWM Processor IC
13
Power Stage Driver IC
M1
M2
2
L1
C1
20
Load
1
14
10
Power Multiplier Control
-1/2 Vcc
3/2 Vcc
3
L2
C2
M3
M4
Digital Audio Input
30
Vcc

Fig. 11

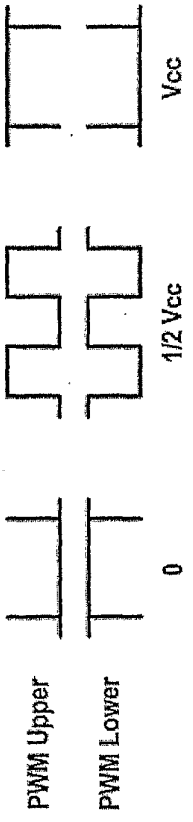
Vcc
1/2 Vcc
0
PWM Upper
PWM Lower

Fig. 12

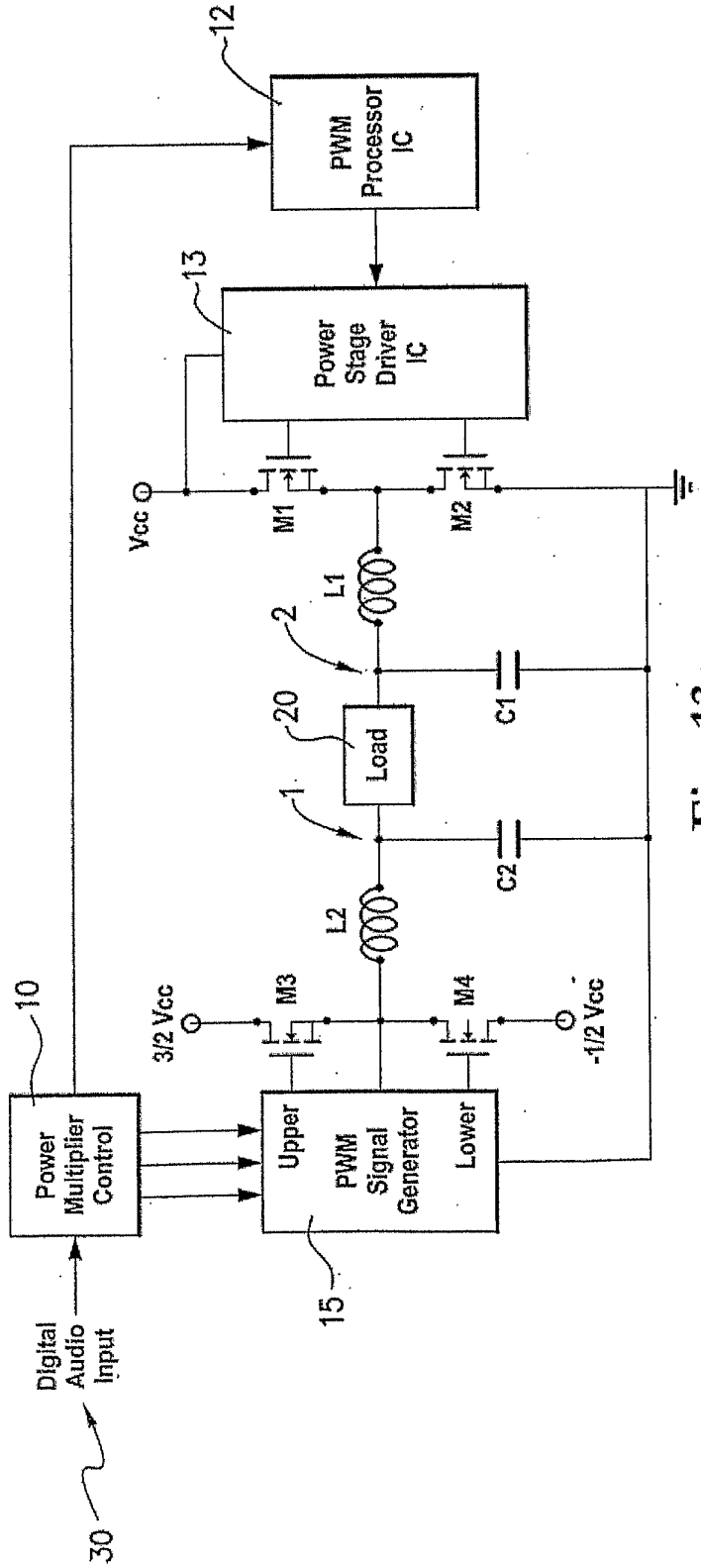
12
PWM Processor IC
13
Power Stage Driver IC
Vcc
M1
M2
L1
2
C1
20
Load
1
C2
L2
3/2 Vcc
M3
M4
-1/2 Vcc
10
Power Multiplier Control
Upper
PWM Signal Generator
Lower
15
Digital Audio Input
30

Fig. 13

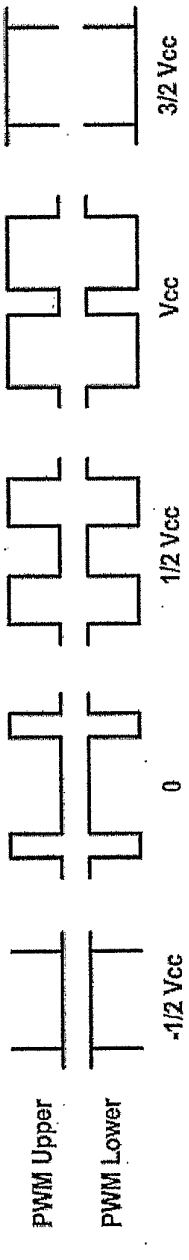
3/2 Vcc
Vcc
1/2 Vcc
0
-1/2 Vcc
PWM Upper
PWM Lower

Fig. 14

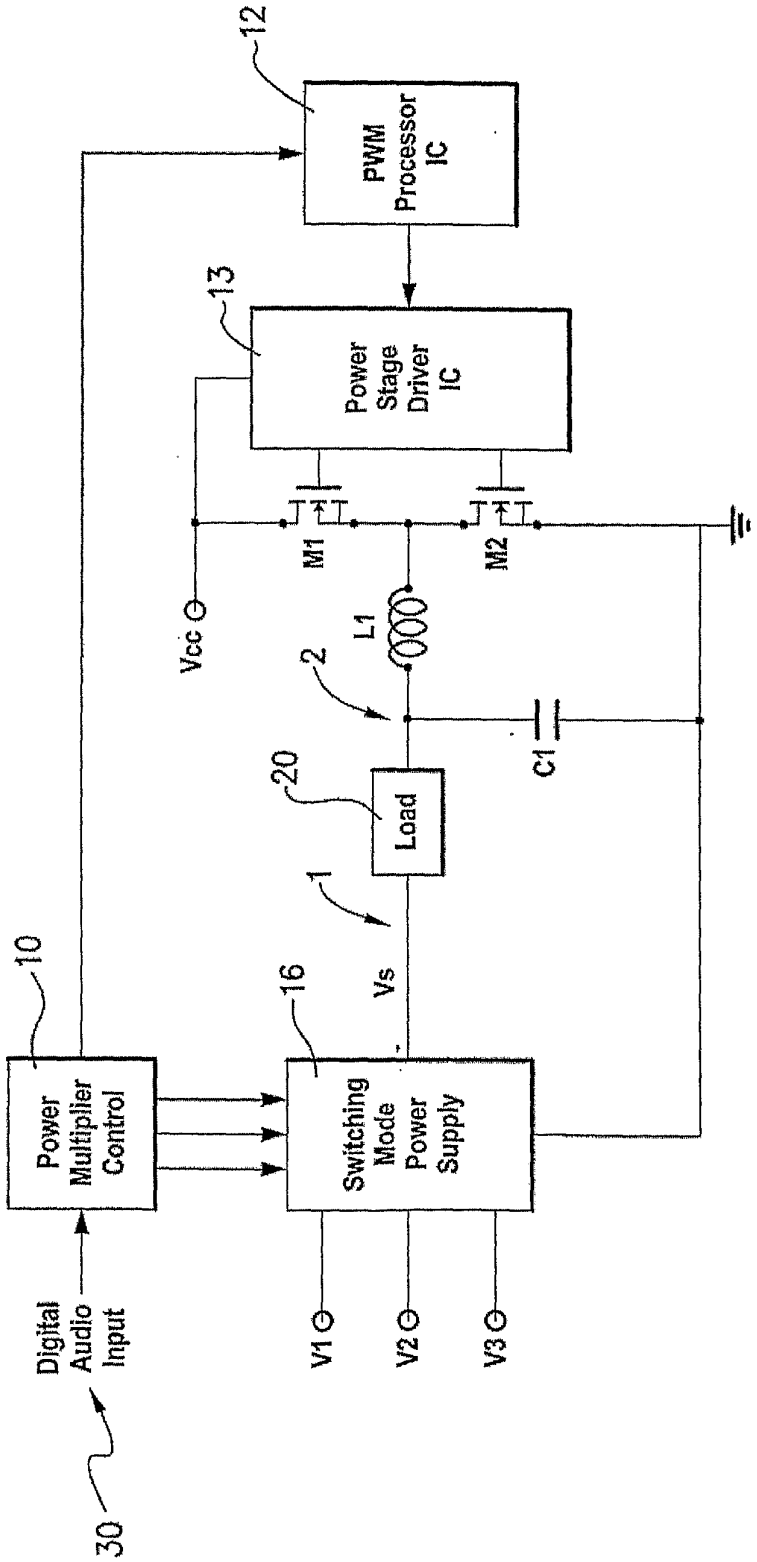
12
PWM Processor IC
13
Power Stage Driver IC
M1
M2
Vcc
L1
2
C1
20
Load
1
Vs
10
16
Power Multiplier Control
Switching Mode Power Supply
V1
V2
V3
Digital Audio Input
30

Fig. 15

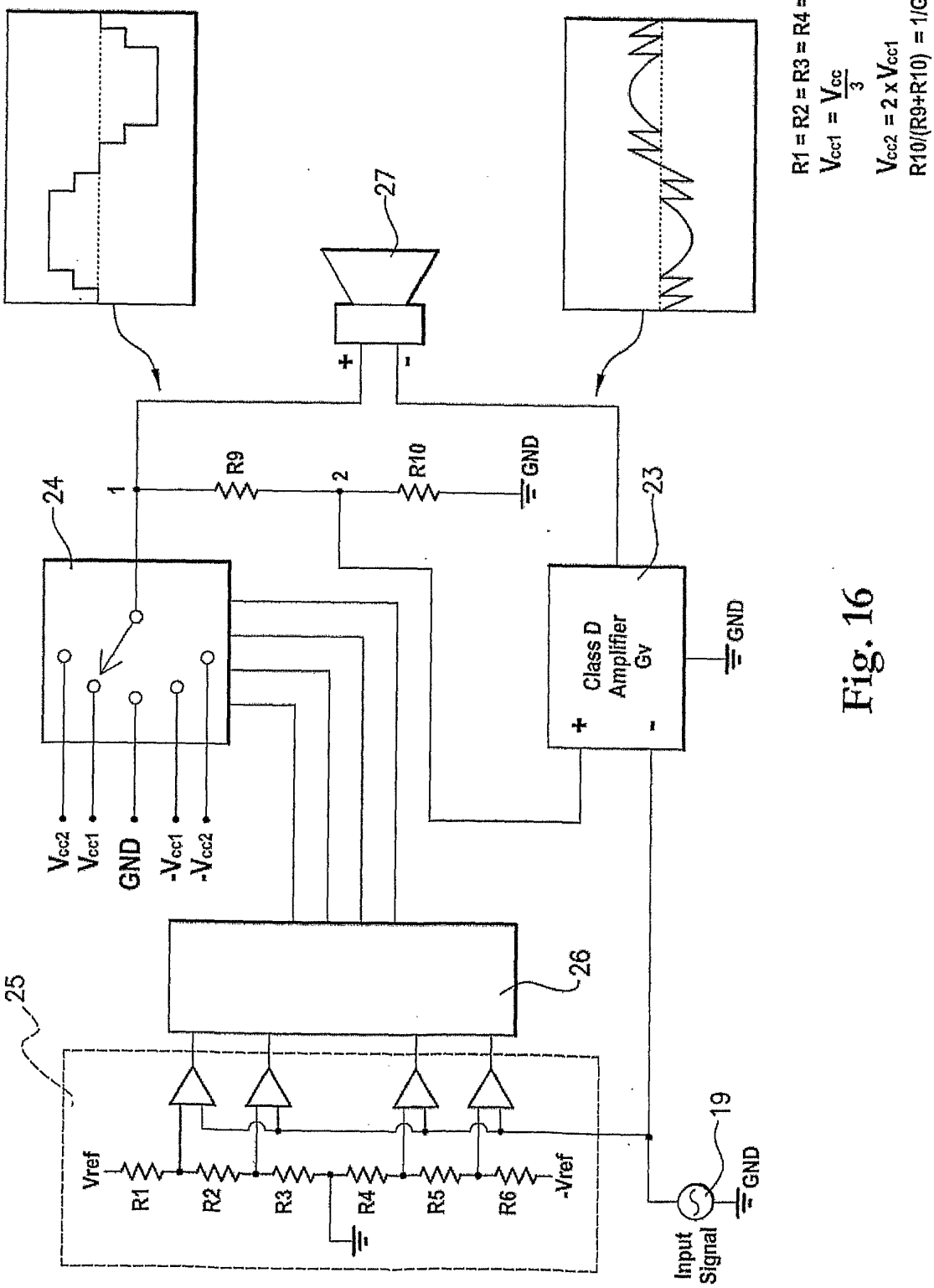
R1 = R2 = R3 = R4 = R5 = R6
$V_{cc1} = \frac{V_{cc}}{3}$
$V_{cc2} = 2 \times V_{cc1}$
R10/(R9+R10) = 1/Gv
27
+
-
R9
R10
GND
1
2
24
23
Class D
Amplifier
Gv
GND
V_{cc2}
V_{cc1}
GND
$-V_{cc1}$
$-V_{cc2}$
26
25
Vref
R1
R2
R3
R4
R5
R6
-Vref
19
Input
Signal
GND

Fig. 16