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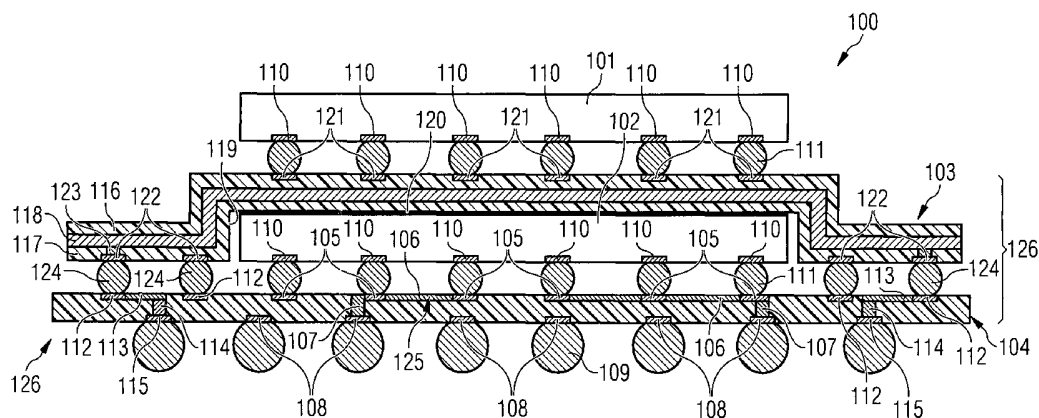
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(54) Title: SEMICONDUCTOR CHIP ASSEMBLY INCLUDING STACKED COMPONENTS AND METHOD FOR PRODUCING IT



(57) Abstract: A stacked electronic component (100) comprises a substrate board (104) and a first semiconductor chip (101) mounted by a flip chip technique to the substrate board (104). An intermediate rewiring tape (103) having a recess (119), is mounted to the rear side of the first semiconductor chip (102), the recess (119) of the intermediate rewiring tape accommodate the first semiconductor chip. A second semiconductor chip (101) is mounted to the intermediate rewiring layer by a flip chip technique.

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Description

SEMICONDUCTOR CHIP ASSEMBLY INCLUDING STACKED COMPONENTS AND METHOD FOR PRODUCING IT

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The invention relates to a semiconductor chip assembly, a stacked electronic component including the assembly and methods for producing the assembly and electronic component.

10 Increased miniaturisation and cost reduction are among some of the development aims currently addresses in semiconductor technology. It is desired that both the outer size of semiconductor packages is reduced and that the number of integrated circuits within a package of a given size, the so-called pack-
15 ing density, is increased.

One method by which the size of a package can be decreased is by mounting the chips on a substrate by a flip chip technique. This technique is advantageous as both the height and lateral
20 space required by a package including the flip chip contacts is less than that required by packages with wire bonds. Additionally, in flip chip technology electrical contacting between the chip and its substrate occurs in parallel for all the flip contacts rather than serially as for wire bonded
25 chips. This increases manufacturing speeds and, therefore, reduces costs.

Further increases in the packing density of electronic packages are achieved by providing multi-chip modules in which two
30 or more chips are stacked on top of one another. However, a stacked multi-chip module is difficult to achieve for two or

more chips mounted using a flip-chip technique due to the central arrangement of the flip chip contacts.

US 2002-074637 A1 discloses an electronic component which includes stacked semiconductor chip electrically connected by flip chip contacts. Each semiconductor chip or die is provided with conductive redistribution traces both its active front and passive rear surfaces. The conductive traces on the two opposing faces of each die are electrically connected by conductive tracks disposed on the side of the chip. The manufacturing process of such a stacked component is, therefore, complicated and expensive.

It is, therefore, an object of the invention to provide a semiconductor chip assembly which enables the density of the integrated circuits to be increased within a package of a given size and which can be produced using more cost effective manufacturing methods.

It is a further object of the invention to provide an electronic component including the semiconductor chip assembly which includes at least two stacked semiconductor chips and a method for its production.

This is achieved by the subject matter of the independent claims. Further improvements are provided by the subject matter of the dependent claims.

A semiconductor chip assembly, according to the invention, includes a substrate board. The substrate board typically comprises a glass fibre matrix such as FR4 or BT and includes a redistribution structure. The substrate board, according to

the invention, includes a plurality of first contact areas positioned on the upper surface towards the lateral centre which are electrically connected by a plurality of first conductor tracks and a plurality of first vias to first outer contact areas positioned on the bottom surface of the substrate board to provide a first redistribution structure.

The substrate board further includes a plurality of second contact areas positioned on the upper surface towards the periphery of the substrate board. The second contact areas are electrically connected by second conductor tracks and second vias to second outer contact areas positioned on the bottom surface of the substrate board and provide a second redistribution structure.

The semiconductor chip assembly according to the invention also includes at least one semiconductor chip, including a plurality of chip contact areas on its active surface. A first semiconductor chip is mounted in the lateral centre on the upper surface of the substrate board by electrical connections between the chip contact areas and the first contact areas.

Preferably, the lateral arrangement of the first contact areas on the upper surface of the substrate board corresponds to the lateral arrangement of the chip contact areas on the active surface of the chip. Preferably, the first semiconductor chip is mounted by a flip chip technique by a microscopic solder ball positioned between each chip contact pad and its corresponding contact area on the substrate board. The first semiconductor chip is thereby electrically connected to the first redistribution structure.

The semiconductor chip assembly according to the invention also includes a pre-formed intermediate rewiring tape. The pre-formed intermediate rewiring tape includes third contact areas, positioned towards the centre of its upper surface, and
5 fourth contact areas, positioned on the bottom surface towards the periphery. The third and fourth contact areas are electrically connected by tape conductor tracks located in the centre of the intermediate rewiring tape and being positioned between and surrounded by between an upper and lower electrically in-
10 sulating film. The electrically insulating film preferably comprises polyimide and the conductor tracks preferably comprise copper or a copper alloy.

The use of a pre-formed intermediate rewiring structure provides a simple cost effective method to provide a rewiring
15 structure for the upper semiconductor chip in a stacked electronic component, particularly for a semiconductor chip mounted using a flip chip technique as portions of the rewiring tracks can be positioned under the upper chip. Electrical
20 contacts to the intermediate rewiring structure and therefore the upper chip are advantageously provided in the periphery of the intermediate rewiring tape. This enables an easy reliable contact to the upper chip of the stack to be formed.

25 The pre-formed intermediate rewiring tapes are, preferably, fabricated in the form of a strip including a plurality of intermediate rewiring tapes arranged along the length. The intermediate rewiring tapes are manufactured cost effectively using simple known techniques.

30

The pre-formed intermediate wiring tape further includes a recess surrounded by peripheral regions which protrude laterally

outwards from the recess. The recess is formed with a flat bottom and the laterally protruding regions lie in a plane approximately parallel to that of the bottom of the recess.

- 5 Preferably, the recess is formed over the whole width of the tape so that the laterally protruding regions extend on only two opposing sides of the recess. This has the advantage that the lateral size of the rewiring tape is reduced.
- 10 The fourth contact areas are therefore located in the protruding region and the third contact areas in the central region. The recess of the intermediate rewiring tape is mounted to the rear side of the first semiconductor chip, and the fourth contact areas of the intermediate rewiring tape are electrically
- 15 connected to the second contact areas of the substrate board.

Preferably, the fourth contact areas of the intermediate rewiring tape have a lateral arrangement which corresponds to the lateral arrangement of the second contact areas of the

20 substrate board. The fourth and second connect areas are advantageously electrically connected by a plurality of solder balls.

The contact areas on the upper and lower surface of the intermediate rewiring tape are provided by metallic contact pads

25 positioned on metallic vias which are positioned through the upper and lower electrically insulating films. This method has the advantage that the lateral size of the vias and contact areas can be independently controlled.

30

Alternatively, the contact areas of the intermediate rewiring tape are provided by providing an appropriate arrangement of

apertures in the electrically insulating films which expose the underlying conductor track. This method has the advantage that fewer masking and deposition steps are required.

- 5 Preferably, the recess of the intermediate rewiring tape is attached to the rear side of the first semiconductor chip by adhesive. The first semiconductor chip is, therefore, accommodated within the recess and the plane of the laterally outwardly protruding regions lie in approximately the same plane
10 as the active surface of the first semiconductor chip.

This arrangement of the pre-formed intermediate tape enables the rewiring tape to be attached directly to the rear side of the semiconductor chip without requiring an intermediate electrically insulating layer. The production of the semiconductor
15 chip assembly is simplified.

Preferably, the intermediate rewiring tape includes tape conductor tracks on two or more electrically isolated inner layers. This enables a more complex redistribution structure to
20 be provided.

Preferably, the flip chip contacts and the space between the active surface of the chip and the substrate are protected by underfill material. This protects the contact from corrosion
25 due to moisture. Preferably the semiconductor chips are also encapsulated by plastic mould material, the contacts between the intermediate rewiring foil and the substrate are encapsulated by plastic mould material. The plastic mould material
30 provides further mechanical protection for the electrical connections and protection from moisture penetration and, therefore, corrosion of the contacts.

A stacked electronic component including the semiconductor assembly according to the invention further includes a second semiconductor chip mounted on the upper surface of the intermediate rewiring tape.

Preferably, the lateral arrangement of the third contact areas on the upper surface of the intermediate rewiring tape corresponds to that of the chip contact areas on second semiconductor chip. The second semiconductor chip is, preferably, electrically connected to the rewiring tape by a flip chip technique whereby microscopic solder balls are provided between the chip contact areas and third contact areas enabling the electrical connection between the upper semiconductor chip and the intermediate rewiring tape.

This enables a stacked electronic component which includes two semiconductor chips are mounted by a flip chip technique on one side of a substrate board. This increases the packing density of the electronic component while not increasing the lateral space required by the component on the external substrate.

The invention also provides methods to assemble a semiconductor chip assembly. The method includes the steps of providing a substrate board including a plurality of first contact areas on the upper surface, the first contact areas being located approximately in the lateral centre and electrically connected by first conductor tracks and first vias to first outer contact areas positioned on the bottom surface of the substrate board and provides a first redistribution structure. The substrate further includes second contact areas positioned to-

wards the periphery of its upper surface which are connected by second conductor tracks and second vias to the outer contact areas positioned on the bottom surface of the substrate board and provides a section of the second redistribution
5 structure.

At least one semiconductor chip with chip contact areas on its active surface is provided. A first semiconductor chip is mounted on the substrate board by the chip contact pads and
10 first contact pads of the substrate board. Preferably, the semiconductor chip is mounted by a flip chip technique by a microscopic solder ball positioned between each chip contact pad and its corresponding first contact pad.

15 A rewiring strip is provided which includes an upper and lower polyimide foil with tape conductor tracks lying in the centre of the rewiring tape and being surrounded by the polyimide foils. The rewiring strip includes a plurality of intermediate rewiring tapes arranged at intervals along the length of the
20 strip, each intermediate rewiring tape having a plurality of third contact areas positioned in the upper surface connected by the tape conductor tracks to fourth contact areas positioned in the bottom surface. The fourth contact areas are laterally positioned outside of the third contact areas at the
25 periphery of the rewiring tape.

The intermediate rewiring tape for the semiconductor chip assembly is formed from the rewiring strip by pressing a section of the rewiring tape strip into a mould of a template holder
30 and applying heat to provide a flat bottomed recess in its central portion. The third contact areas are therefore positioned in the upper surface of the intermediate rewiring tape

in the central regions raised by the recess. The fourth contact areas are positioned in the lower surface of the intermediate rewiring tape in the laterally protruding peripheral regions.

5

Adhesive is applied to the upper rear surface of the lower semiconductor chip and the recess of the pre-formed rewiring tape is attached to the rear surface of the semiconductor chip. The third contact areas of the intermediate rewiring substrate face upwards away from the substrate board and the fourth contact areas of the rewiring tape face the substrate. The first semiconductor chip is accommodated within the recess. The fourth contact areas are electrically connected to the second contact pads of the substrate board.

10

The template holder is removed leaving the pre-formed rewiring tape attached to the substrate board and lower semiconductor chip and provide a semiconductor chip assembly according to the invention.

15

Preferably, the lateral arrangement of the first contact areas on the upper surface of the substrate board corresponds to the lateral arrangement of the chip contact areas of the semiconductor chip which is to be mounted on the substrate board. The semiconductor chip is then mounted to the substrate board by flip chip contacts, i.e. microscopic solder balls, between the chip contact pads and the first contact areas. This reduces the height and lateral dimensions of the semiconductor chip assembly and consequently the electronic component.

20

Preferably, the fourth contact areas positioned on the lower surface of the rewiring tape are provided with a lateral ar-

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rangement which corresponds to the lateral arrangement of the second contact areas. Solder balls are then attached to the fourth contact areas positioned on the bottom surface of the rewiring tape. This provides a simple reliable electrical connection to be provided between the intermediate rewiring tape and the substrate board.

Preferably, the lower semiconductor chip is underfilled and, preferably, also encapsulated by plastic mould material before the intermediate rewiring tape is attached as the chip can be more easily accessed.

Preferably, the contacts between the intermediate rewiring foil and the substrate are encapsulated by plastic mould material to provide protection from moisture penetration and corrosion.

The electrical connection between the first semiconductor chip and the intermediate rewiring tape and the board is performed using single solder reflow process. This has the advantage of reducing the number of manufacturing steps which reduces the manufacturing costs.

A method to assemble a stacked electronic component, according to the invention, includes the further step of mounting a second semiconductor chip on the upper surface of the intermediate rewiring tape to form a stacked electronic component.

Preferably, the third contact areas positioned on the upper surface of the rewiring tape are provided with an arrangement corresponding to that of the chip contact areas on second semiconductor chip. The second semiconductor chip is, prefera-

bly, electrically connected to the rewiring tape using a flip chip technique by microscopic solder balls between the chip contact areas and third contact areas. An electronic component with a high packing density and small footprint is, therefore, provided.

Alternatively, the upper and lower semiconductor chips and the intermediate rewiring layer are encapsulated by plastic mould material in one process step after the stack is assembled.

10 This advantageously reduced the number of process steps required.

A semiconductor assembly including stacked flip chips according to the invention provides an electronic package in which the density of the integrated circuits within the package is increased. The semiconductor chip assembly enables flip chip bonding can be used. The mechanical and electrical connection between the chip and the substrate is formed underneath the chip, therefore, reducing the lateral size of the package.

20 The stacked electronic component can also be fabricated cost effectively as the bonding is performed in parallel and can be performed in one solder reflow process to electrically connect two or more chips and the intermediate rewiring layers to the substrate board. The further disadvantages of wire bonding such as the inductance of the wires and shorting between the wires are also avoided.

The assembly according to the invention is very flexible as either similar flip chips or different flip chips can be mounted to form a stack as the pre-formed intermediate tape is designed to have an appropriate arrangement of contact areas

or bump terminals for the upper chip. The contact pad arrangement for the upper chip is, therefore, independent of the arrangement of the contact areas on the substrate board for the lower semiconductor chip.

5

The assembly according to the invention has the added advantage that a single solder reflow process can be used to electrically connect two or more flip chips in the stack. This further simplifies the manufacturing process.

10

The pre-formed intermediate rewiring tape also has the advantage that the intermediate rewiring tape can be accurately mounted onto the rear surface of a lower semiconductor chip without requiring significant pressure to be applied to either the semiconductor chip or the underlying substrate in order to produce reliable mechanical and electrical connections.

20

An embodiment of the invention will now be described by reference to the figures.

Figure 1 shows a stacked electronic component according to a first embodiment of the invention, and

25

Figure 2 illustrates a step in the method to produce a stacked electronic component according to Figure 1.

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Figure 1 shows a stacked electronic component 100 according to a first embodiment of the invention. Stacked electronic component 100 includes two semiconductor chips 101, 102, one intermediate rewiring tape 103 and a substrate board 104. The semiconductor chip 102 is mounted on the upper surface of the substrate board 104 by a flip chip technique. The intermediate

rewiring tape 103 is positioned on the upper rear surface of the semiconductor chip 102. The upper semiconductor chip 101 is mounted on the upper surface of the intermediate rewiring tape 103, above the lower semiconductor chip 102 to form a
5 stacked electronic component 100.

In this embodiment of the invention, each semiconductor chip 101, 102 of the stacked flip-chip assembly 100 is a BGA package and has approximately the same size. Each semiconductor
10 chip 101 and 102 includes a plurality of chip contact pads 110 on its upper active surface. Typically the chip contact pads 110 are arranged in a perfectly square grid array towards the periphery of the active surface. In the embodiment of the invention shown in Figure 1, six of the plurality of chip con-
15 tact pads 110 are depicted for each of the semiconductor chips 101 and 102. Microscopic solder balls 111 which comprise the flip chip contacts are positioned on the chip contact pads 110 to provide the electrical connection to the semiconductor chip 101 and 102.

20

The substrate board 104 of the stacked electronic component 100 includes in its central portion a first rewiring structure 125 for the lower semiconductor chip 102 which is mounted directly on the upper surface of the substrate board 104. The
25 substrate board 104 further includes a second rewiring structure 126 located in its periphery for the upper semiconductor chip 101 of the assembly 100.

The first rewiring structure 125 includes a plurality of first
30 contact areas 105 laterally positioned towards the centre of the upper surface of the substrate board 104. The lateral arrangement of the first contact areas 105 corresponds to the

lateral arrangement of the chip contact areas 110 on the lower semiconductor chip 102. Therefore, six of the plurality of first contact areas 105 are depicted in Figure 1.

5 The plurality of first contact areas 105 are electrically connected by conductor tracks 106 and vias 107 to a plurality of first outer contact pads 108 of the stacked electronic component 100. This provides the first rewiring structure 125 for the lower semiconductor chip 102.

10

The plurality of first outer contact pads 108 are positioned on the bottom surface of the substrate board 104. A solder ball 109 is positioned on each of the outer contact pads 108 and allow the flip-chip assembly 100 including the two semiconductor chips 101 and 102 to be mounted on, and electrically connected to, an external substrate such as a printed circuit board which is not shown in the figure for clarity.

15 The semiconductor chip 102 is mounted to the substrate board 104 by the microscopic solder balls 111 which are positioned between the chip contact pads 110 on the active surface of the semiconductor chip 102 and the contact areas 105 of the first rewiring structure 125 of the substrate board 104.

20 The second rewiring structure 126 is positioned at the periphery of the substrate board 104 and includes a plurality of second contact areas 112 which are arranged at the periphery of the upper surface of the substrate board 104. The second plurality of contact areas 112 are electrically connected by second conductor tracks 113 and second vias 114 to a second plurality of outer contact areas 115 positioned on the bottom surface of the substrate board 104. Solder balls 109 are also

25

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positioned on the second plurality of the outer contact areas 115. The second contact areas 112, second conductor tracks 113 and second vias 114 provide a part of the second rewiring structure 126 for the upper semiconductor chip 101 of the
5 stacked electronic component 100.

The intermediate rewiring tape 103 is positioned on the upper rear surface of the lower semiconductor chip 102. The intermediate rewiring tape has a multi-layer structure which, in this
10 embodiment of the invention, includes an upper 116 and lower 117 electrically insulating polyimide film and a plurality of tape conductor tracks 118 of the rewiring structure arranged in the centre of the intermediate rewiring tape 103 between the upper 116 and lower 117 polyimide films.

15

The intermediate rewiring tape 103 further includes a plurality of third contact areas 121 positioned in the upper surface central portion of the intermediate rewiring tape 103 which are connected to the conductor tracks 118. The lateral ar-
20 rangement of the third contact areas 121 corresponds to the lateral arrangement of the chip contact pads 110 of the upper semiconductor chip 101.

A fourth plurality of contact pads 122 is arranged on the bot-
25 tom surface at the periphery of the rewiring tape 103. The fourth contact pads 122 are electrically connected by vias 123 to the tape conductor tracks 118 to the plurality of third contact areas 121 of the intermediate rewiring tape 103.

30 The lateral arrangement of the fourth contact pads 122 corresponds to the arrangement of the plurality of second contacts areas 112 positioned at the periphery of the upper surface of

the substrate board 104 and provides a part of the rewiring structure of upper semiconductor chip 101.

According to the invention, the intermediate rewiring tape 103 is pre-formed to provide a flat bottomed recess 119. The recess 119 is laterally slightly larger than the lower semiconductor chip 102 and has a depth of approximately that of the semiconductor chip 102. The side walls of the recess 119 are approximately perpendicular to the bottom of the recess.

The intermediate rewiring tape 103 is pre-formed so that the upper surface of the central portion of the intermediate rewiring tape 103 facing away from the recess 119 provides a flat surface. The third plurality of contact pads 121 are positioned in the upper surface of the intermediate rewiring tape in this central flat region.

The lower surface of the intermediate rewiring tape 103 outside of the recess 119, lies on a plane parallel to that of the bottom of the recess 119 and lies in approximately the same plane as the upper active surface of the lower semiconductor chip 102 when mounted on the rear surface of the semiconductor chip 102.

The fourth contact pads 122 are positioned in the periphery of the intermediate rewiring tape 103 and lie outside of pre-formed recess 119 of the intermediate tape 103 and lie in a horizontal plane above the corresponding contact pads 112 of the substrate board 104.

The dimensions of the recess are chosen so that the solder balls 124 positioned between the second contact areas 112 and

fourth contact areas 122 are approximately the same size as the microscopic solder balls 111 attached to the chip contact areas 110 of the semiconductor chip 102.

5 A solder ball 124 is positioned between the second contact pads 112 of the substrate board 104 and the fourth contact areas 122 of the intermediate rewiring tape 10. The solder balls 124 electrically connect the second 112 and fourth 122 contact areas and, therefore, the upper semiconductor chip 101 to the
10 substrate board 104 and completes the rewiring structure 126 for the second semiconductor chip 101.

The recess 119 in the intermediate rewiring tape 103 extends across the width of the rewiring tape. Therefore, the protruding regions extend only from two opposing sides of the recess
15 119. This arrangement is not visible in the cross-sectional view of the figures.

As is explained in more detail with reference to Figure 2, the intermediate tape 103 is pre-formed by pressing a section of
20 the rewiring tape 103 into a mould while being heated. This is performed in such a way so that the conductor tracks 118 positioned in the centres of the intermediate rewiring tape 103 are not damaged. This is facilitated by the provision of bending or flexing lines appropriately positioned in the rewiring
25 tape 103.

A layer of adhesive 120 is positioned on the upper rear surface of the lower semiconductor chip 102 and attaches the rear
30 surface of the semiconductor chip 102 to the flat bottom of the recess 119. The intermediate rewiring tape 103 is mounted on the semiconductor chip 102 so that the semiconductor chip

102 is accommodated within the recess 119 and the bottom surface of the rewiring tape 103 outside of the recess lies in approximately the same plane as the active surface of the lower semiconductor chip 102.

5

The upper semiconductor chip 101 is also a ball-grid array type package and includes an active surface with integrated circuit devices and chip contact areas 110. The upper semiconductor chip 101 is mounted to intermediate rewiring tape using the flip chip technique. A microscopic solder ball 105 is positioned between each of the contact areas 110 on the upper surface of the semiconductor 101 and a fourth contact area 121 of the rewiring tape 103.

15 The upper semiconductor chip 101 is electrically connected to the substrate board 104 by the second rewiring structure 126 which includes the tape conductor tracks 118 and tape vias 123 which connect the third 121 and fourth 122 pluralities of contact areas of the intermediate rewiring tape 103 and then by the solder ball 124 to the section of second rewiring structure provided by the second contact pads 112, second conductor track 113 and second vias 114 to the outer contact area 115 of the substrate board 104.

25 A stacked electronic component 100 is, therefore, provided by the invention. Although the embodiment shown in Figure 1 includes an assembly of two stacked flip chips, the invention can be used to provide a stacked module containing three or more stacked semiconductor chips.

30

Figure 2 shows a step in the method to produce a stacked electronic component according to the invention. Parts of the em-

bodiment which are essentially the same as the embodiment of Figure 1 are designated by the same reference number and are not necessarily described again.

5 Firstly, a substrate board 104 is provided. The central portion of the substrate board includes a rewiring structure 125 for the lower semiconductor chip 102 which is mounted on its upper surface. The rewiring structure includes a plurality of contact areas 105 on the upper surface whose lateral arrange-
10 ment corresponds to the lateral arrangement of the chip contact areas 110 of the semiconductor chip 102 which is to be mounted on the substrate board 104. The contact areas 105 are connected by conductor tracks 106 and vias 107 to outer connect areas 108 positioned on the bottom surface of the sub-
15 strate board 104.

The substrate further includes a second rewiring structure for the upper semiconductor chip 101 of the stack positioned towards its periphery including contact areas 112 on its upper
20 surface which are connected by conductor tracks 113 and vias 113 to the outer contact areas 115 positioned on the bottom surface of the substrate board 104.

A semiconductor chip 102 is then mounted by the flip chip
25 technique on the substrate board 104 by microscopic solder balls 111 positioned between the chip contact pads 110 and first contact pads 105 of the substrate board 104.

The rewiring tape 103 is provided in the form of a long strip
30 127 including an upper 116 polyimide film and a lower 117 polyimide film. The rewiring structure for each intermediate rewiring tape 103 including the tape conductor tracks 118 is

positioned between the two polyimide films. The rewiring strip 127 includes a plurality of intermediate rewiring structures 103 arranged at intervals along the length of the strip.

- 5 A pre-formed intermediate rewiring tape 103 includes an upper 116 and lower 117 polyimide foil. A plurality of third contact areas 121 are positioned in the central portion of the upper surface of the intermediate tape 103 and are connected by conductor tracks 118 to fourth contact areas 122 positioned in
10 the bottom surface at the periphery of the rewiring tape 103.

The lateral arrangement of the third contact areas corresponds to the lateral arrangement of the semiconductor chip 101 which is to be mounted on the intermediate substrate tape. The lateral
15 arrangement of the fourth contact areas corresponds to that of the second contact areas positioned in the periphery of the substrate board 104. The tape conductor tracks 118 lie in the centre of the rewiring tape 103

- 20 The intermediate rewiring tape 103 for the assembly 100 is formed by pressing a section of the rewiring tape strip 127 into the mould 128 of a template holder 129 in order to form a flat bottomed recess 119 in its central portion.

- 25 The recess 119 is laterally slightly larger than the lower semiconductor chip 102 and has a depth of approximately that of the semiconductor chip. The recess 119 is formed in the bottom surface of the rewiring tape 103 so that the third contact areas 121 are arranged in the upper surface of the intermediate rewiring tape which is raised by the recess 119 and
30 the fourth contact areas 122 lie in the bottom surface of the rewiring tape 103 outside of the recess 119.

The portion of the pre-formed intermediate tape 103 including the fourth contact areas protrudes laterally outwards from two opposing sides of the recess 119 and the bottom surface lies
5 in a plane parallel to the flat bottom of the recess 119. The section of the strip is cut to provide the pre-formed intermediate tape 103 for the assembly 100.

Solder balls 124 are then attached to the fourth contact areas
10 122 positioned on the bottom surface of the rewiring tape 103.

A layer of adhesive is applied the upper rear surface of the lower semiconductor chip 101. The pre-formed rewiring tape 103 is lowered onto the semiconductor chip 101 so that the flat
15 bottom of the recess 119 is attached to the rear surface of the semiconductor chip 101 and the semiconductor chip 101 is accommodated within the recess 119 of the rewiring tape 103. The solder balls 124 attached to the bottom surface of the peripheral fourth contact areas 122 of the rewiring tape 103 are
20 positioned on the second contact pads 112 at the periphery of the substrate board 104.

The solder is reflowed to electrically connect the intermediate rewiring tape 103 to the substrate board 104 and the template holder 129 removed leaving the pre-formed rewiring tape
25 103 attached to the substrate board 104 and lower semiconductor chip 102.

A second semiconductor chip 101 is then mounted on the upper
30 surface of the intermediate rewiring tape 103 using the flip-chip technique by microscopic solder balls positioned between the chip contact pads 110 and plurality of third contact pads

of the intermediate rewiring tape 103. The upper semiconductor chip 101 is, therefore electrically connected to the substrate board 104 by the second rewiring structure provided by in the intermediate rewiring tape 103 and periphery of the substrate board 104.

5

The stacked electronic component 100 is then encapsulated by a plastic mould material which is not shown in the figures for clarity.

10

Reference numbers

	100	stacked electronic component
	101	upper semiconductor chip
5	102	lower semiconductor chip
	103	intermediate rewiring tape
	104	substrate board
	105	first contact area
	106	first conductor track
10	107	first via
	108	outer contact area
	109	solder ball
	110	chip contact pad
	111	microscopic solder ball
15	112	second contact area
	113	second conductor track
	114	second via
	115	second outer contact are
	116	first polyimide foil
20	117	second polyimide foil
	118	tape contactor track
	119	recess
	120	adhesive
	121	third contact area
25	122	fourth contact area
	123	tape via
	124	solder ball
	125	first rewiring structure
	126	second rewiring structure
30	127	rewiring tape strip
	128	mould
	129	template holder

Claims

1. Semiconductor chip assembly comprising the following features:

- 5 - a substrate board (104) including a plurality of first contact areas (105) and a plurality of second contact areas (112) on its upper surface,
- at least one semiconductor chip (101) including a plurality of chip contact areas (110) on its active surface, a first semiconductor chip (102) being mounted on
- 10 the substrate board (104) by the chip contact areas (110) and the first contact areas (105),
- an intermediate rewiring tape (103) including tape conductor tracks (118) located between an upper (116) and
- 15 lower (117) electrically insulating film, and electrically connecting third contact areas (121) and fourth contact areas (112),

 wherein the intermediate wiring tape (103) has a recess (119), the recess (119) of the intermediate rewiring tape being mounted to the rear side of the first semiconductor

20 chip (102), and the fourth contact areas (122) of the intermediate rewiring tape being electrically connected to the second contact areas (112) of the substrate board (104).

25

2. Semiconductor chip assembly according to claim 1 characterised in that

 the fourth contact areas (122) of the intermediate rewiring tape (103) have a lateral arrangement which corresponds to the lateral arrangement of the second contact

30 areas (112) of the substrate board (104) and are electrically

cally connected to the second contact areas (112) by solder ball connections (124).

3. A semiconductor chip assembly according to claim 1 or
5 claim 2

characterised in that
the recess (119) of the intermediate rewiring tape (103)
is attached to the rear side of the first semiconductor
chip (101) by adhesive (120).

10

4. A semiconductor chip assembly according to one of the pre-
vious claims

characterised in that
the intermediate rewiring tape (103) includes tape conduc-
tor tracks (118) lying on two or more electrically iso-
lated inner layers.

15

5. A semiconductor chip assembly according to one of the pre-
vious claims

characterised in that
the first semiconductor chip (101) is encapsulated by
plastic mould material.

20

6. A semiconductor chip assembly according to one of the pre-
vious claims

characterised in that
the contacts (124) between the intermediate rewiring tape
(103) and the substrate (104) are encapsulated by plastic
mould material.

25

30

7. Stacked electronic component (100) comprising:

- the semiconductor assembly of one of claims 1 to 6, and

- a second semiconductor chip (101) mounted on the upper surface of the intermediate rewiring tape (103).

8. A stacked electronic component (100) according to claim 7
5 characterised in that

the lateral arrangement of the third contact areas (121) corresponds to that of the chip contact areas (110) on the second semiconductor chip (101) and the second semiconductor chip (101) is electrically connected to the rewiring
10 tape (103) by microscopic solder balls (111) between the chip contact areas (110) and third contact areas (121).

9. A stacked electronic component (100) according to claim 7
or claim 8

15 characterised in that
the semiconductor chips (101, 102) are encapsulated by plastic mould material.

10. Method to assemble a semiconductor chip assembly including
20 the steps of:

- providing a substrate board (104) including a plurality of first contact areas (105) and second contact areas (112) positioned on its upper surface,
- providing at least one semiconductor chip (102) with
25 chip contact areas (110) on its active surface;
- mounting a first semiconductor chip (102) on the substrate board (104) with the chip contact pads (110) and first contact pads (105) of the substrate board (104),
- providing a rewiring strip (127) which includes tape
30 conductor tracks (118) lying between an upper (116) and lower (117) polyimide foil tape, the rewiring strip (127) including a plurality of intermediate rewiring

tapes (103) arranged at intervals along the length of the strip (127), each intermediate rewiring tape 103 having a plurality of third contact areas (121) and fourth contact areas (122) connected by tape conductor tracks (118),

- forming the intermediate rewiring tape (103) for the assembly (100) from the rewiring strip (127) by pressing a section of the rewiring strip (127) into a mould (128) of a template holder (129) to provide a flat bottomed recess (119) in its central portion, and separating the intermediate rewiring tape (103) from the rewiring strip (127),
- applying adhesive (120) to the upper rear surface of the first semiconductor chip (102),
- attaching the pre-formed intermediate rewiring tape (103) to the rear surface of the first semiconductor chip (102),
- electrically connecting the fourth contact areas (122) of the intermediate rewiring tape (103) to the second contact pads (112) of the substrate board (104), and
- removing the template holder (129) leaving the pre-formed intermediate rewiring tape (103) attached to the substrate board (104) and lower semiconductor chip (102).

11. Method to assemble a semiconductor chip assembly according to claim 10

characterised in that

the fourth contact areas (122) of the intermediate rewiring tape (103) are provided with a lateral arrangement which corresponds to the lateral arrangement of the second contact areas (112) of the substrate board (104) and sol-

der balls (124) are attached to the fourth contact areas (122) positioned on the bottom surface of the intermediate rewiring tape (103).

5 12.Method to assemble a semiconductor chip assembly according to claim 10 or claim 11 characterised in that the first semiconductor chip (102) is encapsulated by plastic mould material before the intermediate rewiring
10 tape (103) is attached.

13.Method to assemble a semiconductor chip assembly according to one of claims 10 to 12 characterised in that
15 characterised in that the contacts (124) between the intermediate rewiring foil (103) and the substrate (104) are encapsulated by plastic mould material.

14.Method to assemble a stacked electronic component (100)
20 comprising the steps of:
providing a semiconductor chip assembly of one of claims 10 to 13,
mounting a second semiconductor chip (101) on the upper surface of the intermediate rewiring tape (103).

25

15.Method to assemble a stacked electronic component (100) according to claim 14 characterised in that the third contact areas (121) are provided with an arrangement corresponding to that of the chip contact areas
30 (110) on second semiconductor chip (101) and the second semiconductor chip (101) is electrically connected to the

rewiring tape (103) by microscopic solder balls (111) between the chip contact areas (110) and third contact areas (121).

5 16.Method to assemble a stacked electronic component (100)
according to claim 14 or claim 15
characterised in that
the electrical connection between the semiconductor chips
(102) and the substrate board (104), the second semicon-
10 ductor chip (101) and the intermediate rewiring substrate
(103) and the intermediate rewiring substrate (103) and
the substrate board (104) is performed in one process
step.

15 17.Method to assemble a stacked electronic component (100)
according to one of claims 14 to 16,
characterised in that
the semiconductor chips (101, 102) are encapsulated by
plastic mould material in one process step.

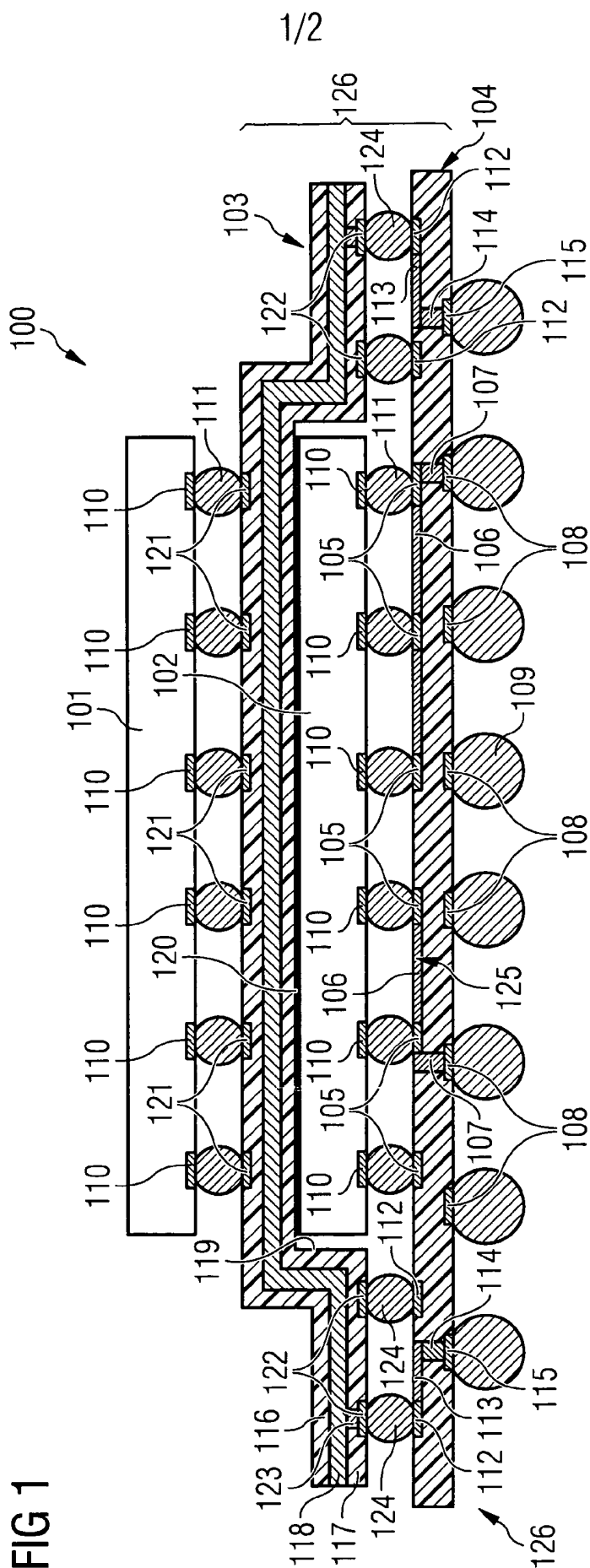


FIG 1

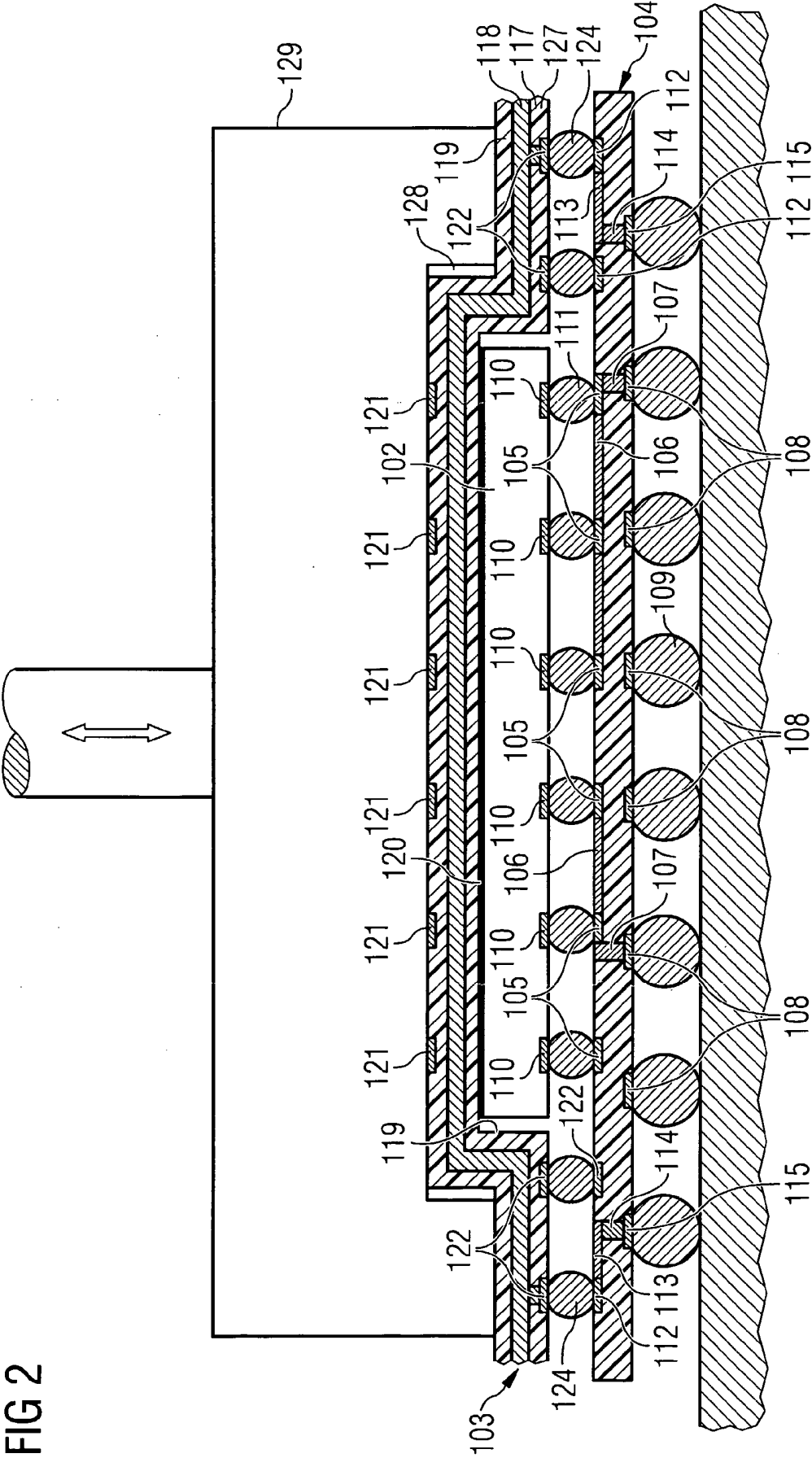


FIG 2

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PCT/IB2004/003175

IPC 7 H01L25/065 H01L25/11

B. FIELDS SEARCHED

IPC 7 H05K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	US 2003/165051 A1 (KLEDZIK KENNETH J ET AL) 4 September 2003 (2003-09-04) abstract paragraphs ‘0011!, ‘0046!, ‘0049!, ‘0054!, ‘0058! figures 2,4,8a,11 ----- -/--	1,2,4,7, 8 3,5,6, 9-17

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search

16 June 2005

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27/06/2005

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INTERNATIONAL SEARCH REPORT

International Application No

PCT/IB2004/003175

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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