(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 December 2010 (16.12.2010)

PCT

(10) International Publication Number
WO 2010/143944 A1

(51) International Patent Classification:
H05B 41/392 (2006.01) *H01J 61/56* (2006.01)
H05B 33/08 (2006.01)

(21) International Application Number:
PCT/NL2010/050054

(22) International Filing Date:
5 February 2010 (05.02.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2003011 12 June 2009 (12.06.2009) NL
2003677 20 October 2009 (20.10.2009) NL
1037553 14 December 2009 (14.12.2009) NL

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

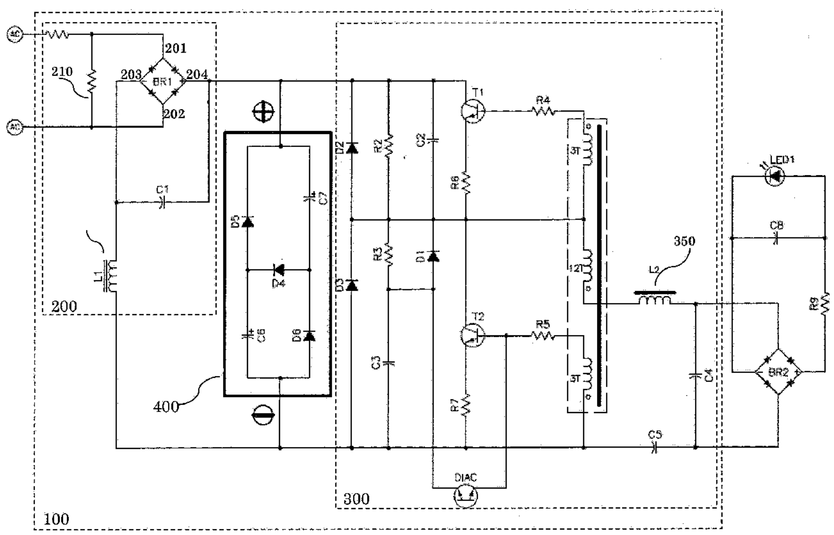
(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: POWER FACTOR CORRECTOR DEVICE FOR A DIMMING CIRCUIT

Figure 2



(57) **Abstract**: The invention relates to a power factor corrector device (500) for a dimming circuit, comprising: a power factor corrector circuit (400) comprising at least one capacitor (Cl, C2), to be coupled to a low frequency DC bridge rectifier output (203; 204); the power factor corrector circuit (400) including a flyback diode (Dl, D2, D3) coupled in parallel over said at least one capacitor (Cl, C2); and a clamping capacitor (C3) coupled in parallel to the power factor corrector circuit (400) adapted to clamp a high frequency ripple of a high-frequency switching-mode ballast device. The overall effect of the network is to extend as much as possible the —otherwise severely restricted- angle of conducted current drawn from the supply line.

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TITLE: Power factor corrector device for a dimming circuit.

FIELD OF THE INVENTION

The invention relates to a power factor corrector device for a dimming circuit.

BACKGROUND OF THE INVENTION

With the progress in lighting technology (and under continuous global pressure to develop more energy-efficient transducers) other kind of lamps has become popular, namely fluorescent lamps (F-L) and, lately, the high-brightness light-emitting diodes (LED-L) lamps. Both these lamps are no longer, such as the incandescent lamp, made of a simple, single resistive element but consist of several components of very different and disparate electrical properties themselves. Therefore, the total load that they present to the AC sinusoidal supply is very different from the simplex behaviour of a pure resistor. This calls for novel designs of ballast devices for dimming circuits.

In addition, the present and growing demand for compact H-B LED lamps constant current devices-controllers has motivated several well known electronic manufacturing firms to design, produce, and make commercially available Integrated Circuits (ICs) exclusively for this specific purpose.

As these ICs are custom-made and differ from each other in the topology of their respective working principles and power handling, the application designer has a very restricted choice when intending to design an in-house, brand-new, competitive and well-spread range of modern solid-state luminaries for household, commerce and industry.

The so called ballast has evolved from the already mentioned electro-magnetic to the sophisticated electronic types of today. Specifically, for the operational low-voltage halogen-incandescent luminaries they have even adopted the general commercial term of electronic transformers, with its implied meaning of simple voltage-down-converters (nominally 230 Volts AC household mains potential being in this case a relative high-voltage source.).

Thanks mainly to the amalgamation of the active components into integrated-circuits (ICs) and SMD (Surface-Mounted Devices) passive components generally available today, these LED lamps controllers have become very compact and attractive for being implemented within the tight enclosures of household-type incandescent and Compact Fluorescent Lamps (CFLs) of similar geometry and volume; thereby increasing its desirability.

These electronic device-drivers are in fact no more than very efficient SMPS (Switching-Mode Power-Supplies) in miniature. They are implemented in various general and well documented topologies, and new ones are being constantly developed as the requirements evolve with the availability of newer light transducers of different physical and electric properties and new electronic design techniques and manufacturing integration.

SUMMARY OF THE INVENTION:

The present invention aims to offer a price -and performance-competitive power factor corrector device for a dimming circuit that does not rely on source-scarce and relative expensive ICs: as their core, their source-power interface, as well as all their enhanced features. In addition it is aimed to incorporate such a power factor corrector device into a ballast device standard topology from end to end design that can be applied and easily extrapolated to a complete range and type of lamps of diverse power and applications.

In accordance with a first aspect of the invention a capacitive, two-terminal passive power factor corrector device is provided according to the features of claim 1.

In accordance with some aspects of the invention, a power factor corrector circuit is provided comprising at least one capacitor, to be coupled to a low frequency DC bridge rectifier output; the power factor corrector circuit including a flyback diode coupled in parallel over said at least one capacitor; and a clamping capacitor coupled in parallel to the power factor corrector circuit adapted to clamp a high frequency ripple of a high-frequency switching-mode ballast device.

According to another aspect, a high-frequency switching-mode ballast device for a dimming circuit is provided, the ballast device comprising:

a bridge rectifier section having an AC input and a DC bridge rectifier output;

a high frequency oscillator circuit including a main ballast coil assembly, coupled to the DC bridge rectifier output; and

a power factor corrector device comprising a power factor corrector circuit and a clamping capacitor.

In accordance with some other aspects of the invention, a dimmable CFL high-frequency switching-mode ballast device for a dimming circuit is provided, the ballast device comprising:

a power factor corrector circuit and a clamping capacitor coupled in parallel with the power factor corrector circuit.

In accordance with some other aspects of the invention, a dimmable energy saving lamp is provided comprising a light-transducer low-pressure gas tube including filaments arranged for starting the tube light transducing process; a high-frequency switching-mode ballast device for driving the gas tube, the ballast device comprising a bridge rectifier section having an AC input and a DC bridge rectifier output; a high frequency oscillator circuit coupled to the bridge rectifier output; and a main ballast coil assembly coupled to the oscillator circuit and arranged in series with the gas tube filaments; and further comprising a power factor corrector device comprising a power factor corrector circuit and a clamping capacitor coupled in parallel with the power factor corrector circuit.

The passive elements employed in the power factor corrector device provide the device with an impedance of a primarily capacitive character seen between the two terminals.

The overall effect of the power factor corrector circuit is to extend as much as possible the –otherwise severely restricted– angle of conducted current drawn from the supply line.

The overall effect of this power factor corrector device is to counter act a source for EMC induced by the power factor corrector circuit before it enters the ballast device.

Furthermore, the power factor corrector device is suited to be implemented in a dimming circuit as well as in a ballast device.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will further be elaborated with reference to the following Figures:

Fig 1: Block diagram of a dimming circuit for a LED lamp

Fig 2: Detailed circuit diagram of a 3W dimmable LED lamp according to the block diagram of Figure 1.

Fig. 3: Layout scheme of Power Factor Corrector circuit.

Fig. 4: Block diagram of Fig. 1 including the LED lamp.

Fig 5: Block diagram of the CFL

Fig 6: Detailed circuit diagram of Figure 5.

Fig. 7: Standard circuit diagram of a conventional 11W CFL.

Fig. 8 Circuit diagram of a modified power factor corrector device

Fig. 9 Mechanical construction diagram of the power factor corrector device of fig. 9

Fig. 10: Detailed circuit diagram of another CFL

Fig. 11 Pair of E-cores with primary and secondary coils

In the figures, similar or corresponding elements will be addressed using the same reference numerals.

Fig. 12. EMC frequency sweep of a CFL;

Fig. 13 EMC frequency sweep of a CFL with a Power Factor Corrector device;

DETAILED DESCRIPTION OF EMBODIMENTS

LED EMBODIMENT

Great progress has been made in the last part of the 20th century by the lighting industry in order to meet the new trend, especially in the field of fluorescent lamps: steadily the original the so-called electromagnetic ballast had made way for more efficient electronic types, and even the modern fluorescent tubes themselves have today a much better lumen-per-watt energy-conversion ratio.

The race is on for a lighting source with the least disadvantages and the most efficient input-power lumen-output ratio. The modern LED lamps seem to fulfil that requirement. Their main properties, vis-à-vis older technologies are:

- mechanical compactness and robustness, light and packing-friendly,
- lower operating voltage, less inherent operational stress,
- no brittle glass or vacuum enclosure required for normal operation,
- no direct heated metal transducer used,
- no mercury, amalgam or foreign catalyst required for energy conversion,
- inherent solid-state reliability and longer estimated working life,
- best lumen-watt ratio than incandescent and fluorescent lamps,
- no toxic residual chemicals precautions needed when replaced, disposed,

- availability in different primary colours and power ratings,
- steadily getting better as price-performance specifications evolve,
- solid-state's lower manufacturing risks,
- growing general consumer's budget-conscious acceptability,
- progressive tightening of official efficient legislation worldwide.

Although they seem to be a good bet for the future (as far as lighting-delivery transducers technology and range of applications is concerned), the developing engineer has to be aware of certain inherent limitations and restrictions for implementing successful commercial lamps, such as:

- normal low DC operational voltages coupled with relative high currents,
- point of source light transducer might need added distribution optics,
- concentrated energy will need some sort of thermal management,
- versatility, longer life and efficiency must not compromise real and perceived manufacturing, distribution and retail final cost barriers in order to make the technology, appealable and viable.

Therefore the challenge is to translate the obvious potential advantages of the LED lamps into a real-world competitive and popular price-performance product.

As the cost of the original High-Brightness (H-B) LED devices have come down in price dramatically in the last couple of years, the focus have been put squarely in the design and implementation of suitable low-cost drivers to match them, coupled with the desired goal of making a modern, more efficient and longer-lasting direct-replacement product for the ubiquitous household incandescent bulb.

The Power factor (PF) is defined as the cosine of the phase-angle between the load's voltage and current waves, which is a unit-less number between 1 and 0. When the PF=1, the voltage and current waves are in perfect sync, and all the energy that is supplied is consumed by the load (the PF of a purely resistive load is equal to 1). When the PF<1, the voltages and current waves are out-of-step, and only part of the energy supplied is consumed by the load, the rest being cyclically absorbed and then reflected back, at the frequency of the AC supply (in standard reticulation distribution, meaning 50 or 60 Hz).

Whereas incandescent lamps are purely-resistive loads, Fluorescent Lamps and high-brightness LED lamps include some substantial capacitive reactance themselves. Accordingly, their Power Factor is poor due to the resulting V/I phase-shift, and the part of the total power supply available to do real work is therefore somehow compromised by the presence of a concurrent reactive power term. Phase-cut dimmers are generally not suitable for dimming these poor PF lamps.

As this type of dimmer is advanced, it greatly distorts the incoming voltage wave-front progressively, and the higher harmonics elements so generated tend to increase even further the original reactance value-part of the load (at the nominal mains frequency), which leads to an even grater V/I phase-shift, a dramatic reduction of the originally inherent poor PF that this type of lamps have, and finally, an increased loss of the real available power.

This vicious-circle manifests itself as mild to severe flickering of the lamps as the dimmer control is advanced, and is most-evident when attempting to dim them below 50% (of their nominal maximum power output). The reactive part of the load, capacitive and/or inductive (Xc and/or Xl), induces a phase-shift between the supplied voltage wave-front and its consequential resultant load-current. The relative amount of phase-shift that thus occurs is a magnitude so called power-factor of that specific load.

Therefore, a purely inductive or purely capacitive load results in a relative phase-shift of minus/plus 90 degrees and a PF=0. Purely inductive or pure capacitive loads consume no power on average, but merely cyclically absorb and reflect the input power totally. Importantly then, the closer the PF is to 0, the less real power is available in the load transducer circuit to do work efficiently.

Turning now to Figure 1, the block diagram of the dimming circuit, coupled to AC mains is divided into four areas:
10) Triac-dimmer minimum-load interface.
20) Low-frequency AC to DC rectifier-converter.
30) Passive Power Factor Correction compensator integrated network device.
40) High-frequency DC to AC self-oscillating inverter.

Referring specifically to the 10 – 40 sections of Figure 1, the following is observed:

(10) Triac-dimmer minimum-load interface.

Most commercial dimmers are of the phase-cut topology and have at their core a high-voltage AC bipolar gating-controller device, an industry-standard electronic component known as a TRIAC. These dimmers, being low-cost due to their small component count, have historically been –and they still are- the most popular brightness controller for incandescent luminaries, hence their wide use in the average household, worldwide.

Though their electronic design principle is fairly standard, their actual manufacture implementation still differs quite a lot from brand to brand. Moreover, depending of the particular TRIAC device used, all have a specific - and perhaps diverse- maximum power-handling capability.

More importantly, in the present context of sourcing variable power to the relative much lower power LED lamps, is the -also generally stated in the product's packaging- specific minimum load requirement. This is mainly due to an inherent restricting electrical property of all TRIACS devices and it is very well published and understood.

In the present invention design, a fixed resistor of relative medium K-ohms value helps to equalize the performance of many disparate dimmer devices, especially at low brightness levels, as it presents a constant and fixed minimum working load to the wide-spread brands and types of light-controlling TRIAC-core products commercially available in the marketplace: their average response become smoother, less prone to flickering, less noisy, a more reliable operational life-span can be expected, and their general performance becomes more predictable.

Some contributions may include:

- To present a constant pure-resistive component to offset, at least partially, the reactively inherent characteristic of any CFL's input impedance.
- To help equalize the performance of the very disparate dimmer electronic designs dimming ranges, and the mechanical variations in their control-pot geometry span-travels.
- To present the dimmer's gating device (the TRIAC core) with a minimum load current to keep it conducting for a longer angle span, especially at the critical low-brightness dimming settings, when the avoidance of flickering is

highly desirable, not only just for aesthetics but also due to sound electronic design principles.

- As a perfect resistive element of fixed value, always in parallel with the changing lamp’s reactance (as it is progressively dimmed), it helps to keep the overall PF as high as possible, and therefore contributes –although partially, as compared to the principal contribution of the power factor corrector device described above- to keep the overall harmonic distortion in-check, as well.

(20) Low-frequency AC to DC rectifier-converter.

This is implemented as a high-voltage full diode-bridge rectifier topology 200 of standard-grade inverse-recovery response. Its many possible current-capacity rating values are directly proportional to the specific stated AC overall power consumption.

(30) POWER-FACTOR CORRECTOR.

A Power-Factor Corrector (PFC) is an electronic sub-circuit 400 needed to help reduce as much as possible the phase-shift between the input Voltage and Current wave fronts due to the presence of a complex/non-linear load.

A non-linear load (linear-load= perfect resistor) will generate some sort of spurious, non-desired harmonic (higher multiples) frequencies that, as they all add-up, will distort somehow, the generally clean sinusoidal fundamental low-frequency Mains supply wave-front (50/60 Hz). The greater the non-linearity factor, the worse the harmonic distortion will be.

Very strict International Standards are being currently enforced world-wide in respect of the electronic pollution limits that apply specifically to any kind of load/appliance/circuit connected to the L.V. Public Utility Supply distribution lines (110/220VAC) and that includes all luminaries.

There are two main power factor corrector implementation approaches: they are so called passive and active. Respectively, each presents the design and the manufacturing engineers with their own set of electronic and mechanical advantages and restrictions, notably challenging in the case of the CFLs. But the general idea, or rather common goal, is to make, somehow, the load as to look as much resistive as possible, taking in consideration the best price/performance, mechanical space/electronic complexity, and total design effort/features compromises.

According to an aspect of the present invention, a passive power factor corrector has been chosen for its simplicity, robustness, low-cost and, - as the provided comparative tests will confirm - it's very promising results.

The power factor corrector according to an aspect of the invention is practically realized by the integration within a single component sub-assembly (resembling an ordinary polarized 2-terminal electrolytic capacitor) of an electrical network of 2 capacitors and 3 rectifier diodes, placed just after the bridge rectifier 200, superseding a single reservoir capacitor characteristic of standard Low-PF lamps and at the same classical position. The overall effect of this network is to extend as much as possible the - otherwise severely restricted - angle of conducted Current drawn from the Supply line within the reference of the positive and the negative excursions of the input Voltage mains cycle/period.

Accordingly the power factor corrector circuit 400 comprises a two-terminal network of three serially switched diodes; wherein first and second diodes are coupled in parallel with a first polarized capacitor and wherein second and third diodes are coupled in parallel with a second polarized capacitor; the two-terminal network coupled in parallel to the bridge converter. The flyback diodes D4, D5, D6 or steering diodes make the capacitors' distributed overall charging and discharging process (from the supply and to the load respectively) smoother, predictable, balanced, self-adjusting and more independent of the load's demands. The overall input Current waveform tends to better follow the input Voltage waveform, and as its greatly improved average shape shows, brings into view a clear indication that the non-linearity conductive restrictions of the load have been largely overcome. According to an aspect, the present invention accordingly provides a front-end, highly efficient passive high power factor correction.

When integrating the electronic components of the capacitive circuit in a single electronic device, an example of which is illustrated in Fig 4, the result of the tight mechanical integration of 5 standard electronic components within this new 2-terminal Power-Factor Correction Device saves footprint space and interconnection tracks and holes on the PCB.

Accordingly, the power factor corrector circuit 400 is preferably designed as a two pin connectable device. The input impedance of the CFL now becomes less reactive, therefore with a marked and more defined resistive behaviour than was originally predicted if no power factor corrector were to be implemented. Much less energy bounces-back towards the supply-lines: the nasty harmonics are greatly restricted and the harmonic distortion is brought within acceptable specification's margins.

40) High-frequency DC to AC self-oscillating inverter.

The challenge presented by the need of a general-purpose and very compact power converter is magnified by the desire for a cost-effective but reliable

SMPS universal design topology that could be applied successfully to a full range of mains-powered luminaries.

Although new specific ICs available for this very purpose have started to appear in the marketplace, variations of tried and tested discrete components topologies can work as well as the emerging new-ones, and can be as good for its perceived price-performance competitiveness.

One of the most popular and reliable have been the so called DC-bus powered, High-Frequency, Half-Bridge AC Driver configuration, that is one of the group of ideals in order to excite non-linear/complex loads.
Again, modern manufacturing techniques have gravitated to amalgamate and miniaturize the main critical components of general-purpose Half-Bridge Drivers into Integrated Circuits, custom-made by well known power-control oriented design houses, and also manufactured under their licences by several third-party electronics concerns.

As the output load impedance of the converter remains relatively fairly constant, and its input power DC-BUS voltage varies with the progressive dimmer operation, a variable current control is developed onto the LED devices themselves, therefore proportionally varying their brightness.

A simple design calculation to properly rate all the current-carrying components of the basic topology design core, in order to encompass all the products within a set range of industry-standard power outputs, then becomes a very simple scale and straight-forward proportionality task.

According to an aspect, no specialized high voltage IC-driver is used but a discrete high voltage switched mode power supply.

Figure 2 refers to a detailed block diagram showing practical implementation of the device. Accordingly, there is shown a high-frequency switching-mode ballast device 100 for a dimming circuit, the ballast device 100 comprising a bridge rectifier section 200 having an AC input 201; 202 and a DC bridge rectifier output 203; 204; a high frequency oscillator circuit 300 including a main ballast coil assembly 350, coupled to the DC bridge rectifier output 203; 204; and further comprising a power factor corrector circuit 400 comprising at least one capacitor C6, C7, coupled in parallel to the DC bridge rectifier output 203; 204; the power factor corrector circuit 400 including a flyback diode D4, D5, D6 coupled in parallel over said at least one capacitor C6, C7. A resistive network (210) may be coupled to the DC bridge rectifier input to further enhance the power factor.

Figure 3 shows a detailed layout scheme for the power factor corrector functional circuit which may be applied in other electrical layouts for improving a power factor.

Figure 4 shows an embodiment, wherein the dimming circuit is arranged for driving a (H-B) LED 60.

Basically, a LED is a current-driven energy-transducer device and can be driven electrically only by a direct (unipolar or single polarity -generally labelled as DC-) energy-source. Its maximum normalized current has a tight specification and can not otherwise be exceeded without a predictable sure failure: in electronic terms it has a very low dynamic impedance. Therefore the control of its current is the most important requirement for the associated electronic driver.

Its normal operating voltage is relatively very low (only a few volts) and once it is progressively achieved (i.e.: as a slow rise from 0 Volts can testify), it will remain relatively constant. Thereafter it will revert to its constant-current drive requirement, so long as it is operated within the range of its maximum specified current limit.

H-B LED devices are basically designed for constant current operation to attaint their maximum specified efficiency, therefore there is a general perception that they can not be directly dimmable by voltage drivers means.

According to an aspect of the present invention, as opposed to industry standard current driven control topologies, the present invention provides a voltage driven and dimming control design for a LED device. Accordingly, the LED-device according to the invention comprises a ballast device providing a voltage driven dimming control design.

For a discussion of block elements 10-40, reference is made to Figure 1. In addition, for driving the HB-LED 60, block element 50 references a high-frequency AC to DC rectifier and ripple-compensation network.
Since the LED devices are essentially unipolar in their normal operational drive requirements, a high frequency and efficient AC to DC conversion is implemented in the present invention. The use of an inverse fast-recovery full-wave rectifier diode-bridge configuration aids to this purpose in a simple, compact and robust way, which rating can as well be scaled to each particular LED lamp nominal power output.

According to an aspect, the driver is of a fixed frequency, and no frequency control is required.

In order to extend to its maximum dimming performance capabilities of the LED lamps, an optional and proportionally rated relative low voltage electrolytic capacitor could be added in parallel with the output DC polarized terminals of the high-frequency rectifier diode-bridge to aid to minimize any onset of flickering behaviour that could appear on the LED devices at very low brightness levels, if so required. It could, as well, help to the generally smoother transitional operation of the dimmer controller itself, as it is exercised throughout its full range.

CFL EMBODIMENT

Before further elaboration on the drawings 5-8, the following is considered regarding the switching behaviour of ballast devices for CFLs. The problem is not the household dimmer or the CFLs themselves. The reason for this poor performance resides mainly in the electronic-properties (characteristic impedance) miss-match between them.

This dynamic inter-action between the source energy device and its corresponding load counterpart is seldom perfectly efficient, and there is always certain loss when attempting their practical inter-coupling.

When an AC load is not a perfect resistor (as generally is the case in the incandescent-type lamps), the electrical source-energy is not converted into light-energy in its entirety: curiously, some part of the incoming-energy is absorbed by the load (and converted into light and heat) and some of it is rejected, or more appropriate, bounced-back towards the source. The load circuit reacts against its source, so to speak due to its reactance.

An AC complex-impedance-load is therefore one that has some resistance AND some reactance values. The reactive components of the load are the cause of losses and wasted applied energy; therefore, the aim of any good engineering electronics AC design is to keep the resistive/reactive-ratio of the load as high as possible in order to obtain the maximum desirable -but practical(i.e. cost-effective)- energy-transfer (efficiency) effect. One way to express this important ratio is called: the Power-Factor of the load. Another way (mainly concerning known complex loads) might be: the relative index of the load's capability to do real work.

As indicated above, Power-Factor (PF) can be described as the resultant amount of phase-shift angle between Voltage and Current that can be induced by any load (with some reactive component/s in them) when an AC electrical source-energy is applied to it. The magnitude of the PF is defined as the value of the cosine of said angle, therefore, a unit-less number between 1 and 0.

When the AC load is a pure resistor, practically all the energy is transferred to the load, (as –by definition- there are no reactive components in them), and therefore no phase-shift can occur: the PF= 1.0 (theoretically).
Voltage and Current are said to be always in-phase: the work efficiency of the circuit is maximum.

When an AC load is a pure reactance (i.e. a perfect Capacitor and/or a perfect Inductor), the load not only bounces-back all the incoming energy: but the resultant phase shift is theoretically +/- 90 degrees now, and therefore the PF = 0.0. Transfer efficiency is at minimum, as only heat losses are generated.

In between these two extreme examples, the real-world of generally useful electronics application resides. One of the most ubiquitous is the modern, so-called, energy-saving CFL.

A CFL is composed of a few dozen different electronic components, but basically can be thought-of a miniature high-frequency switching-mode power supply (HFSMPS) driving a light-transducer low-pressure gas tube 160. The overall input impedance of the CFLs are far removed from the theoretical pure-resistive concept, (vis-à-vis: the incandescent paradigm) as their Power Supply (PS) front-end are made (on purpose) highly capacitive due to the need for reservoir or smoothing DC capacitors of very significant value, as any good AC/DC/AC frequency converter design must have for its intended stable and reliable long-term operation.

This relatively significant capacitive character of the input impedance of the classical front-end of the PS of any standard fluorescent lamps tends not only to lower their PF, but as a direct consequence (due to their added full bridge rectifier-diodes standard configuration and conductive behaviour), distorts the incoming Current supply waveform itself, proportionally increasing the Total Harmonics Distortion (THD).

Turning now to Figure 5, the block diagram is divided into two areas:

(A) Integrated front-end area including aspects according to the invention;
(B) Conventional circuit elements of CFL circuitry including a rectifier;

Just for completion and without limitation we refer to the details of Figure 2 to provide an embodiment of the conventional circuitry of the areas indicated as B-1 (ballast)– B-2 (Bridge rectifier section) and B-3 (dimmer); variations and modifications to this standard circuitry are known and deemed to be included in the specification.

Referring specifically to the A1 – A4 sections of Figure 5, the following is observed:
(1) POWER-FACTOR CORRECTOR.

A Power-Factor Corrector (PFC) is an electronic sub-circuit needed to help reduce as much as possible the phase-shift between the input Voltage and Current wave fronts due to the presence of a complex/non-linear load.

A non-linear load (linear-load= perfect resistor) will generate some sort of spurious, non-desired harmonic (higher multiples) frequencies that, as they all add-up, will distort somehow, the generally clean sinusoidal fundamental low-frequency Mains supply wave-front (50/60 Hz). The greater the non-linearity factor, the worse the harmonic distortion will be.

As already referred to, very strict International Standards are being currently enforced world-wide in respect of the electronic pollution limits that apply specifically to any kind of load/appliance/circuit connected to the L.V. Public Utility Supply distribution lines (110/220VAC) and that includes all luminaries; therefore, CFLs fall within the scope of this sector.

Also, as already referred to, there are two main power factor corrector implementation approaches: they are so called passive and active. Respectively, each presents the design and the manufacturing engineers with their own set of electronic and mechanical advantages and restrictions, notably challenging in the case of the CFLs.
But the general idea, or rather common goal is to make, somehow, the load as to look as much resistive as possible, taking in consideration the best price/performance, mechanical space/electronic complexity, and total design effort/features compromises.

In the context of this specification, a passive power factor corrector has been chosen for its simplicity, robustness, low-cost and, –as the provided comparative tests will confirm-, its very promising results.

The power factor corrector according to one aspect of the invention is practically realized by the integration within a single component sub-assembly (resembling an ordinary polarized 2-terminal electrolytic capacitor) of an electrical network of 2 capacitors and 3 rectifier diodes, placed just after the bridge rectifier B2, superseding the single reservoir capacitor characteristic of standard Low-PF lamps and at the same classical position. The overall effect of this network is to extend as much as possible the – otherwise severely restricted- angle of conducted Current drawn from the Supply line within the reference of the positive and the negative excursions of the input Voltage mains cycle/period.

Accordingly, the power factor corrector circuit A1 comprises a two-terminal network of three serially switched diodes, wherein the first and second diodes are coupled in parallel with a first polarized capacitor and wherein the second and third diodes are coupled in parallel with a second polarized capacitor; the two-terminal network is coupled in parallel to the bridge converter. The flyback diodes (D4, D5, D6) or steering diodes make the capacitors' distributed overall charging and discharging process (from the supply and to the load respectively) smoother, predictable, balanced, self-adjusting and more independent of the load's demands. The overall input Current waveform tends to better follow the input Voltage waveform, and as is greatly improved average shape shows, brings into view a clear indication that the non-linearity conductive restrictions of the load have been largely overcome.

When integrating the electronic components of the capacitive circuit in a single electronic device, an example of which is illustrated in Fig 3, the result of the tight mechanical integration of 5 standard electronic components within this new 2-terminal Power-Factor Correction Device saves footprint space and interconnection tracks and holes on the PCB.

Accordingly, the power factor corrector circuit A1 is preferably designed as a two pin connectable device. The input impedance of the CFL now becomes less reactive, therefore with a marked and more defined resistive behaviour than was originally predicted if no power factor corrector were to be implemented. Much less energy bounces-back towards the supply-lines: the nasty harmonics are greatly restricted and the harmonic distortion is brought within acceptable specification's margins.

(2) ELECTRO-MAGNETIC COMPATIBILITY COUNTER-MEASURES.

The A2 block of Figure 5 is a schematic illustration of a low pass filter including an inductor A2 coupled in parallel to the power factor corrector circuit A1 to provide a low pass filter. More particularly, an L-R High Frequency Low-Pass Filter (HF-LPF) A2 is configured in series with the total circuit load's current-return-path 130.

Harmonic distortion can be measured with specialized relative low-frequency response analyzers (up to the 40^{th} Harmonic of the fundamental Mains frequency, -50 or 60 Hz.-, that means roughly up to 25KHz or so.). The current pass-specification usually keeps a special watch for the third and the fifth ones, still within the realm of very low frequencies, indeed.

If the power source is a theoretical constant sinusoidal one, and the load is relatively stable, the upper terms of the harmonic distortion will be greatly reduced. Therefore, with just a properly rated and good performance power factor corrector device added to any CFL's front-end, their overall electronic design will be expected to be within the desired specs.

But that is only part of the whole EMC (Electro-Magnetic Compatibility) assessment that all electrical and electronic products must comply with.

Any HFSMPS (high-frequency, switching-mode power supply) is a source of interfering harmonics also, and every CFL must have one due to its inherent AC/DC/AC switching frequency-conversion topology.
As the fundamental of the built-in converter of any CFL is already at around 40KHz and above, we can expect very high frequencies to be present in the total electrical circuit as well, as the load that the converter (more precisely, inverter at this stage) sees, is a highly non-linear one (as it includes the highly complex electronic dynamic behaviour of the tube itself.). Without being restricted to a specific lower limit, high frequency will be meant to indicate at least in the KHz range, more specifically at least 20 KHz and higher to MHz frequencies relevant for EMC specifications; where low frequency will be meant to indicate lower than this lower limit, especially, in the range of 50/60 Hz and lower harmonic multiples, relevant for THD specifications.
If we add to this scenario the possibility of varying the input power to the tube by means of varying the power input to the whole lamp (and its core non-sinusoidal switching driver) with a waveform-chopping device (any Phase-Cut dimmer comes into view from here on), we have in every CFL itself a potential interference-generator of very important magnitude indeed.

As this EMC-passing regulation extends a mandatory test up to 30MHz, means must be provided to minimize the HF fundamental and its harmonics so generated by the SMPS driving the fluorescent tube circuit.

To this effect, a L-R High Frequency Low-Pass Filter (HF-LPF) is configured in series with the total circuit load's current-return-path towards the Mains power source. The inductive element (L1, Fig. 6) is located in series with the total DC current return circuit, and the resistance element (R1, Fig. 6), that does double-duty as a safety current-limiter in case of a short-circuit inside the whole CFL assembly, is complementarily located in series with the total AC input current path into the lamp.

The inductor is implemented as a HF-choke made of a copper-wire coil wounded around a ferrite core, and the resistor is a low-value, high-power one. All and each element's current-carrying capacity of the L-R filter must be dimensioned according to the rated output (20-1; 20-2) maximum brightness required for each CFL, taking in consideration, as well, the extra dissipation required to deal effectively with the onset of spurious higher power-terms of significant value, specially when dimming.

A full disclosure of the typical values of the components of this HF-LPF is given (as a general practical, feature-enhanced, actual lab implementation example, that has been built based on an standard 11W CFL, and used here with the only purpose as to provide real, complementary and fair comparative test results to the solid validity of this mainly theoretical document) with reference to Figure 6, below.

In another preferred embodiment, a DC electrolytic capacitor is added in parallel with the high power factor switching arrangement, see figure 10 capacitor C3.
The low frequency ripple generated by the high power factor switching topology, is introduced to the DC supply rail and hence forth amplified by the two switching transistors at high frequency generating harmonic and electromagnetic interference. This subsequent low frequency interference would on its own not pose substantial difficulty, but is amplified by the high frequency switching transistors, possibly creating EMC incompatibility on to the mains Voltage return line. This effect also manifests itself as heat, generated in inductor L1 acting as a choke and having to deal with the subsequent harmonic distortion now apparent in the circuit, making this

design less desirable and more energy hungry. It now has been surprisingly found that in order to counter the effects hereof, an electrolytic capacitor can be added as a clamp to minimise the effect of the ripple being generated by the high power factor topology. This electrolytic capacitor needs to be calibrated as to find a balance between the EMC, THD and overall performance of the device. This configuration is by no means conventional as it seems counterproductive, by making the HPF switch topology less efficient and increasing the THD generated by the device. However, when properly calibrated, the high power factor switching arrangement has been found to properly operate within the desired specs.

It is envisioned that this capacitor should be of very low value in the order of between 200nF and 900nF and appropriate Voltage for its intended application market. As a typical example, before the adding of this electrolytic capacitor, a typical value for the power factor in a CFL of power value between 5W and 25W would be between 0,9 and 0,96, after adding the capacitive device correctly calibrated, a typical value would be in the order of 0,85 to 0,9, still qualifying under international standards as a HPF device. For a CFL of 7W, for example, 0,27μF, 9W = 0,3μF, 11W=0,3μF, 15W=0,47μF, 20W=0,6μF, 25W=0,47μF.

(3) MAINS-PORT'S DIMMER/LAMP INTERFACE.

Conventional so called Phase-Cut dimmers have at its AC controlled-current core a bi-polar gating electronic component popularly known as a TRIAC. Accordingly, in an embodiment, the dimming circuit B3 is of a phase-cut off type typically including a TRIAC. As these types of dimmers have been (and still are) the de-facto standard for the entry-level household sector, and as good as their advantages are, such as: low-price, ruggedness and compactness, unfortunately those face-value advantages are offset by the poor control of the brightness of any standard, off the shelf (and so rightly labelled) non-dimmable CFLs.

When a typical consumer takes them home and attempts to connect them to an existent dimming circuit B3 for the first time, erratic, noisy and severe flickering behaviour soon follows, just only after a few minutes into the trial.

Persistent manipulation of the dimmer or re-starting the lamps at low levels, usually leads to the permanent failure of the CFLs, (sometimes of both devices) fairly soon into the continuous repeat of this helpless attempts.

Just a simple resistor (or resistor network) of proper value and rating, placed at the input mains' port of the CFLs can make the performance of any phase-cut dimmer more predictable and repeatable. A practical value and rating is given in Figure 6. Accordingly, preferably, a resistive network A3 is provided coupled in parallel to the DC bridge rectifier input (10-1; 10-2) to interface with a dimming circuit B3.

(4) TUBE'S FILAMENTS HEATING.

As already mentioned above, the integrity of the filaments 70 at each end of the florescent tube is a clear indication of the relative life-condition of any CFL.

The filaments 70 are necessary to help start the ionization process of the compound heavy-metal and complex gas structures inside the tube's rarefied low-pressure vacuum that finally starts to break its initial high impedance state (due to the initial presence of a high-voltage differential potential) in order for an arc to develop across it length and thus starts the lamp (strike phase).

The high current burst that immediately follows –as the impedance of the lamp instantly decreases dramatically- excites the mercury gas inside with enough energy as its free electrons are able to release visible light-bearing photons as they collide with the atoms of the phosphor coating inside. Finally, after a few of seconds, when the lamp has reached its optimal balanced temperature, automatically acquires its natural steady-state phase, developing its specifically-designed public parameters, such as its normal running current, nominal power rating and stated luminance output (20-1; 20-2).

This situation is normally referred to as a CFL's cold start-up.

The hard-metal filament's core-base are themselves coated with a chemical substance that favours the emissions of primary-source electrons as to greatly facilitate the reliable but complex series of processes that finally bring the lamp to its strike phase. Therefore their integrity, or otherwise the lack of it, is the weakest link in the tube, and they constitute mainly the initial load when the driving electronics are started as the mains power is initially applied to the lamp: the filaments 70 take an initial substantial stress each time the lamp is powered up.

Eventually, with time and the repeated power-ups, the special chemical coating on the filaments 70 begin to literally peel off due to the normal wear and tear of the inter-collision of atoms and electrons due primarily to the relative big surge start-up and (although at a much lesser rate) the normal arc AC currents (back and forth) from end to end of the tube.

This has the effect of start pitting the sensitive coating, exposing the bare hard-metal and, at this stage, the deterioration of the filaments 70 continuing to occur at an accelerated rate, until eventually one (or both) breaks up and an open filament situation develops.

From now on, it will be almost impossible to start the CFL. A so-called tube's black-end will be symptomatic of this progressively undesirable development.

As to add further value to the features already described in this specification, it is herewith proposed to add a constant filament heating feature that will not only facilitate the initial emission of source electrons, but will soft-start the CFLs with much less electronic overall stress, will help to keep the integrity of their filaments 70 (as their coatings will be less prone to the rate of pitting otherwise occurring with the cold-start situation) and therefore, as a great bonus to the consumer, extend substantially their normal useful life expectancy, more particularly when dimming is applied.

The implementation is again, simple, rugged and reliable enough to always guarantee a soft-start from initial power-up and an automatic filaments 70 protection when attempting to re-start an already extinguished lamp at low brightness dimming levels.

The inductance of the choke and the start capacitance values defines the resonant frequency-circuit that builds-up the required high voltage necessary to generate the necessary initial burst of arc-current that will start the lamp.

Until the resonance point is not achieved, the lamp will not have a enough high-voltage to start-up; therefore, if for some brief time (while at the same time some current is allowed to pass through both filaments 70) their naturally low cold resistance will steadily increase, automatically pre-heating them and will start to generate source electrons just prior to the initiation of the ignition phase.

To realize that important condition during this initial phase, heating supply current for both filaments 70 is obtained from a transformer configuration built-in within the main ballast coil assembly: two independent small-turn coils 140 are added electrically independent and in parallel with each filament.

After the lamps strikes, and from now-on until the overall mains power supply to the lamp is interrupted, the filaments 70 will always be provided with their heating current, even in the case the lamp has apparently extinguished (due to over-extension of its useful dimming range, or maybe due to a sudden or progressive drop in ambient temperature),as their internal oscillator still will be operational. This can substantially improve a dimmed CFL's lifetime.

Therefore, a residual AC current will still pass though the filaments 70 (as the driver electronics are still powered, although with lower incoming mains current), as to keep them still in a relative warm situation. A small increase in the input supply mains current (usually just by tweaking upwards the dimmer's control pot.) will then normally be enough to soft-start and re-ignite the lamp, safely and with no electronic stuttering (no apparent flickering) whatsoever, thus avoiding a filaments 70 wearing, continuous cold re-starting, vicious-circle condition of popular previous designs.

Typical secondary's coil parameters are given with reference to Figure 6 in the section just below (only for the 11W CFL reference design, and presented here only as a specific practical implementation example).
Accordingly, it is shown that the dimmable energy saving lamp preferably comprising a gas tube 160 filament heating circuit. The heating circuit may be provided by small-turn coils that are added electrically independent and in parallel with each filament; arranged in transformer configuration built-in within the main ballast coil assembly.

Fig. 6 refers to a detailed block diagram showing practical implementation of the device.

Fig. 7 shows, for reference purposes, a conventional layout of a high-frequency, switching-mode power supply arrangement without the power factor corrector functional circuit.

Topology, component values and (when required) their ratings are disclosed. The easy integration possibility of the enhanced circuit into a conventional standard CFL topology, is plain evident. The new circuitry has been numbered according to their detailed described sections (in the text above), and identified within dashed lines.

Although a specific type and specific power (prototype-quality) CFL have been constructed to assess the real-world application of the principles disclosed in this document, the integration of all and/or some of the enhancements in order to improve the performance and features over any standard design (as has been the aim of this specification), can be extended and applied successfully across a wide board of all CFLs, and higher-power Electronic Ballasts that are at the core of all modern and efficient luminaries, (including the H.V. LED devices), of any topology and/or any power whatsoever; the only concern being the assessment of the final values and ratings of the components involved. In conclusion, standard off-the-shelf CFLs are not designed to be compatible with the standard household Triac-type/Phase-cut dimmer devices. The incorporation of a novel front-end sub-assembly substantially optimizes their inherent low Power-Factor, and reduces overall components count. Means for a filament's constant heating feature have been included within the preferred embodiment, as to greatly extend their normal expected life span.

2-TERMINAL HPF COMPENSATOR DEVICE:

The PFC-device of fig. 8 is, similar to the device of Figure 3, implemented as a 2-pin element.

Fig. 9 shows a physical arrangement for this scheme with dielectric 102, 103 and metallic foils 104, 105 allowing a compact housing. In particular, a clamping capacitor C301 is shown formed by a segmented outer foil 104 coupled to the + terminal, opposite an inner foil 105 and divided by a dielectric 103 to provide indicative values between 200 and 900nF. In particular, non limiting values are: for a 7W CFL lamp: a 0.27uF/400V clamping capacitor; for a 9W lamp: a 0.3uF/400V clamping capacitor; for a 11W lamp a 0.3uF/400V capacitor; for a 15W lamp; a 0.47uF/400V clamping capacitor; for a 20W lamp, a 0.6uF/400V clamping capacitor; and for a 25W lamp; a 0.47uF/400V clamping capacitor

Outer foil 104 is further segmented and electrically coupled via diode D201 opposite segmented inner foil 105 that is electrically coupled via diode D101 and divided by a dielectric 102 to provide two corresponding capacitors C201 and C101 with indicative capacitive values between 5 and 25 uF/250V.

A diode D301 divides dielectric 102 and is coupled in flyback configuration to the diodes D201 and D101 to form a two-terminal network of three serially switched flyback diodes (D101, D201, D301); wherein the first and second diodes (D201, D301) are coupled in parallel with a first polarized capacitor (C101) and wherein the second and third diodes (D301, D101) are coupled in parallel with a second polarized capacitor (C201).

As opposed to active P(ower) F(actor) C(orrection) devices in the form of customs multi-pins ICs, the implementation of the present compact and highly reliable passive PFC made of inexpensive and readily available components, make this new design attractive and embodied possibly including some of the following advantages:

- rugged and compact single unit integrated two pin construction in the form of a standard electrolytic capacitor; which provides substantial PCB footprint saving as opposed to multi-pin active PFC IC devices.
- 500V DC H.V. constant withstanding capacity.
- Easy to adapt to different power inputs, directly from the manufacturing factory floor.
- Inexpensive, multi-sourced and ready available integral parts.

Integrated Capacitor C301 can help with the passing margin of EMC regulations, greatly improving the performance (and minimizing the pitfalls) of current passive HPF designs, without adding any other EMC active nor passive components ("counter-measures") into any CFL PCB design.

The HPF device module design helps the CFL run cooler; less spent heat means more efficiency power-transfer conversion ratio and better Lumen/Watt product specification.

The present design allows ready configuration of an electrolytic capacitor production machine and is impervious to Electrostatic Discharge (no sensitive active components in circuit).

Fig. 10 shows another embodiment in addition to the shown power factor corrector circuit (400) of Fig. 2 wherein a clamping capacitor may be coupled in parallel to the power factor corrector circuit (400). In this manner an enhanced power factor corrector device (500) is provided.

Fig. 11 INTEGRATED CFL BALLAST COIL ASSEMBLY L3 AND FILAMENTS HEATER TRANSFORMER:

As opposed to non-dimmable CFLs (whose power input-output ratio is kept constant), the dimmable variety performance is greatly enhanced by the constant heating of their filaments while dimming, as it mainly helps to improve the life-time span of the lamp, and aids in its easy re-strike when the dimmer is brought back-up from its minimum settings.

Most designs employ discrete/stand-alone single (or several) dedicated "ring-core" ferrite coils/transformers in series with the main ballast coil current path. In this design a pair of E-cores is applied, allowing a compact housing; a first core element 312 including a main coil winding 150, and a second core element 412 coupled to the first core 312 providing for the secondary windings 401 and 402 in transformer configuration. Accordingly, the secondary windings 401 and 402 are provided as small-turn coils that are added electrically independent and in parallel with each filament; arranged in transformer configuration built-in within the main ballast coil assembly 312; 150.

POWER FACTOR CORRECTOR DEVICE

As described above with reference to Fig 3, a power factor corrector circuit (PFC-circuit) can be applied in dimming circuits for driving LEDs as well as CFLs (or a combination of both). To counter act the EMC induced by such a PFC-circuit a clamping capacitor is coupled in parallel therewith as shown in fig. 8. Such PFC-device is implemented in another CFL embodiment as shown in figure 10.

This modification diminishes the power factor slightly, but improves the EMC performance greatly, as the source thereof is removed before it can be amplified by the circuitry portion of a conventional ballast device. In this manner the parasitic interference over the classic HPF Cap/diodes standard design is drastically reduced. Furthermore, it improves the running of the lamp as it is quieter, cooler and highly efficient.

Below are test results showing the difference in Power Factor performance before and after the clamping capacitor modification as displayed on the digital front panel of a UI3000 Electronic Ballast Tester.

Before mod:
(1) Vac Input (rms) = 248.9V.
(2) Iac Input (rms) = 0.068A.
(3) Power Input = 16.2W.
(4) Power Factor = 0.962.

After mod: (small electrol. cap added => 2x 2.2uF/250V in series...)
(1) Vac Input (rms) = 248.1V.
(2) Iac Input (rms) = 0.081A.
(3) Power Input = 15.9W.
(4) Power Factor = 0.784.

The enhancement of the EMC performance is shown in Figs. 12 and 13. They show the result of an EMC frequency sweep of a CFL before (Fig 12) and after (Fig 13) providing the clamping capacitor. The sweep of measured frequencies ranges from 100 kHz. to 2 MHz. The plots show the amount of energy measured in μV on the vertical axis in dB plotted against the EMC frequencies on the horizontal axis. Comparison of the plots indicates a decrease in the levels of EMC. In particular in the range of 100 - 400 kHz (scale is 200 kHz. / div.) the decrease is at least 10 dB or more (scale is 10 dB / div.).

The elements employed for the power factor corrector device and the power factor corrector circuit comprised therein, are all passive elements. Passive elements, such as resistors, capacitors and diodes, do not generate energy or provide power gain, but merely store or dissipate energy. Whereas, active elements, such as current sources, voltage sources and transistors, do generate energy or at least can provide power gain.

The electrical impedance of a circuit of passive elements can be expressed as a complex quantity in terms of a Real part and an Imaginary part, wherein the Real part relates to the resistance and the Imaginary part relates to the reactance. When no inductors are present the reactance is primarily capacitive, and hence the impedance has a substantially capacitive character. However, this does not exclude some resistive character as well.

As in the PFC-device and PFC-circuit no inductors are employed, as particularly in the embodiments with only capacitors and diodes, the electrical behaviour has a primarily capacitive character. The arrangement of the capacitors and the diodes as flyback diodes has the effect of routing the Current in correspondence with the voltage polarity.

The present design has various mechanical/electrical advantages:
- integrated concept saves parts, wiring, assembly time and PCB foot-print;
- compactness means more reliability and ruggedness;
- no interconnecting loose wires;
- heating of the filaments starts instantly as the internal oscillator is powered up, even before the lamps strikes (assured pre-heating, always eases the stress on the tube and the electronic components, again helping to the optimum strike repeatability situation, reliability and longevity of the lamp);
- EMC conducted and radiated interference is kept to a minimum as a single point-source which can be dedicatedly shielded;
- rugged integration means easy handling and efficient mechanical compactness.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments. In particular, as shown in various embodiments, the clamping capacitor may be dispensed with.

The PFC-circuit comprising 2 capacitors and three diodes can also be arranged from a number of N capacitors and N + 1 diodes, while providing a first direct path along all the diodes in one direction and a second path along all the capacitors in the opposite direction.

Although a specific type and specific power (prototype-quality) LEDs have been constructed to assess the real-world application of the principles disclosed herein, the integration of all and/or some of the enhancements in order to improve the performance and features over any standard design (as has been the aim of this specification), can be extended and applied successfully across a wide board of all the LEDs, and higher-power electronic ballast that are at the core of all modern and efficient luminaries, of any topology and/or any power whatsoever; the only concern being the assessment of the final values and ratings of the components involved.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor or other unit may fulfil the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measured cannot be used to advantage. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS

1. A power factor corrector device (500) for a dimming circuit, comprising:

- a capacitive two-terminal passive power factor corrector circuit (400), comprising at least one capacitor (C1, C2), to be coupled to a low frequency DC bridge rectifier output (203; 204); the power factor corrector circuit (400) including a flyback diode (D1, D2, D3) coupled in parallel over said at least one capacitor (C1, C2); and
- a clamping capacitor (C3) coupled in parallel to the power factor corrector circuit (400) adapted to clamp a high frequency ripple of a high-frequency switching-mode ballast device.

2. The power factor corrector device according to claim 1, wherein the power factor corrector circuit (400) comprises a two-terminal network of three serially switched flyback diodes (D1, D2, D3); wherein first and second diodes (D2, D3) are coupled in parallel with a first polarized capacitor (C1) and wherein second and third diodes (D3, D1) are coupled in parallel with a second polarized capacitor (C2).

3. The power factor corrector device according to claim 2, wherein the power factor corrector device is designed as a two pin connectable device (500).

4. A high-frequency switching-mode ballast device (100) for a dimming circuit, the ballast device (100) comprising:

- a bridge rectifier section (200) having an AC input (201; 202) and a DC bridge rectifier output (203; 204);
- a high frequency oscillator circuit (300) including a main ballast coil assembly (350), coupled to the DC bridge rectifier output (203; 204); and further comprising
- a power factor corrector device according to any of the claims 1-3.

5. The ballast device according to claim 4, wherein the two-terminal network of the power factor corrector device (500) is coupled in parallel to the bridge rectifier section.

6. The ballast device according to claim 4, further comprising a resistive network (210) coupled in parallel to the DC bridge rectifier input (201; 202).

7. The ballast device according to claim 4, wherein the dimming circuit is of a phase-cut off type.

8. The ballast device according to claim 7, wherein the dimming circuit includes a triac.

9. The ballast device according to claim 4, further comprising a H-B LED device (60).

10. A dimmable energy saving lamp comprising:
- a H-B LED device;
- a high-frequency switching-mode ballast device 100 according to any of the claims 4-8.

11. A dimmable energy saving lamp comprising:
- a light-transducer low-pressure gas tube 160 including filaments 70 arranged for starting the tube light transducing process;
- a high-frequency switching-mode ballast device 100 according to any of the claims 4-9.

12. The dimmable energy saving lamp according to claim 11, further comprising a low pass filter A2 including an inductor L1 coupled in parallel to the power factor corrector circuit A1 to provide a low pass filter.

13. The dimmable energy saving lamp according to claim 11, further comprising a resistive network A3 coupled in parallel to the DC bridge rectifier input (10-1; 10-2) to interface with a dimming circuit B3.

14. The dimmable energy saving lamp according to claim 11, further comprising a gas tube 160 filament heating circuit A4.

15. The dimmable energy saving lamp according to claim 14, wherein the heating circuit A4 is provided by small-turn coils 140 that are added electrically independent and in parallel with each filament; arranged in transformer configuration built-in within the main ballast coil assembly 150.

16. A dimming circuit comprising:

- a phase-cut off dimmer section to be coupled to AC mains;
- a bridge rectifier section (200) having an AC input (201; 202) coupled to the dimmer section; and a DC bridge rectifier output (203; 204); and
- a power factor corrector device according to any of the claims 1-3.

17. The dimming circuit, further comprising a DC-AC converter section coupled to the power factor corrector device and providing AC output terminals for the dimming circuit.

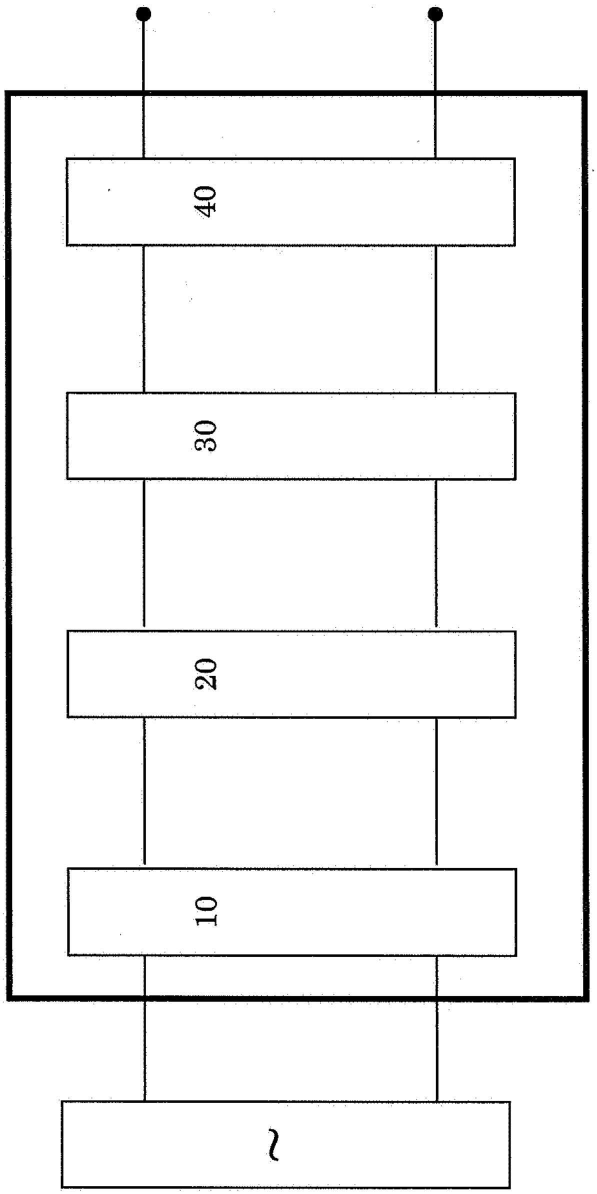
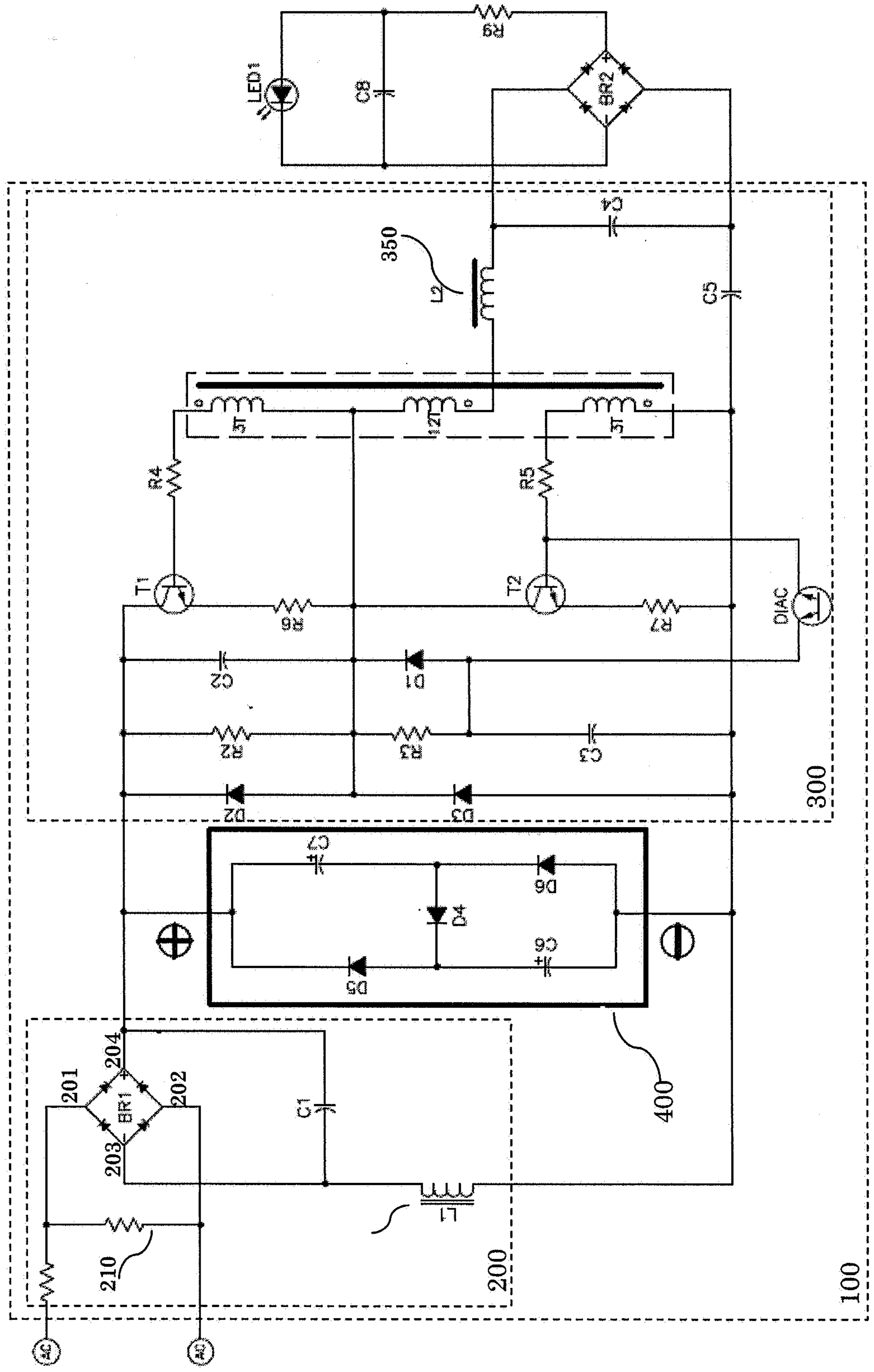


Figure 1

Figure 2


LED1
C8
R9
BR2
C4
350
L2
C5
3T
12T
3T
R4
R5
T1
T2
DIAC
R6
R7
C2
D1
R2
R3
C3
D2
D3
300
C7
D6
D4
C6
D5
400
201
202
203
204
BR1
C1
L1
210
200
100
AC
AC

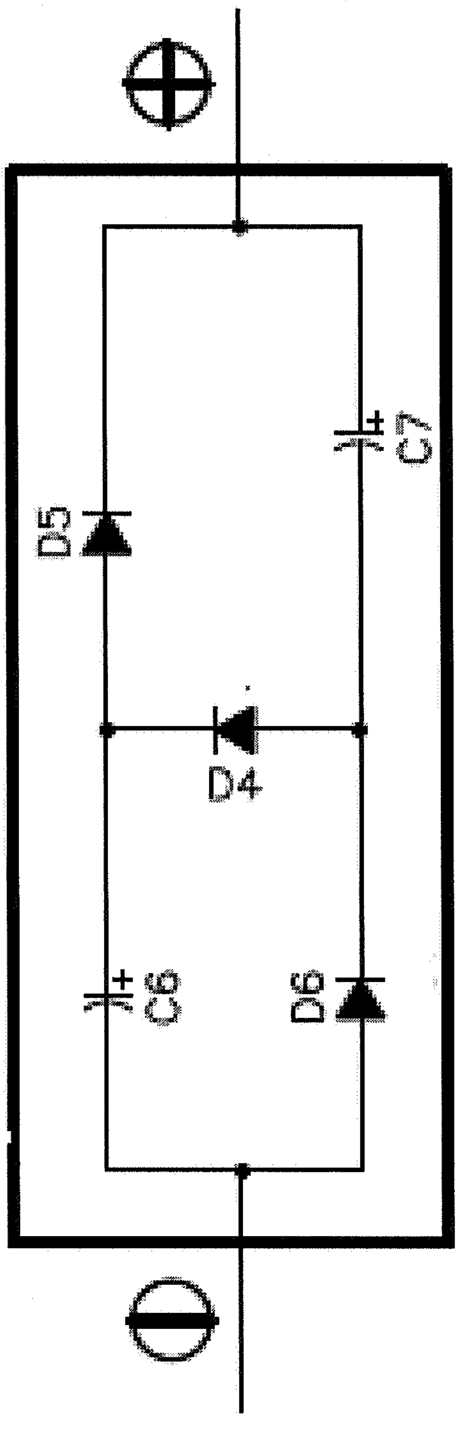


Figure 3

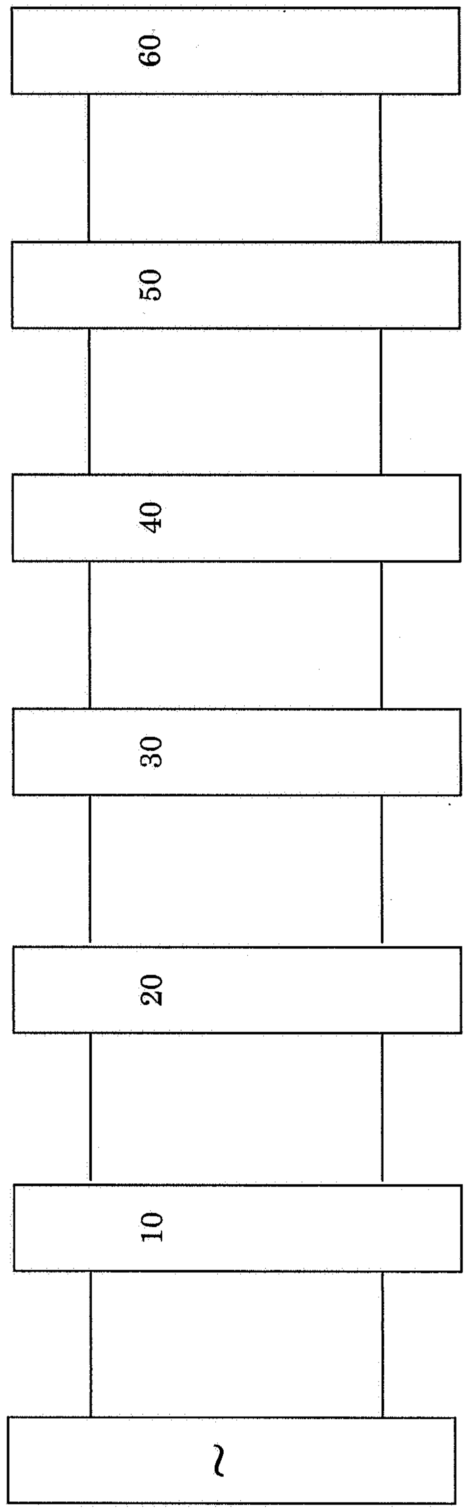


Figure 4

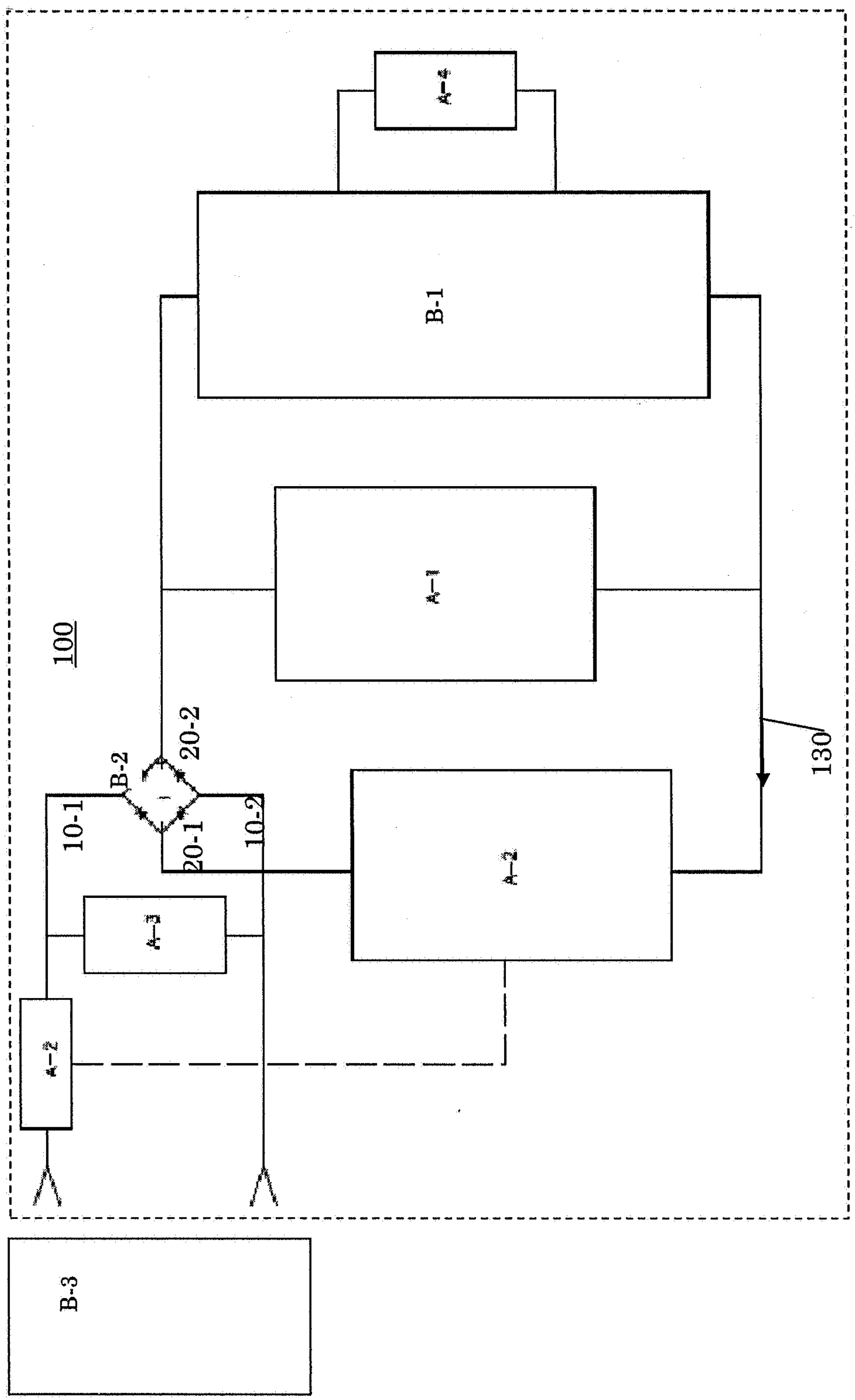


Figure 5

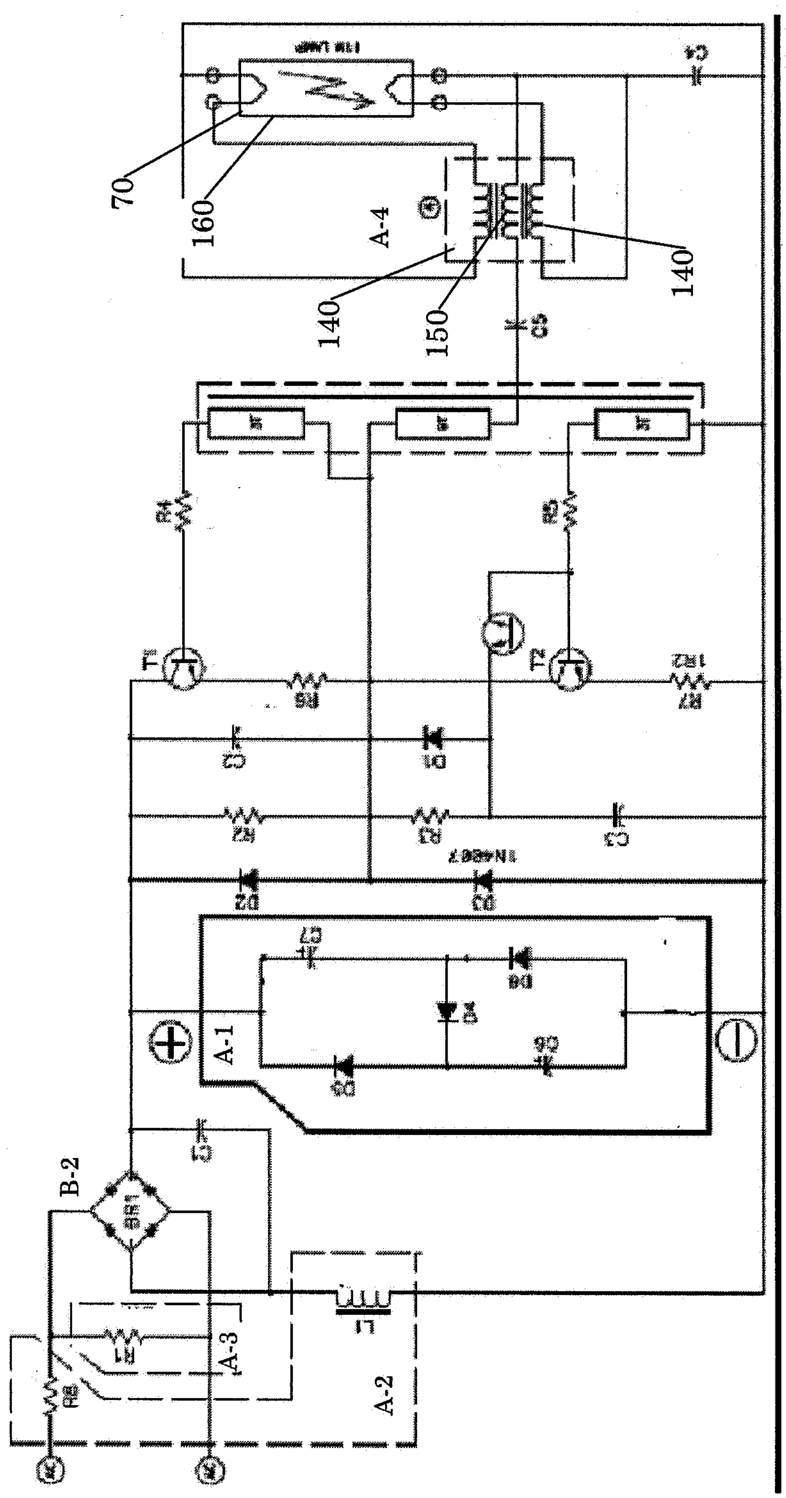


Figure 6

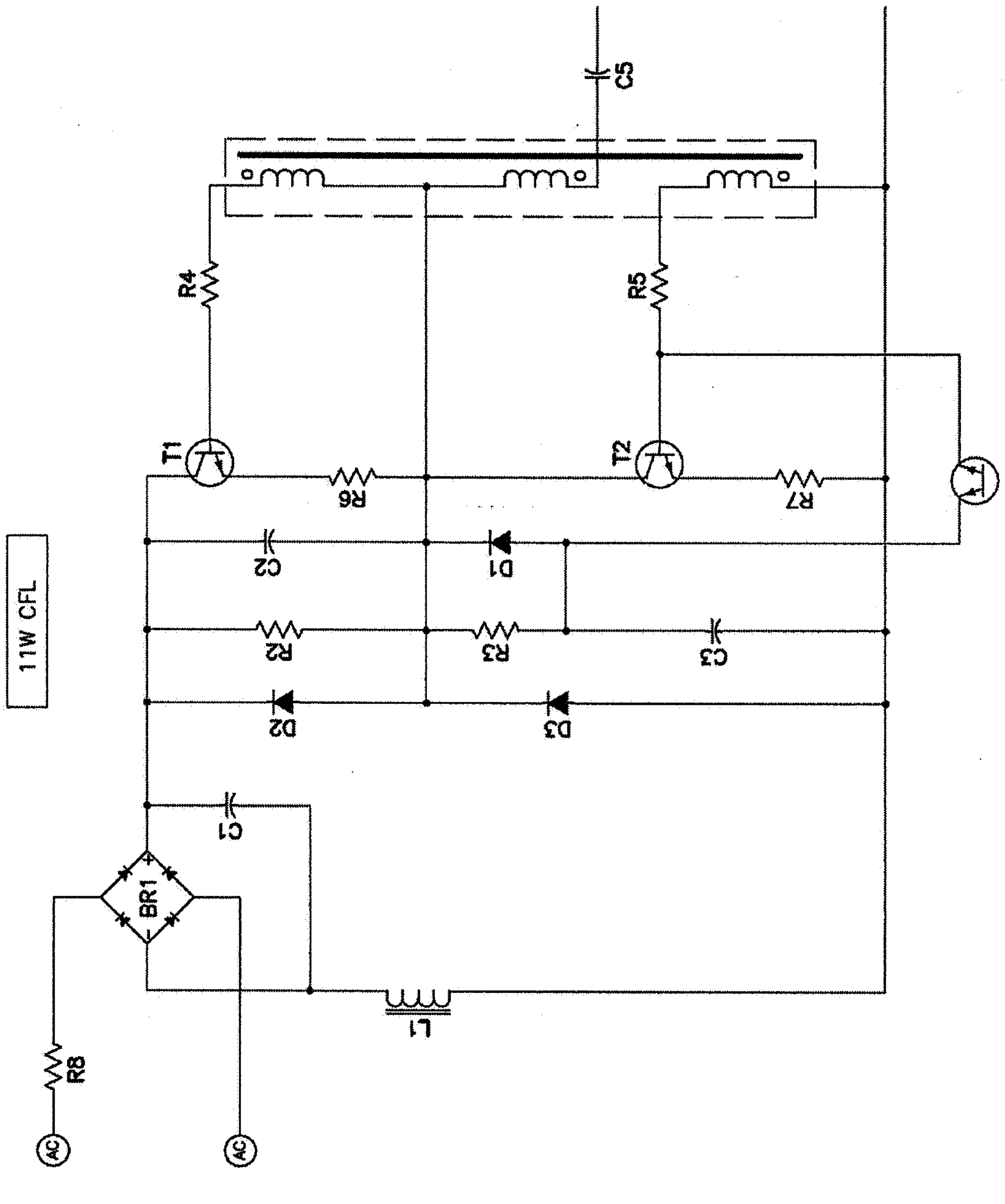


Figure 7

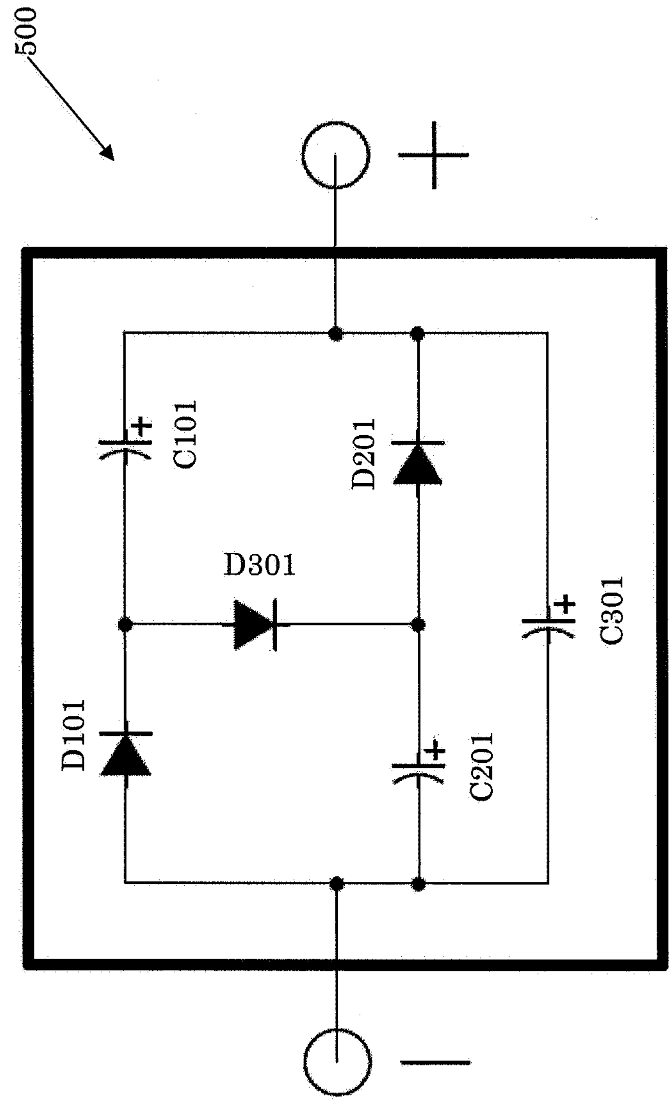


Figure 8

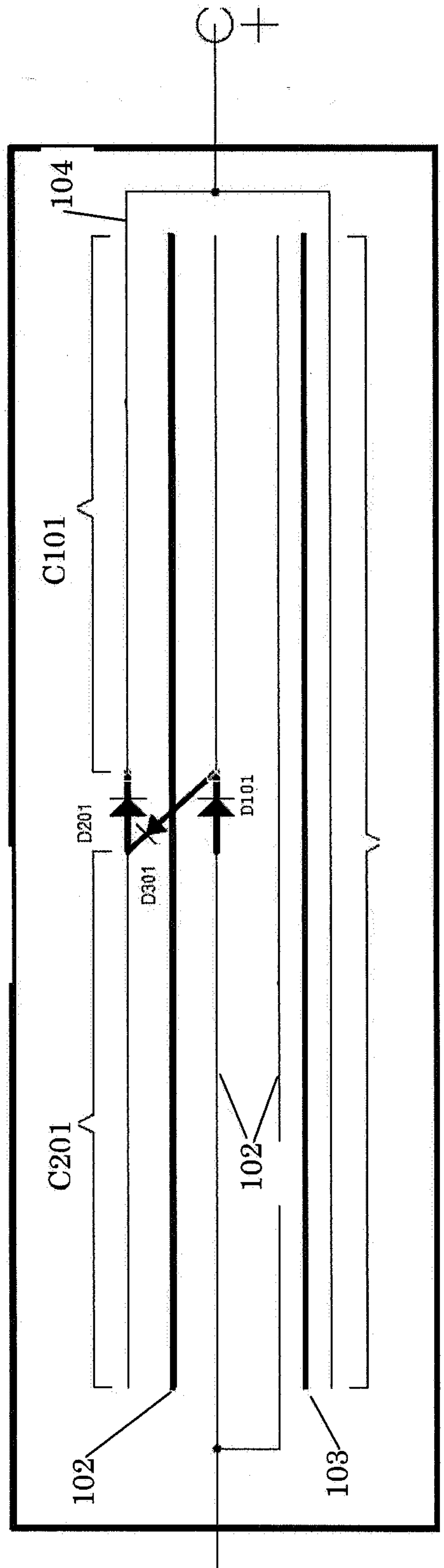


Figure 9

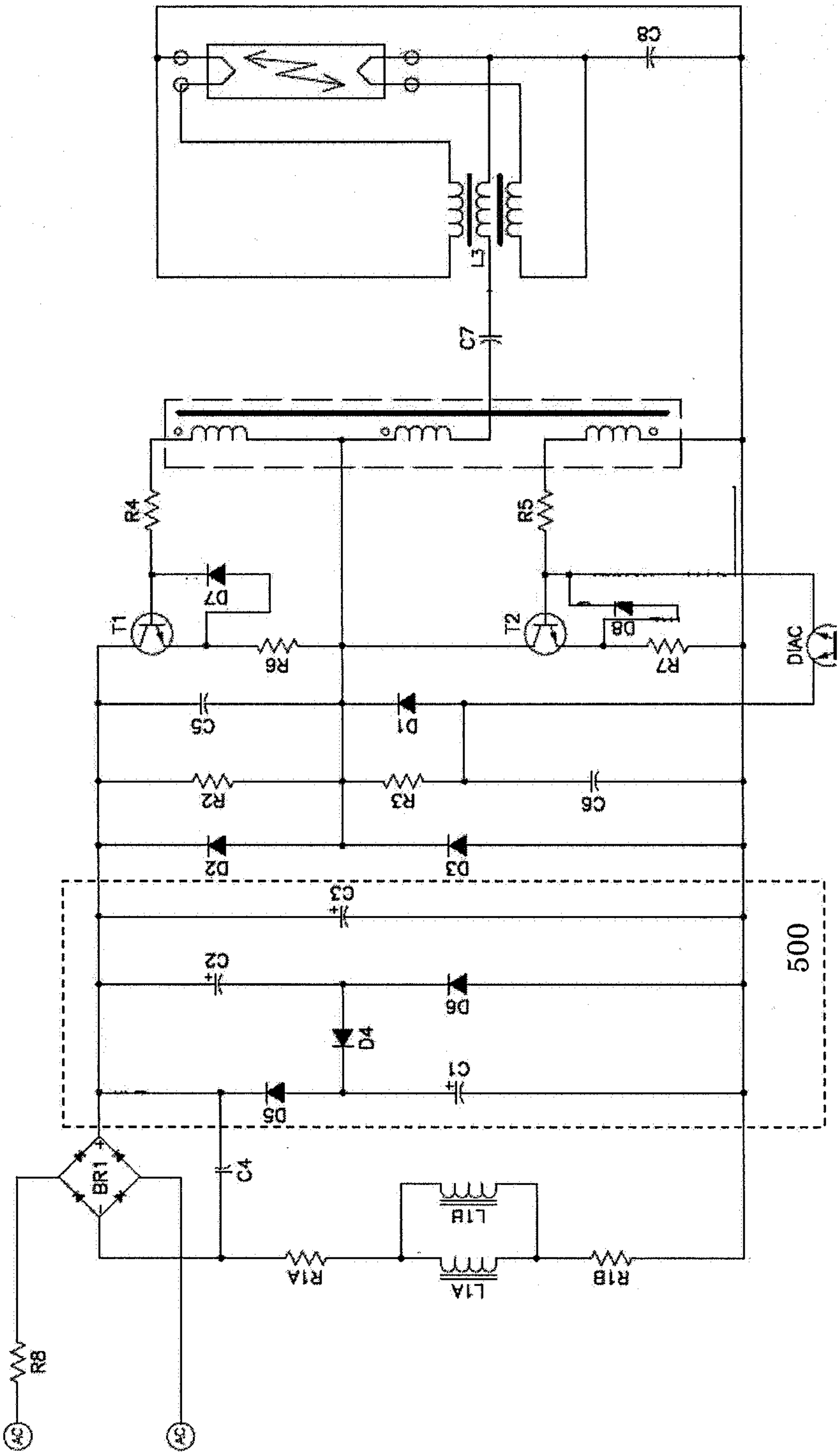

AC
AC
R8
BR1
R1A
L1A
L1B
R1B
C4
D5
C1
D4
D6
C2
C3
500
D2
D3
R2
R3
C6
C5
D1
R6
R7
T1
T2
D7
D8
DIAC
R4
R5
C7
L3
C8

Figure 10

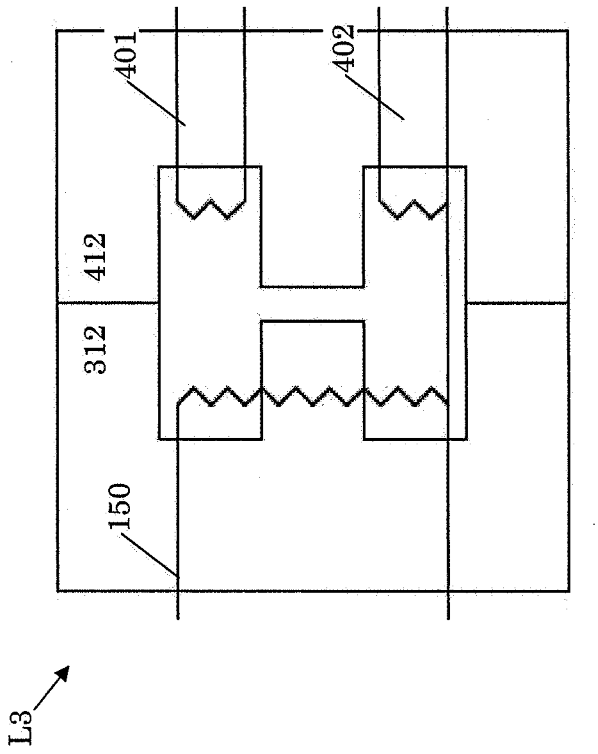


Figure 11

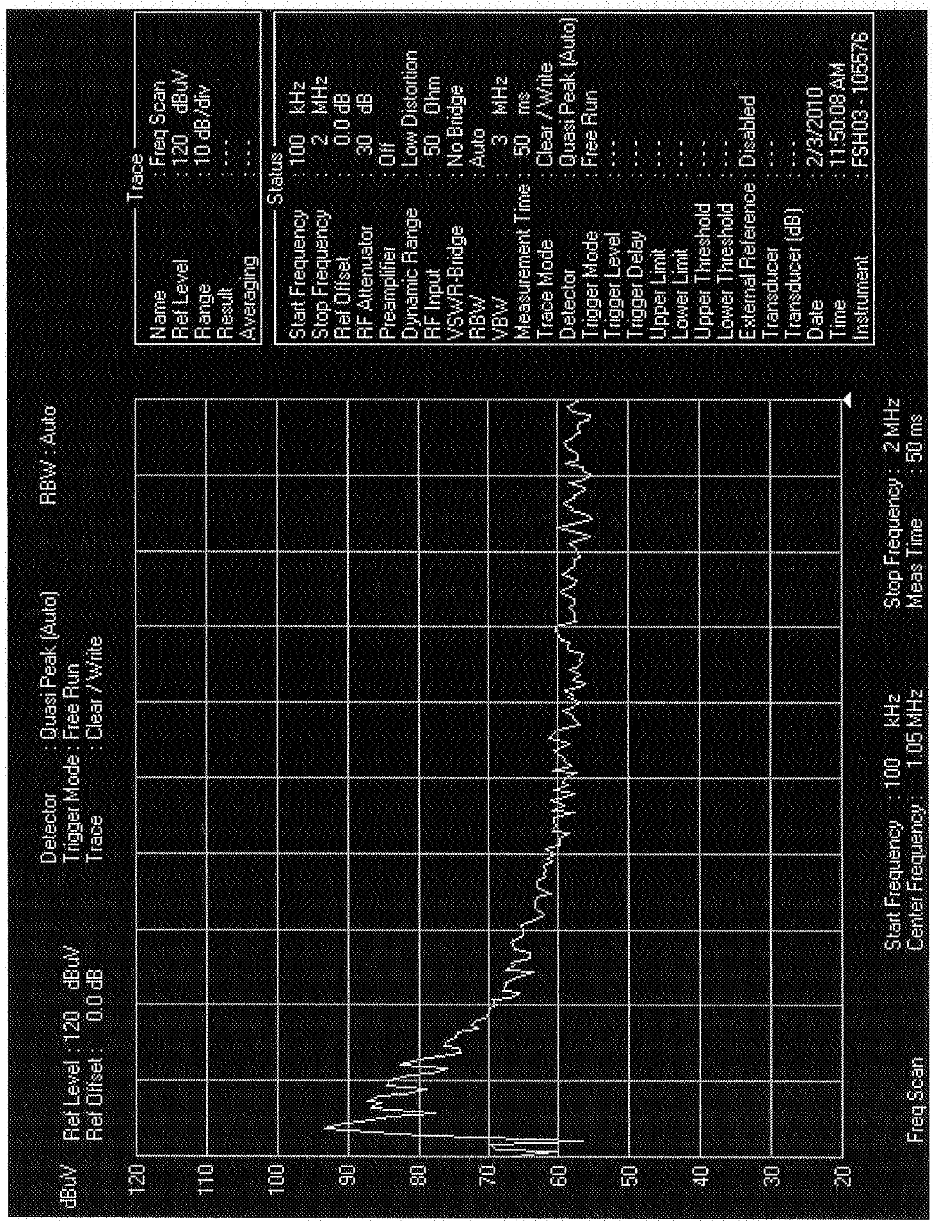

dBuV
Ref Level : 120 dBuV
Ref Offset : 0.0 dB
Detector : Quasi Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : Auto
120
110
100
90
80
70
60
50
40
30
20
Freq Scan
Start Frequency : 100 kHz
Center Frequency : 1.05 MHz
Stop Frequency : 2 MHz
Meas Time : 50 ms
Trace
Name : Freq Scan
Ref Level : 120 dBuV
Range : 10 dB/div
Result : - - -
Averaging : - - -
Status
Start Frequency : 100 kHz
Stop Frequency : 2 MHz
Ref Offset : 0.0 dB
RF Attenuator : 30 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
VSWR-Bridge : No Bridge
RBW : Auto
VBW : 3 MHz
Measurement Time : 50 ms
Trace Mode : Clear / Write
Detector : Quasi Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
Upper Threshold : - - -
Lower Threshold : - - -
External Reference : Disabled
Transducer : - - -
Transducer (dB) : - - -
Date : 2/3/2010
Time : 11:50:08 AM
Instrument : FSH03 - 105576

Figure 12

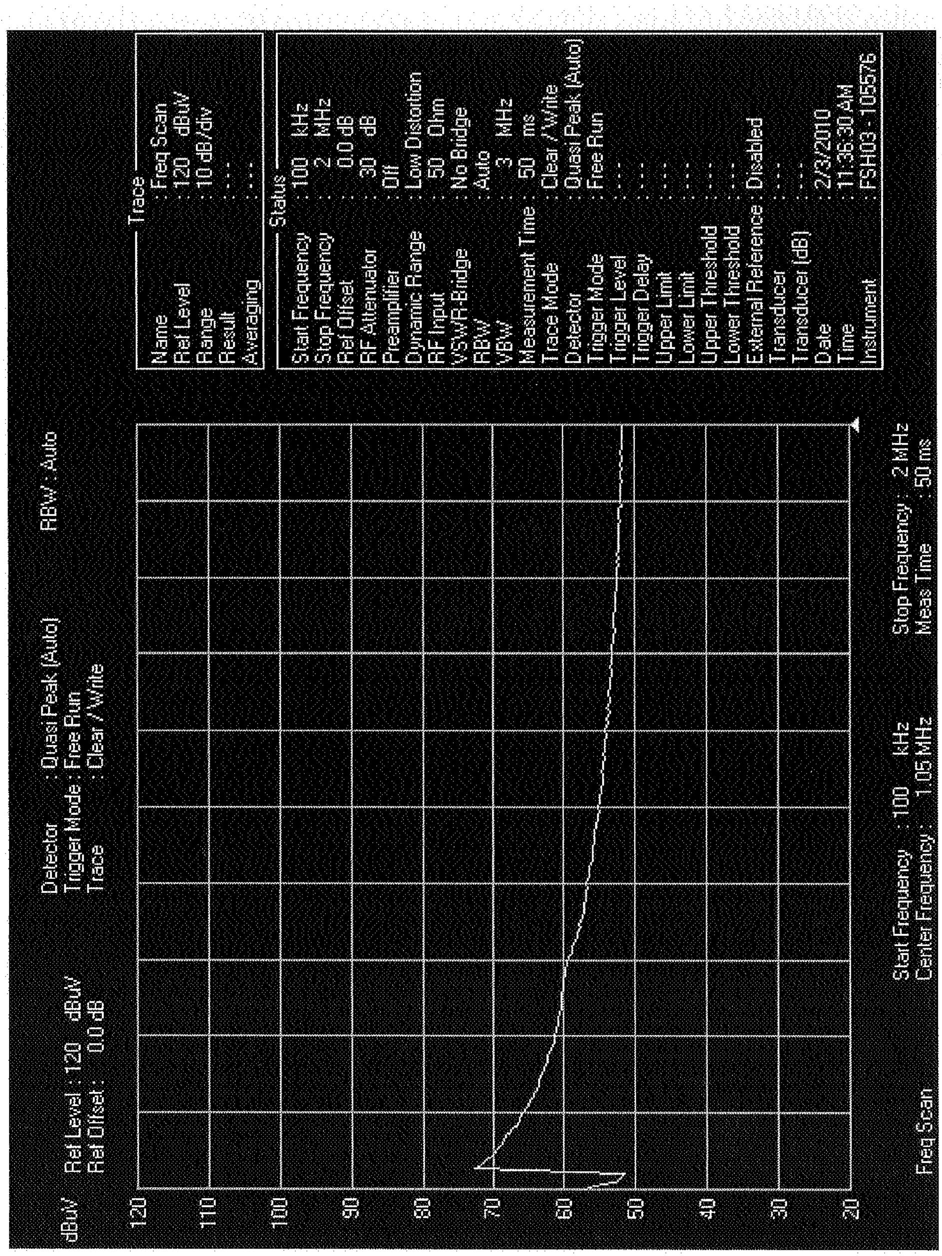

dBuV
Ref Level : 120 dBuV
Ref Offset : 0.0 dB
Detector : Quasi Peak (Auto)
Trigger Mode : Free Run
Trace : Clear / Write
RBW : Auto
120
110
100
90
80
70
60
50
40
30
20
Freq Scan
Start Frequency : 100 kHz
Center Frequency : 1.05 MHz
Stop Frequency : 2 MHz
Meas Time : 50 ms
Trace
Name : Freq Scan
Ref Level : 120 dBuV
Range : 10 dB/div
Result : - - -
Averaging : - - -
Status
Start Frequency : 100 kHz
Stop Frequency : 2 MHz
Ref Offset : 0.0 dB
RF Attenuator : 30 dB
Preamplifier : Off
Dynamic Range : Low Distortion
RF Input : 50 Ohm
VSWR-Bridge : No Bridge
RBW : Auto
VBW : 3 MHz
Measurement Time : 50 ms
Trace Mode : Clear / Write
Detector : Quasi Peak (Auto)
Trigger Mode : Free Run
Trigger Level : - - -
Trigger Delay : - - -
Upper Limit : - - -
Lower Limit : - - -
Upper Threshold : - - -
Lower Threshold : - - -
External Reference : Disabled
Transducer : - - -
Transducer (dB) : - - -
Date : 2/3/2010
Time : 11:36:30 AM
Instrument : FSH03 - 105576

Figure 13

INTERNATIONAL SEARCH REPORT

International application No
PCT/NL2010/050054

A. CLASSIFICATION OF SUBJECT MATTER
INV. H05B41/392 H05B33/08
ADD. H01J61/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H05B H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	POWER INTEGRATIONS: "Low Cost Dimmable LED Ballast Using the Valley Fill Current Shaping Circuit" DI-171 DESIGN IDEA LINKSWITCH-TN, September 2009 (2009-09), XP002580882 San Jose, CA, USA	1,2
Y,P	the whole document -----	3-17
Y	US 2005/184679 A1 (ATRA CHANDRASHEKARA [IN] ET AL) 25 August 2005 (2005-08-25) paragraphs [0003], [0007], [0014], [0023]; figure 3 -----	3-17
Y	WO 2009/061173 A1 (INNO IND ENGINEERING LTD; STEUR FRANCISCUS ADRIANUS [NL]) 14 May 2009 (2009-05-14) page 5, line 20 - page 8, line 12; figures 1-3 -----	6,13
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 May 2010	27/05/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Albertsson, Gustav

Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	DE 195 36 634 A1 (SEMPERLUX GMBH [DE]) 27 March 1997 (1997-03-27) column 1, line 41 - line 51; figures 2-3	12
Y	EP 1 605 734 A1 (LUTRON ELECTRONICS CO [US]) 14 December 2005 (2005-12-14) paragraphs [0022], [0039] - [0045], [0055], [0057]; figures 1,2,12-14,17,18	15
A	JP 2001 319797 A (TOSHIBA LIGHTING & TECHNOLOGY) 16 November 2001 (2001-11-16) abstract; figures 1-4	12
A	DE 102 42 326 A1 (TRIDONICATCO GMBH & CO KG DORN [AT]) 18 March 2004 (2004-03-18) abstract; figures 1c,2	1-3

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/NL2010/050054

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WO 2009061173	A1	14-05-2009	NONE			
DE 19536634	A1	27-03-1997	NONE			
EP 1605734	A1	14-12-2005	AT	448670	T	15-11-2009
			ES	2336082	T3	08-04-2010
			JP	4031429	B2	09-01-2008
			JP	2004533200	T	28-10-2004
			WO	03001855	A1	03-01-2003
JP 2001319797	A	16-11-2001	NONE			
DE 10242326	A1	18-03-2004	NONE			