



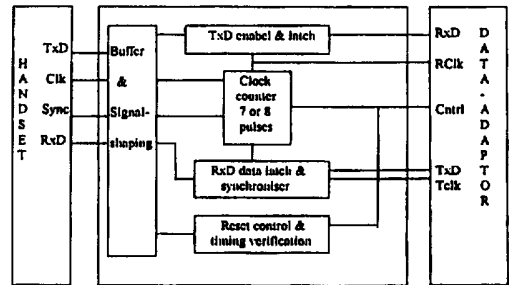
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<p>(51) International Patent Classification <sup>6</sup> : <b>H04Q 7/32</b></p>	<p><b>A1</b></p>	<p>(11) International Publication Number: <b>WO 97/39596</b> (43) International Publication Date: 23 October 1997 (23.10.97)</p>
<p>(21) International Application Number: PCT/BE97/00046 (22) International Filing Date: 15 April 1997 (15.04.97) (30) Priority Data: 9600323 15 April 1996 (15.04.96) BE (71) Applicant (for all designated States except US): OPTION INTERNATIONAL [BE/BE]; Vaart 25, Bus 8, B-3000 Leuven (BE). (72) Inventors; and (75) Inventors/Applicants (for US only): VAN DAELE, Johan [BE/BE]; Vaart 25, Bus 8, B-3000 Leuven (BE). GOMMERS, Serge [BE/BE]; Vaart 25, Bus 8, B-3000 Leuven (BE). COBER, Ben [BE/BE]; Vaart 25, Bus 8, B-3000 Leuven (BE). (74) Agents: VOSSWINKEL, P. et al.; Gevers Patents, Holidaystraat 5, B-1831 Diegem (BE).</p>	<p>(81) Designated States: AU, NO, SG, US, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p><b>Published</b> <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments. In English translation (filed in Dutch).</i></p>	

(54) Title: ADAPTER FOR DATA TRANSMISSION BETWEEN A MOBILE TELEPHONE AND A DATA TERMINAL

(57) Abstract

The present invention relates to an adapter for data transmission between a mobile telephone and a data terminal, which adapter comprises a card and a cable, which card is provided to be connected to the data terminal, which cable is provided to be connected, on the one hand, to the mobile telephone and, on the other hand, to the card and wherein the telephone is provided with a generator for generating clock and synchronisation signals. According to the invention, the adapter comprises an interface which is provided, on the one hand, for receiving data characters from the card independently from said clock signals and for differentiating synch characters and data characters from each other and for transmitting each of the data characters in an assigned time slot to the telephone, and which interface is provided, on the other hand, for providing a predetermined number of clock signals to the card, under control of a synchronisation signal.



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**“Adapter for data transmission between a mobile telephone and a data terminal.”**

5 The present invention relates to an adapter for data transmission between a mobile telephone and a data terminal, which adapter comprises a card and a cable, which card is provided to be connected to the data terminal, which cable is provided to be connected, on the one hand, to the mobile telephone and, on the other hand, to the card and wherein the telephone is provided with a generator for generating clock and synchronisation signals.

10 Such an adapter is known from EP-A-0 655 873 and is provided to be used in modern digital cellular systems, such as for example the known GSM system (“Global System for Mobile communication”). In such a system, different services are offered to the user, which are subdivided in three categories : telecommunication, transmission and additional services.

15 Telecommunication services are services which enable users to perform data transmission such as telephone calls, emergency calls, automatic fax messages and services for short messages.

20 The bearer services are provided on the card and enable to use the telecommunication services. These are subdivided according to protocols which are used for data transmission. An example therefor is the circuit switched data transfer.

25 The known adapter according to EP-A-0 655 873 is provided with a buffer for storing data, originating from the mobile telephone, respectively the data terminal. Means are further provided for

- 2 -

feeding the buffer from the adapter so that the mobile telephone battery is saved as much as possible.

A drawback of the adapter according to EP-A-0 655 873 is that the adapter must be provided with the required hardware interfaces and have sufficient processing capacity available for enabling data  
5 transmission. For this required processing capacity, a number controllers are available on the market, such as i.a. MC68302 from Motorola ®. These controllers are relatively powerful and therefore also relatively expensive to buy. With less powerful controllers, which i.a. have less  
10 processing capacity available, data transmission is hitherto very difficult to realise.

An object of the invention is to realise an adapter, which enables to perform data transmission with less powerful processing capacity without reducing the transmission quality.

15 According to the invention, the adapter is characterised in that the adapter comprises an interface which is provided, on the one hand, for receiving data characters from the card independently from said clock signals and for differentiating synch characters and data characters from each other and for transmitting each of the data  
20 characters in an assigned time slot to the telephone, and which interface is provided, on the other hand, for providing a predetermined number of clock signals to the card, under control of a synchronisation signal.

The invention will now be described in detail referring to the annexed figures, wherein :

25 Figure 1 illustrates the configuration of hardware and software in a telephone and an adapter;

Figure 2 illustrates the state of the art;

Figure 3 illustrates a block diagram of the interface according to the invention with the telephone and the card;

- 3 -

Figure 4 shows a time diagram for communication between telephone and card;

Figures 5 and 6 show time diagrams for communication between card and telephone;

5           Figures 7 and 8 show time diagrams for synchronisation and bus enabling;

Figure 9 is a flowchart for starting up;

Figure 10 is a detailed view of the interface signals;

Figure 11 is a detailed view of the interface circuit.

10           In the adapter according to the invention, use is made of a serial bus, connecting two processors with each other. This bus is a fast synchronous link with bit rates up to 500.000 bits per second.

In order to achieve this, there has to be assumed that both processors are equipped with the required hardware interfaces and processing capacity. This is not always evident.

15           In order to solve this problem, use is not only made of an active bus, but also of a converter : the buffer from Figure 2 is replaced by an intelligent interface. This can be an ordinary processor or a programmable logic, from the type PAL ("Programmable Array Logic"), GAL or EPLD ("Erasable and Programmable Logic Device").

20           The interface provides not only the electrical separation of the two processors, but will also take care that the second processor (the processor in the card or adapter) can run off synchronisation and will only receive relevant data, without synch characters. Electrical separation means that current does not run directly from the telephone to the card and vice versa. The card is provided with an asynchronous UART delivering asynchronous pulses to the bus. In the interface, means are provided for translating these asynchronous pulses in synchronous, in order to provide synchronous pulses to the telephone and vice versa.

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- 4 -

**Operation of the interface :**

The operation of this adapter is independent from the data and can therefore be used both for data and for control messages. The bits run contiguously from the telephone to the adapter. The processor  
5 from the adapter checks by counting the number of bits if the bits are data bits or synch bits.

Since not all the processors are provided with a synchronous serial port, the signals from Figure 1 are processed in the following way :

10                   Receive data (RxD), i.e. from the telephone to the card (Figure 4) : from the entire train of clock pulses (HClk), only the 8 flanks (PRClk), wherein data characters (HDATA-Tx) are effectively present on the RxD line, are selected. In this way, the PRCLK can be used as interrupt for bits to be received (HDATA-Tx). The UART in the card is  
15 only active under control of PRClk.

                  Transmit data (TxD), i.e. from the card to the telephone (Figure 5) : the data (PDATA-Tx) is first buffered in a latch from the interface and is only transmitted to the telephone (HDATA-Rx) in the assigned time slot if HClk and Hsync are active. In this way, it is not  
20 necessary having the processor executing this time critical task. The data characters are thus sent independently from Hclk. Care has only to be taken that the data characters are sent between two successive Hsync pulses.

                  Clock (Clk) : signal is converted to a digital compatible  
25 level, for example TTL.

                  Sync : signal is not transmitted in a time critical manner any more.

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- 5 -

**Description of the block diagram (Figure 3) :**

- buffer and signal shape part :

all signals from and to the telephone are buffered, (see above) in order to make them free from disturbances and also for  
5 adapting the levels (CMOS, TTL, 3.3 V, ...) to the levels from the used processor in the data adapter card. The clock signal HClk is moreover amplified (sinus to block) in order to obtain precise flanks. For this purpose, part A from the circuit shown in Figure 11 is used. In this way, the operation of the interface is rendered less noise and high frequency  
10 sensible. For this purpose, a resistance R4 is i.a. used between the output I/08 and the input CLK 1/12 (Figure 10). The resistance suppresses under- and overshoot with high speed signals.

- clock counter 7 or 8 pulses (Figure 7) :

15 the clock is controlled in a continuous stream of pulses. Since an ordinary UART, i.e. an UART which is not bit synchronously, can work byte asynchronously, such as in the Rockwell ® L1300 series, cannot work with a synchronisation signal, only the usable clock pulses (i.e. the clock pulses for which data is available on the RxD line) are  
20 transmitted. In the case of 8 bits per character, there are 8 clock pulses. If use is made of a Rockwell ® processor type L1300, and this is particular for the invention, then, for the first character to be received after a hardware reset, only 7 clock pulses may be transmitted. For this purpose, use is made of a 7 or 8 counter. The set up is performed with  
25 one of the control lines (Cntrl). Figure 7 mentions also the first series of PRCLK 7 pulses and the second 8 pulses. This is realised by sending on PIDLE a toggle signal and by switching PCLR from high to low. The toggle is taken over by PRCLK and the transition of PCLR makes PRCLK high. The successive HSYNC enables the first series on PRCLK to pass.

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- 6 -

- TxD enable latch :

Data comes from the telephone to the data adapter. This information is buffered, brought to a digital level, and sent via a switch (part B in Figure 11) to the adapter. This switch switches only the data upon duration of the character, then the RxD line is kept high or low, depending on the way of programming. The pulses PRCLK enable that the buffered data HDATA-Tx is transferred to the card (PDATA-Rx). Possibly present interference signals on HDATA-Tx, which are received by the telephone, will also not be transmitted (PDATA-RX) to the card.

10

- RxD data latch and synchroniser :

Data comes from the data adapter to the telephone (Figure 5). Since the processor in the data adapter has not always the required processing capacity or the specific hardware available, the data stream to the telephone in this unit, and this is specific for this invention, is stored in the interface and only transmitted upon request of the telephone, thus within the assigned time slot, i.e. with the exact clock pulses and directly after the sync signal (HSync). The processor can then store between two sync pulses, with a lower tempo, the subsequent character in the interface. The processor must however take care of that between two pulses, data characters are effectively transmitted.

15

- reset control & timing verification (Figure 7) :

This unit takes care of that timing occurs synchronously with the telephone, after turning on the first clock train consists of 7 pulses, the wake-up procedure from the telephone is initiated and difference is made between sync characters and data characters.

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The wake-up from the handset occurs by clamping the TxD line to a high level (PCLR). Since the UART in the Rockwell ® processor

- 7 -

cannot send data without the presence of any clock pulses, this must be solved here by adding an additional control line.

Wake-up procedure (Fig. 7 and 8) :

- 5 PCLR : reset : reset signal for interface  
 HSYNC : sync signal : signal from the telephone  
 HCLK : clock signal : buffered and amplified clock signal from the telephone which becomes active only after PSTART and the subsequent HSYNC pulses become low.
- 10 HDATA-TX : transmit line from the telephone  
 PRCLK : clock, 7 or 8 pulses, to the data interface  
 PSYNC : sync signal : buffered from the telephone to the data interface  
 PDATA-RX : transmit line to the data interface

- 15 This diagram shows clearly how the clock pulses are transmitted in a filtered manner to the data adapter. The received data on PDATA-RX is the buffered data, only released during PCLK, to the data adapter.

- 20 Figure 5 : sync characters from the card to the telephone :
- PIDLE : I/O line data adapter indicates that sync characters must be sent to the telephone  
 PTCLK : clock, inverse value from HCLK, used for time controlling data transmission to buffer
- 25 PDATA-TX : data from data adapter to buffer  
 HDATA-RX : data from buffer to telephone, according to timing requested by the telephone bus.

- 30 If the IDLE line is kept low, then the data (HDATA-RX) is also low during the SYNC pulses. This is a possibility for the data adapter for generating a sync character.

- 8 -

Figure 6 : data characters from the card to the telephone :

PIDLE : I/O line data adapter indicates that sync characters must be sent to the telephone

5 PTCLK : clock, inverse value from HCLK, used for time controlling data transmission to buffer

PDATA-TX : data from data adapter to buffer

HDATA-RX : data from buffer to telephone, according to timing requested by the telephone bus.

10 If the IDLE line is kept high, then the data (HDATA-RX) is also high during the SYNC pulses. The characters now transmitted are considered as real data characters.

After starting up the data adapter, PCLR is active high (Figure 7). The data adapter switches the PIDLE line high and low, and in this way also PRCLK until the data adapter is in synchronisation with the bus.

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PCLR is then switched low, and after a SYNC pulse, the continuous operation of the buffer starts : 7 or 8 clock pulses are transmitted to the data adapter.

20

Figure 8 : wake-up handset :

PSTART : I/O line from the data adapter, in this way HDATA-RX becomes high, without requiring clock pulses for this purpose.

Since use is made of a synchronous EPLD (buffer) no output can be modified from level without clock pulses; PIDLE, PCLR and PSTART can obviate this. If the handset is connected, it will send clock and sync pulses.

25

In Figure 9, this wake-up procedure is clarified by means of a flowchart. First of all, PIDLE and PCLR are low (20) since the telephone is not active. On PSTART, a pulse is now generated (21) by

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- 9 -

means of which a timer is started. A HSYNC must now be supplied by the telephone which starts HCLK which is monitored (22,23). If a clock pulse is not received within the set-up time (24), then it is established (26) that the telephone is not turned on. If a clock pulse is received  
5 (23 Y), then it is established (25) that the telephone is turned on and the transmission is enabled.

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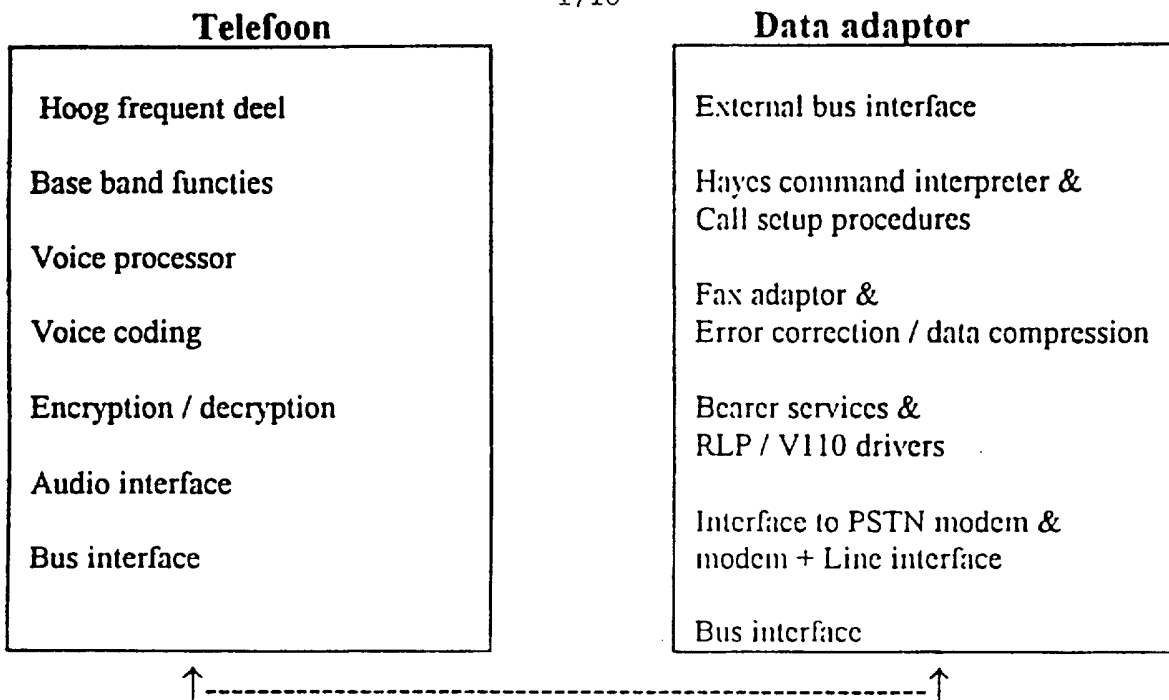
CLAIMS

1. An adapter for data transmission between a mobile telephone and a data terminal, which adapter comprises a card and a cable, which card is provided to be connected to the data terminal, which  
5 cable is provided to be connected, on the one hand, to the mobile telephone and, on the other hand, to the card and wherein the telephone is provided with a generator for generating clock and synchronisation signals, characterised in that the adapter comprises an interface which is provided, on the one hand, for receiving data characters from the card  
10 independently from said clock signals and for differentiating synch characters and data characters from each other and for transmitting each of the data characters in an assigned time slot to the telephone, and which interface is provided, on the other hand, for providing a predetermined number of clock signals to the card, under control of a  
15 synchronisation signal.

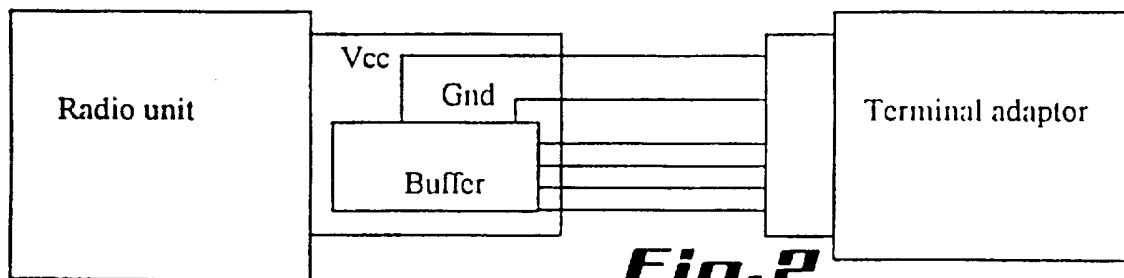
2. The adapter according to claim 1, characterised in that it comprises a serial bus.

3. The adapter according to claim 1 or 2, characterised in that said interface is provided for electrically separating said card from  
20 said telephone.

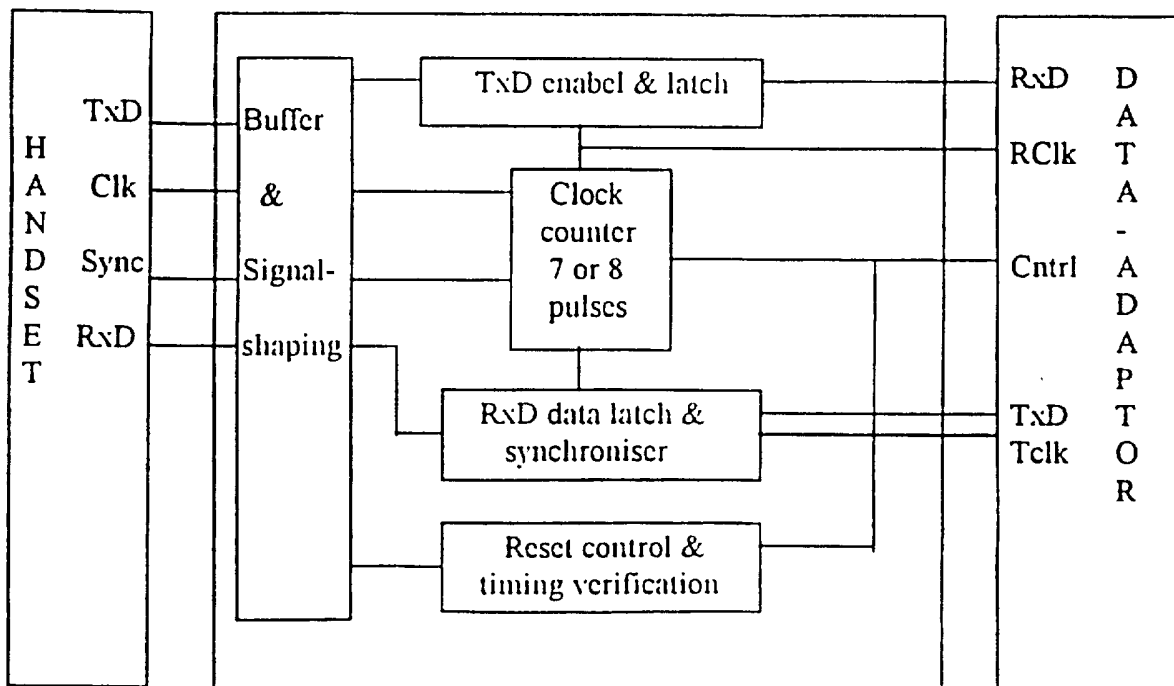
4. The adapter according to any one of the preceding claims, characterised in that said interface is provided for amplifying said clock signals.



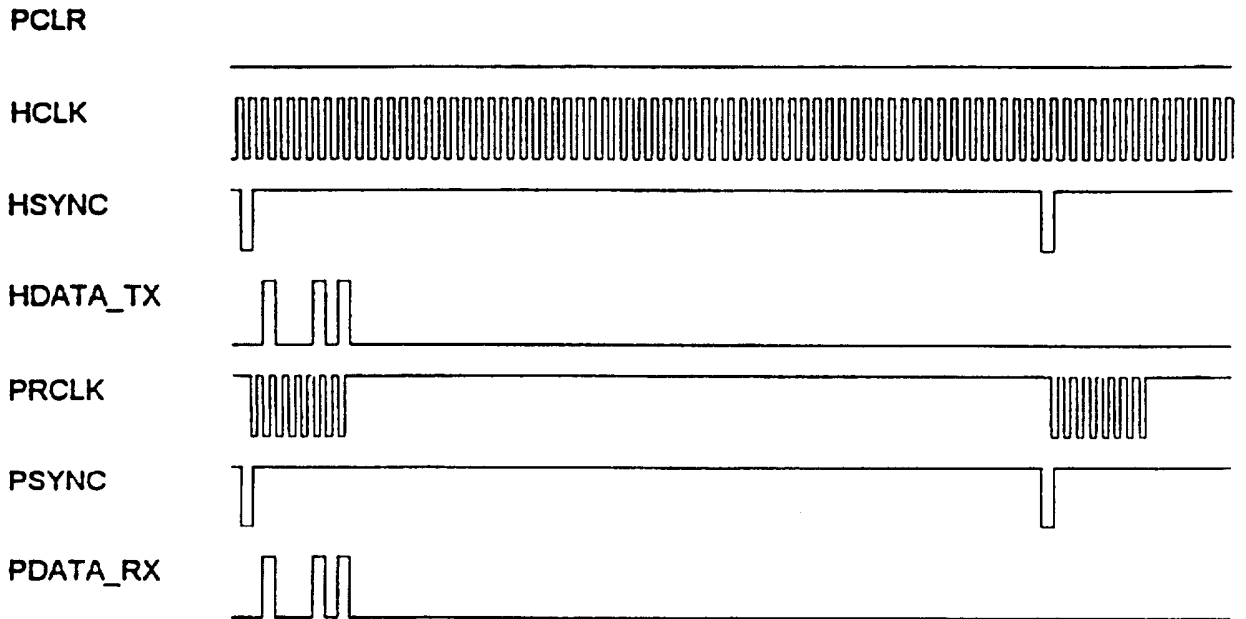
**Fig.1**



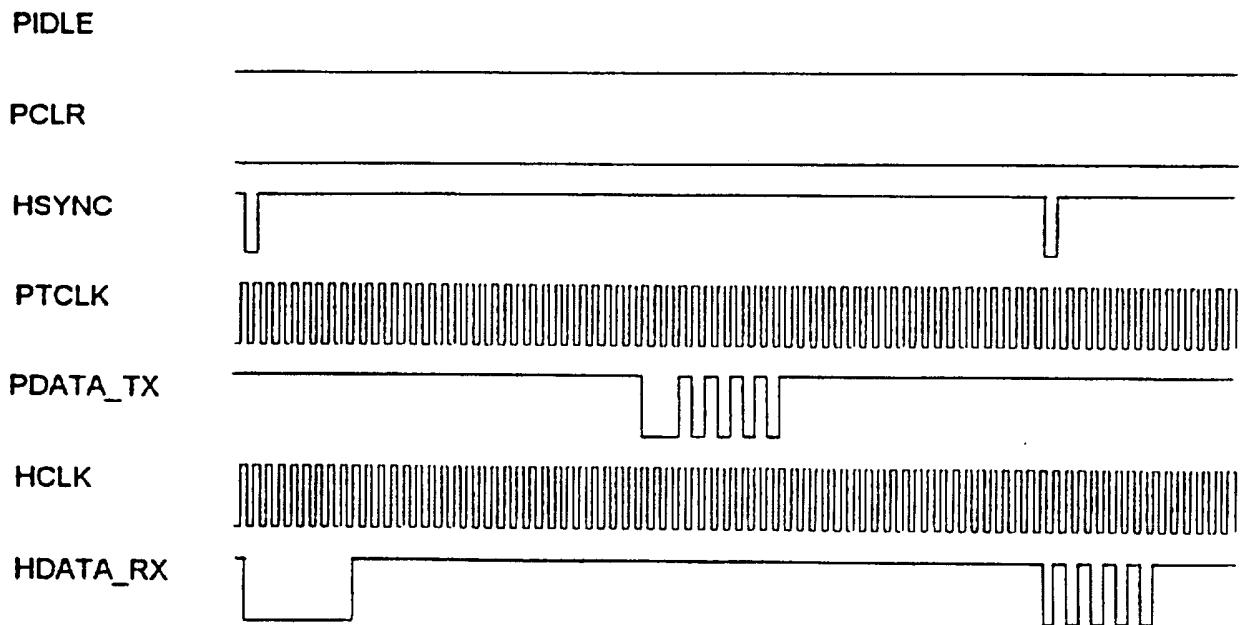
**Fig.2**



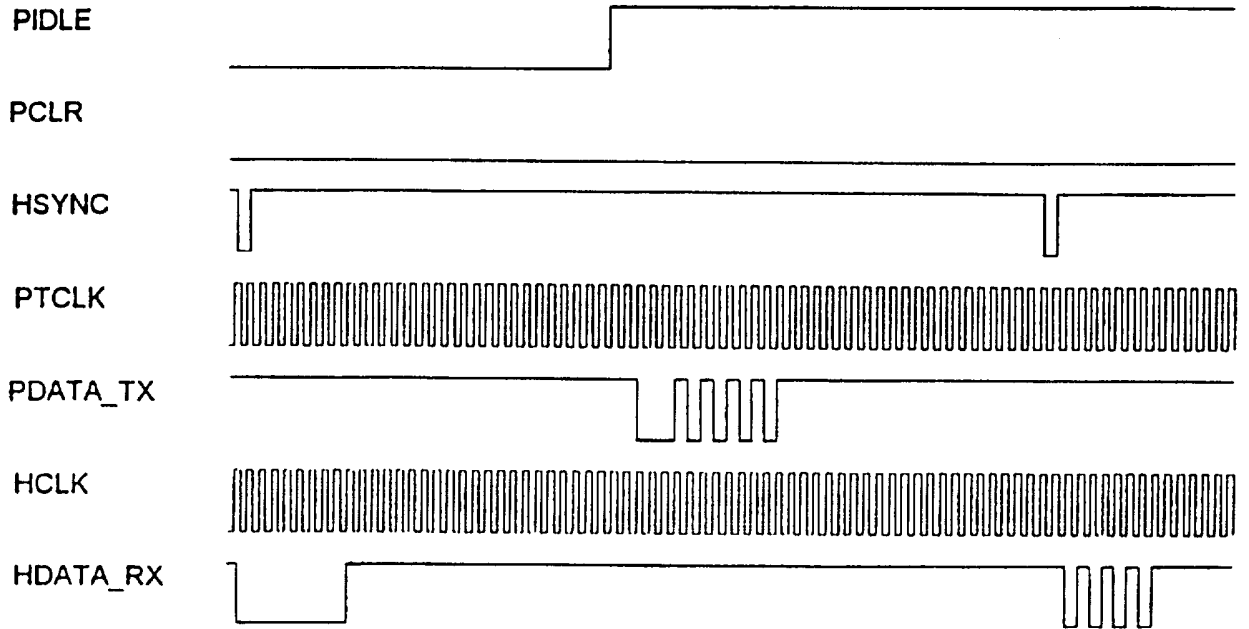
**Fig.3**



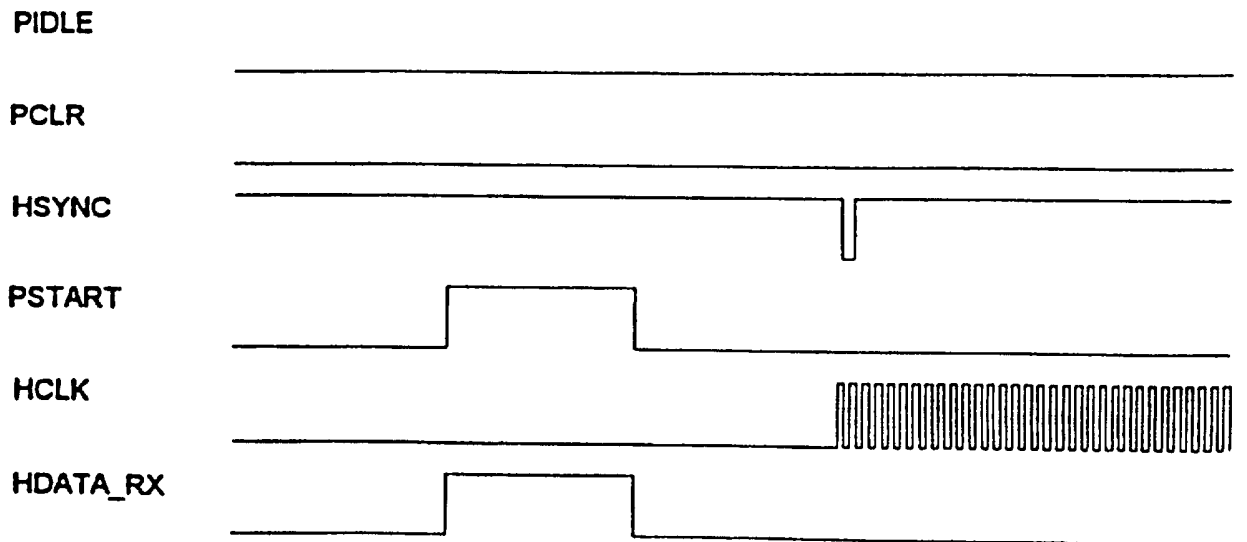
**Fig. 4**



**Fig. 5**



**Fig. 6**

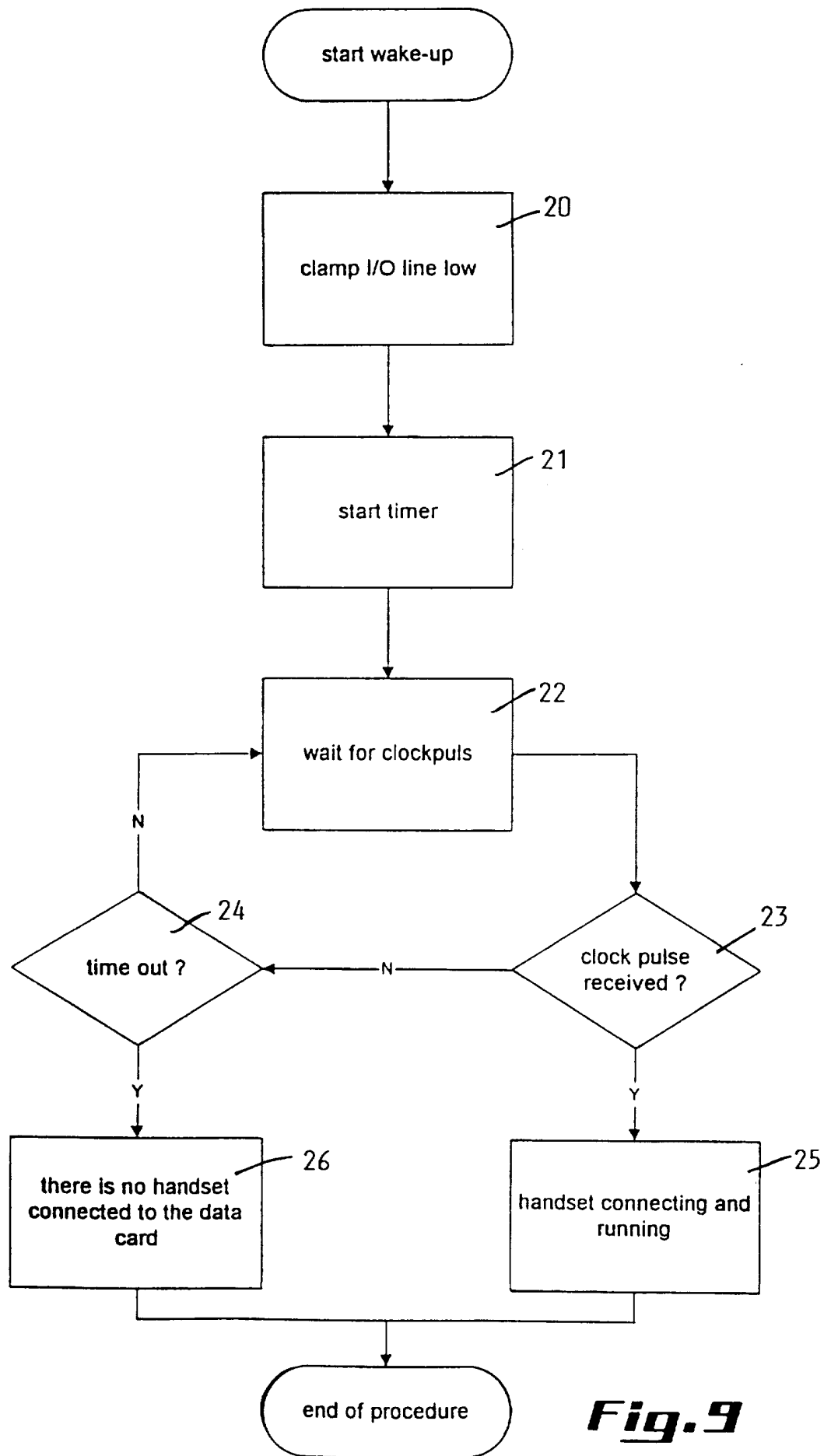


**Fig. 8**



**Fig. 7**

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**Fig. 9**



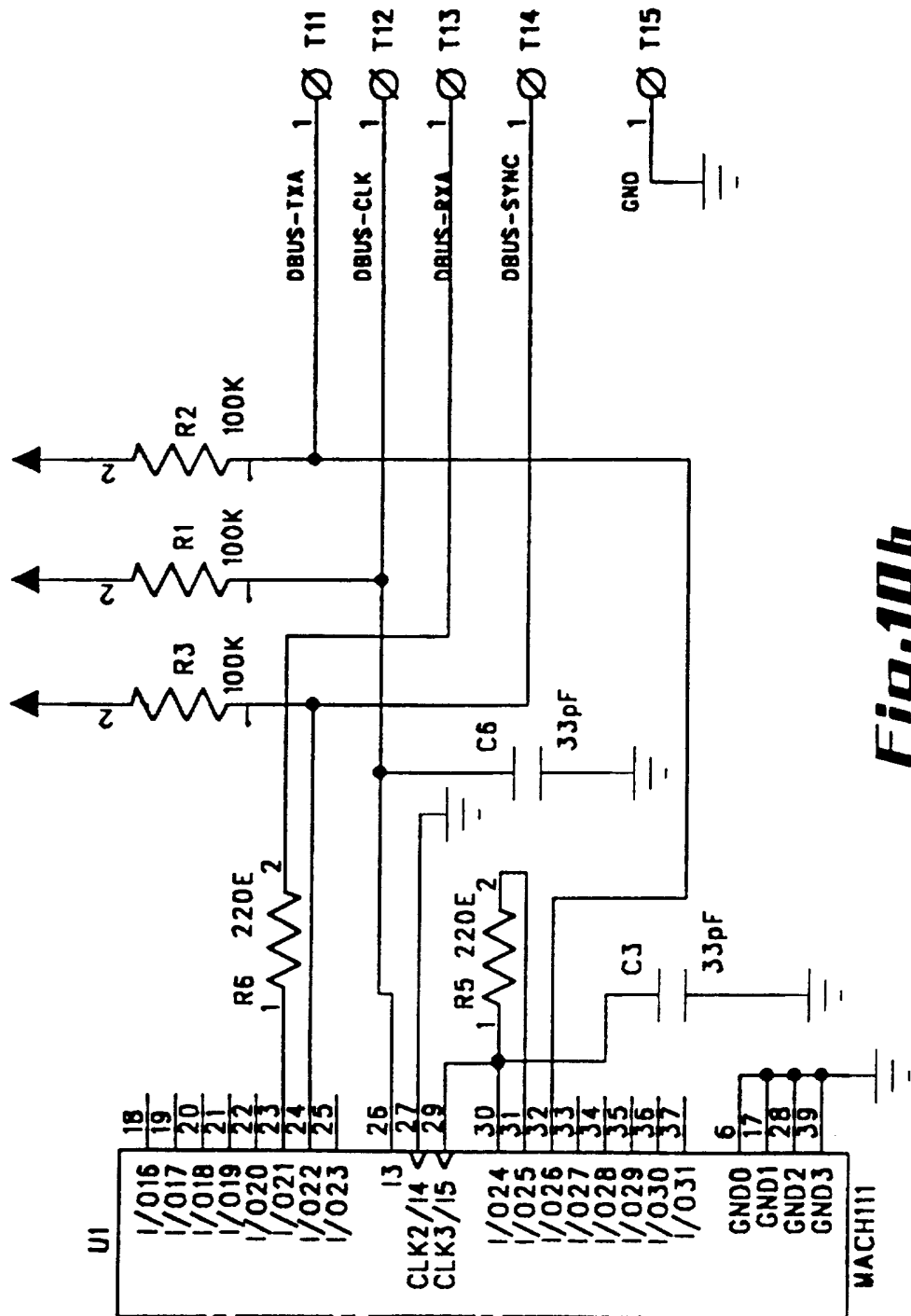
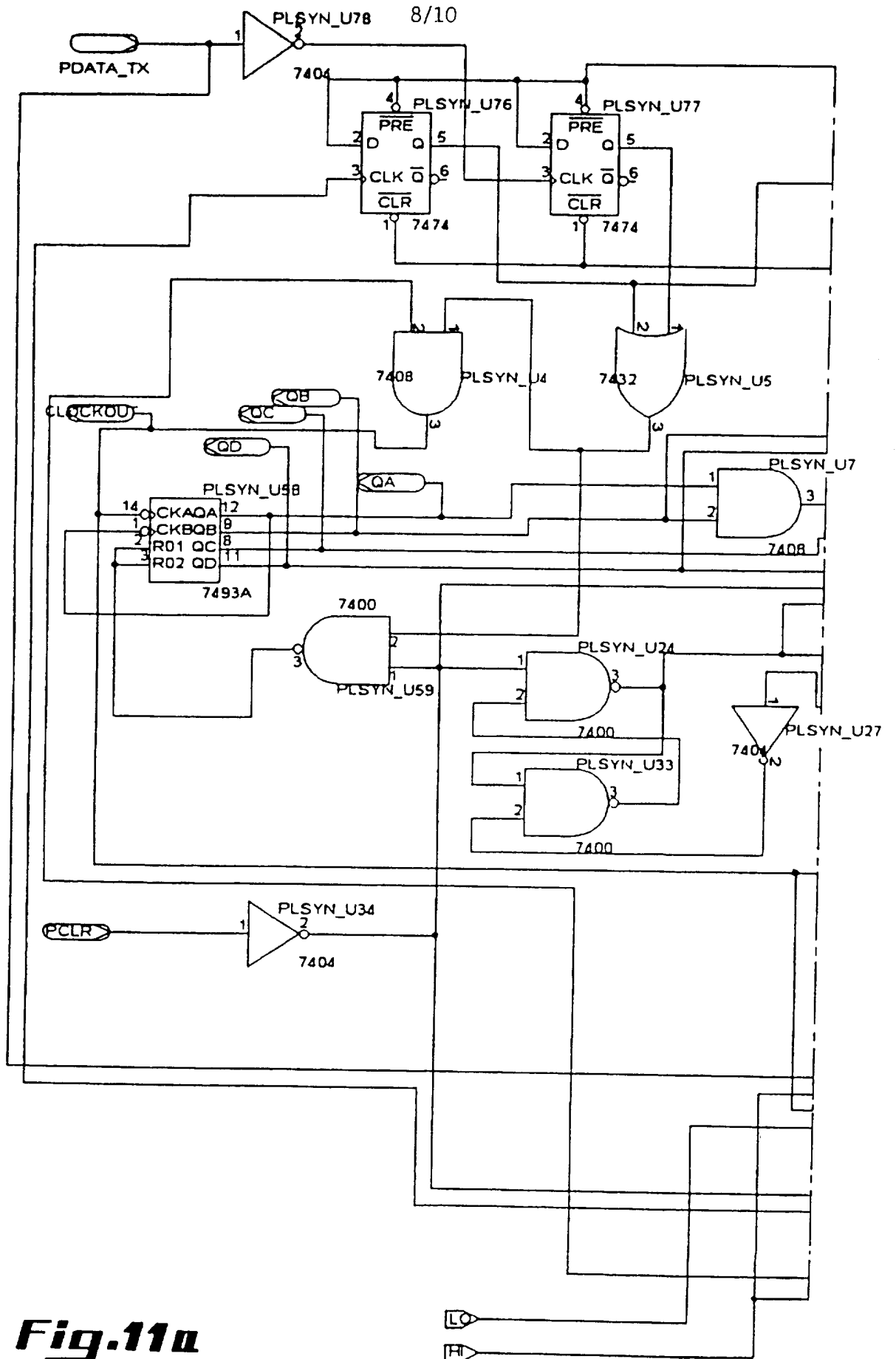
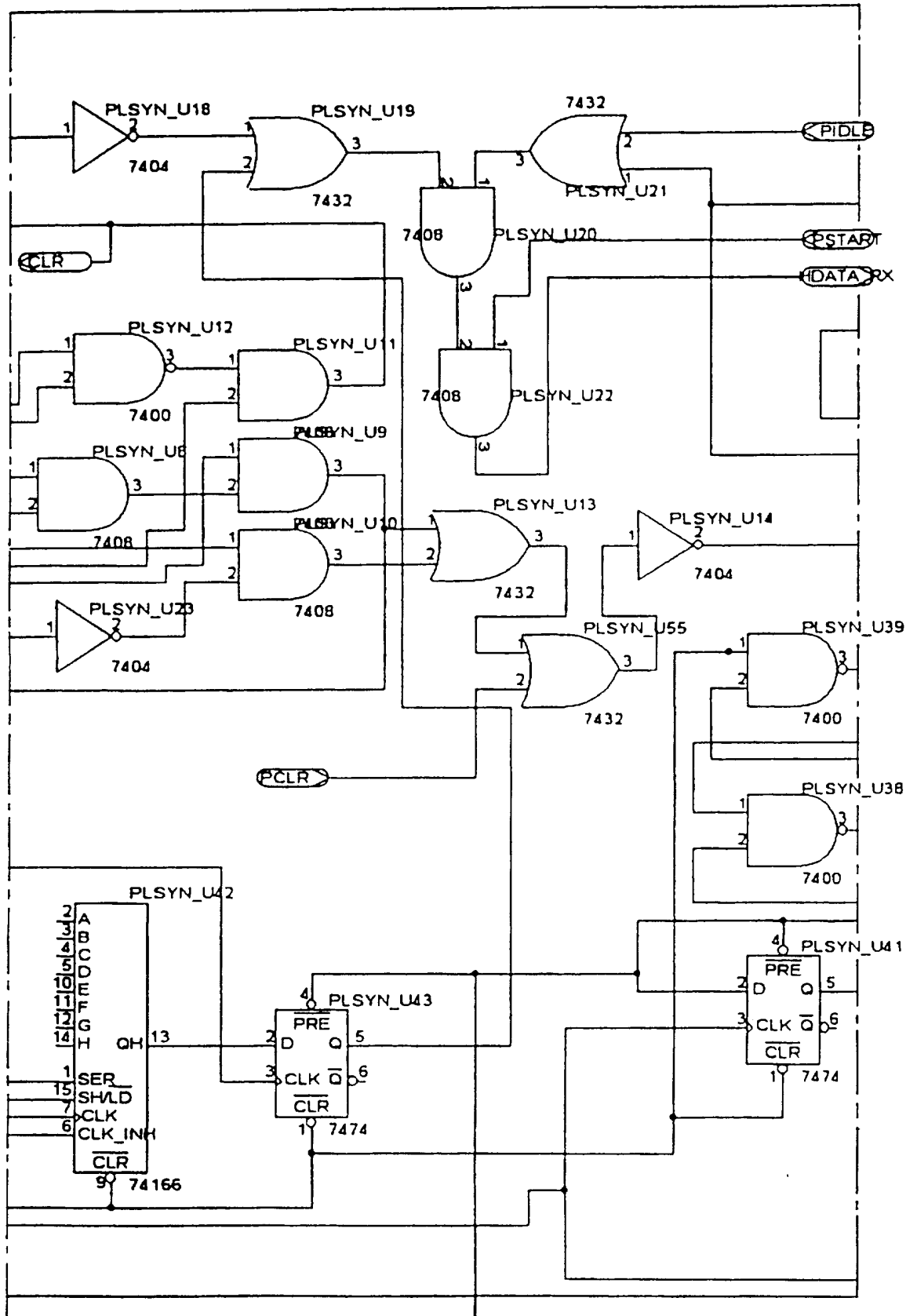


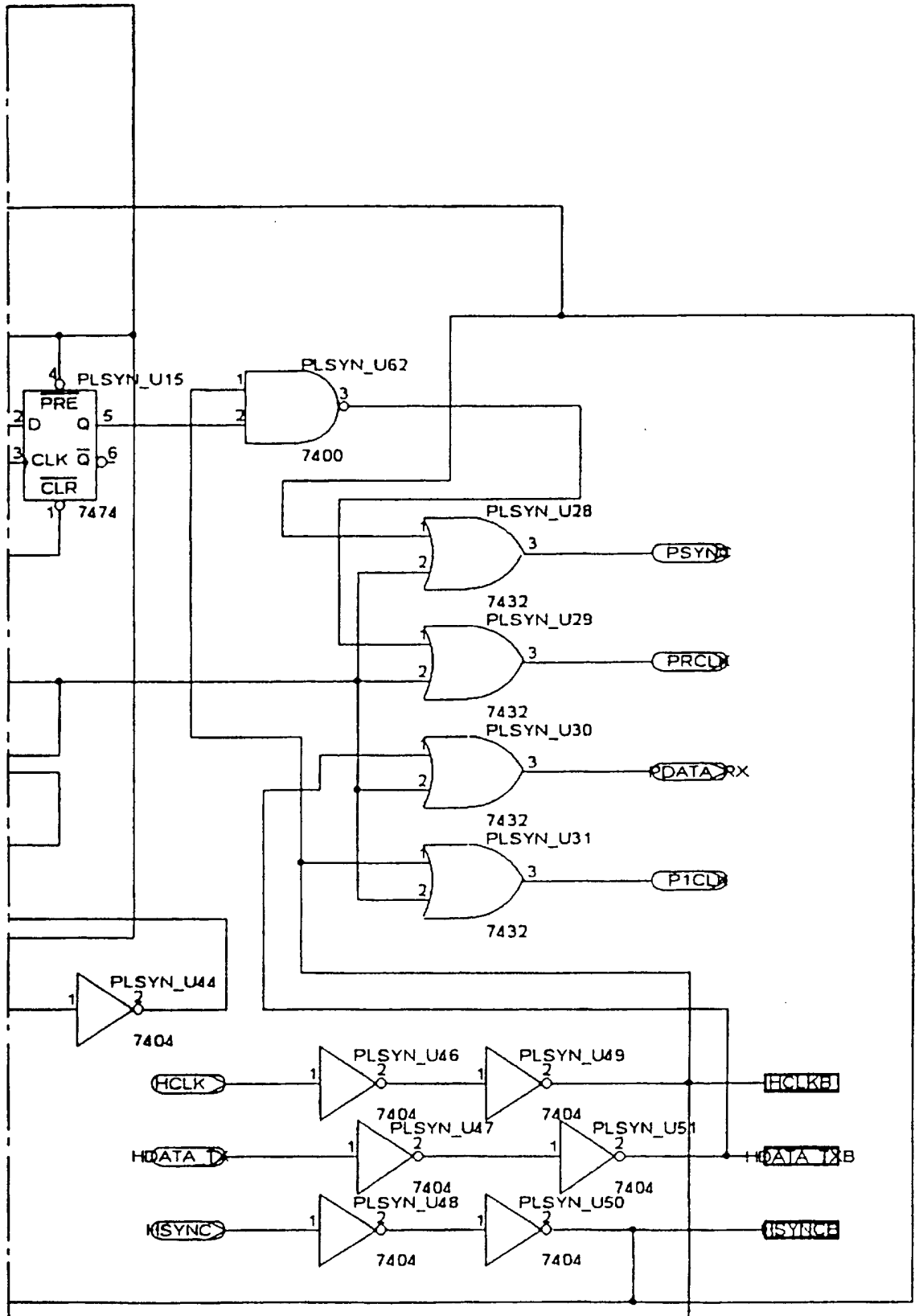
Fig. 10b



**Fig.11a**



**Fig.11b**



**Fig.11c**

# INTERNATIONAL SEARCH REPORT

Internat. Application No

PCT/BE 97/00046

**A. CLASSIFICATION OF SUBJECT MATTER**

IPC 6 H04Q7/32

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H04Q H04L H04J G06F

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**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 655 873 A (NOKIA MOBILE PHONES LTD) 31 May 1995 cited in the application see page 4, line 35 - page 5, line 4 see page 5, line 35 - line 39 see figures 1A-C,2 ---	1-4
A	WO 94 11998 A (COMPAQ COMPUTER CORP) 26 May 1994 see page 7, line 33 - page 8, line 2 see page 10, line 26 - line 31 see page 21, line 29 - page 23, line 31; figures 1B,2,6A,6B see page 7, line 33 - page 8, line 2 --- -/--	1-3

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Date of the actual completion of the international search

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 249 218 A (SAINTON JOSEPH B) 28 September 1993 see column 5, line 10 - line 62 see column 13, line 1 - line 7 see column 14, line 24 - line 52; figures 1A,3 ---	1,2
A	US 5 214 650 A (RENNER ROBERT E ET AL) 25 May 1993 see column 12, line 50 - line 59; figure 10 -----	1

## INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/BE 97/00046

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0655873 A	31-05-95	FI 935347 A DE 655873 T ES 2096537 T	31-05-95 15-05-97 16-03-97
WO 9411998 A	26-05-94	AT 147922 T AU 5726794 A CA 2147119 A DE 69307537 D EP 0668005 A EP 0741480 A JP 8503583 T	15-02-97 08-06-94 26-05-94 27-02-97 23-08-95 06-11-96 16-04-96
US 5249218 A	28-09-93	AU 3939693 A BG 98359 A BR 9305468 A CA 2110722 A CZ 9400026 A EP 0587862 A HU 67256 A JP 6508255 T NO 934401 A SK 1494 A WO 9320643 A US 5367563 A	08-11-93 15-08-94 02-08-94 14-10-93 13-04-94 23-03-94 28-03-95 14-09-94 04-02-94 11-05-94 14-10-93 22-11-94
US 5214650 A	25-05-93	CA 2051818 A	20-05-92