

- [54] **SYNCHRONIZING-PULSE GENERATING DEVICE FOR AN APPARATUS FOR CONTROLLING THE AUTOMATIC MUSICAL PERFORMANCE OF A KEYED INSTRUMENT**
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- [51] Int. Cl. **G10f 5/00**
- [58] Field of Search 84/1.01, 1.02, 1.03, 1.28, 84/464, 470, DIG. 29, 115

[56] **References Cited**
UNITED STATES PATENTS

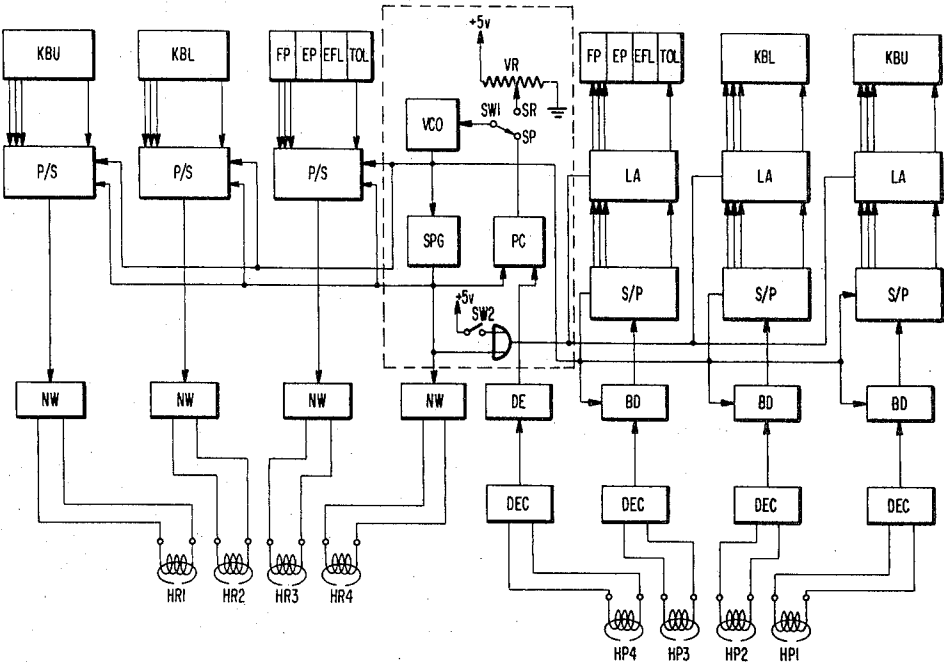
3,539,701	11/1970	Milde.....	84/1.28
3,604,299	9/1971	Englund.....	84/1.03
3,610,799	10/1971	Watson.....	84/1.01

3,610,801	10/1971	Fredkin et al.	84/1.03
3,634,596	1/1972	Rupert	84/1.28
3,647,929	3/1972	Milde, Jr.	84/1.01
3,683,096	8/1972	Peterson et al.	84/1.03 X
3,697,661	10/1972	Deutsch	84/1.01
3,771,406	11/1973	Wheelwright.....	84/464
3,774,494	11/1973	Reid, Sr. et al.	84/470
3,781,452	12/1973	Vaclair	84/1.28
3,784,717	1/1974	Okamoto	84/470
3,789,719	2/1974	Maillet.....	84/115
3,800,060	3/1974	Hallman, Jr.	84/1.01 X

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[57] **ABSTRACT**
In an apparatus for automatically controlling the playing of an organ from recorded keyboard control and synchronizing signals, a synchronizing-pulse generating circuit corrects the phase of the reproduced synchronizing signal so that it is properly tuned relative to the corresponding reproduced keyboard control signals.

4 Claims, 11 Drawing Figures



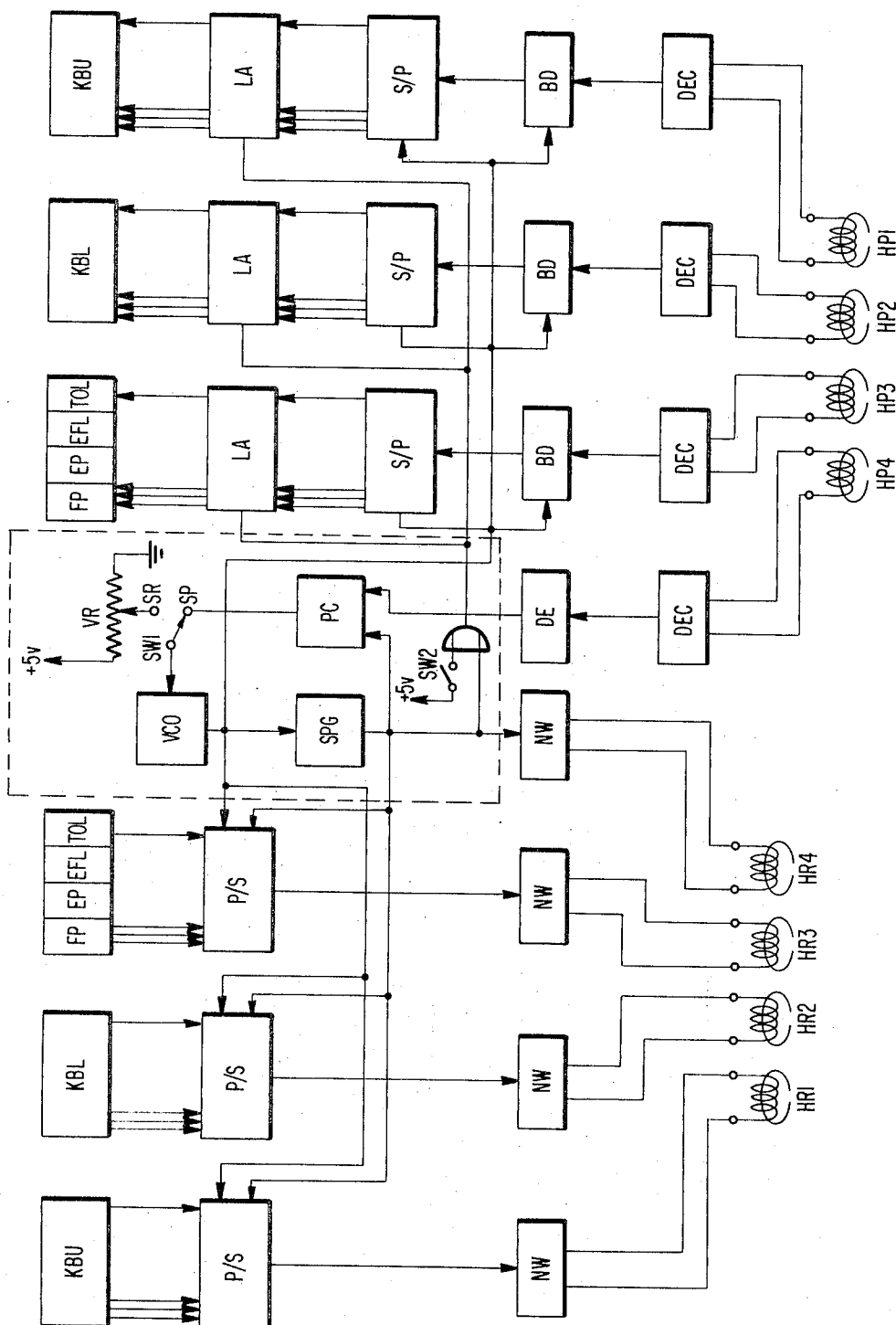


FIG. 1

FIG 2

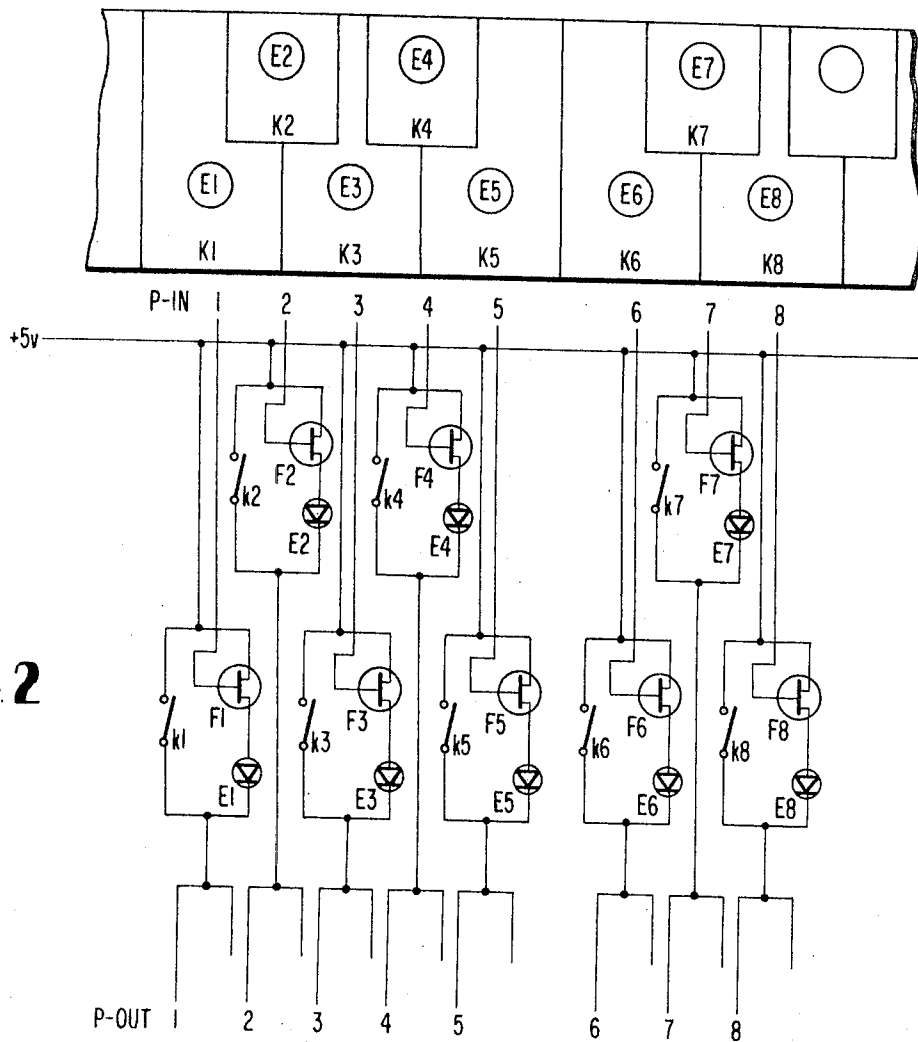
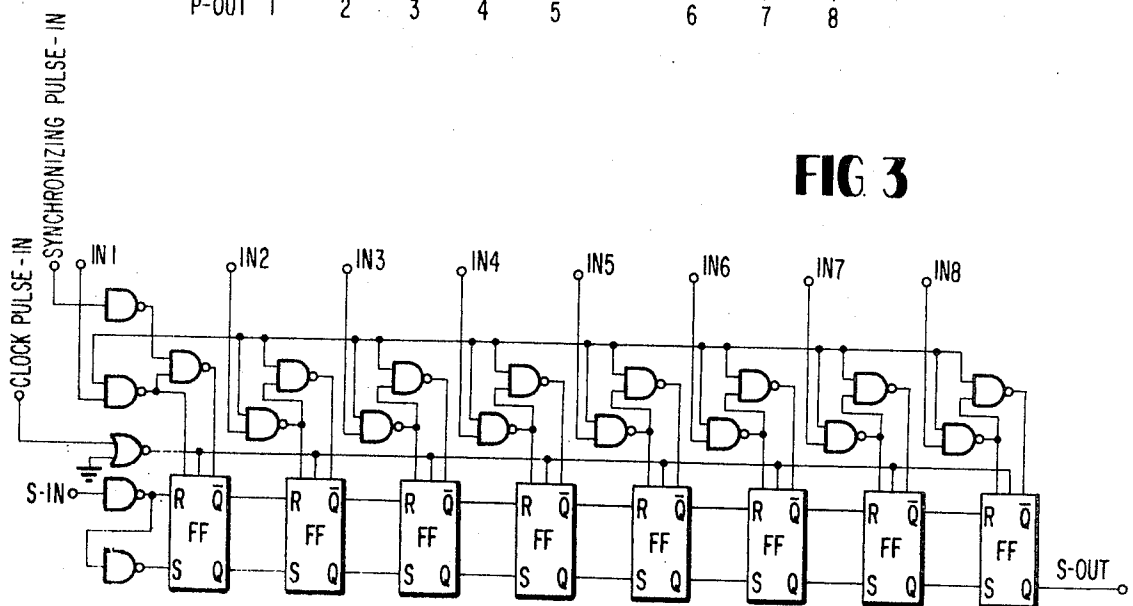


FIG 3



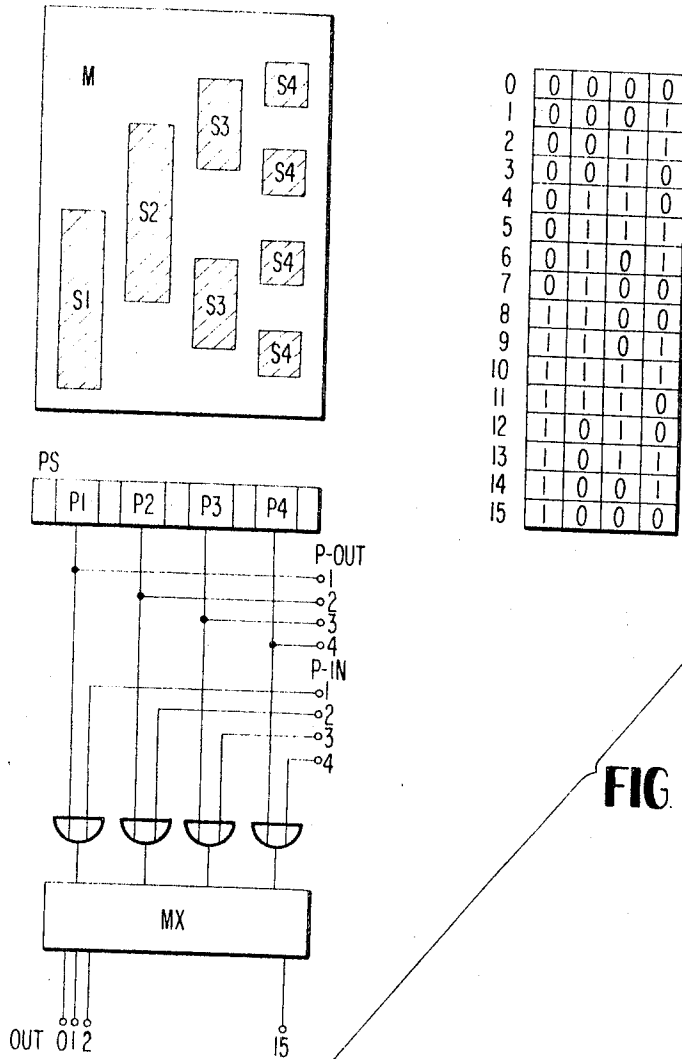


FIG 4

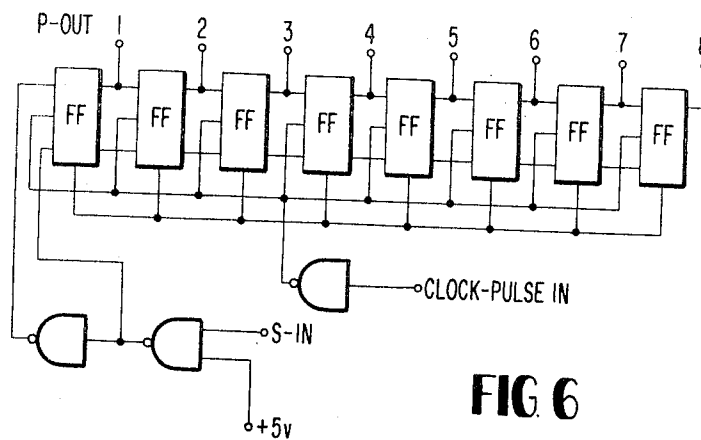


FIG 6

FIG 5B

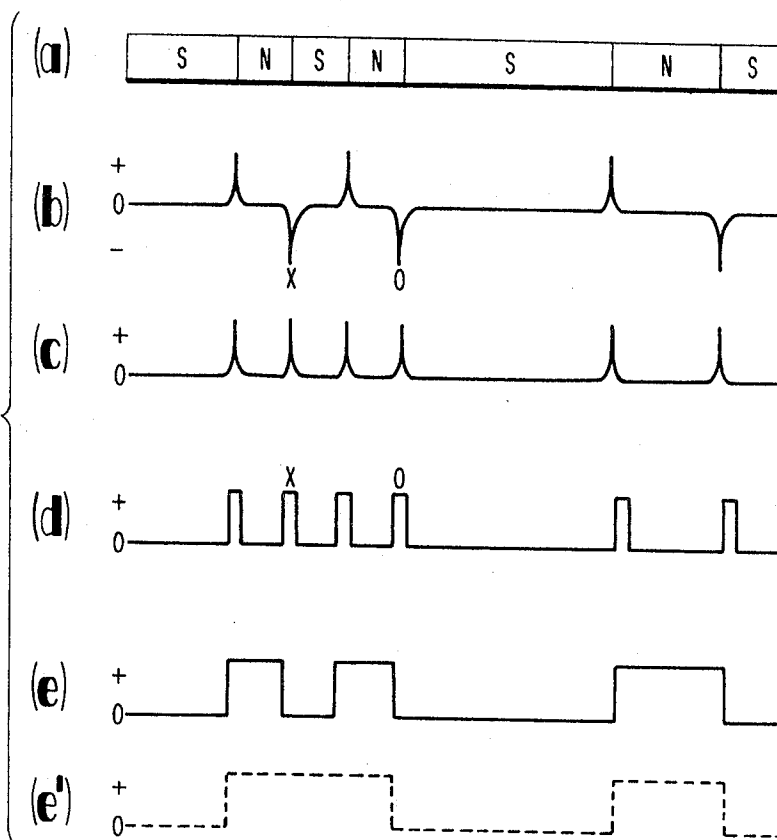


FIG 5A

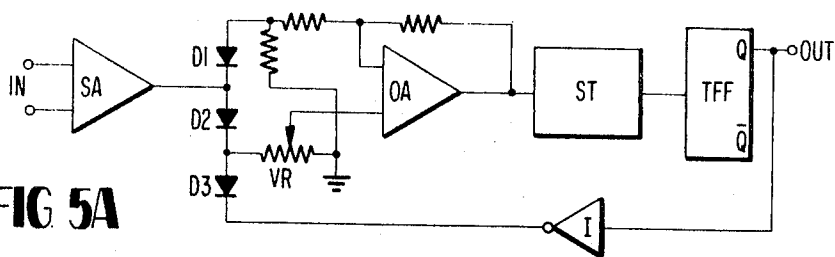
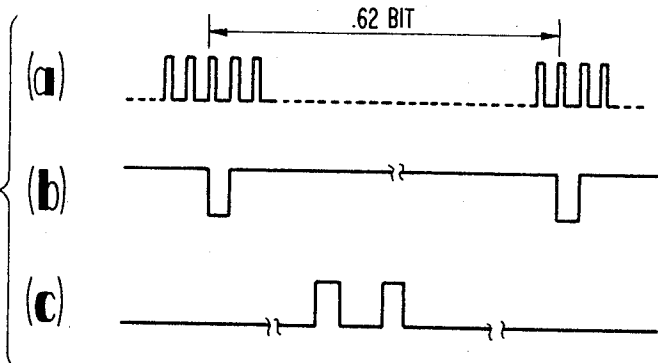


FIG 7



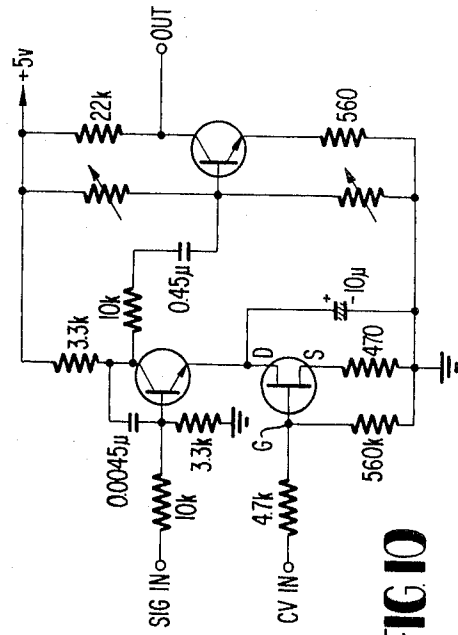
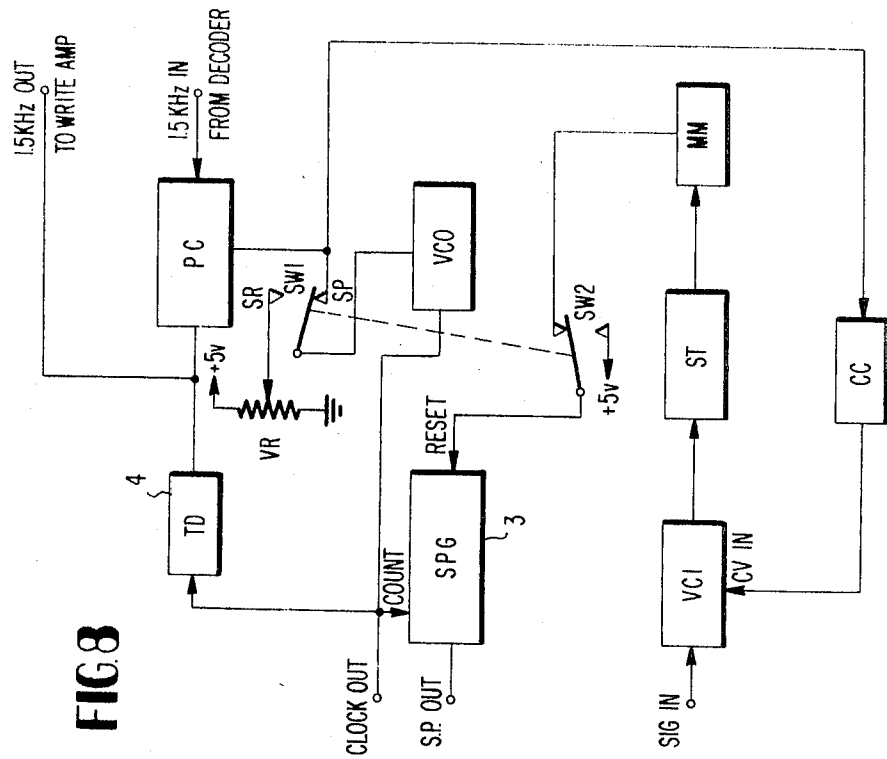
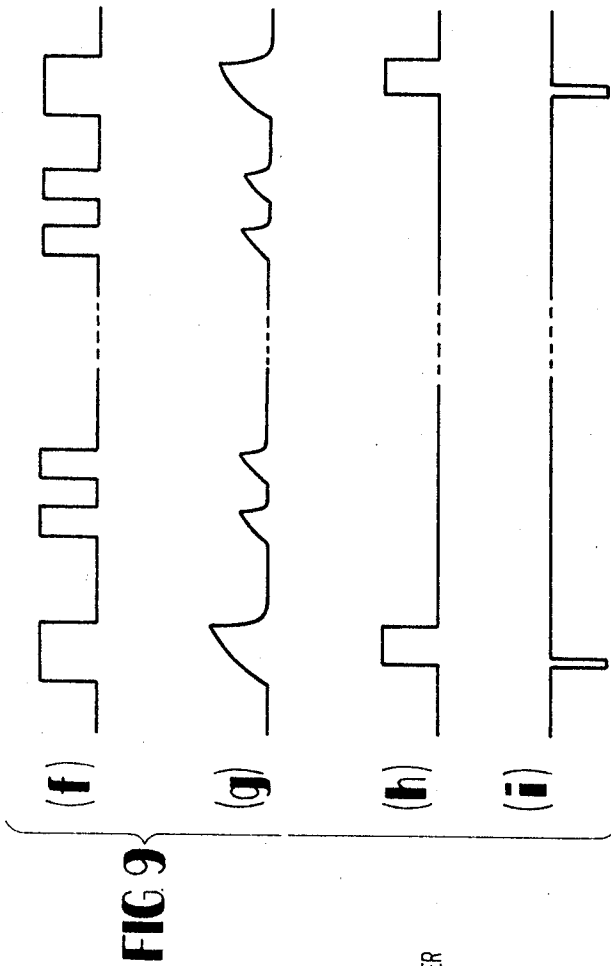


FIG 10

SYNCHRONIZING-PULSE GENERATING DEVICE FOR AN APPARATUS FOR CONTROLLING THE AUTOMATIC MUSICAL PERFORMANCE OF A KEYED INSTRUMENT

BACKGROUND OF THE INVENTION

1. Field of the Invention:

This invention relates to a synchronizing pulse generating device for use in an apparatus for automatically playing a keyed instrument under the control of recorded digital signals representing the keying pattern of keyboards, tone levers, effect levers and the like which are operated to play a musical composition on a keyed instrument; and more particularly to a synchronizing pulse generating device improved so that an exact, stable automatic musical performance can be achieved even if the tape recorder used for the recording and reproducing of the control signals is not highly efficient.

2. Description of the Prior Art:

There has been disclosed in copending application Ser. No. 417,331, filed Nov. 19, 1973, for "Automatic Musical Performance Method and Apparatus for a Keyed Instrument" filed by Tutomu Fukui and Tsutomu Suzuqui and assigned to the assignee of the present application, an apparatus for automatically playing a keyed instrument, such as an electronic organ, which apparatus includes: reproducing means for reproducing a synchronizing pulse signal and a serial pulse-line signal recorded on a recording medium, such as a magnetic recording tape, in accordance with a musical performance of the electronic organ; a circuit for generating a clock-pulse signal by receiving the reproduced synchronizing pulse signal; a serial-in, parallel-out converting circuit for converting a serial pulse-line signal into a parallel signal group by receiving the clock-pulse signal; and a latch circuit for storing an input signal coming from the serial-in, parallel-out converting circuit as an output signal by receiving each synchronizing pulse signal until the next synchronizing pulse signal arrives.

This automatic apparatus records the synchronizing pulse signal on a synchronizing track of the recording medium as it is, and controls the clock-pulse generating circuit by a phase comparison of the reproduced synchronizing pulse signal with a synchronizing pulse signal generated by a synchronizing pulse generating circuit. However, since the phase comparison is made only at the rate of once every predetermined several bits of the clock pulses, the phase difference between a reproduced serial pulse-line signal and a clock-pulse signal generated from the last phase comparison with the synchronizing pulse signal and the next phase comparison is compensated by a DC voltage obtained by smoothing an error signal generated every predetermined several bits through an integrating circuit having a long time constant. This means that the phase comparison between the serial pulse-line signal and the clock-pulse signal cannot follow the high frequency jitter or flutter component that the tape recorder mechanism has. Therefore, it is necessary to use a relatively high performance recording-reproducing mechanism.

SUMMARY OF THE INVENTION

The primary object of the present invention is to provide a synchronizing pulse generating device whereby exact, stable automatic musical performance may be carried out even if the mechanism for transporting the

recording medium is not of the high performance type.

Now, one embodiment of an automatic music performance apparatus in accordance with the present invention method will be explained in detail in conjunction with the accompanying drawings. A one-gate type organ with indirect keying is used in this embodiment, but a direct keying type organ may be used with the present invention by adding a few circuits or devices, or by mechanically operating keys.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing the whole construction of an automatic music performance apparatus in accordance with the present invention.

FIG. 2 is a partial view of an upper key board and its attached device.

FIG. 3 is a partial view of a parallel serial converter.

FIG. 4 is an explanation diagram of an expression pedal device.

FIGS. 5A and 5B are a block diagram of a decoder circuit and a diagram showing signal waveforms at some points, respectively.

FIG. 6 is a partial view of a serial parallel converter.

FIG. 7 is a diagram showing a clock-pulse signal, a synchronizing pulse signal and keying signals.

FIG. 8 is a block diagram showing a synchronizing pulse generating device in accordance with one embodiment of the present invention.

FIG. 9 is a diagram showing signal waveforms at various points of the generating device.

FIG. 10 is a circuit diagram showing one embodiment of a voltage-controlled integrating circuit used in the generating device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 is a block diagram showing the entire construction of the present apparatus including the following elements: upper key board KBU; foot pedal FP; effect lever EFL; parallel-to-serial converting circuit P/S; non-return-to-zero writing amplifier N/W; lower key board KBL; expression pedal EP; tone lever TOL; magnetic recording heads HR1-HR4; clock-pulse generating circuit VCO; synchronizing pulse generating circuit SPG; phase comparison circuit PC; play-back heads HP1-HP-4; decoder circuit DEC; delay circuit DE; bit-delay circuit BD; serial-in, parallel-out converting circuit S/P; and latching circuit LA.

Next, main elements of the above-mentioned construction elements will be explained in detail.

FIG. 2 represents a portion of keys in the upper key-board KBU and circuits attached to them. Natural and chromatic keys K1 to K8 of the upper keyboard KBU have switches k1 to k8 turned on and off by touching them in each corresponding place, respectively. By operation of these switches k1 to k8, tone generators, not shown, of the electric organ are controlled to emit a sound in accordance with the keys touched, and control signals to be recorded for automatic musical performance are generated. P-OUT 1 to P-OUT 8 are output lines coupled to parallel-to-serial converter P/S. Further, the switches k1 to k8 are respectively connected in parallel with series circuits of field effect transistors F1 to F8 and electro-luminous diodes E1 to E8. These field effect transistors turn on or off, in automatic performance, by receiving control signals from the latching circuit LA through input lines P-IN1 to P-

IN8, whereby the electro-luminous diodes E1 to E8 buried in each of keys (or other indicating means corresponding with the keyboards) light to indicate playing-back keys, and the electric organ is controlled for automatic performance just as the switches $k1$ to $k8$ turn on and off. The explanations, for the lower keyboard KBL, the foot pedals FP, the effect levers EFL and the tone levers TOL and so on, will be omitted because these basically have the same constructions as the upper keyboard KBU.

FIG. 3 represents one kind of 8-bit parallel-in, serial-out converter. A parallel-to-serial converter having the required number of bits in multiples of eight may be constructed by connecting the output line S-OUT of one to the input line S-IN of another. This parallel-to-serial converter P/S is a circuit for converting a group of parallel ON-OFF signals appearing in parallel by manipulating each keyboard KBU, KBL and FP and/or each lever EFL and TOL into a serial pulse line signal changing with the passing of time (in this embodiment, an 8-bit parallel-in, serial-out shift register is used). The parallel-to-serial converter used in practice has as many bits as the switches contained in all the control key means, such as keyboards, levers and pedals. In this embodiment, 61-bit parallel-to serial converters are used for each of the upper and lower keyboards KBU and KBL, respectively. As to the others, another parallel-to-serial converter having 61 bits in total, namely 4 bits for the expression pedal, 13 bits for the foot pedals and 44 bits for the tone levers TOL and the effect levers EFL, is used.

FIG. 4 is a schematic diagram of the expression pedal EP. A shutter M is operated by an expression pedal (not shown), which shutter M slides in accordance with pressing of the pedal between light sources and photo-sensors PS. The shutter M has in it slits S1 to S4 cut through in accordance with the illustrated 16-step gray code corresponding with the decimal numbers zero to fifteen. Each of photo-transistors P1 to P4 of the photo-sensor PS detects the light passing through the slits S and encodes the pressing depth of the expression pedal as a volume control signal. This encoded 4-bit volume control signal is applied to the parallel-to-serial converter P/S through output lines P-OUT1 to P-OUT4, converted in the same manner as the keyboard signals into a serial pulse line signal changing with the passing of time, and then recorded.

On the one hand, the volume control signal is applied to a diode matrix circuit MX through OR circuits, whereby the matrix circuit MX produces an output signal at a corresponding one of output terminals OUT0 to OUT15. A conventional volume control circuit (not shown) is controlled by the output signal. For automatic performance, volume control signals coming from a latching circuit LA to input lines P-IN are applied to the diode matrix circuit MX to control the volume control circuit just as in manual performance.

FIGS. 5A and 5B represent a decoder circuit DEC and waveforms at some points of the circuit, respectively. Each decoder circuit DEC amplifies signals reproduced by means of the corresponding play-back head HP1 to HP4 and reforms them to the original recording signal waveforms. The circuit is composed of a sensing amplifier SA, diodes D1 to D3, an operational amplifier OA, a Schmitt trigger circuit ST, a T-type flip flop circuit TFF, an inverter I and so on. When magnetic signals on a magnetic tape as shown at (a) of FIG.

5B are picked up by means of the play-back heads, the output signals become pulse signals as shown at (b). When such pulse signals come to the decoder circuit DEC, the signals are amplified to a sufficient level by the sensing amplifier SA, separated according to polarity by diodes D1 and D2, and applied to the inputs of the operational amplifier OA. At the time, negative pulses adding through the diode D1 are applied to the inverting input terminal and positive pulses adding through the Diode D2 are applied to the non-inverting input terminal; therefore, the output signals from the operational amplifier OA are a full-wave rectified version of the output signals of the sensing amplifier SA. The output waveform of amplifier OA is shown at line (c).

The waveform of the output signal of the operational amplifier OA is shaped by the Schmitt trigger circuit ST into a square pulse line signal shown in (d), and then is applied to the T-type flip flop TFF. Since the output of this T-type flip flop TFF functions to switch its output on each positive going edge of the input signal, the input signal (d) is converted into a signal as shown in (e) and this becomes an output signal of the decoder circuit DEC.

The decoder circuit described so far is subject to producing an improperly inverted output signal relative to the required signal when an input pulse is not reproduced on account of dropping-out of a magnetic tape and the like. Consequently, a feed-back circuit composed of an inverter I and a diode D3 is so added as to minimize error caused by such a condition. If, for example, the pulse marked by "x" in FIG. 5B is not played back, the errors in the output signal are kept to a few because the output signal of the decoder circuit DEC becomes as shown in (e'). Namely, when the output signal level of the T-type flip flop TFF is positive (+), the output signal of the inverter I goes to the zero level to render diode D3 conducting, and thus the next positive going pulse coming from the sensing amplifier SA does not reach the operational amplifier OA. If the decoder circuit DEC is further improved so that a negative going pulse also does not add to the operational amplifier OA when the output of the flip flop TFF is at the zero level, the error caused by the dropping-out of the tape is further minimized. In this decoder, the diodes D1 and D2 and the operational amplifier OA are used for making the polarities of the output signal of the sensing amplifier SA uniform, but this function may be performed by other means, such as a full wave rectification circuit. Even in this case, of course, a feedback circuit, such as described above, is necessary for rectifying an input signal, subject to drop out error, in the proper order of positive-negative-positive-negative. The inverter I used in the feedback circuit is used primarily to isolate the input and output of amplifier OA from each other; therefore, the inverter I is not necessary if the $\bar{Q}$ output terminal of the flip flop TFF is used for the feedback circuit.

FIG. 6 shows a serial-to-parallel converter S/P. This circuit S/P converts into a group of original parallel pulses, the serial pulse line signal changing with the passing of time and arriving at input lines S-IN via a decoder circuit DEC and a bit-delay circuit BD. In this embodiment, a conventional 61-bit serial-in, parallel-out shift-register is used as a parallel-to-serial converter.

Next, the operation of the automatic musical performance apparatus will be explained. First, the explanation will begin with the recording of a keying pattern or control signals. To place the apparatus in the state for recording control signals, the movable contact of switch SW1 in FIG. 1 is placed in engagement with the fixed contact SR. Therefore, a clock-pulse generating circuit VCO, the frequency of which is voltage-controlled, is controlled by a fixed voltage to generate a clock-pulse signal of 3000Hz as shown on line (a) of FIG. 7. A synchronizing-pulse generating circuit SPG counts the clock-pulses to generate as a synchronizing pulse signal 1 pulse every 62 bits, as shown on line (b) of FIG. 7.

Consequently, when an organist plays or operates the upper keyboard KBU, the lower keyboard KBL, the foot pedals FP, the expression pedal EP, the effect lever EFL, and the tone levers TOL to produce music, the switches corresponding to each key and each lever and the like turn on and off in response to the manual playing or operations of the organist, and the output signals obtained from these switches fed to the corresponding parallel-to-serial converters P/S. For example, when keys K1 and K4 of the upper keyboard KBU are touched at the same time, switches k1 and k4 close respectively, and thereby DC current or signals are fed to the corresponding parallel-to-serial converter P/S through output lines P-OUT1 and P-OUT4. The signals corresponding to keys K1 to K4 fed to the parallel-to-serial converter P/S are applied through input lines IN1 and IN4 to the shift register shown in FIG. 3. These key signals are preset at once in corresponding shift register flip flops FF by synchronizing pulse having a pulse width of one bit and which occurs about every 1/48 second. The preset signals are then shifted out of the shift register in order by incoming clock-pulses, and thus are converted to a serial pulse line signal as shown in line (e) of FIG. 7. Namely, an input signal group applied in parallel to the parallel-to-serial converter P/S is converted into a serial pulse line signal changing with the passing of time, and then is applied to its corresponding writing amplifier NW. The serial pulse line signal applied to the writing amplifier NW is changed here from an unbalanced signal mode to a balanced signal mode, and is recorded in NRZ (No Return to Zero) form by means of the recording head HR1 on a first track of the magnetic recording tape.

The circuit operation as mentioned above may be applied to the other keyboard KBL, the foot pedal FP and all the levers EFL and TOL in the same manner as to the upper keyboard KBU. As for the expression pedal EP, there is no difference from the upper keyboard KBU except for encoding a pressed depth of the expression pedal into a four-bit pulse signal.

The signal from the lower keyboard KBL is recorded on a second track, the other signals on a third track, and the synchronizing pulse signal on a fourth track, respectively.

Explained below is an example of an automatic musical performance carried out in accordance with the signals recorded by the method described above. Four channels of the pulse line signals are picked up by means of the play-back heads HP1 to HP4 corresponding with each recorded track. Each channel is applied to a corresponding decoder DEC where the signals are amplified, recovered to the unbalanced signal mode, and are decoded to the original recording signal by the

diodes D1 and D2, the operational amplifier OA, the Schmitt trigger circuit ST and the flip flop TFF, all as described above in connection with FIG. 5.

The decoded signals of the first to third-tracks, i.e. the signals obtained by the operation of every key, lever and pedal, are applied to the bit-delay circuits BD to be delayed by one bit therein. On the one hand, the decoded fourth-track synchronizing pulse signal is delayed by the delay circuit DE which is capable of delaying it for any time during a one-bit time period by the time necessary for compensating for the time lag between the synchronizing pulse signal and other operation signals, which time lag occurs in the process of recording and reproducing.

The synchronizing pulse signal thus reproduced and recovered enters the phase comparing circuit PC consisting of a phase-locked loop circuit together with the clock-pulse generating circuit VCO, and is compared in phase with the output signal of the synchronizing-pulse generating circuit SPG. The result of the phase comparison is fed back to the clock-pulse generating circuit VCO through a switch SW1 shown in FIG. 1. Therefore, the pulse signals having the most appropriate phase relationship between them are always applied from both the clock-pulse generating circuit VCO and the synchronizing pulse generating circuit SPG to any other circuits.

Each serial pulse line signal going out of every bit-delay circuit BD enters the shift register of the serial-to-parallel converter S/P (FIG. 6) via the input line S-IN thereof in proper order and synchronized with the clock-pulse signal added to it at the same time. Consequently, the same signal appears on the output line Pn-OUT of the nth flip flop FF of the shift register one clock-pulse bit later than it appears on the (n-1)th output line P(n-1)-OUT. Namely, the signals are shifted bit by bit through every output line of the shift register to accomplish serial-to-parallel conversion. Assuming that time stopped at some bit of the clock-pulse signal, then serial pulse line output signals at that time will correspond to the serial pulse line signal already converted into a parallel signal pattern. Therefore, in practice a parallel signal group, changing its contents with the frequency of the clock-pulse signal, appears on the output lines P-OUT of the flip flops FF, and it is applied to the latching circuit LA.

The signal group applied to the latching circuit LA as a parallel pulse signal group changing with the frequency of the clock-pulse signal is stored in the latching circuit LA when the synchronizing pulse signal having a pulse width of one-bit adds to it. Namely, the latching circuit stores a pattern of the parallel signal group coming to the latching circuit LA at the very time when the synchronizing pulse signal is about to add to it, and then holds it as the output of the latching circuit through about 1/48 second until the next synchronizing pulse signal comes, regardless of the presence or absence of input signals.

Every output signal of the latching circuit obtained like this is applied to a gate circuit corresponding to every key, every lever or the like, for example a gate electrode of the every field effect transistor as shown in FIG. 2 in order to turn it on and off, whereby the electroluminescent diode lights to indicate a playing key, and the electric organ is automatically controlled just as an organist manually plays the electric organ. The electric organ is perfectly controlled for playing organ

music on the basis of this chain of operations explained above.

In this embodiment, the present invention is applied to an electric organ. However, the present invention may be applied to other different kinds of keyed instruments, for example an electronic piano or an ordinary piano. When the present invention is applied to an ordinary piano, the object is achieved by automatically controlling the keys by operating an electro-magnetic plunger with the output signal of the latching circuit, but it is necessary to add another device for reconstruction of the strength and weakness of touching force applied to the keys.

The method and apparatus of the present invention is described above have achieved the foregoing objects perfectly, and further have the following features or merits.

First, since the present invention converts into a serial pulse line signal a parallel signal group formed by ON-OFF signals produced by operating keys and then records and reproduces the converted serial pulse line signal, the recording and the reproducing of the signals not only may be carried out by the use of an ordinary tape recorder of simple construction and without making use of a digital tape recorder having many recording tracks, but in addition the tone quality and musical interval is never modified by wow or flutter of the tape.

Second, the invention permits an organ to be played by hand simultaneously with an automatic music performance by the organ; therefore, the invention permits a player to play only the melody of a musical composition to the accompaniment of the music being automatically played by the apparatus.

Third, since indicating means are provided for indicating the keys being played, one can listen to the music while observing the variation of the keying pattern. Further, it is preferable during the teaching of an organ lesson that a luminous indicating element be mounted in every key.

Fourth, one is capable of listening to a recorded music transposed at one's option in automatic music performance because one is able to transpose a recorded music at one's option only to delay keying signals or a synchronizing pulse signal. Yet, since signals of low-pitched sound positions are shifted to high-pitched sound positions if all the bits being between two adjacent synchronizing pulses are used for keying signals, it is necessary to establish a number of total bits between two adjacent synchronizing pulses in a total number of a number of keys and a number of delay bits necessary for transposition.

Further, one is able to change musical performance speed without modifying a musical interval.

FIG. 8 represents one embodiment of a synchronizing pulse generating device in accordance with the present invention. This synchronizing pulse generating device acts as a substitute for the portion encircled by the dotted line in FIG. 1. Signals as shown in FIG. 9(f), composed of both a synchronizing pulse signal and control or clock signals necessary for musical performance are played back by play back head HP4 and applied to a voltage-controlled integrating circuit VCI in FIG. 8. Waveforms of signals integrated through the voltage-controlled integrating circuit VCI become output signal waveforms having a large difference of voltage level between the synchronizing pulse signal and the clock pulse signal as shown in FIG. 9(g), assuming that the

pulse width of the synchronizing pulse signal is chosen to be twice as large as that of the clock pulse signal. This output signal is then applied to a Schmitt trigger circuit ST whose triggering level is between the peak values of the clock pulse signal and the synchronizing pulse signal, and thus a signal as shown in FIG. 9(h) appears at an output terminal of the Schmitt trigger circuit ST regardless of the presence of the clock pulse signal. The synchronizing pulse signal selected like this is used as a reset signal for instructing the synchronizing-pulse generating circuit SPG to begin counting incoming clock pulses from VCO, whereby the synchronizing-pulse generating circuit SPG is able to generate as an output signal a corrected synchronizing pulse synchronized with the recorded signal play back by play back head HP4.

In addition, if the reset pulse width is larger than that of the clock pulse, the synchronizing-pulse generating circuit SPG may count one bit more or less than the actual number, when the reset signal falls on the positive going or negative going edge of the clock pulse from VCO. To prevent such an error, mono-stable multivibrator MM causes the pulse width of the reset signal to be smaller than that of the clock pulse, as shown in FIG. 9(i), and the output of MM is applied to the reset input terminal of the synchronizing-pulse generating circuit SPG.

Further, when the reproduction speed of the recording medium is changed to change the speed of a musical performance being automatically played, the pulse width of the reproduced pulses changes in response to the reproduction speed. Therefore, if the voltage-controlled integrating circuit VCI is not controlled to compensate for this change, either the synchronizing pulse signal would not be selected by the Schmitt trigger circuit ST, or the keyboard signal would not trigger the Schmitt trigger circuit ST, because the peak value of the output signal of the voltage-controlled integrating circuit VCI changes in response to changing of the reproduction speed, even though the ratio of the peak values of the signals shown in FIG. 9(g) is fixed. For preventing such an error, a control voltage for controlling the integrating property may be applied to the voltage-controlled integrating circuit VCI. When, for example, a circuit as shown in FIG. 10 is used as the voltage-controlled integrating circuit VCI, it is able to freely control the peak value of the output signal appearing at an output terminal thereof by regulating the control voltage to be applied to a control terminal CVin. This control voltage is obtained by applying the DC voltage output of the phase comparison circuit PC to a characteristic converting circuit CC for converting the voltage to a desired characteristic control voltage. Consequently, the peak value of the waveform shown in FIG. 9(g) is maintained substantially constant even though the pulse width of the reproduced pulses changes in response to changing of the reproduction speed of the recording medium.

It is possible to directly use the clock pulse as a synchronizing signal, but it is possible also to use the clock-pulse signal divided in which may be a T-type flip flop to divide by two and provide a 1.5KHz to the write amplifier for recording head HR4. This same 1.5KHz output is also supplied as one input to the phase comparator PC, the other input to phase comparator PC being the signals shown in FIG. 9(f). In any case, there is scarcely the chance of an error due to a mis-operation.

Moreover, there is scarcely the risk of a mis-operation in any case, even if there is a high frequency jitter or flutter component in the transportation of the recording medium, because the phase compensation is made once every bit or several bits.

What is claimed is:

1. A synchronizing pulse generating device for use in an apparatus for automatically controlling the playing of a keyed instrument including reproducing means for reproducing a composite recorded synchronizing pulse signal and a recorded clock pulse signal and for reproducing a recorded serial keying signal; variable clock-pulse generating means for generating a clock pulse; serial-to-parallel signal converting means for converting the reproduced serial keying signal into a parallel-signal group in response to the receipt of a clock pulse from said clock-pulse generating means; and latching circuit means sequentially operated by successive synchronizing pulses for sequentially storing as output signals thereof the parallel-signal group from said serial-to-parallel signal converting means, said synchronizing pulse generating device comprising:

- a. synchronizing-pulse detecting means connected to said reproducing means for discriminating said recorded synchronizing pulse signal;
- b. synchronizing-pulse generating means for receiving the clock pulses from said clock-pulse generating means as a counting input, and for receiving from said synchronizing pulse detecting means the reproduced synchronizing pulse signal as a reset input, to generate a phase-corrected synchronizing pulse signal; and
- c. phase comparator means connected to said reproducing means and to said clock-pulse generating means for producing an error voltage for controlling the frequency of said variable clock-pulse gen-

erating means, said synchronizing pulse signal being synchronized with said serial keying signal and with said clock pulse signal, for reading out the parallel-signal group stored in said latching means.

2. A synchronizing pulse generating device as recited in claim 1 wherein said synchronizing pulse signal has a longer time duration than said clock pulse signal and said synchronizing pulse detecting means includes:

- a. integrating means for time integrating said synchronizing pulse signal and said clock pulse signal, and
- b. threshold trigger means connected to the output of said integrating means for generating an output reset pulse only when the output of said integrating means exceeds a value proportional to the ratio of the duration of said synchronizing pulse signal and said clock pulse signal.

3. A synchronizing pulse generating device as recited in claim 2 wherein said integrating means is a voltage controlled integrator having a variable integration rate depending on the value of an applied control voltage and said applied control voltage is derived from the output of said phase comparator means.

4. A synchronizing pulse generating device as recited in claim 3 wherein said threshold trigger means includes:

- a. a Schmitt trigger for producing an output pulse having a duration equal to the time the output of said integrating means exceeds a predetermined threshold value; and
- b. a monostable multivibrator responsive to the leading edge of said output pulse for generating a reset pulse having a duration less than said clock pulse signal.

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