ABSTRACT

A light emitting diode chip, a light emitting diode package structure and a method for forming the same are provided. The light emitting diode chip includes a bonding layer, which has a plurality of voids, or a minimum horizontal distance between a surrounding boundary of the light emitting diode chip and the bonding layer is larger than 0. The light emitting diode chip, the light emitting diode package structure and the method may improve the product yields and enhance the light emitting efficiency.
FIG. 9

FIG. 10
FIG. 27A

FIG. 27B
FIG. 55

FIG. 56
FIG. 59

FIG. 60
FIG. 67A

FIG. 67B
START

Forming an ESD protection element on a sub-mount, wherein the ESD protection element is disposed along the edges of a first surface on the sub-mount and is embedded in the sub-mount

S31

Forming an electrode on the ESD protection element

S32

Providing a stacked structure and bonding the same on the first surface of the sub-mount, wherein the stacked structure is located apart from the electrode

S33

Forming an isolation layer on the electrode, the stacked structure and the space between the electrode and the stacked structure

S34

Removing a part of the isolation layer over the electrode and a part of the isolation layer over the stacked structure to expose the electrode and the stacked structure

S35

Forming a conductive thin film layer on the electrode and the stacked structure for electrically connecting the electrode to the stacked structure

S36

Forming another electrode on a second surface of the sub-mount opposite the first surface

S37

Dicing the sub-mount to form a LED structure

S38

END

FIG. 90
START

Forming an electrode on a sub-mount, wherein the electrode is disposed along the edges of a first surface on the sub-mount ~ S41

Providing a stacked structure and bonding the same on the first surface of the sub-mount, wherein the stacked structure is located apart from the electrode ~ S42

Forming an isolation layer on the electrode, the stacked structure and the space between the electrode and the stacked structure ~ S43

Removing a part of the isolation layer over the electrode and a part of the isolation layer over the stacked structure to expose the electrode and the stacked structure ~ S44

Forming a conductive thin film layer on the electrode and the stacked structure for electrically connecting the electrode to the stacked structure ~ S45

Forming another electrode on a second surface of the sub-mount opposite the first surface ~ S46

Dicing the sub-mount to form a LED structure ~ S47

END

FIG. 91
FIG. 92C

FIG. 92D
FIG. 92E

FIG. 92F
FIG. 93

FIG. 94
FIG. 115E

FIG. 115F
FIG. 116C

FIG. 116D
FIG. 120A

FIG. 120B
FIG. 128C

FIG. 129A
FIG. 130D
LIGHT EMITTING DIODE CHIP, LIGHT EMITTING DIODE PACKAGE STRUCTURE, AND METHOD FOR FORMING THE SAME

TECHNICAL FIELD

[0001] The present disclosure relates to a diode chip and package structure employing the same, and in particular relates to a light emitting diode chip and light emitting diode package structure employing the same.

BACKGROUND

[0002] Conventional process for fabricating a thin film light emitting diode (thin film LED) can be divided into two parts. The first part includes the growth of an epi wafer (an epi wafer is a wafer of semiconducting material made by epitaxial growth (called epitaxy) for use in making microelectronic devices such as light-emitting diodes (LEDs). The second part includes bonding the resulting epi wafer to a carrier substrate (such as a submount or a packaging substrate), removing the growth substrate, and performing the subsequent semiconductor process such as etching, exposing, development and coating steps. However, it's difficult to measure the optoelectronic properties, e.g. current-voltage characteristics and spectral characteristics, of the resulted epi wafer in the fabricating processes of the thin film LED, but only can measure the thin film LED in almost the last fabricating process such as the packaging step.

[0003] In above processes, since the semiconductor processes in performed on a whole wafer, thereby only 50% of the chips on the resulted epi wafer can reach the desired optoelectronic properties such as current-voltage characteristics and spectral characteristics. However, the carrier substrate is still bonded to the whole wafer. That is, even if another 50% of the chips which can't reach the desired requirements (such as having defects or a poor luminescence efficiency) on the wafer is known, these chips are still bonded to the respective packaging elements and performing the subsequent processes. Accordingly, the carrier substrate is wasted, and consumes time and increases the cost for the subsequent processes. Unfortunately, while the thin film LEDs are in mass production, the specification and the trade deadline are forced by clients. Therefore, how to improve the product yields and reduce the cost are important issues for the manufacturers.

[0004] Light emitting diodes (LEDs) have high brightness, low volume, low power consumption and long operating lifespan and as such, are used in a variety of display products. The luminescent principle of LEDs is as follows. A voltage is applied to a diode to drive an electron and a hole combination. The combination releases light from the diode. A conventional thin GaN LED product is manufactured by bonding an epi wafer to a carrier (such as a submount substrate or a package substrate).

[0005] FIG. 1 is a sectional view illustrating a conventional LED package with a vertical-structure epi wafer mounted therein. Referring to FIG. 1, the LED package 210 includes a package substrate 212 and a vertical-structure epi wafer 214 mounted on an electrode 216 of the package substrate 212. The epi wafer 214 includes a substrate 218, semiconductor layers 220 sequentially stacked on the substrate 218 and an electrode 222 such as a bonding metal.

[0006] There are several problems associated with the conventional package structure described above. First, poor alignment may be a significant problem that can result in the rejection of an entire connector assembly. Second, the thickness of the electrode 222 of the epi wafer 214 must be precise, since an electrode 222 that is too thin, results in poor connection and adhesion. Further, in order for bonding, heat and pressure are applied to bond the epi wafer 214 to the substrate 212. At this time, due to the pressure, the bonding material of an electrode 222 that is too thick, will protrude laterally and may cause an short circuit 23 of the semiconductor layers 220, as FIG. 2 shows. Such a short circuit may cause the LED chip to lose its functional abilities. Third, due to the high temperature required for bonding, the LED package 210 suffers from residual stress after cooling. Fourth, due to dimensional restrictions of laser beams, cracks may be observed after removal of the whole substrate 218 by laser lift-off processes.

[0007] In other aspect, conventional method for manufacturing a thin film light emitting diode (LED) would bond a complete wafer, which will be diced to form a plurality of LEDs afterwards, on a substrate by heating the substrate and the wafer thereon. If the wafer has a non-uniform surface, the wafer is prone to fracture on the process of bonding. Besides, the conventional bonding temperature is about 400°C and is regarded as a high temperature that would influence the quality of the wafer. Therefore, after the substrate and the wafer are bonded together and cooled down to a room temperature, a non-uniform stress distribution would occur to the wafer, weakening the structure of the wafer, and further affecting the sequential manufacturing process of LEDs.

[0008] At present, a conventional thin film LED normally has the problem of limited light emitting efficiency due to the deposition of metal electrode. For example, the metal electrode is directly disposed on the light emitting surface of the thin film LED. Thus, for a 12-mil LED, one-third light emitting area is usually lost due to the metal electrode. And for a 40-mil LED, one-ninth light emitting area is wasted. Besides, the electric current on the connection portion between the LED and the metal electrode is normally the highest, and is likely to cause energy loss.

[0009] The quality of light emitting device, such as the light-emitting diode (LED), is also very dependent on the luminance uniformity. After the LED dies have been fabricated in accomplishment, many LED dies are attached on a carrier or substrate for packaging. In packaging process, the florescent material or generally called wavelength conversion material is coated over the LED dies to produce the light, such as white light.

[0010] In actual mass production, the process of die attachment process usually cannot be ideally controlled. As a result, the LED dies are usually not aligned to the ideal position. For example, some LED dies may be twisted by a certain angle and the location may be shifted from a designed location. Further, a mask layer for filling the florescent material on the LED die may also have fabrication errors and/or be in misalignment, for example. As a result, the florescent material would be non-uniformly coated over the LED dies, causing difference between the LED dies resulting in different luminosity in use. In addition, each LED die itself may further have non-uniform luminance in different illuminating angles. When the LED dies are composed into a light source, the luminance of the light source would be non-uniform as well. Thus, to improve the uniformity of luminance of LED units in fabrication is an issue to be further developed.
Therefore, it is desirable to devise a novel light emitting diode package that improves upon the aforementioned problems.

SUMMARY

According to an embodiment, a method for forming a light emitting diode, comprising: providing a substrate having a first semiconductor layer, a light emitting layer and a second semiconductor layer formed thereon sequentially; performing a patterning process to the first semiconductor layer, the light emitting layer and the second semiconductor layer to define a plurality of protruded portions and a plurality of depressed portions, wherein a remaining portion of the first semiconductor layer covers the substrate in the depressed portions; forming a plurality of first electrodes on the first semiconductor layer in the depressed portions; forming a plurality of second electrodes on the second semiconductor layer in the protruded portions; cutting the substrate along a scribe line located on the depressed portion, for separating a plurality of light emitting diode chips, wherein the light emitting diode chip has a bonding layer and a remained substrate portion, wherein the bonding layer has a plurality of voids, or a minimum horizontal distant between a surrounding boundary of the light emitting diode chip and the bonding layer is larger than 0; bonding the light emitting diode chip with a carrier substrate via the bonding layer, forming a surrounding layer on the carrier substrate to surround the light emitting diode; removing the remained substrate portion to form a cavity; and filling a wavelength conversion layer into the cavity.

The disclosure provides a light emitting diode structure, comprising: a substrate; a first semiconductor layer disposed on the substrate, wherein the first semiconductor layer comprises a depressed portion and a protruded portion; a light emitting layer disposed on the protruded portion of the first semiconductor layer; a second semiconductor layer disposed on the light emitting layer; a first electrode disposed on the depressed portion of the first semiconductor layer; and a second electrode disposed on the second semiconductor layer, wherein the contacting area between the second electrode and the second semiconductor layer occupies at least about 20% of the surface area of the second semiconductor layer.

In another embodiment, a light emitting diode chip, comprising: a substrate having a boundary; a first semiconductor layer disposed on the substrate; a light emitting layer disposed on the first semiconductor layer; and a second semiconductor layer disposed on the light emitting layer, wherein the light emitting diode chip comprises only one polarity electrode disposed on the second semiconductor layer, and the electrode and the boundary has a minimum horizontal distance therebetween of at least about 10 μm.

In yet another embodiment, a method for fabricating the light emitting diode, comprising: providing a substrate having a first semiconductor layer, a light emitting layer and a second semiconductor layer formed thereon sequentially; performing a patterning process to the first semiconductor layer, the light emitting layer and the second semiconductor layer to define a plurality of protruded areas and a plurality of depressed areas, wherein a remaining portion of the first semiconductor layer covers the substrate in the depressed areas; forming a plurality of first electrodes on the first semiconductor layer in the depressed areas; and forming a plurality of second electrodes on the second semiconductor layer in the protruded areas.

The disclosure provides a light emitting diode chip, including: a substrate having a surrounding boundary; a first semiconductor layer, a light emitting layer, and a second semiconductor layer subsequently disposed on the substrate; and electrode islands disposed on the second semiconductor layer.

In another embodiment, a light emitting diode package structure including: a substrate having a surrounding boundary; a carrier substrate; and a bonding layer for bonding the light emitting diode chip with the carrier substrate, wherein the bonding layer has a plurality of voids, wherein the light emitting diode includes: a substrate; and a first semiconductor layer, a light emitting layer, and a second semiconductor layer subsequently disposed on the substrate.

The disclosure achieves the above-identified object by providing a LED structure that includes a submount, a stacked structure, an electrode, an isolation layer and a conductive thin film layer. The submount, has a first surface and a second surface opposite the first surface. The stacked structure has a first semiconductor layer, an active layer and a second semiconductor layer that are laminated on the first surface. The electrode is disposed apart from the stacked structure on the first surface. The isolation layer is disposed on the first surface and surrounds the stacked structure as well as covers the lateral sides of the active layer. The conductive thin film layer connects the electrode to the stacked structure.

The disclosure achieves the above-identified object also by providing a LED packaging structure that includes a packaging substrate, at least one stacked structure, at least one first electrode, at least one second electrode, an isolation layer, at least one conductive thin film layer, and a transparent sealant. The at least one stacked structure has a first semiconductor layer, an active layer and a second semiconductor layer that are laminated on the surface of the packaging structure. The at least one first electrode is disposed apart from the at least one stacked structure on the surface. The at least one second electrode is disposed on the packaging substrate and electrically connected to the at least one stacked structure. The isolation layer is disposed on the surface and surrounds the at least one stacked structure as well as covers the lateral sides of the active layer. The at least one conductive thin film layer connects the at least one first electrode to the at least one stacked structure, and covers the at least one stacked structure. The transparent sealant covers the at least one conductive thin film layer.

The disclosure achieves the above-identified object further by providing a method of forming a LED structure. The method includes the steps stated below. An electrostatic discharge (ESD) protection element is formed on a submount, wherein the ESD protection element is disposed along the edges of a first surface on the submount and is embedded in the submount. Then, a first electrode is formed on the ESD protection element. Next, a stacked structure is provided and bonded on the first surface of the submount, wherein the stacked structure is located apart from the first electrode. Then, an isolation layer is formed on the first electrode, the stacked structure and the space between the first electrode and the stacked structure. Next, part of the isolation layer over the first electrode and part of the isolation layer over the stacked structure are removed to expose the first electrode and the stacked structure. Then, a conductive thin film layer is formed on the first electrode and the stacked structure for electrically connecting the first electrode to the stacked structure. Next, a
second electrode is formed on a second surface of the submount opposite the first surface. Then, the submount is diced to form a LED structure.

[0022] The disclosure achieves the above-identified object further by providing a method of forming a LED structure. The method comprises the steps of: forming a first electrode on a submount, wherein the first electrode is disposed along the edges of a first surface on the submount; providing a stacked structure and bonding the stacked structure on the first surface of the submount, wherein the stacked structure is located apart from the first electrode; forming an isolation layer on the first electrode; the stacked structure and the space between the first electrode and the stacked structure; removing part of the isolation layer over the first electrode and part of the isolation layer over the stacked structure to expose the first electrode and the stacked structure; forming a conductive thin film layer on the first electrode and the stacked structure for electrically connecting the first electrode to the stacked structure; forming a second electrode on a second surface of the submount opposite the first surface; and dicing the submount to form a LED structure.

[0023] The disclosure provides a light emitting diode structure comprizing: a substrate with a light emitting semiconductor stacked layer formed thereon; a surrounding layer located on the substrate to surround the light emitting semiconductor stacked layer, constituting a cavity; and a wavelength conversion layer filled into the cavity.

[0024] In another embodiment, a method for fabricating the light emitting diode structure comprizing: providing a light emitting diode having a bonding material, a stacked layer and a substrate; bonding the light emitting diode on a carrier via the bonding material; forming a surrounding layer to surround the light emitting diode; removing the substrate to form a cavity; and filling a wavelength conversion layer into the cavity.

[0025] In yet another embodiment, a method for fabricating the light emitting diode structure comprizing: bonding a light emitting diode via a bonding material; forming a removable cap on a top portion of the light emitting diode; forming a surrounding layer to surround the light emitting diode; removing the removable cap to form a cavity; and filling a wavelength conversion layer into the cavity.

[0026] A detailed description is given in the following embodiments with reference to the accompanying drawings.

**BRIEF DESCRIPTION OF THE DRAWINGS**

[0027] The present disclosure can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

[0028] FIG. 1 is a cross-section of a conventional LED package structure.

[0029] FIG. 2 is a cross-section of a conventional LED package structure with a short circuit.

[0030] FIG. 3 is a cross-section of a light emitting diode according to an embodiment.

[0031] FIGS. 4 to 10 and 12 to 13 are cross-sections of light emitting diodes according to embodiments.

[0032] FIGS. 11A to 11C are cross-sections of light emitting diodes according to embodiments.

[0033] FIG. 14 is a top view of the light emitting diode of FIG. 3, and FIG. 3 is the cross-section along the section 1-1' in FIG. 14.

[0034] FIGS. 15 to 17 are top views of the light emitting diodes according to embodiments.

[0035] FIGS. 18A to 20A are top views showing the process for fabricating the light emitting diode of FIG. 1.

[0036] FIGS. 18B to 20B are cross-sections respectively corresponding to FIGS. 18A-20A.

[0037] FIGS. 21A-26A are top views showing the process for cutting the light emitting diode.

[0038] FIGS. 21B-26B are cross-sections respectively corresponding to FIGS. 21A-26A.

[0039] FIGS. 27A-27C are cross-sections of a light emitting diode according to an embodiment, which are respectively obtained via the cutting process shown in FIG. 21A, FIG. 11B, and FIG. 11C.

[0040] FIGS. 28 to 37 are cross-sections of the light emitting diode chips according to other embodiments.

[0041] FIG. 38 is a cross-section of a light emitting diode according to an embodiment, which is obtained via the cutting process shown in FIG. 23A.

[0042] FIGS. 39 and 40 are cross-sections of light emitting diodes according to some embodiments.

[0043] FIGS. 41 to 46 are cross-sections of light emitting diode package structures according to some embodiments.

[0044] FIGS. 47 to 62 are cross-sections of light emitting diode chips according to embodiments.

[0045] FIG. 63 is a cross-section of a nozzle used to chuck the diode chip by suction and then to put the diode chip on a carrier substrate.

[0046] FIGS. 64 and 65 are schematic diagrams of the adsorptive surface of the nozzle shown in FIG. 63.

[0047] FIG. 66A is a cross-section showing a method for bonding a light emitting diode chip to a carrier substrate according to an embodiment.

[0048] FIG. 66B is a cross-section showing a light emitting diode package structure fabricated by the method shown in FIG. 66A.

[0049] FIGS. 67A and 67B are cross-sections showing a light emitting diode package structure according to an embodiment.

[0050] FIG. 68A is a cross-section showing a method for bonding a light emitting diode chip to a carrier substrate according to another embodiment.

[0051] FIG. 68B is a cross-section showing a light emitting diode package structure fabricated by the method shown in FIG. 68A.

[0052] FIGS. 69 to 72 are cross-sections showing a method for bonding a light emitting diode chip to a carrier substrate according to yet another embodiment.

[0053] FIGS. 73 to 76 are cross-sections showing a method for fabricating the package structures according to embodiments.

[0054] FIGS. 77 to 79 are cross-sections showing another method for fabricating the package structures according to embodiments.

[0055] FIG. 80 is a photograph of a conventional LED package structure with wire light shielding.

[0056] FIGS. 81 to 85B are cross-sections of light emitting diode package structures according to other embodiments.

[0057] FIG. 86 is a diagram showing a light emitting diode (LED) structure according to a preferred embodiment.

[0058] FIG. 87 is a diagram showing the top view of the LED structure in FIG. 86.

[0059] FIG. 88 is a diagram showing the c-c' cross-sectional view of the LED structure in FIG. 86.
[0060] FIG. 89 is a circuit diagram showing the electrical connection of the stacked structure, the submount and the ESD protection element.

[0061] FIG. 90 is a flowchart showing a method of forming a LED structure according to a preferred embodiment.

[0062] FIG. 91 is a flowchart showing a method of forming another LED structure according to a preferred embodiment.

[0063] FIGS. 92A to 92G are diagrams sequentially showing the formation of a LED structure in accordance with the steps of the method in FIG. 90.

[0064] FIG. 93 is a diagram showing a conductive thin film layer with a plurality of openings.

[0065] FIGS. 94 and 95 are diagrams each showing a conductive thin film layer with a light extracting feature.

[0066] FIG. 96 is a diagram showing a LED structure filled with phosphor.

[0067] FIG. 97A is a diagram showing a LED structure having an electrode not fully surrounding its sacked structure.

[0068] FIG. 97B is a diagram showing the top view of the LED structure in FIG. 97A.

[0069] FIGS. 98A and 98B are diagrams showing a LED packaging structure according to a preferred embodiment.

[0070] FIG. 98C is a top view of the LED packaging structure in FIG. 98A.

[0071] FIGS. 98D and 98E are cross-sectional views of the LED packaging structure in FIG. 98C along lines A-A' and B-B' respectively.

[0072] FIG. 99 is a diagram showing a LED packaging structure having a plurality of light emitting areas.

[0073] FIGS. 100A and 100B are diagrams each showing an auxiliary electrode disposed on the conductive thin film layer, and

[0074] FIGS. 101A and 101B are diagrams each showing an interface layer having a plurality of partitions.

[0075] FIG. 102 is a cross-section schematically illustrating a structure of LED die, according to an embodiment.

[0076] FIGS. 103A to 103F are top views schematically illustrating several configurations of the LED dies attached on the carrier, according to embodiments.

[0077] FIGS. 104A to 104D are cross-sections schematically illustrating packaging processes to form the LED packaging unit, according to an embodiment.

[0078] FIGS. 105A to 105D are cross-sections schematically illustrating packaging processes to form the LED packaging unit, according to an embodiment.

[0079] FIGS. 106-108 are cross-sections schematically illustrating the LED package structures, according to various embodiments.

[0080] FIGS. 109A-109B are cross-sections schematically illustrating a fabrication process to form the LED package structure, according to another embodiment.

[0081] FIGS. 110 and 111 are cross-sections schematically illustrating LED package structures, according to embodiments.

[0082] FIGS. 112A and 112B are cross-sections schematically illustrating another LED package structure, according to an embodiment.

[0083] FIGS. 113A and 113B are drawings schematically illustrating phenomena at the peripheral portion 300 in FIG. 112A.

[0084] FIG. 114 is a cross-section layer schematically illustrating a structure of the LED package according to another embodiment.

[0085] FIGS. 115A to 115F are cross-sections schematically illustrating a fabrication process for a LED package, according to another embodiment.

[0086] FIGS. 116A to 116H are cross-sections schematically illustrating a fabrication process.

[0087] FIGS. 117A to 117B are cross-sections schematically illustrating another packaging process based on flip-chip package, according to an embodiment.

[0088] FIGS. 118A to 118B are cross-sections schematically illustrating another packaging process based on flip-chip package, according to an embodiment.

[0089] FIG. 119 is a cross-section schematically illustrating another embodiment of the LED package.

[0090] FIGS. 120A-120B are cross-sections schematically illustrating another packaging process based on flip-chip package, according to an embodiment.

[0091] FIGS. 121A to 121B are cross-sections schematically illustrating another packaging process based on flip-chip package, according to an embodiment.

[0092] FIGS. 122A to 122J are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0093] FIGS. 123A to 123F are cross-sections schematically illustrating the same structure in FIGS. 122A to 122J but in different fabrication processes, according to an embodiment.

[0094] FIGS. 124A to 124C are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0095] FIGS. 125A to 125C are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0096] FIGS. 126A and 126B are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0097] FIGS. 127A to 127D are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0098] FIGS. 128A to 128C are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0099] FIGS. 129A to 129D are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0100] FIGS. 130A to 130D are cross-sections schematically illustrating a fabrication process for a structure, according to an embodiment.

[0101] FIGS. 131A to 131D are top views schematically illustrating a fabrication process for a structure, according to an embodiment.

[0102] FIG. 132 is the cross-section along the section A-A' in FIG. 131A.

[0103] FIGS. 133A to 133D are top views schematically illustrating a fabrication process for a structure, according to an embodiment.

[0104] FIG. 134 is the cross-section along the section B-B' in FIG. 133A.

DETAILED DESCRIPTION

[0105] According to an embodiment, the emitting diode structure 10 may have a structure as illustrated in FIG. 3. The emitting diode structure 10 includes a substrate 12 and a first semiconductor layer 14 disposed thereon, wherein the first semiconductor layer 14 includes a depressed portion 11 and a protruded portion 13. The depressed portion 11 and the
protruded portion 13 may have a height difference H. A light emitting layer 16 is disposed on the protruded portion 13 of the first semiconductor layer 14. A second semiconductor layer 18 is disposed on the light emitting layer 16. A first electrode 20 is disposed on the depressed portion 11 of the first semiconductor layer 14. A second electrode 22 is disposed on the second semiconductor layer 18, wherein the second electrode 22 may have a reflectivity index larger than 70% to the dominant wavelength of the vertical incident light emitted by the light emitting layer. The substrate 12 may be any substrates suitable for the growth of the LEDs semiconductor layers, for example, the substrate 12 may be formed of aluminum oxide substrate (sapphire substrate), silicon carbide substrate, or gallium arsenic substrate. The substrate may have a thickness larger than 150 μm, or larger than 200 μm (if the substrate is the silicon carbide substrate, or the gallium arsenic substrate). The emitting layer 16 may have a multiple quantum wells (MQW) structure. The emitting layer 16 may be a semiconductor layer formed of a semiconductor material selected from the groups consisting of III-V group elements, II-V group elements, IV group elements, IV-IV group elements or combinations thereof, such as AlN, GaN, AlGaN, InGaN, AlInGaN, GaP, GaAsP, AlGaInP or AlGaAs. The first semiconductor layer 16 and the second semiconductor layer 18 are a N-type epitaxial layer and a P-type epitaxial layer, respectively. Note that the types of the epitaxial layers can be exchanged, but not to limit the present disclosure. The first semiconductor layer 16 and the second semiconductor layer 18 also may be formed of a semiconductor material selected from the groups consisting of III-V group elements, II-V group elements, IV group elements, IV-IV group elements or combinations thereof. For example, the first semiconductor layer 14 is N-type GaN semiconductor when the second semiconductor layer 16 is P-type GaN semiconductor, vice versa, the first semiconductor layer 14 is P-type GaN semiconductor when the second semiconductor layer 16 is N-type GaN semiconductor. The emitting layer also may be GaN semiconductor. The first electrode 22 may include an Ohmic contact material such as Pd, Pt, Ni, Au, Ag or combinations thereof, a diffusion layer, a bonding metal layer, a transparent conductive film such as indium tin oxide (ITO), cadmium tin oxide (CTO), antimony tin oxide (ATO), zinc oxide or zinc oxide, a reflective layer, or combinations thereof. The first electrode 20 may have a thickness larger than 2000 Å, or larger than 5000 Å, or further larger than 1 μm. Additionally, the first electrode 20 and the second electrode 22 may have a same Ohmic contact material. For example, the second electrode 22 may have a reflective layer 21 and a bonding metal layer 23 (thickness larger than 5000 Å or 1 μm), as shown in FIG. 4. The reflective layer 21 may have an area larger than the bonding metal layer 23, as shown in FIG. 5. In embodiments according to the present disclosure, the first electrode 20 and the second electrode 22 may have any suitable shapes or any shapes known in the art, such as a polygon, a circle or combinations thereof, however, for the sake of simplifying the figures, merely a rectangular shape is illustrated.

[0106] In the emitting diode structure 10 according to an embodiment, the first electrode 20 and the second electrode 22 are formed on the first semiconductor layer 14 and the second semiconductor layer 18, respectively. Therefore, the current-voltage characteristics and spectral characteristics of the stack structure (a semi-finished product of the LED chip) of the first semiconductor layer 14, the emitting layer 16 and the second semiconductor layer 18 can be measured in front processes (while fabricating the epi wafer), by measuring the first electrode 20 and the second electrode 22. Thus, the defectives and the chips out of the specification may be filtered.

[0107] In the emitting diode structure 10 according to another embodiment, the second electrode 22 may be only disposed on a portion of the second semiconductor layer 18 and expose a portion of an upper surface of the second semiconductor layer 18, as shown in FIG. 6. It should be noted that the contacting area between the second electrode 22 and the second semiconductor layer 18 occupies about 20% of the area (the area of the upper surface) of the second semiconductor layer 18 or more (e.g., 30%, 50% or more).

Referring to FIG. 7, the emitting diode structure further includes a passivation layer 24 disposed on the second semiconductor layer 18 and covers the exposed upper surface of the second semiconductor layer 18, wherein the passivation layer may be formed of a dielectric material or a Schottky contact material such as silicon oxide, silicon nitride, aluminum nitride, titanium oxide, aluminum oxide or combinations thereof. According to other embodiments, the passivation 24 may be further extended to cover the sidewalls of the second semiconductor layer 18, the sidewalls of the emitting layer 16 and the sidewalls of the protruded portion 13 of the first semiconductor layer 14, as shown in FIG. 8 and FIG. 9, to prevent from these layers being damaged in the subsequent processes. Furthermore, the passivation layer 24 may be further extended to cover the depressed portion 11 of the first semiconductor layer 14, as shown in FIG. 10 and FIG. 11. Further, in the patterning process for forming the depressed portion 11 and the protruded portion 13, the first semiconductor layer 14 between the depressed portion 11 and the protruded portion 13 can be removed, and thus the depressed portion 11 does not directly contact to the protruded portion 13, as shown in FIG. 11B and FIG. 11C. Since the passivation layer 24 is an insulating film, the second electrode 24 may be further extended onto the passivation layer, as shown in FIG. 12.

[0108] In addition, a patterned passivation layer 24 may be interposed between the first electrode 18 and the second electrode 22, and the second semiconductor layer 18 which is not coated by the patterned passivation layer 24 directly contacts with the second electrode 22 for forming a current-improved structure, as shown in FIG. 13.

[0109] Please refer to FIG. 14, illustrated is a top view of the emitting diode structure 10 shown in FIG. 3 (FIG. 3 is a cross-view along the section 1-1’ in FIG. 14). As shown in FIG. 14, the first electrode 20 is disposed on the first semiconductor layer 14. Therefore, only the second electrode 22 on the stack structure 25 (a semi-finished product of the LED chip) and an electrical difference with the adjacent first electrode 20 are provided, the current-voltage characteristics and spectral characteristics of the stack structure 25 can be measured. Thus, the defectives and the chips out of the specification may be filtered. In addition, a plurality of the first electrodes 20 disposed on the first semiconductor layer 14 may be electrically connected to each other through a conductive circuitry 27, and a line structure or a network structure is thus formed for convenience to introduce continuous chips analysis, as shown in FIG. 15 and FIG. 16. Please refer to FIG. 17, except to a polygon, the above described stack structure (a semi-finished product of the LED chip) also may be a patterned stack structures, for example, formed by the multiple elements.
In the following, a method for forming the emitting diode structure 10 according to the embodiment shown in FIG. 1 will be detailed described with references made to the accompanying drawings.

First, please refer to FIG. 18A and FIG. 18B (a cross view of a portion of FIG. 18A), a substrate 12 is provided, and a first semiconductor layer 14, a light emitting layer 16 and a second semiconductor layer 18 are formed on the substrate 12 in order, wherein the forming methods of the first semiconductor layer 14, the light emitting layer 16 and a second semiconductor layer 18 are not limited, and any suitable methods in the art can be used, for example, chemical vapor deposition (CVD), metal organic chemical vapor deposition (MOCVD), plasma enhanced chemical vapor deposition (PECVD) or sputter.

Next, please refer to FIG. 19A and FIG. 19B (a cross view of a portion of FIG. 19A), a patterning process is performed on the first semiconductor layer 14, the light emitting layer 16 and a second semiconductor layer 18, and defines to a plurality of depressed portions 30 and a plurality of protruded portions 32. After the patterning process, only a depressed portion 11 of the first semiconductor layer 14A is remained on the epi substrate 12 in the depressed portion 30. A protruded portion 13, the light emitting layer 16 and the second semiconductor layer 18A are remained on the epi substrate 12 in the protruded portion 32. The patterning process may be a lithography process.

Finally, please refer to FIG. 20A and FIG. 20B (a cross view of a portion of FIG. 20A), a plurality of first electrodes 20 are formed on the first semiconductor layer 14A in the depressed portion 30, and a plurality of second electrodes 22 are formed on the semiconductor layer 18A in the protruded portion 32.

Furthermore, according to other embodiments, the forming method of the emitting diode structure further includes forming a patterned passivation layer on the second semiconductor layer before forming the second electrode. The patterned passivation layer may be further extended to the sidewalls of the second semiconductor layer, the sidewalls of the light emitting layer and the sidewalls of the protruded portion of the first semiconductor layer. Alternatively, the patterned passivation layer may be further extended to the first semiconductor layer in the depressed portion. Furthermore, the second electrode is formed on a portion of the second semiconductor layer and exposes a portion of the upper surface of the second semiconductor layer. The passivation layer may be formed on the exposed surface of the second semiconductor layer.

After the processes of the emitting diode structure 10 are finished, the current-voltage characteristics and spectral characteristics of a structure of 25 (a semi-finished product of the LED chip) may be measured by measuring the first electrode 20 and the second electrode 22. The chips which can achieve the desired requirements are marked.

Please refer to FIG. 21A and FIG. 21B (a cross view of a portion of FIG. 21A), after the measurement, a scribe process is performed to the emitting diode structure 10. The process includes cutting the substrate 12 along a scribe line, thereby forming a plurality of emitting chips. Because the chips can achieve the desired requirements have been marked, these marked chips can be selected to perform the subsequent processes. As shown in FIG. 21A and FIG. 21B, the scribe line 50 may overlie the first electrode 22 in the depressed portion 30, wherein the scribe line can have a width of between 10 nm and 1 mm. In addition, please refer to FIG. 22A and FIG. 22B (a cross view of a portion of FIG. 22A), the scribe line 50 also may overlie the whole depressed portion 30. Furthermore, please refer to FIG. 23A and FIG. 23B (a cross view of a portion of FIG. 23A), double scribe lines 50 also can be used in one depressed portion 30. This method may reduce cracks in the depressed portion 30 after the laser lift-off. According to another embodiment, in the embodiment illustrated in FIG. 6, the scribe line 50 may further have a range to a portion of the protruded portion 32 adjacent to the depressed portion 30, as shown in FIG. 24A and FIG. 24B (a cross view of a portion of FIG. 24A). Note that the scribe line 50 should have a range away from the second electrode 22, for preventing from damaging the chips.

On the other hand, according to other embodiments, for example, referring to FIG. 25A and FIG. 26A, the second electrode 22 for measuring current-voltage characteristics and spectral characteristics of the stacked structure 25 (a semi-finished product of the LED chips) may be not formed away from the scribe line, i.e. predetermined area for the semi-finished product of the LED chips, for example, referring to FIG. 25B and FIG. 26B. As such, the distance between the chips may be reduced and the scribe lines are narrower. Thus, more chips may be formed on each substrate 12. Furthermore, a flip-chip structure may be formed on the second electrode 22 for increasing the area utilization of the epi wafer. According to other embodiments, after measuring, a passivation layer 24 can be formed on the substrate 12, and then a planarization process (such as chemical mechanical planarization) can be subjected to the passivation layer 24 to expose the second electrode 22, referring to FIGS. 127A and 127B. Next, the substrate is cut along the scribe line 50, referring to FIG. 127C. Finally, the passivation layer 24 can be removed to obtain light emitting diode chips, referring to FIG. 127D. According to another embodiment, after forming the passivation layer 24, the passivation layer located on the scribe line 50 can be removed first, referring to FIGS. 128A and 128B. Therefore, in the cutting process, there is no passivation layer which is contacted to the cutting machine, obtaining the light emitting diode chips, referring to FIG. 128C.

Please refer to FIG. 27A, illustrated is a cross view of a LED chip 100 by using the cutting method described in FIG. 21B. The LED chip 100 includes a substrate 12 having a boundary 80. A first semiconductor layer 14 having a protruded portion 13 and a depressed portion 11 is formed on the substrate 12. A light emitting layer 16 is formed on the protruded portion 13 of the first semiconductor layer 14. A second semiconductor layer 18 is formed on the light emitting layer 16. It should be noted that the resulted LED chips may have only one polarity electrode 22 (i.e. a positive or negative electrode), but have none of a second polarity electrode. The electrode 22 may be disposed on the second semiconductor layer 18. A minimum horizontal space W between the electrode 22 and the boundary 80 of the substrate 12 may be about 10 μm or more, or preferably, about 20 μm or more. Please refer to FIGS. 27B and 27C, illustrated are cross views of a LED chip 100 by using the cutting method described in FIGS. 11B and 11C, wherein the scribe line 50 is disposed above the first electrode 20 remaining a part of the first electrode 20 and the depressed portion 11 disposed on the substrate 12. Furthermore, according to another embodiment, the electrode 22 of the LED chip 100 may be disposed on a portion of the second semiconductor layer 18 and exposes a portion of the upper surface 19 of the second semiconductor layer 18, as
shown in FIG. 28. The contacting area between the second electrode 22 and the second semiconductor layer 18 may occupy about 20% of the surface area (upper surface) of the second semiconductor layer 18, or preferably, about 50% or more. In addition, the LED chip 100 may further include a passivation layer formed on the exposed upper surface 19 of the second semiconductor layer 18, as shown in FIG. 29. The passivation layer 24 may be further extended to sidewalls of the second semiconductor layer 18, the sidewalls of the emitting layer 16 and the sidewalls of the protruded portion 13 of the first semiconductor layer 14, as shown in FIG. 30. Furthermore, the passivation layer 24 may be further extended to the upper surface of the depressed portion 11 of the first semiconductor layer 14, as shown in FIG. 31. Additionally, the second electrode 22 of the LED chip 100 may include a reflecting layer 21 and a bonding metal layer 23, wherein the reflecting layer 21 is spaced apart with the bonding metal layer 23. The bonding metal layer 23 may have an area less than that of the upper surface 19 of the second semiconductor layer 18 and covers a portion of the passivation layer 24 and the reflecting layer 21, as shown in FIG. 32.

According to an embodiment, the electrode 22 of the LED chip 100 may also be formed on the passivation layer 24, but the electrode 22 may still have a portion directly contacting with the second semiconductor layer 18, as shown in FIG. 33. The passivation layer 24 may be also a passivation layer and disposed between the second semiconductor layer 18 and the electrode 22. A portion of the second semiconductor layer 18 which is not covered by the passivated passivation layer 24 directly contacts the electrode 22, and a current-improved structure is thus formed, as shown in FIG. 34. In this embodiment, also the passivation layer 24 may be extended to the sidewalls of the second semiconductor layer 18, the sidewalls of the emitting layer 16 and the sidewalls of the protruded portion 13 of the first semiconductor layer 14, as shown in FIG. 35. Furthermore, the passivation layer 24 may be further extended to the upper surface of the depressed portion 11 of the first semiconductor layer 14, as shown in FIG. 36. In other embodiments, the electrode 22 may be extended onto the passivation layer 24 and separated with emitting layer 16 and the first semiconductor layer 14 by the electrode 22, as shown in FIG. 37.

Please refer to FIG. 38, illustrated is a cross view of the LED chip 100 by using the cutting method described in FIG. 23B. The LED chip 100 includes a substrate 12 having a boundary 80. A first semiconductor layer 14 is formed on the substrate 12. A light emitting layer 16 is formed on the first semiconductor layer 14. A second semiconductor layer 18 is formed on the light emitting layer 16. The LED chip may have only a electrode 22 (i.e. a positive or negative electrode), but have none of a second electrode. The electrode 22 may be formed on the semiconductor layer 18 and exposes the upper surface 19 of the semiconductor layer 18. Note that a minimum horizontal space W between the electrode 22 and the boundary 80 of the substrate 12 may be about 10 µm or more, or preferably, about 20 µm or more. Furthermore, according to an embodiment, referring to FIG. 39, a passivation layer 24 is formed on the exposed upper surface 19 of the second semiconductor layer 18. In addition, according to another embodiment, referring to FIG. 40, the LED chip 100 may have tapered sidewalks 111 which have a narrower portion along the substrate 12 than the tip portion.

In other embodiments, the light emitting diode chip 100 can be further bounded with a carrier substrate, such as a submount 110 (having a contact pad 123), obtaining a light emitting diode package structure 200, referring to FIG. 41, and FIG. 42. Further, the submount 110, except to the contact pad 123, can further include a contact pad 124 to electrically connect to the light emitting diode chip 100, referring to FIGS. 43 and 44. Moreover, the light emitting diode chip 100 can be bonded with a package substrate 120 (having circuits 125), obtaining a light emitting diode package structure 200, referring to FIG. 45 and FIG. 46. The obtained light emitting diode package structure 200 can be further subjected to subsequently fabricating process, such as laser lift-off, surface roughness, electrode formation, contact pad formation, fluorescent powder coating, wire formation, cutting, or classification.

In order to solve the aforementioned problems, the disclosure provides a light emitting diode chip and a light emitting diode package structure employing the same, having increased production yield and reduced production costs.

The following description is of the best-contemplated mode of carrying out the disclosure. This description is made for the purpose of illustrating the general principles and should not be taken in a limiting sense. The scope is best determined by reference to the appended claims.

According to yet other embodiments, referring to FIGS. 129A to 129D, after bonding the light emitting diode chip 100 on a submount, a passivation layer 132 can be formed on the substrate to serve as a underfill layer. Next, the substrate of the light emitting diode chip can be removed by LLO (laser lift off) process or wet etching process. Next, a dry etching 137, substituting for conventional polishing process, can be performed to remove the un-doped portion or high doped portion of the light emitting diode chip. Referring to FIGS. 130A to 130D, according to yet other embodiments, the passivation layer 132 can be formed on the whole substrate and can be removed after formation of the light emitting diode package.

According to an embodiment, referring to FIGS. 47 and 48, the embodiment provides a light emitting diode chip 400 including a substrate 402 with a surrounding boundary 401. A first semiconductor layer 404 is disposed on a top surface 403 of the substrate 402. A light emitting layer 406 is disposed on the first semiconductor layer 404, and a second semiconductor layer 408 is disposed on the light emitting layer 406. It should be noted, that the light emitting diode chip 400 includes electrode islands 410 disposed on the top surface 405 of the second semiconductor layer 408, wherein any two adjacent electrode islands 410 can have a minimum horizontal distant W1 equal to or larger than 1 µm. Further, the total area of the top surface 407 of all electrode islands 410 and the area of a top surface 403 of the substrate 402 is equal to or less than 95%, and/or the total area of the top surface 407 of all electrode islands 410 and the area of a top surface 405 of the second semiconductor layer 408 is equal to or less than 95%.

The substrate 402 can be any suitable substrates for growing epitaxial layers thereon, such as an aluminium oxide substrate (sapphire substrate), a silicon Carbide substrate, or a gallium arsenide substrate. The substrate 402 can have a thickness of more than 150 µm. If the substrate 402 is a silicon Carbide substrate or a gallium arsenide substrate, the thickness of the substrate can be more than 600 µm. The light emitting layer 406 can be a semiconductor material layer and have a multiple quantum well structure, selected from a group of group III-V semiconductor compounds, group II-VI semiconductor compounds, group IV semiconductor compounds,
group IV-IV semiconductor compounds, and combinations thereof, such as AlN, GaN, AlGaN, InGaN, AlInGaN, GaP, GaAsP, GaNP, AlGaNP, or AlGaAs. The first semiconductor layer 404 and the second semiconductor layer 408 can be an N-type semiconductor layer and a P-type semiconductor layer, respectively, or alternatively a P-type semiconductor layer and an N-type semiconductor layer, respectively. The first semiconductor layer 404 and the second semiconductor layer 408 can be group II-VI semiconductor compounds, group II-V semiconductor compounds, group IV semiconductor compounds, group IV-V semiconductor compounds, and combinations thereof. For example, if the first semiconductor layer 14 is an N-type GaN semiconductor layer, the second semiconductor layer 408 can be a P-type GaN semiconductor layer and the light emitting layer would be a GaN semiconductor layer. Further, if the first semiconductor layer 404 is a P-type GaN semiconductor layer, the second semiconductor layer 408 can be an N-type GaN semiconductor layer. The electrode islands 410 can be an Ohmic-contact material (such as: Pd, Pt, Ni, Au, Ag, or combinations thereof), a diffusion barrier layer, a metal bonding layer (metal bonding layer), a reflective layer, or combinations thereof. The electrode islands 410 have a thickness which is equal to or larger than 1 μm, and the distance between the electrode islands 410 is equal to or larger than 1 μm. The shape of the electrode islands 410 is unlimited, and the electrode island 410 has a cross-section profile in the shape of a polygon (please refer to FIG. 49), a semicircle (please refer to FIG. 50), or combinations thereof. Referring to FIGS. 51 and 52, the light emitting diode chip 400 can further include a reflective layer 412 disposed between the second semiconductor layer 408 and the electrode islands 410, thereby increasing the light extraction efficiency of the device. The reflective layer has reflectivity of more than 70% with the light emitted from the light emitting layer 406.

Further, the suitable package formation of the light emitting diode chip 400 as disclosed in the embodiment is vertical package. Referring to FIG. 53, in order to facilitate subsequent electrical connections, the light emitting diode chip 400 can further include an electrode 414 disposed on a bottom surface 407 (opposite to the top surface 403) of the substrate 402, and the electrode 414 is opposite to the electrodes 410. Since the electrodes 410 formed on the second semiconductor layer 408 have an island structure, the two adjacent electrodes 410 are separated from each other by a specific distance W1, thereby preventing a bonding layer (including the electrodes 410) from contacting the light emitting layer 406 or first semiconductor layer 404 and eliminating short circuit defects after a lamination step of a bonding process is performed.

According to another embodiment, in order to further avoid short circuit, the minimum horizontal distance W2 between the surrounding boundary 401 of the substrate 402 and each electrode islands 410 is equal to or more than 10 μm, for any substrate 402 size. Namely, the nearest electrode island 410 which is against the surrounding boundary 401 is separated from the surrounding boundary 401 by a distance equal to or larger than 10 μm, such as 20 μm. For Example, referring to FIG. 54, if the substrate 402 has a cross-sectional width of 40 mil, the nearest electrode island 410 which is against the surrounding boundary 401 has to be separated from the surrounding boundary 401 by a distance equal to or larger than 10 μm. Further, even if the substrate 402 has a cross-sectional width of 12 mil, referring to FIG. 55, the nearest electrode island 410 which is against the surrounding boundary 401 still has to be separated from the surrounding boundary 401 by a distance equal to or larger than 10 μm.

According to other embodiments, the light emitting diode chip 400 can further include a passivation layer 416 disposed on a side wall of the first semiconductor layer 404, a side wall of the light emitting layer 406, and a side wall of the second semiconductor layer 408, as FIG. 56 shows; thereby separating the light emitting layer 406 from a subsequently formed bonding layer. Therefore, the passivation layer 416 can prevent the bonding layer from becoming directly in contact with the light emitting layer 406 or the first semiconductor layer 404. Further, the passivation layer 416 can extend to a top surface of the second semiconductor layer 408, as FIGS. 57 and 58 show. Moreover, the passivation layer 416 of the electrode islands can further extend to and under a side wall of a portion of the electrode islands, as FIGS. 59 and 60 show. Suitable material of the passivation layer 24 can be dielectric material or schottky contact material, such as silicon oxide, silicon nitride, aluminium nitride, titanium oxide, aluminium oxide, or combinations thereof. In other embodiments, referring to FIGS. 61 and 62, the light emitting diode chip 400 can include taper side-walls 409 toward the substrate 402.

The light emitting diode chip can further be bonded to a carrier substrate, obtaining a light emitting diode package structure. In the bonding process, referring to FIG. 63, a nozzle 650 can be used to chock the diode chip 400 by suction and then to put the diode chip on a carrier substrate 420. Particularly, the nozzle 650 can preferably have an adsorptive surface 660 as shown in FIG. 64 (having a plurality of air inlets 670 replacing the conventional adsorptive surface as shown in FIG. 65 (having a single air inlet 670)), for improving the section strength.

Referring to FIG. 66A, the carrier substrate 420 (such as a submount substrate) includes a metal bonding layer 422 for subsequent bonding with the light emitting diode chip 400 and ensuring electrical connection therebetween, since the bonding process of the embodiment exhibits improved alignment. Referring to FIG. 66B, after bonding, the light emitting diode package structure 600 is obtained. The light emitting diode chip 400 is bonded to the carrier substrate 420 via a bonding layer 424, wherein the bonding layer 424 includes the electrode islands 410 and the metal bonding layer 422, and the bonding layer 424 has a thickness which is equal to or less than 50 μm. It should be noted, that after performing the lamination step of the bonding process, the bonding layer 424 of the light emitting diode package structure 600 has a plurality of voids 426 (which means that at least one of the electrode islands 410 and the metal bonding layer 422 has an island structure before bonding).

The bonding layer 424 has a plurality of voids 426 means that the bonding layer does not absolutely overflow to contact the side wall of the first semiconductor layer 404 and the light emitting layer 406 after the lamination step. Referring to FIG. 66B, after bonding, a minimum horizontal distance between the surrounding boundary 401 and the electrode islands 410 is larger than 0. Referring to FIG. 67A, except for the metal bonding layer 422, the light emitting diode package structure 600 can further include a metal bonding layer 428 (such as a reflective layer) formed between the carrier substrate 420 and the bonding layer 424. The metal bonding layer 428 is disposed between the bonding layer 424 and the substrate 420, thereby reflecting the light emitted by the light.
emitting diode chip 400 though the voids 426 and increasing the light extraction efficiency of the device. Due to the metal bonding layer 428, the metal bonding layer 422 can be shrunk. Namely, the minimum horizontal distant W3 between the surrounding boundary 401 of the substrate 402 and the metal bonding layer 422 can be more than 0, preferably equal to or more than 10 μm. The other aspect is that the shrunk metal bonding layer 422 can prevent the light emitting diode chip 400 from directly contacting the circuit disposed on the carrier substrate 420. Further, after bonding, a minimum horizontal distant between the surrounding boundary 401 and the metal bonding layer 422 is still larger than 0, as FIG. 67B shows. The shrunk metal bonding layer 422 have additional advantages for preventing the light emitting diode chip 400 from contacting to the designed circuit on the carrier substrate resulting in current leakage and increasing the tolerance for cutting inaccuracy for avoiding crack after LLO (laser lift off).

[0133] According to yet another embodiment, since the method exhibits improved alignment quality, the metal bonding layer 422 can have an island structure (i.e. including a plurality of electrode islands), wherein the island of the metal bonding layer 422 has a cross-section profile in the shape of a polygon, a semicircle, or combinations thereof, as FIGS. 68A and 68B show. The ratio between the total area of a top surface 421 of the metal bonding layer 422 and the area of a surface 403 of the substrate 402 is equal to or less than 95%. It should be noted, that after bonding, the bonding layer 424 of the light emitting diode package structure 600 still has a plurality of voids 426.

[0134] Further, referring to FIGS. 69 and 70, the light emitting diode chip 400 can have a plate electrode 410 for bonding to the metal bonding layer 422 of the carrier substrate 420, wherein the minimum horizontal distant W2 between the surrounding boundary 401 of the substrate 402 and the plate electrode 410 is more than 0, preferably more than 10 μm. The shrunk plate electrode 410 can prevent the light emitting diode chip 400 from current leakage.

[0135] According to other embodiments, the light emitting diode package structure 600 can further include a passivation layer 416 disposed on a side wall of the first semiconductor layer 404, a side wall of the light emitting layer 406, and a side wall of the second semiconductor layer 408. Further, the passivation layer 416 can extend to a top surface 405 of the second semiconductor layer 408, as FIG. 71 shows. Therefore, after bonding the light emitting diode chip 400 with the carrier substrate 420, the passivation layer 416 prevents the bonding layer 424 from becoming directly in contact with the light emitting layer 406 or the first semiconductor layer 404.

[0136] Further, referring to FIG. 72, the carrier substrate 420 employed by the light emitting diode package structure 600 can have a plurality of recesses 430 on a top surface of the carrier substrate 420, thereby preventing the bonding layer 424 from overflowing. Particularly, the reflective layer 428 can be blanketed formed on the top surface of the carrier substrate 420 to cover the side wall and the bottom surface of the recesses.

[0137] According to other embodiments, the carrier substrate 420 of the light emitting diode package structure 600 can be a package substrate with a designed circuit 435 for completing the electrical connections of the electrode islands 410, as FIG. 73 shows. Next, the substrate 402 of the light emitting diode chip 400 can be removed by LLO (laser lift off) process 431 (if the substrate is GaAs, SiC, Si or ZnO, it can be removed by wet etching process), as FIG. 74 shows. Next, a photosis form 432 is form to cover the carrier substrate 420 and the electrode islands 410, exposing the surface of the first semiconductor layer 404, as FIG. 75 shows. Finally, a dry etching 437, substituting for conventional polishing process, can be performed to remove the un-doped portion or high doped portion of the light emitting diode chip 400, as FIG. 76 shows.

[0138] According to yet other embodiments, the light emitting diode chip 400 with taper side-walls shown in FIG. 61 can be disposed on the carrier substrate 420 by bonding the electrode 410 with the metal bonding layer 422, as FIG. 77 shows. After bonding and LLO process, a passivation layer 416 can be conformally formed on the taper side-walls the light emitting diode chip 400 and the top surface of the carrier substrate 420, as FIG. 78 shows. Finally, a planar circuit pattern 437 can be formed on the passivation layer 416 to electrically connect to the first semiconductor layer 404, as FIG. 79 shows.

[0139] According to yet other embodiments, the light emitting diode chip 400 with taper side-walls shown in FIG. 61 can be disposed on the carrier substrate 420 by bonding the electrode 410 with the metal bonding layer 422, as FIG. 77 shows. After bonding and LLO process (or wet etching process), a passivation layer 416 can be conformally formed on the taper side-walls the light emitting diode chip 400 and the top surface of the carrier substrate 420, as FIG. 78 shows. Finally, a planar circuit pattern 437 can be formed on the passivation layer 416 to electrically connect to the first semiconductor layer 404, as FIG. 79 shows.

[0140] Further, in order to avoid the reduction of luminous intensity resulting from the light shielding of the wire (as shown in FIG. 80), the light emitting diode package structure 600 can be designed to prevent light shielding, i.e. there is no opaque wire disposed on the electrode 414. Referring to FIGS. 81 and 82, the light emitting diode package structure 600 can further include a metal pad 440, a passivation layer 442, and a transparent electrode 444, wherein the metal pad 444 surrounds the light emitting diode chip 400 and does not directly contact with the electrode 414. Further, the transparent electrode 444 is blanketed formed on the electrode 414 and electrically connected to the metal pad 440.

[0141] Moreover, referring to FIG. 83, a surrounding metal wall 450 can be formed on the transparent electrode 444 over the metal pad 440 by electroplating. Next, since the surrounding metal wall 450 and transparent electrode 444 can constitute an opening, and then a fluorescent powder 452 can be filled with the opening, achieving the object for emitting light, referring to FIG. 84. According to another embodiment, the surrounding metal wall 450 can be formed to be located immediately adjacent to the light emitting diode chip 400, thereby increasing the stability of the package structure and enhancing the light emitting efficiency, referring to FIG. 85A. Further, since the metal pad 440 can be designed to be various shape and the surrounding metal wall 450 (or photoresist) can be further patented, the shapeable light emitting diode package structure can be obtained, referring to FIG. 85B.

[0142] FIGS. 131A to 131D are a series of top views of yet other embodiments showing the fabrication process of a light emitting diode package structure of FIG. 132. First, a submount with a metal bonding layer 428 is provided, referring to FIG. 131A. Next, a light emitting diode chip 400 is bonded to the metal bonding layer 428, referring to FIG. 131B. Next, a metal pad 440 and a passivation layer 442 is formed on the
substrate 420, and it should be noted that a part of the metal pad 440 is separated by the passivation layer 442 from the metal bonding layer 428 which is directly bonded to the light emitting diode chip 400. Finally, the transparent electrode 444 is formed over the metal pad 440 by electroplating. FIG. 132 is the cross-section along the section A-A' in FIG. 131A. FIGS. 133A to 133D are a series of top views of yet other embodiments showing the fabrication process of a light emitting diode package structure of FIG. 134. First, a submount with metal bonding layers 428A and 428B is provided, wherein the metal bonding layers 428A and 428B can be patterned. Next, a light emitting diode chip 400 is bonded to the metal bonding layer 428B, referring to FIG. 133B. Next, a passivation layer 442 is formed on the substrate 420 to cover a part of the metal bonding layer 428B. Finally, the transparent electrode 444 is formed by electroplating, and it should be noted that the transparent electrode 444 should be separated by the passivation layer 442 from the metal bonding layer 428B which is directly bonded to the light emitting diode chip 400. FIG. 134 is the cross-section along the section B-B' in FIG. 133A.

[0143] FIG. 86 is a diagram showing a light emitting diode (LED) structure 500 according to a preferred embodiment. FIG. 87 is a diagram showing the top view of the LED structure 500 in FIG. 86. FIG. 88 is a diagram showing the c'-c' cross-sectional view of the LED structure 500 in FIG. 86. The LED structure 500 includes a submount 510, a stacked structure 520, an electrode 531, an isolation layer 540 and a conductive thin film layer 550. As shown in FIG. 88, the submount 510 has a first surface 5100A and a second surface 5100B opposite the first surface 5100A. The stacked structure 520 has a first semiconductor layer 521, an active layer 523 and a second semiconductor layer 525 that are laminated on the first surface 5100A. The electrode 531 is disposed apart from the stacked structure 520 on the first surface 5100A. The isolation layer 540 surrounds the stacked structure 520 as well as covers the lateral sides of the stacked structure 520 on the first surface 5100A. The conductive thin film layer 550 connects the electrode 531 to the stacked structure 520.

[0144] In the embodiment, the conductive thin film layer 550 totally covers the electrode 130, the isolation layer 540 and the stacked structure 520, for example, for electrically connecting the electrode 531 to the stacked structure 520. However, the invention is not limited thereto, the conductive thin film layer 550 can just cover a part of the electrode 531. Furthermore, the conductive thin film layer 550 has weak adhesion for attaching to other elements such as metal bumps, which are used for wire bonding. Preferably, as shown in FIG. 86, a plurality of metal pads 552 are disposed on the conductive thin film layer 550 to assist the conductive thin film layer 550 in connecting with metal bumps. The metal pads 552 can be formed on the conductive thin film layer 550 by plating. Or, the conductive thin film layer 550 can be partially removed by, for example, etching, to expose parts of the electrode 531, such that the exposed parts of the electrode 531 can be used as the metal pads 552.

[0145] In the embodiment, although the isolation layer 540 surrounds all the lateral sides of the stacked structure 520 (shown in FIG. 88) and the conductive thin film layer 550 covers the isolation layer 540 and the stacked structure 520, the invention is not limited thereto. The isolation layer 540 needs only to cover the lateral sides of the active layer 523. Besides, the isolation layer 540 can merely be disposed along three lateral sides of the stacked structure 520, and the conductive thin film layer 550 can just cover a part of the isolation layer 540 and the stacked structure 520.

[0146] The LED structure 500 further includes an electrostatic discharge (ESD) protection element 560, another electrode 533 and an interface layer 570. The ESD protection element 560 is disposed under the electrode 531 and embedded in the submount 510. The electrode 533 is disposed on the second surface 5100B of the submount 510. The interface layer 570 is disposed between the stacked structure 520 and the submount 510.

[0147] The active layer 523 has a p-n junction region for emitting light when applied by a bias voltage, and the first and second semiconductor layers 521, 525 are used as cladding layers for the active layer 523. In the preferred embodiment, the first semiconductor layer 521 is a single layer that includes, for example, an n-type semiconductor such as n-GaN, and the second semiconductor layer 525 is also a single layer that includes, for example, a p-type semiconductor such as p-GaN. However, the invention is not limited thereto. Each of the first and second semiconductor layers 521, 525 can also be multi-layer structure, such as a NPN structure or a PNP structure.

[0148] In the embodiment, the electrode 531 is disposed along the lateral sides of the stacked structure 520, as shown in FIG. 87. The material of the electrodes 531 and 533 is, for example, metal, such as Cu, Ag, Au etc. And since the electrodes 531 and 533 are disposed on two opposite sides (shown in FIG. 88) of the submount 510, the submount 510 is preferably conductive. For example, the material of the submount 510 is a doped semiconductor. Further considering the composition of the stacked structure 520, the submount 510 is preferably formed by n-type silicon. And the material of the ESD protection element 560 is preferably a p-type silicon, so as to form a p-n junction with the submount 510. FIG. 89 is a circuit diagram showing the electrical connection of the stacked structure, the submount and the ESD protection element. The p-n junction between the ESD protection element 560 and the submount 510 is served as a Zener diode that requires a high reverse bias voltage to cross, so the ESD protection element 540 is capable of avoiding electric current flowing in the direction from the submount 510 to the electrode 531, hence providing an ESD protection function for the LED structure 500.

[0149] In addition, as the electrode 531 is disposed along all the lateral sides of the stacked structure 520, the stacked structure 520 is not covered by the electrode 531 and its whole top surface is served as light emitting area, producing the largest light emitting effect.

[0150] The electrode 533 is disposed on the different side from the electrode 531 in the embodiment. However, the electrode 533 also can be disposed on the same side as the electrode 531 but located apart from the electrode 531 to avoid unnecessary electrical connection, so the material of the submount 510 is not limited to be conductive and can be formed by any undoped semiconductor or ceramic material.

[0151] The material of the isolation layer 540 disposed between the electrode 531 and the stacked structure 520 is, for example, silicon oxide for preventing the stacked structure 520 from directly connecting the electrode 531. The light transmittance of the conductive thin film layer 550 for a primary wavelength of the light generated by the active layer 523 is greater than 60%. In addition, the material of the conductive thin film layer 550 is selected from one group consisted of In2O3, SnO2, ZrO, CdO, TiN, In2O3:Sn(ITO),
ZnO:In(IZO), ZnO:Ga(GZO), ZnO:Al(AZO), SnO2:F, TiO2:Ta, In2O3-ZnO, CdIn2O4, CdSnO2, Mg(OH)2-C, ITO, IZO, GZO, AZO, ATO, FTO, NiO, and an alloy consisted of the above elements. Preferably, the material of the conductive thin film layer 550 is selected from one group consisted of ITO, IZO, GZO, AZO, ATO, FTO, NiO, and an alloy consisted of the above elements. The interface layer 570 between the stacked structure 520 and the submount 510 can be served either as an adhesive layer or as a reflector layer in the LED structure 500, however the invention is not limited thereto. The interface layer 570 can provide both an adhesive function and a reflective function for the stacked structure 520. For example, the interface layer 570 includes a metal reflector for reflecting the light generated by the active layer 523. Moreover, the interface layer 570 further includes an adhesive for combining the stacked structure 520 and the submount 510.

[0152] It is noted that, since the electrode 531 is disposed along all the lateral sides of the stacked structure 520 and is electrically connected to the stacked structure 520 by the conductive thin film layer 550, electric current flows inwards in the direction from the electrode 531 to the stacked structure 520 when voltage is applied to the electrodes 531 and 533, avoiding the electric current concentrating on a single portion of the stacked structure 520. Thus, the energy loss of the applied voltage is reduced, and the energy usage is enhanced accordingly.

[0153] FIG. 90 is a flowchart showing a method of forming a LED structure according to a preferred embodiment. The method includes steps S31 to S38 elaborated in the following accompanying with FIGS. 92A to 92G that sequentially show the formation of a LED structure in accordance with the steps of the method in FIG. 90. In step S31, an ESD protection element is formed on a submount, wherein the ESD protection element is disposed along the edges of a first surface on the submount and is embedded in the submount. As shown in FIG. 92A, when fabricating, a large-sized submount 510 is normally provided and a plurality of areas on the large-sized submount 510 are predetermined. The thickness of the large-sized submount 510 is usually less than 700 micrometer in consideration of heat effect. A plurality of ESD protection elements 560 are formed on the large-sized submount 510 and within the predetermined areas. Besides, the ESD protection elements 560 are disposed along the edges of the first surface 5100A within each predetermined area of the large-sized submount 510 and are embedded in the large-sized submount 510.

[0154] Next, in step S32, an electrode is formed on the ESD protection element. As shown in FIG. 92B, a plurality of electrodes 531 are formed on the first surface 5100A in accordance with the ESD protection elements 560.

[0155] Then, the method proceeds to step S33 that a stacked structure is provided and is bonded on the first surface of the submount, wherein the stacked structure is located apart from the electrode. In FIG. 92C, the stacked structure 520 and an interface layer 570 are formed on a temporary substrate 580 in advance before being bonded to the large-sized submount 510. The temporary substrate 580 is, for example, a sapphire (Al2O3) substrate, silicon carbide substrate, or gallium arsenic substrate. Normally, the materials of the first semiconductor layer 521, active layer 523, second semiconductor layer 525 and interface layer 570 are formed and laminated on a large-sized temporary substrate (not shown) in order, and then the large-sized temporary substrate and the materials thereon are diced to form a plurality of the temporary substrates 580 with the stacked structures 520 and interface layers 570. As shown in FIG. 92C, each temporary substrate 580, on which the stacked structure 520 and the interface layer 570 are loaded, is then reversed to face the first surface 5100A of the large-sized submount 510. After that, the interface layer 570 and the large-sized submount 510 can be bonded together by applying ultrasonic energy and heat onto the large-sized submount 510.

[0156] Due to the characteristic of ultrasonic wave, the bonding temperature in the embodiment ranges from about 100°C to 200°C. The bonding temperature is much lower than conventional bonding temperature, which is about 400°C, causing least change to the quality of the LED structure, such as stress distribution, so the strength of the LED structure is maintained.

[0157] When the stacked structure 520 and interface layer 570 are fixed on the large-sized submount 510, the temporary substrate 580 should be detached from the stacked structure 520. As the first semiconductor layer 521 is formed by n-GaN, a laser lift-off method can be used to detach the temporary substrate 580 due to the characteristic of n-GaN. For example, when the first semiconductor layer 521 is projected by a laser beam, the portion of the first semiconductor layer 521 that connects the temporary substrate 580 absorbs the energy of laser beam and then has decomposition reaction to generate nitrogen gas, loosing the connection between the first semiconductor layer 521 and the temporary substrate 580. It is noted that, because the temporary substrates 580 are small-sized after diced and are peeled off the stacked structures 520 respectively, each of the temporary substrates 580 produces less pulling force to the stacked structures 520 during the procedure of detaching, hence easing the damage to the stacked structures 520. Also, with the help of nitrogen gas, each of the temporary substrates 580 is more easily separated from the stacked structures 520. As shown in FIG. 92D, during the fabrication procedure, a plurality of stacked structures 520 are formed on the large-sized submount 510 at the same time within the predetermined areas and located apart from the electrodes 531.

[0158] Next, in step S34, an isolation layer is formed on the electrode, the stacked structure and the space between the electrode and the stacked structure. As shown in FIG. 92E, an overall isolation layer 540 is formed over the electrodes 531, the stacked structures 520 and the spaces between the electrodes 531 and the stacked structures 520. The overall isolation layer 540 is mainly used for avoiding direct electrical connection between the stacked structures 520 and the electrodes 531. The overall isolation layer 540 can be formed by spinning or plasma enhanced chemical vapor deposition (PECVD).

[0159] Then, in step S35, part of the isolation layer over the electrode and part of the isolation layer over the stacked structure are removed to expose the electrode and the stacked structure. As shown in FIG. 92E, the isolation layer 540 over the electrodes 531 and over the stacked structures 520 can be removed by etching, so as to detach the isolation layers 540 between the stacked structures 520 and the electrodes 531 on the submount 510, as shown in FIG. 92F.

[0160] Next, in step S36, a conductive thin film layer is formed on the electrode and the stacked structure for electrically connecting the electrode to the stacked structure. As shown in FIG. 92G, conductive material such as ITO, IZO, GZO, AZO, ATO, FTO, NIO etc. is used and coated over the
exposed surfaces of the electrodes 531 and stacked structures 520, as well as over the isolation layers 540, thereby forming a conductive thin film layer 550 to electrically connect the electrodes 531 with the stacked structures 520.

[0161] Then, in step S37, another electrode is formed on a second surface of the submount opposite the first surface. As shown in FIG. 92G, an electrode 533 is formed on the second surface 51003 of the large-sized submount 510 and is opposite the electrodes 531. Herein the fabrication of a plurality of LED structures 500, which are not yet separated, is completed. Afterwards, as stated in step S38, the submount is diced to form a LED structure. As shown in FIG. 92G, the large-sized submount 510 are diced along the dashed lines (only one is shown for illustration) that are preferably in accordance with the edges of the predetermined areas, and then the manufacture of each individual LED structure 500 (shown in FIG. 88) is finished.

[0162] FIG. 91 is a flowchart showing a method of forming another LED structure according to a preferred embodiment. The LED structure manufactured according to the method in FIG. 91 is different from the LED structure manufactured according to the method in FIG. 90 in the absence of ESD protection element. As shown in FIG. 91, the method includes steps S41 to S47 that also can be elaborated by FIGS. 92A to 92G but the ESD protection elements in FIGS. 92A to 92G could be left out. In step S41, an electrode is formed on a submount, wherein the electrode is disposed along the edges of a first surface on the submount. Then, in step S42, a stacked structure is provided and bonded on the first surface of the submount, wherein the stacked structure is located apart from the electrode. Next, in step S43, an isolation layer is formed on the electrode, the stacked structure and the space between the electrode and the stacked structure. Then, a part of the isolation layer over the electrode and a part of the isolation layer over the stacked structure are removed to expose the electrode and the stacked structure. Next, a conductive thin film layer is formed on the electrode and the stacked structure for electrically connecting the electrode to the stacked structure. Then, another electrode is formed on a second surface of the submount opposite the first surface. Afterwards, the submount is diced to form a LED structure.

[0163] In the above embodiment the conductive thin film layer 550 is an intact and uniform thin film layer, however the invention is not limited thereto. For example, the conductive thin film layer 550 can be designed as a thin film with openings or concaves that partially hollow out or thin out the conductive thin film layer 550. The openings or concaves are preferably located corresponding to the stacked structure 520 for changing the light transmission rate of the conductive thin film layer 550. FIG. 93 is a diagram showing a conductive thin film layer 550 with a plurality of openings 550α. The openings 550α do not block the light from the stacked structure 520, effectively improving the light transmission rate of the conductive thin film layer 550, and further enhancing the light usage of the stacked structure 520.

[0164] FIGS. 94 and 95 are diagrams each showing a conductive thin film layer 550α with a light extracting feature. As shown in FIG. 94, the light extracting feature includes a plurality of sawteeth 550bα. The sawteeth 550bα are located above the top surface of the stacked structure 520, for example, micro-structures that can be formed by roughening the outer surface of the conductive thin film layer 550. The light emitted from the stacked structure 520 is scattered in different directions by the sawteeth 550bα so as to increase the light emitting area of the stacked structure 520. As shown in FIG. 95, the light extracting feature includes a plurality of pillars 550bα. The pillars 550bα are, for example, nanostructures. Moreover, as a conductive thin film layer is designed to have concaves, the light extracting feature can also be formed on the surfaces within the concaves.

[0165] The LED structure disclosed in the above embodiment can further be used with phosphor for generating light of different color. FIG. 96 is a diagram showing a LED structure 700 filled with phosphor 702. The LED structure 700 includes a submount 710, a stacked structure 720, two electrodes 731 and 733, an isolation layer 740, a conductive thin film layer 750, an ESD protection element 260 and an interface layer 770. The submount 710 has a cavity 712 on its first surface 7100A. The stacked structure 720 is disposed within the cavity 712 and is positioned lower than the top of the electrode 731. And as the electrode 731 is disposed on the lateral side of the stacked structure 720, there is a concave 700α formed on the LED structure 700. The concave 700α facilitates the conformal coating of phosphor due to the reason that the concave 700α can be fully filled with the phosphor 702 easily.

[0166] As shown in FIG. 87, the electrode 531 in the above embodiment is disposed along all lateral sides of the stacked structure 520, however the invention is not limited thereto. FIG. 97A is a diagram showing a LED structure 800 having an electrode 831 not fully surrounding its stacked structure 820, and FIG. 97B is a diagram showing the top view of the LED structure 800 in FIG. 97A. The electrode 831 of the LED structure 800 is disposed along three lateral sides of the stacked structure 820, and another electrode 833 is disposed on the unoccupied lateral side apart from the electrode 831 on the stacked structure 820. An isolation layer 840 is used for isolating the electrodes 831 and 833 and the stacked structure 820 to avoid unnecessary electrical connection. A conductive thin film 850 is disposed over the electrode 831 and the stacked structure 820. As the electrode 831 does not completely surround the LED structure 800, the LED structure 800 can be combined with other LED structures via a plurality of conductive lines 890, so as to produce a larger light emitting area.

[0167] The design of lateral electrode can be applied to a LED package structure and is elaborated below by accompanying drawings. FIGS. 98A and 98E are diagrams showing a LED packaging structure according to a preferred embodiment. FIG. 98C is a top view of the LED packaging structure in FIG. 98A, and FIGS. 98D and 98E are cross-sectional views of the LED packaging structure in FIG. 98C along lines A-A' and B-B' respectively. In FIG. 98A, the LED packaging structure 900 includes a packaging substrate 901 and a transparent sealant 403 that is disposed on the packaging substrate 901. As shown in FIG. 98B, the LED packaging structure 900 further includes at least one stacked structure 905, at least one first electrode 907, at least one second electrode 909, an isolation layer 911, and at least one conductive thin film layer 913. The stacked structure 905 is disposed on a first surface 901α of the packaging substrate 901 and its design is similar to that of the stacked structure 520 shown in FIG. 88 and is not repeated herein. The first electrode 907 is disposed on the first surface 901α and apart from the stacked structure 905. The isolation layer 911 is disposed on the first surface 901α and surrounds the stacked structure 905 as well as covers the lateral sides of the stacked structure 905, and the isolation layer 911 also fills the gap between the first and second
electrodes 907 and 909. The conductive thin film layer 913 connects the first electrode 907 to the stacked structure 905. The second electrode 909 is disposed on the packaging substrate 901 and is electrically connected to the stacked structure 905. Preferably, the second electrode 909 is disposed between the stacked structure 905 and the packaging substrate 901. The transparent sealant 903 covers the conductive thin film layer 913 as well as the isolation layer 911 for protecting the LED packaging structure 900.

[0168] The packaging substrate 901 is, for example, a semiconductor substrate that is electro-conductive, and its thickness is preferably greater than 800 micrometer for loading the components mentioned above. As shown in FIG. 98D, the LED packaging structure 900 further includes at least one ESD protection element 915 disposed under the first electrode 907 and embedded in the packaging substrate 901. The material of the packaging substrate 901 is not limited to be electro-conductive. For example, the packaging substrate 901 can also be any type of substrate such as metal-based substrate, silicon-based substrate, ceramic-based substrate, printed circuit board (PCB), flexible printed circuit board (FCB) etc.

[0169] As shown in FIG. 98E, the packaging substrate 901 includes two through holes 901B and 901C, which extend from the first surface 901A to a second surface 901D opposite the first surface 901A as well as correspond to the first electrode 907 and the second electrode 909 respectively. As the packaging substrate 901 is attached to other electronic device, the first electrode 907 and the second electrode 909 can be electrically connected to its driving source by the through holes 901B and 901C and two bonding pads 921 and 923. As the packaging substrate 901 is electro-conductive, the insulation of the through holes 901B and 901C should be considered. Preferably, another isolation layer 917 is disposed between the through holes 901B and 901C and the packaging substrate 901. However, as the packaging substrate 901 is formed by a non-conductive material such as ceramic, the isolation layer 917 and the ESD protection element 915 (shown in FIG. 98D) can be left out.

[0170] FIG. 99 is a diagram showing a LED packaging structure having a plurality of light emitting areas. The LED packaging structure 900 has a plurality of stacked structures (not shown), which are formed on the packaging substrate 901 and each correspond to one light emitting area 9001. A plurality of first electrodes 907 and a plurality of second electrodes 909 are disposed on the packaging substrate 901. The LED packaging structure 900 provides a total light emitting area larger than that of the LED packaging structure 900 (shown in FIG. 98C).

[0171] The connection between the stacked structure and the electrode makes use of the conductive thin film layer in the above embodiment. However, the electric current in the conductive thin film layer may not be always steady. Thus, an auxiliary electrode can be used to assist the electrical connection between the stacked structure and the electrode. FIGS. 100A and 100B are diagrams each showing an auxiliary electrode disposed on the conductive thin film layer. As shown in both FIGS. 100A and 100B, the auxiliary electrode 190 is disposed on the conductive thin film layer 550 and covers a part of the conductive thin film layer 550. The auxiliary electrode 190 is a cross structure for example, and the four ends of the cross structure correspond to the four corners (as shown in FIG. 100A) or four edges (as shown in FIG. 100B) of the conductive thin film layer 550, respectively, and extend to the electrode 531, thus the electrical connection between the stacked structure 520 and the electrode 531 is enhanced. Besides, the auxiliary electrode 590 can be further disposed along the lateral sides of the stacked structure 520. Furthermore, for increasing the attachment between the conductive thin film layer 550 and other elements such as metal bumps, a plurality of metal pads 552 are disposed on the conductive thin film layer 550.

[0172] The interface layer used for combining the stacked structure with the submount in the above embodiment totally fills the gap between the stacked structure and the submount, however the invention is not limited thereto. FIGS. 101A and 101B are diagrams each showing an interface layer having a plurality of partitions. As shown in FIG. 101A, the interface layer 570 includes partitions 570a which are separated by several vacancies 570b. The interface layer 570 is easy to manufacture and the yield is thus increased. As shown in FIG. 101B, the interface layer 570 includes partitions 570a, and each vacancy between two partitions 570b is filled with a filling material 570c such as resin or silicone.

[0173] The LED structure, LED packaging structure and method of forming a LED structure disclosed in the preferred embodiment have the electrode, which is mostly formed by opaque metal, disposed along the lateral sides of the stacked structure that emits light, so the electrode does not block the light from the stacked structure, rendering the LED structure fit for the requirement of a light emitting device. Besides, the LED structure itself has an electrostatic discharge (ESD) protection element, which can be formed with the submount of the LED structure, for ESD protection of the LED structure, thus neither additional ESD protection device nor conductive line needs to be assembled after the LED structure is fabricated. Therefore, the LED structure in the embodiment is simpler than a conventional LED device equipped with ESD protection device, facilitating the manufacturing process as well as saving the manufacturing cost.

[0174] In order to at least improve the uniformity of luminance for the LED dies in packaging process, the disclosure has propose a novel structure with the fabrication processes. Several embodiments are provided for describing the disclosure but the disclosure is not limited to the provided embodiments.

[0175] FIG. 102 is a cross-sectional view, schematically illustrating a structure of LED die, according to an embodiment. In FIG. 102, when considering the structure being fabricated, a carrier 1100 is serving as the substrate. The carrier 1100, as known, usually has a circuit for connection to the power or any external control circuit. A light emitting semiconductor stacked layer 1102, such as the LED without transparent submount, is disposed on the carrier 1100. The LED is usually, for example, less than 50 microns in thickness and at least includes P-type layer, N-type layer and active layer between the P-type layer, N-type layer, for example. The LED semiconductor structure can be a known structure state-in-the art, without specific limitation. A wavelength conversion layer 1104 on the light-emitting semiconductor stacked layer 1102. A surrounding layer 1106 is disposed on the carrier 1100 and surrounds a sidewall of the light-emitting semiconductor stacked layer 1102 and the wavelength conversion layer 1104. Actually, the space occupied by the wavelength conversion layer 1104 is defined by the transparent submount in the LED die, in which the transparent submount,
such as the sapphire submount, is stripped away during fabrication, and leaves the cavity space for filling the wavelength conversion layer 1104.

[0176] In the structure shown in FIG. 102, the surrounding layer 1106, such as the under fill layer, is surrounding the sidewall of the light-emitting semiconductor stacked layer 1102 by the self-alignment, the wavelength conversion layer 1104 can be formed on the light-emitting semiconductor stacked layer 1102 with uniform thickness and self-alignment. FIG. 103A is a top view, schematically illustrating several configurations of the LED dies attached on the carrier, according to embodiments. In FIG. 102, due to the self-alignment mechanism, the surrounding layer 1106 can be adapted for various configurations for the LED dies on the carrier. In FIG. 103A, the LED die with the wavelength conversion layer 1104 may be regularly disposed on the carrier. The surrounding layer 1106 can be surrounding the sidewall of the wavelength conversion layer 1104. Since the wavelength conversion layer 1104 is liquid phase before being cured, the wavelength conversion layer 1104 can be uniformly filled on the light-emitting semiconductor stacked layer 1102 without worrying the location and twist direction. In FIG. 103B, the LED die is twisted by an angle, which may be intended in design and just an alignment error of the LED die. Likewise, several other configuration in FIGS. 103C-103F can be packaged with the same mechanism. In FIG. 103C, for example, several LED dies are disposed the predetermined locations, according to the designed pattern. In FIG. 103D, the shape of the LED die may also be changed into a rectangle, for example. In FIG. 103E, the LED die is rotated by an angle, such as 45 degrees. In FIG. 103F, it is like the configuration in FIG. 103C but the size and shape of the LED dies are different. In other words, the embodiment can be applied to various LED configurations with self-alignment.

[0177] For the fabrication process, in order to fabricate the structure of LED die, several manners can be performed. FIGS. 104A-104D are cross-sectional views, schematically illustrating packaging processes to form the LED packaging unit, according to an embodiment. In FIG. 104A, a carrier 1200 is provided as a substrate. The carrier 1200 has a circuit fabricated inside for connection to external terminal. A light-emitting device, such as LED die, has the light-emitting semiconductor stacking layers 1206 and the submount 1202. The light-emitting semiconductor stacking layers 1208 is fabricated on the submount 1202. The submount 1202 can be, for example, sapphire. The light-emitting semiconductor stacking layers 1208 includes, for example, n-type semiconductor layer and p-type semiconductor layer 1206 to form diode to emit light. The semiconductor stack layer can include several layers to achieve the mechanism for emitting light. Only the n-type semiconductor layer 1204 and p-type semiconductor layer 1206 are shown for generally indicating the LED. In addition, a metal reflection layer 207 can be also formed on the semiconductor layer 1206 in option. The LED is usually formed on the submount 1202, as known by a person on ordinary skill in the art. The light-emitting semiconductor stacking layers 1208 is fabricated on the submount 1202 generally represents a LED die, as usually known. The light is emitted at a direction toward the submount 1202. The LED die is then packaged onto the carrier 1200 by for example, flip-chip packaging process. The conductive bumps 1210 and 1212 are respectively coupled to the electrode pads of the semiconductor layers 1204 and 1206 in different conductive type. By the conductive bumps 1210 and 1212, the LED die is electrically coupled to the carrier 1200. The structure in FIG. 104A can be formed by convention manners in known structure. The invention is not limited to the specific structure of LED die.

[0178] In FIG. 104B, an surrounding layer 1214, such as molding compound, can be formed to fill the gap between the LED die and the carrier 1200, and then surround the LED die. The surrounding layer 1214 can be the underfill layer in packing. In other word, the surrounding layer 1214 is generally referred as a surrounding layer, alternatively. The top surface 1214a of the surrounding layer 1214 may be lower than the surface of the submount 1202, so that the submount 1202 remains being exposed. However in option, the tip surface 2140 of the surrounding layer 1214 may be slightly higher than the submount 1202 and then also covers the peripheral of the submount 1202. This situation is also acceptable because it does not cause difficult the submount 1202 to lift off later by, for example, thermal effect from laser.

[0179] In FIG. 104C, the submount 1202 is lifted off from the semiconductor layer 1204 by applying laser light on the submount 1202, causing heat. Because there is a tension release at the interface between the submount 1202 and the semiconductor layer 204 after the laser producing the heat, the submount 1202 is easily lifted off and leaves a cavity 1216 in the surrounding layer 1214.

[0180] In FIG. 104D, the cavity 1216 is filled with the wavelength conversion layer 1218 in liquid and then is cured. Because the wavelength conversion layer 1218 is in liquid phase, the top surface can be uniform and is self-aligned to the light-emitting semiconductor stacking layers 1208. In addition, since the wavelength conversion layer 1218 is in liquid phase, the height can be controlled to be lower than or equal to the top surface of the surrounding 1214, for example.

[0181] The LED die in FIGS. 104A-104D is a horizontal type, which means the two electrodes are distributed at the same side with respect to the light-emitting semiconductor stacking layers 1208. However, the LED die in FIG. 102 is the vertical type, which means the two electrodes in different conductive type are at opposite sides with respect to the light-emitting semiconductor stacking layers 1208.

[0182] FIGS. 105A-105D are cross-sectional views, schematically illustrating packaging processes to form the LED packaging unit, according to an embodiment. In FIG. 105A, the carrier 1300 is also provided as the structure base for electric connection. The semiconductor stack layer 1304 of a vertical LED die is bounded on the carrier 1300 by the bonding material 1302. The semiconductor stack layer 1304 includes several different conductive-type layers in stack for emitting light when in operation, and the two electrode layers are on both sides. Here, as can be understood, the electric connection of the semiconductor stack layer 1304 to the circuit in the carrier 1300 is not specifically shown but can be known by the one with ordinary skill in the art. The LED die with the semiconductor stack layer 1304 is accomplished in fabrication before packaging to the carrier 1300. The semiconductor stack layer 1304 generally represents the structure of LED for emitting light and is formed on the submount 1306. Actually, the LED die can be fabricated by the process in state-of-the-art without specific limitation. The semiconductor stack layer 1304 is formed on the submount 1306 during fabrication. In packaging process, the LED die is then attached to the carrier 1300, and a surrounding layer 308 is also formed to surround the sidewall of LED die including the
submount 1306 and the semiconductor stack layer 1304, but the submount 1306 remains being exposed, as discussed in FIGS. 104A-104D.

[0183] In FIG. 105B, by the same mechanism to lift-off the submount 1306, the laser is applied on the submount 1306, so that the submount 1306 is lifted off, leaving the cavity 1310.

[0184] In FIG. 105C, usually, the n-type electrode of the LED die is in contact with the submount 1306, for example. The connection electrode 1312, such as n-type electrode, is bonding to the semiconductor stack layer 1304. The connection electrode 1312 may be the bonding wire.

[0185] In FIG. 105D, after the connection electrode 1312 is bonded to the electrode of the semiconductor stack layer 1304, the wavelength conversion layer 1314 is filled into the cavity 1310 and cured. Here, as mentioned above, the carrier 1300 has the circuit for external connection. The p-type electrode can be connected to the bottom of the semiconductor stack layer 1304 by the circuit in the carrier 1300. This connection structure is also usually known.

[0186] In other words, for the general features in packaging, the disclosure uses the surrounding layer to surround the submount of the LED die. After the submount, the wavelength conversion layer is filled instead. The wavelength conversion layer is formed and aligned to the LED with self-aligning mechanism. It allows the LED die to be freely attached to the carrier without missing alignment between the LED die and the wavelength conversion layer.

[0187] Based on the same mechanism, various modifications can be taken. With respect to the options for forming the connection electrode to the semiconductor stack layer 1304, the electrode can be fabricated in various manners. FIGS. 106-108 are cross-sectional views, schematically illustrating the LED package structures, according to various embodiments.

[0188] In FIG. 106, the structure is similar to the previous embodiments. However, the electrode layer 1320 is in different structure. Before the wavelength conversion layer 1314 is filled into the cavity, the electrode layer 1320 can be formed. The electrode 1320 can be a conductive layer in contact with the semiconductor stack layer 1304 and extend to the top surface of the surrounding layer 1308 through the inner side-wall of the surrounding layer 1308. In this manner, the wire bonding is replaced. After the electrode layer 1320 is formed, the wavelength conversion layer 1314 can be filled and cured.

[0189] In FIG. 107, alternatively, the electrode layer 1320 in FIG. 106 is further modified. In this example, the electrode layer 1322 is similar to the electrode layer 1320 in FIG. 106, but it is formed after the wavelength conversion layer 1314 is formed. However, the wavelength conversion layer 1314 is preferably conductive. However, the electric connection to the semiconductor stack layer 1304 can be formed by the usual fabrication process.

[0190] In FIG. 108, even further, the electrode layer can use the transparent conductive layer (TCL) as the electrode layer 1324. Material of the TCL is usually known, such as indium tin oxide or any other. Since the electrode layer 1324 is transparent, the transparent electrode layer 1324 can be formed over the whole light emitting area, so that the current can be more uniform. In this situation, the wavelength conversion layer 1314 is preferably conductive. However, the transparent electrode layer 1324 can be formed on the semiconductor stack layer 1304 before the wavelength conversion layer 1314 is filled.

[0191] In general, the electrode can be formed in accordance with the design without specific limitation.

[0192] FIGS. 109A-109B are cross-sectional views, schematically illustrating a fabrication process to form the LED package structure, according to another embodiment. In FIG. 109A, the structure is similar to FIG. 104A but the difference is the protruding layer 1280a. When the LED die is fabricated, as the previously described, the submount 1202 is a base for growing the semiconductor layer 1204 and the other layers thereon. The additional protruding layer 1280a is also formed beside the semiconductor layer 1204. The protruding layer 1280a can be, for example, surrounding the semiconductor layer 1204 with contact or not contact. The submount 1202 and the protruding layer 1280a can be different pieces or a single piece as an option. The submount 1202 and the protruding layer 1280a are sacrificial structure, and are to be lifitef off later. In this example, the protruding layer 1280a contacts the side of the semiconductor layer 1204. Then, the LED die is bonded to the carrier 1200 by, for example, the flip-chip packaging process, as described in FIGS. 104B-104C.

[0193] In FIG. 109B, after the submount 1202 with the protruding layer 1280a is lifted off. The protruding layer 1280a produces the additional indent 1280b. After the wavelength conversion layer 1218 is filled into the cavity above the semiconductor layer 1204 layer, the wavelength conversion layer 1218 also fill the indent 1280b. Since this additional structure, the periphery of the semiconductor stack layer 1304 is further surrounded by the wavelength conversion layer 1218. As a result, the emitted light at the side region can also be modified by the wavelength conversion layer 1218 at the indent 1280b. The light can be more uniform in view angle, particularly to the large viewing angle.

[0194] Further, FIG. 110 is a cross-sectional structure, schematically illustrating another LED package structure, according to an embodiment. Depending on the use of the LED package, in FIG. 110, the surrounding layer 290 can be mixed with the fillers 1292, which can absorb light or not absorb light. The surrounding layer 1290 can also be low thermal expansion coefficient, for example. If the fillers 1292 are absorbing light, the emitted light is tended to be confined into a single direction. As a result, the emitted light is directional. However, the wavelength conversion layer can be optionally filled or not. Alternatively, the wavelength conversion layer can also be replaced by other protection material.

[0195] FIG. 111 is a cross-sectional structure, schematically illustrating another LED package structure, according to an embodiment. In FIG. 111, alternatively, the surrounding layer 1290 can be added with the fillers 1294, which are florescent powders. In this situation, the wavelength conversion layer may be omitted. However, the wavelength conversion layer may be still included as an option in design.

[0196] FIG. 112A is a cross-sectional structure, schematically illustrating another LED package structure, according to an embodiment. In FIG. 112A, when the wavelength conversion layer 1218 in liquid phase is filled into the cavity of the surrounding layer 1214, the peripheral portion 1300 of the wavelength conversion layer 1218 in contacting with the surrounding layer 1214 preferably has a surface to be ideally perpendicular to the inner sidewall of the surrounding layer 1214. By choosing the proper materials for the surrounding layer 1214 and the wavelength conversion layer 1218, so as to reduce the surface tension, the surface of the wavelength conversion layer at the peripheral portion 1300 can be tend to
be perpendicular to the inner sidewall of the surrounding layer 1214, as shown in FIG. 112B.

[0197] FIGS. 113A and 113B are drawings, schematically illustrating phenomena at the peripheral portion 300 in FIG. 112A. If the materials between the surrounding layer 1214 and the wavelength conversion layer 1218 causing surface tension, the surface of the wavelength conversion layer 1218 in liquid phase at the contact region can be climbing up or suppressing down on the sidewall of the surrounding layer 1214, as known in physical phenomenon. If the situation exists, the wavelength conversion layer 1218 at the peripheral region would not be ideally perpendicular as shown in FIG. 112B.

[0198] FIG. 114 is a cross-section layer, schematically illustrating a structure of the LED package according to another embodiment. In FIG. 114, the surrounding layer 1214 can be alternatively formed by two parts 1320 and 1322. In other words, the part 1320, such as a material of underfill, can be filled to surround the bonding bumps. Then, another underfill material can be formed to surround the sidewall of the submount (seen i.e. in FIG. 109A as indicated by 1202), as previously described. As a result, the surrounding layer 1214 is composed of two underfill material for more free choices.

[0199] FIGS. 115A-115F are cross-sectional views, schematically illustrating a fabrication process for a LED package, according to another embodiment. In FIG. 115A, for the further alternative structure of LED package, a carrier 1400 is provided. A circuit layer 1402 is formed on the carrier 1400. Actually, the carrier 1400 with the circuit layer 1402 can be formed by any suitable conventional structure without limitation. Herein is just an example. In FIG. 115B, several bonding bumps 404 are formed on the circuit layer 1402 for intended electric connection to the circuit layer 1402. In FIG. 115C, the LED die 1410 having the semiconductor stack layer 406 and the submount 1408 are bonded to the bonding bumps 1404. In FIG. 115D, the surrounding layer 1412, as previously described, is formed to fill around the bonding bumps 1404 and surrounds the sidewall of the LED die 1410. In FIG. 115E, the submount 1408 can be lifted off by, for example, applying the laser for heating the submount 1408. As a result, the semiconductor stack layer 406 of the LED die 1410 is exposed. In FIG. 115F, depending on the actual design, the wavelength conversion layer 1414 can be formed on the exposed semiconductor stack layer 406. Further, an additional layer 1416, including protection layer or any further functional layer, for example, can be formed on the wavelength conversion layer 1414. The additional layer 1416 can even further formed with a lens effect.

[0200] Alternatively with the same concept, FIGS. 116A-116C are cross-sectional views, schematically illustrating a fabrication process. In this embodiment, the submount is not necessary to be lifted off. In FIG. 116A, the semiconductor stack layer 1502 is formed on the submount 1500. The semiconductor stack layer 1502, as previously described, is also usually called epitaxial layer 1502 in short. In FIG. 116B, a removable material layer 1504 is coated on the semiconductor stack layer 1502 with a thickness of, for example, 10 microns or more. Before the LED structure on the submount is sliced into LED die, some additional process may be performed as well. In FIG. 116C, for example, the removable material layer 1504 can be polished to a desired thickness in control. In FIG. 116D, after the LED die is sliced into LED die, the LED dies is bonded to the substrate 1506 by adhesive layer 1508. In FIG. 116E, similar to the previous process, the surrounding layer 1510, such as underfill, is formed to surround the LED die at the peripheral. In FIG. 116F, the removable material layer 1504 is removed, leaving a concave space and the semiconductor stack layer 1502 is exposed. In FIG. 116G, in a packaging process based on bonding wire, the bonding wire 1512 can be bonded to the semiconductor stack layer 1502. In FIG. 116H, a wavelength conversion layer 1514 is filled into the cavity on the semiconductor stack layer 1502. In this manner, the submount 1500 remains in the LED die.

[0201] Further, FIGS. 117A-117B are cross-sectional view, schematically illustrating another packaging process based on flip-chip package, according to an embodiment. In FIG. 16A, based on using the removable material layer, the LED die 1606 with the submount 1604 and the semiconductor stack layer 1602 is connected to the circuit substrate 1600 by bonding pads. The surrounding layer 1612 is formed to surround the sidewall of the LED die. After the removable material layer is removed, a cavity is left and the submount 1604 remains. In FIG. 117B, the wavelength conversion layer 1608 is the filled into the cavity. In this manner, the submount 1604 is not lifted off.

[0202] Further, FIGS. 118A-118B are cross-sectional view, schematically illustrating another packaging process based on flip-chip package, according to an embodiment. In FIG. 118A, if the thickness of the wavelength conversion layer needs to be large, then in continuing to FIG. 117A, the submount 1604 is lifted as well. As a result, the deep cavity is formed. In FIG. 118B, the wavelength conversion layer 1614 is filled into the deep cavity.

[0203] FIG. 119 is a cross-sectional view, schematically illustrating another embodiment of the LED package. In FIG. 119, based on the structure in FIG. 117B, another passivation layer, such as another molding compound 1620 can covers over the LED die for further protection.

[0204] The wavelength conversion layer in previous embodiments is related to the top portion. However, if the side portion is further considered to produce wide angle effect, the wavelength conversion layer can extend to the side portion. FIGS. 120A-120B are cross-sectional views, schematically illustrating another packaging process based on flip-chip package, according to an embodiment. In FIG. 120A, the semiconductor stack layer 1702 on the submount 1700 can be further patterned to have indent region at the side portion. The position of the active layer 1704 in the semiconductor stack layer 1702 can be formed at the upper portion above the indent level. The removable material layer is formed as previously described.

[0205] In FIG. 120B, following the same processes as previously described, the LED die with the submount 1700 is adhered to the circuit substrate 1706. The surrounding layer 1708 surrounds the sidewall of the LED die. The wavelength conversion layer is removed, leaving a cavity space. Then, the wavelength conversion layer 1710 is filled into the cavity space. In this manner, the wavelength conversion layer 1710 can extend to the sidewall of the LED die to surround the active layer 1704.

[0206] Alternatively, the side portion of the wavelength conversion can be modified. FIGS. 121A-121B are cross-sectional views, schematically illustrating another packaging process based on flip-chip package, according to an embodiment. In FIG. 121A, the semiconductor stack layer 1802 with the active later 1804 is formed on the submount 1800. A
trench 1806 can be formed in the semiconductor stack layer 1802 at the peripheral region, surrounding the central portion.

In FIG. 121B, as previously described, the surrounding layer 1808 is formed to surround the sidewall of the LED die. After the removable material layer is removed, a cavity space is left for filling the wavelength conversion layer 1810. Since the wavelength conversion layer 1810 has the side portion, lower than the active layer 1804, the emitted light to the side direction can be also converted by the wavelength conversion layer 1810.

Further alternatively, FIGS. 122A-122J are cross-sectional views, schematically illustrating a fabrication process for a structure, according to an embodiment. In FIG. 122A, a sacrificial substrate 2000 is provided. In FIG. 122B, a sacrificial adhering layer 2002, such as a photoresist, is formed on the sacrificial substrate 2000. The LED dies 2004 are disposed on the sacrificial adhering layer 2002. Here, the LED die may have the submount, as previously described. In FIG. 122D, all the LED dies 2004 are disposed on the sacrificial adhering layer 2002 at the determined positions. In FIG. 122E, the slicing process 2006 is performed to cut into the LED dies 2004 into individual dies. Taking one cut LED die 2004 for descriptions, the LED die 2004 with the sacrificial substrate 2000 and sacrificial adhering layer 2002 is flip-chip adhered on to the substrate 2010 by the adhering layer 2008. The substrate 2010 usually has a circuit structure, as previously described. The proper electric connection for the packaging structure can be known by the one with ordinary skill in the art. In FIG. 122G, a surrounding layer 2012 is formed on the substrate 2010 but the sacrificial substrate 2000 remains exposed. In FIG. 122H, the sacrificial substrate 2000 and the sacrificial adhering layer 2002 are removed to form a concave space 2014, for exposing a top and at least a portion of the sidewall of the LED die 2004. In FIG. 122I, a wire bonding process is performed with bonding wire 2016 for electric connection to the LED die 2004. In FIG. 122J, a wavelength conversion layer 2018, such as fluorescent layer, is filled into the concave space 2014. Since the sacrificial adhering layer 2002 in FIG. 122I is also covering a portion of the sidewall of the LED die 2004, the wavelength conversion layer 2018 can also cover the same portion of the sidewall of the LED die 2004. The luminance at side angle can be improved being more uniform.

FIGS. 123A-123F are cross-sectional views, schematically illustrating the same structure in FIG. 122 but in different fabrication process, according to an embodiment. In FIG. 123A, an LED die 2504 is adhered to a substrate 2500 by an adhering layer 2502. In FIG. 123B, a removable cap 2506 is formed over the top portion of the LED die 2504. In FIG. 123C, a surrounding layer 2508 is formed on the substrate, surrounding the sidewall of the LED die 2504 and the removable cap 2506, in which at least a top of the movable cap 2506 is still exposed. Here, the LED die 2504 may include the submount. In FIG. 123D, the movable cap 2506 is removed. As a result, a concave space 2510 is formed and the LED die 2504 is exposed by the concave space 2510. Also for example, the submount may also be removed as well. However, in this example, the submount remains in this example. In FIG. 123E, the bonding procedure, such as wire bonding, is performed. The bonding wire 2512 is connected to the LED die 2504. In FIG. 123F, the wavelength conversion layer 2514, such as fluorescent material, is filled into the concave space 2510. Since the wavelength conversion layer 2514 also covers at least a portion of sidewall of the LED die 2504, the light illumination is more uniform in wide angle range.

Actually, the above embodiments can be further properly combined to one another for another structure. The present disclosure forms the surrounding layer at least at the sidewall of the submount in LED die in packaging process, wherein the LED die have been formed accomplished. As result, the submount of the LED die in one option can be easily removed and leave a cavity for filling the wavelength conversion layer. Alternatively, the surrounding layer can be also mixed with fillers, for further producing the intended effect for emitting light.

Further, if the submount is intended to remain, the removable material layer can reserve the cavity space for filling the wavelength conversion layer, instead.

Further, in embodiments, when the filled wavelength conversion layer 2618 is uneven (referencing FIG. 124A and FIG. 125A), a planarization process (such as chemical mechanical planarization) can be subjected to the wavelength conversion layer 2618, the metal pads 2612, and the surrounding layer 2610 to form an even top surface of the filled wavelength conversion layer 2618, referring to referring to FIG. 124B and FIG. 125B. After the planarization process, bonding wires 2614 can be bonded to the metal pads 2612 to achieve electrical connection, referring to FIG. 124C and FIG. 125C. Referring to FIG. 126A, the surrounding layer 2610 can consist of two different material, such as a first photoresist layer 2610A and a second photoresist layer 2610B. The first photoresist layer 2610A can serve as a under-fill layer to form the light emitting diode chip bonding structure, and the second photoresist layer 2610B can be optionally removed after filling the wavelength conversion layer 2618, referring to FIG. 126B.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. A method for forming a light emitting diode, comprising:
   - providing a substrate having a first semiconductor layer, a light emitting layer and a second semiconductor layer formed thereon sequentially;
   - performing a patterning process to the first semiconductor layer, the light emitting layer and the second semiconductor layer to define a plurality of protruded portions and a plurality of depressed portions, wherein a remaining portion of the first semiconductor layer covers the substrate in the depressed portions;
   - forming a plurality of first electrodes on the first semiconductor layer in the depressed portions;
   - forming a plurality of second electrodes on the second semiconductor layer in the protruded portions;
   - cutting the substrate along a scribe line located on the depressed portion, for separating a plurality of light emitting diode chips, wherein the light emitting diode chip has a bonding layer and a remained substrate portion, wherein the bonding layer has a plurality of voids,
or a minimum horizontal distance between a surrounding boundary of the light emitting diode chip and the bonding layer is larger than 0;
boning the light emitting diode chip with a carrier substrate via the bonding layer;
forming a surrounding layer on the carrier substrate to surround the light emitting diode;
removing the remained substrate portion to form a cavity; and
filling a wavelength conversion layer into the cavity.
2. A light emitting diode chip, comprising:
a substrate having a boundary;
a first semiconductor layer disposed on the substrate;
a light emitting layer disposed on the first semiconductor layer; and
a second semiconductor layer disposed on the light emitting layer,
wherein the light emitting diode chip is characterized by
only one electrode disposed on the second semiconductor layer, and the electrode and the boundary has a minimum horizontal distance therebetween of at least about 10 μm.
3. The light emitting diode chip of claim 2, wherein the minimum horizontal distance is at least about 20 μm.
4. The light emitting diode chip of claim 2, wherein the electrode is disposed on the second semiconductor layer and exposes a portion of the second semiconductor layer.
5. The light emitting diode chip of claim 4, wherein the electrode is disposed on the second semiconductor layer and exposes a portion of the upper surface of the second semiconductor layer.
6. The light emitting diode chip of claim 5, further comprising a passivation layer disposed on the second semiconductor layer and covers the exposed upper surface of the second semiconductor layer.
7. The light emitting diode chip of claim 2, further comprising a passivation layer disposed on the second semiconductor layer and extends to the sidewalls of the second semiconductor layer, the sidewalls of the light emitting layer and the sidewalls of the protruded portion of the first semiconductor layer, wherein the electrode is disposed on the passivation layer.
8. The light emitting diode chip of claim 2, further comprising a patterned passivation layer disposed between the second semiconductor layer and the electrode, wherein a portion of the electrode directly contacts the second semiconductor layer.
9. The light emitting diode chip of claim 2, wherein the light emitting diode chip has tapered sidewalls.
10. A light emitting diode packaging structure, comprising:
a light emitting diode chip as claimed in claim 2; and
a carrier substrate, wherein the light emitting diode chip is disposed on the carrier substrate.
11. A light emitting diode chip, comprising:
a substrate, having a surrounding boundary;
a first semiconductor layer, a light emitting layer, and a second semiconductor layer subsequently disposed on the substrate; and
electrode islands disposed on the second semiconductor layer.
12. The light emitting diode chip as claimed in claim 11, wherein the ratio between the total area of a top surface of the electrode islands and the area of a top surface of the substrate is equal to or less than 95%.
13. The light emitting diode chip as claimed in claim 11, wherein the electrode island has a thickness which is equal to or more than 1 μm.
14. The light emitting diode chip as claimed in claim 11, further comprising:
a passivation layer disposed on a side wall of the first semiconductor layer, and a side wall of the light emitting layer.
15. The light emitting diode chip as claimed in claim 14, wherein the passivation layer further extends to a side wall of the second semiconductor layer.
16. The light emitting diode chip as claimed in claim 15, wherein the passivation layer further extends to a side wall of a part of the electrode islands.
17. The light emitting diode chip as claimed in claim 11, wherein the electrode island has a cross-section profile in the shape of a semicircle, a polygon, or combinations thereof.
18. The light emitting diode chip as claimed in claim 11, wherein the light emitting diode chip has taper side walls toward the substrate.
19. A light emitting diode package structure, comprising:
a light emitting diode chip having a surrounding boundary; a carrier substrate; and
a bonding layer for bonding the light emitting diode chip with the carrier substrate, wherein the bonding layer has a plurality of voids,
wherein the light emitting diode chip comprises:
a substrate, having the surrounding boundary; and
a first semiconductor layer, a light emitting layer, and a second semiconductor layer subsequently disposed on the substrate, wherein the first semiconductor layer directly contacts the bonding layer.
20. The light emitting diode package structure as claimed in claim 19, wherein the bonding layer comprises:
a first bonding layer, directly contacting the carrier substrate; and
a second bonding layer, directly contacting the second semiconductor layer, wherein at least one of the first bonding layer and the second bonding layer has island structure.
21. The light emitting diode package structure as claimed in claim 20, wherein a minimum horizontal distance between the surrounding boundary and the at least one of the first bonding layer and the second bonding layer is larger than 0.
22. The light emitting diode package structure as claimed in claim 19, further comprising:
a passivation layer disposed on a side wall of the first semiconductor layer, and a side wall of the light emitting layer.
23. The light emitting diode package structure as claimed in claim 19, wherein the light emitting diode chip further comprises an electrode, disposed on the substrate, opposite to the first semiconductor layer.
24. The light emitting diode package structure as claimed in claim 23, wherein there is no opaque wire disposed on the electrode.
25. A light emitting diode package structure, comprising:
a light emitting diode chip having a surrounding boundary; a carrier substrate; and
a bonding layer for bonding the light emitting diode chip with the carrier substrate, wherein the bonding layer has a plurality of voids,
wherein the light emitting diode chip comprises:
a first semiconductor layer; and
a light emitting layer, and a second semiconductor layer
subsequently disposed on the first semiconductor layer,
wherein the first semiconductor layer directly contacts
the bonding layer.

26. A light emitting diode structure, comprising:
a submount having a first surface and a second surface
opposite the first surface;
a stacked structure comprising a first semiconductor layer,
an active layer, and a second semiconductor layer
laminated on the first surface;
a first electrode disposed apart from the stacked structure
on the first surface;
an isolation layer disposed on the first surface, wherein the
isolation layer surrounds the stacked structure and covers
the lateral sides of the active layer; and
a conductive thin film layer for connecting the first elec-
trode to the stacked structure, wherein the conductive
thin film layer covers the stacked structure.

27. The light emitting diode structure as claimed in claim
26, further comprising:
an electrostatic discharge protection element disposed
under the first electrode and embedded in the submount.

28. The light emitting diode structure as claimed in claim
26, further comprising:
a second electrode disposed on the second surface of the
submount.

29. The light emitting diode structure as claimed in claim
26, wherein the first electrode is disposed along all the lateral
sides of the active layer.

30. The light emitting diode structure as claimed in claim
26, wherein the first electrode is disposed along three of the
lateral sides of the stacked structure.

31. The light emitting diode structure as claimed in claim
26, wherein the submount further comprises a cavity on the
first surface for receiving the stacked structure.

32. The light emitting diode structure as claimed in claim
31, further comprising:
a phosphor filling the cavity and covering the stacked struc-
ture.

33. The light emitting diode structure as claimed in claim
26, wherein the conductive thin film layer comprises a plu-
arity of openings corresponding to the stacked structure.

34. The light emitting diode structure as claimed in claim
26, wherein the conductive thin film layer comprises a light
extracting feature corresponding to the stacked structure.

35. The light emitting diode structure as claimed in claim
26, wherein the light transmittance of the conductive thin film
layer for a primary wavelength of the light generated by the
active layer is greater than 60%.

36. The light emitting diode structure as claimed in claim
26, further comprising:
a second electrode disposed apart from the stacked struc-
ture on the first surface of the submount.

37. The light emitting diode structure as claimed in claim
26, further comprising:
an auxiliary electrode disposed on the conductive thin film
layer for connecting the first electrode to the stacked struc-
ture, wherein the auxiliary electrode covers a part of the
conductive thin film layer.

38. A light emitting diode packaging structure, comprising:
a packaging substrate;
at least one stacked structure disposed on the packaging
substrate, wherein the at least one stacked structure com-
prises a first semiconductor layer, an active layer and a
second semiconductor layer laminated on a first surface of
the packaging substrate;
at least one first electrode disposed apart from the at least
one stacked structure on the first surface;
at least one second electrode disposed on the packaging
substrate and electrically connected to the at least one
stacked structure;
an isolation layer disposed on the first surface, wherein the
isolation layer surrounds the at least one stacked struc-
ture and covers the lateral sides of the active layer;
at least one conductive thin film layer for connecting the at
least one first electrode to the at least one stacked struc-
ture, wherein the at least one conductive thin film layer
covers the at least one stacked structure; and
a transparent sealant covering the at least one conductive
thin film layer.

39. The light emitting diode packaging structure as claimed
in claim 38, wherein the packaging substrate is a semi-
conductor substrate, and the light emitting diode packaging
structure further comprises:
at least one electrostatic discharge protection element dis-
posed under the at least one first electrode and embedded in
the packaging substrate.

40. The light emitting diode packaging structure as claimed
in claim 38, wherein the second electrode is disposed between
the packaging substrate and the stacked structure.

41. The light emitting diode packaging structure as claimed
in claim 38, wherein the at least one first electrode is disposed
along all the lateral sides of the active layer.

42. The light emitting diode packaging structure as claimed
in claim 38, wherein the at least one first electrode is disposed
along three of the lateral sides of the at least one stacked
structure.

43. The light emitting diode packaging structure as claimed
in claim 38, further comprising:
an interface layer disposed between the least one stacked
structure and the packaging substrate.

44. The light emitting diode packaging structure as claimed
in claim 38, wherein the at least one conductive thin film layer
comprises a plurality of openings corresponding to the at least
one stacked structure.

45. The light emitting diode packaging structure as claimed
in claim 38, wherein the at least one conductive thin film layer
comprises a light extracting feature corresponding to the at
least one stacked structure.

46. The light emitting diode packaging structure as claimed
in claim 38, wherein the light transmittance of the at least one
conductive thin film layer for a primary wavelength of the
light generated by the active layer is greater than 60%.

47. The light emitting diode packaging structure as claimed
in claim 38, further comprising:
at least one auxiliary electrode disposed on the at least one
conductive thin film layer for connecting the at least one
first electrode to the at least one stacked structure,
wherein the at least one auxiliary electrode covers a part
of the at least one conductive thin film layer.

48. The light emitting diode packaging structure as claimed
in claim 38, wherein the packaging substrate comprises two
through holes extending from the first surface to a second
surface opposite the first surface, and the two through holes correspond to the first electrode and the second electrode respectively.

49. A light emitting diode structure, comprising:
a substrate with a light emitting semiconductor stacked layer formed thereon;
a surrounding layer located on the substrate to surround the light emitting semiconductor stacked layer, constituting a cavity; and
a wavelength conversion layer filled into the cavity.

50. The light emitting diode structure as claimed in claim 49, wherein the wavelength conversion layer further comprises a filler.

51. A method for fabricating a light emitting diode structure, comprising:
providing a light emitting diode having a bonding material, a stacked layer and a substrate;
bonding the light emitting diode on a carrier via the bonding material;
forming a surrounding layer to surround the light emitting diode;
removing the substrate to form a cavity; and
filling a wavelength conversion layer into the cavity.

52. The method as claimed in claim 51, further comprising:
performing a planarization process to the surrounding layer and the wavelength conversion layer, forcing a top surface of the wavelength conversion layer being perpendicular to sidewalls of the surrounding layer.