(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 April 2011 (21.04.2011)

PCT

(10) International Publication Number
WO 2011/044833 A1

(51) International Patent Classification:
H01L 23/52 (2006.01) *H01L 23/522* (2006.01)

(21) International Application Number:
PCT/CN2010/077670

(22) International Filing Date:
12 October 2010 (12.10.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
200910205812.9 14 October 2009 (14.10.2009) CN

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: SEMICONDUCTOR DEVICE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

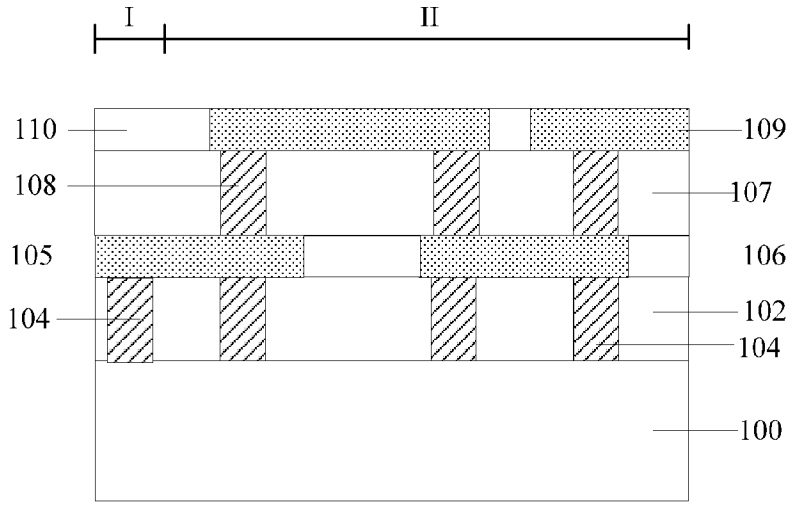

Figure 9

(57) Abstract: A semiconductor device structure and a method for manufacturing the same are provided. The semiconductor device structure includes a semiconductor substrate having a device area and a virtual area, the virtual area being located at an edge of the semiconductor substrate; a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in the virtual area and electrically connected to the substrate; a metal layer disposed in contact with the first and second plugs to provide a conductive path; wherein the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

WO 2011/044833 A1

Published:

— *with international search report (Art. 21(3))*

SEMICONDUCTOR DEVICE STRUCTURE AND METHOD FOR MANUFACTURING THE SAME

Field of the Disclosure

[0001] The present disclosure relates to the field of manufacturing a semiconductor device and, more particularly, to a semiconductor device structure in which accumulated charges are released by a virtual conductive plug connected with a semiconductor substrate, and a method for manufacturing the same.

Background of the Disclosure

[0002] Along with rapid development of Ultra Large Scale Integration (ULSI) technologies, miniaturization of the layout design principle of a semiconductor device has been continuously advancing, the number of integrated elements has been increasing, the wiring of a large scale integrated circuit has been increasingly complicated, and the metal wiring has become finer, thinner and narrower. In this case, attention has been paid to a multilayer interconnection formed, in part, by deposition of a conductive plug in a contact hole as one interconnection technology playing a role in improving a product yield.

[0003] In a common interconnection line process used during existing manufacturing of a semiconductor product, a conductive plug is formed to interconnect metal lines at respective layers, which is outlined below.

[0004] Referring to Figure 1, a semiconductor substrate 1 includes a first insulation layer 2 with trenches 3 formed by etching, with the first insulation layer 2 and the trenches 3 provided on a surface of the semiconductor substrate 1. The semiconductor substrate 1 may be either a logic structure with layers of metal lines or a metal line layer on the surface of a layer of logic structure, and the first insulation layer 2 electrically isolates the current of the generated semiconductor product so that it flows only through an interconnection line.

[0005] Referring to Figure 2, the trenches 3 are filled up with a conductive substance layer to form first conductive plugs 4, wherein the material of the conductive substance may be tungsten, copper, etc. The first conductive plugs 4 are connected with the logic structure with layers of metal lines or with the metal line layer on the surface of a layer of logic structure, both of which may be formed in the semiconductor substrate 1. A process of forming the first conductive plugs 4 is as follows. The conductive substance layer is deposited (not shown) on the surface of the first insulation layer 2 to fill up the

trenches 3 with the conductive substance layer, using a chemical vapor deposition method. Next, the conductive substance layer on the surface of the first insulation layer 2 is removed using a chemical mechanical polishing method to leave only the conductive substance layer in the trenches 3.

[0006] Referring to Figure 3, first metal wiring layers 5, comprising a material of aluminum or copper, etc., are deposited on the surface of the first insulation layer 2 to cover the first conductive plugs 4. The first metal wiring layers 5 are isolated by first medium layers 6, where the first metal wiring layers 5 and the first medium layers 6 have the same thickness.

[0007] Referring to Figure 4, a second insulation layer 7 is deposited on the first metal wiring layers 5 and the first medium layers 6. The second insulation layer 7 is etched to form trenches therein traversing the thickness thereof to expose the first metal wiring layers 5. Using a chemical vapor deposition method, a conductive substance is deposited on the second insulation layer 7 to fill up the trenches with the conductive substance. Using a chemical mechanical polishing method, the conductive substance layer on the second insulation layer 7 is removed to leave only the conductive substance in the trenches. Thus, second conductive plugs 8 are formed, connected with the first metal wiring layers 5. Second metal wiring layers 9, comprising a material of aluminum, copper, etc., are deposited on the surface of the second insulation layer 7 to cover the second conductive plugs 8. The second metal wiring layers 9 are isolated by second medium layers 10, where the second metal wiring layers 9 and the second medium layers 10 have the same thickness.

[0008] More information on the foregoing process flow can be found in Chinese Patent Application No. 03109677.8.

[0009] In the existing process of forming an interconnection line(s) discussed above, plasma etching used for forming conductive plugs may result in residual charges being accumulated gradually in the metal wiring layers, and a discharging phenomenon may be induced under some conditions. Therefore, a discharging phenomenon between the metal wiring layers and the semiconductor substrate may arise during a subsequent test process, resulting in a failure of the test.

Summary of the Disclosure

[0010] A semiconductor device structure and a method for manufacturing the same for preventing residual charges due to plasma etching from being gradually accumulated within metal wiring layers during formation of a conductive plug through etching is

provided.

[0011] A semiconductor device structure, including a semiconductor substrate having a device area and a virtual area, the virtual area being located at an edge of the semiconductor substrate; a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in the virtual area and electrically connected to the substrate; a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween; wherein the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

[0012] Optionally, the material of the metal layer is copper or aluminum. The metal layer is formed using an electroplating method or a chemical vapor deposition method.

[0013] Optionally, the material of the insulation layer is silicon dioxide or doped silicon oxide. The thickness of the insulation layer is less than 10000Å. The insulation layer is formed using chemical vapor deposition method.

[0014] A method for manufacturing a semiconductor device structure, includes forming a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in a virtual area located at an edge of a semiconductor substrate and electrically connected to the substrate; forming a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween; wherein the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

[0015] Optionally, the material of the metal layer is copper or aluminum.

[0016] Optionally, the material of the insulation layer is silicon dioxide or doped silicon oxide. The thickness of the insulation layer is less than 10000Å.

[0017] A semiconductor device structure, including a semiconductor substrate having a device area and a virtual area, the virtual area being located at an edge of the semiconductor substrate; a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in the virtual area and electrically connected to the substrate; a first insulating layer provided on the substrate surface and between the first and second conductive plugs; a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween; a second insulating layer formed on the metal layer; wherein the first conductive plug passes through the first and second insulating layers to provide the electrical connection to the substrate, and the first

conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

[0018] A method for manufacturing a semiconductor device structure, including forming a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in a virtual area located at an edge of a semiconductor substrate and electrically connected to the substrate; forming a first insulating layer provided on the substrate surface and between the first and second conductive plugs; forming a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween; forming a second insulating layer formed on the metal layer; wherein the first conductive plug passes through the first and second insulating layers to provide the electrical connection to the substrate, and the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

[0019] Any of the metal wiring layers are extended into a virtual area for direct connection with a semiconductor substrate in the virtual area through a virtual conductive plug in an insulation layer. The semiconductor substrate has a function of grounding, and the direct connection of the metal wiring layers with the semiconductor substrate can release charges accumulated in the metal wiring layers and the insulation layer during etching to thereby avoid both a crystal lattice defect and device damage due to the residual charges.

Brief Description of the Drawings

[0020] Figure 1 to Figure 4 are schematic diagrams of manufacturing an interconnection line structure in the prior art;

[0021] Figure 5 is a flow chart of an embodiment of manufacturing a semiconductor device structure including an interconnection line structure according to the invention;

[0022] Figure 6 to Figure 9 are schematic diagrams of a first embodiment of forming an interconnection line structure according to the invention; and

[0023] Figure 10 to Figure 13 are schematic diagrams of a second embodiment of forming an interconnection line structure according to the invention.

Detailed Description of Embodiments

[0024] In order to address one or more of the above discussed problem, methods and apparatuses that extend metal wiring layers into a virtual area to provide a direct connection with the semiconductor substrate in the virtual area through a virtual conductive plug in an insulation layer are provided. Such apparatuses and methods provide for a semiconductor substrate with a grounding function. This direct connection of the metal wiring layer with the semiconductor substrate can provide a release of charges accumulated in the metal wiring layer and the insulation layer during etching to avoid both a crystal lattice defect and device damage due to the residual charges.

[0025] Figure 5 is a flow chart of an embodiment of manufacturing a semiconductor device structure including an interconnection line structure. Step S11 is performed to prepare a semiconductor substrate divided into a device area and a virtual area, which is located at an edge of the semiconductor substrate. Step S12 provides for several alternately formed insulation layers. The alternately formed insulation layers are provided with conductive plugs in the device area and in the virtual area, which are formed to traverse the thickness thereof, and several metal wiring layers provided on the semiconductor substrate. In step S13, the respective metal wiring layers are connected to conductive plugs in the device area, such that the metal wiring layers directly connect with the semiconductor substrate through the conductive plugs in the virtual area.

[0026] Various embodiments will be discussed hereinafter with reference to the drawings.

[0027] Figure 6 to Figure 9 are schematic diagrams of a first embodiment of forming an interconnection line structure. As illustrated in Figure 6, a semiconductor substrate 100 is prepared, which may be either a logic structure with layers of metal lines or a metal line layer on the surface of a layer of logic structure. The semiconductor substrate 100 is divided into a device area II, and a virtual area I which is located at an edge of the semiconductor substrate 100. A first insulation layer 102 is formed on the surface of the semiconductor substrate 100. The first insulation layer 102 may, for example, be formed having a thickness of less than 10000Å. The first insulation layer 102 may be formed using, for example, a chemical vapor deposition method. In the present embodiment, the material of the first insulation layer 102 may be silicon oxide. Alternatively, the first insulation layer 102 may be formed of doped silicon oxide. One or more first trenches 103 traversing the thickness of the first insulation layer 102 are formed in the device area II, and one or more other first trenches 103 traversing the thickness of the first insulation layer 102 are formed in the virtual area I. The number and arrangement of trenches 103

illustrated in Figure 6 is exemplary only. It will now be apparent to one of ordinary skill in the art that the multiple trenches 103 may be provided to the substrate 100 as a different number with a different arrangement, without departing from the scope of the discussion herein. For example, more than one trench 103 may be provided in virtual area I.

[0028] With reference to Figure 6, the first insulation layer 102 provides electric isolation, so that current of a resulting semiconductor product will flow only through an interconnection line. A formation process consistent with the above embodiment is as follows. A photoresist layer (not shown) is spin-coated on the first insulation layer 102 and subject to exposure and development processes to define corresponding first trench patterns, corresponding to the first trenches 103, on the photoresist layer in the virtual area I and the device area II. The first insulation layer 102 is etched using the photoresist layer as a mask along the trench patterns. For example, a dry etching method may be used to etch the first insulation layer 102 and expose the semiconductor substrate 100 using the photoresist layer as a mask. For example, C_4F_8 may be used as the etching gas for the dry etching method. A dose of the etchant may depend upon the thickness of the first insulation layer 102.

[0029] Figure 7 illustrates another step in the formation of a semiconductor device consistent with the first embodiment. As illustrated in Figure 7, the first trenches 203 in the virtual area I are filled with a conductive substance layer to form first conductive plugs 104; and the first trenches 203 in the device area II are filled with the same conductive substance layer to form others of the first conductive plugs 104. The first conductive plugs 104 provide electrical connections to the substrate 100.

[0030] With further reference to Figure 7, a formation process consistent with the above described embodiment is described. First, a first conductive substance layer is deposited (not shown) on the first insulation layer 102 to fill up the first trenches 103 with the first conductive substance layer. Next, the first conductive substance layer on the first insulation layer 102 is removed to form the first conductive plugs 104. A chemical machine polishing method may, for example, be used to form the first conductive plugs 104 from the first conductive substance layer in the first trenches 103. The material of the first conductive substance layer in the present embodiment may be tungsten, copper, etc. Tungsten may be deposited, for example, using a physical vapor deposition method, wherein a solid target of tungsten is bombarded using plasma, so that tungsten is deposited as a film in the first trenches 103.

[0031] Figure 8 illustrates a further step in the formation of a semiconductor device consistent with the first embodiment. As illustrated in Figure 8, first metal wiring layers

105 are provided on the surface of the first insulation layer 102 to cover the first conductive plugs 104. A part of the first metal wiring layers 105 covers the first conductive plugs 104 in the virtual area I. First metal wiring layers 105 are isolated by first medium layers 106, the first medium layers 106 having the same thickness as the first metal wiring layer 105. First metal wiring layers 105 may comprise, for example, tungsten, aluminum or copper, etc.

[0032] With further reference to Figure 8, in order to form the first metal wiring layers 105, a first metal layer of a material, for example, tungsten, aluminum or copper, etc, is formed on the first insulation layer 102 (not shown). The first metal layer may be formed, for example, using a physical vapor deposition method. A photoresist layer (not shown) is provided on the surface of the first metal layer. In order to prevent the photoresist from being stripped due to insufficient adhesion of the photoresist to, for example, tungsten, an adhesive layer (not shown) may be formed on the surface of the first metal layer before coating the photoresist, and subsequently the photoresist layer can be coated on the adhesive layer. A Dielectric Anti-Reflection Coating (DARC) layer, e.g., SiON, may be formed the material of the adhesive layer. Next the photoresist layer is exposed and developed to form first metal wiring pattern corresponding to the first metal wiring layers 105. Then the first metal layer is etched using the photoresist layer as a mask along the first metal wiring pattern to form the first metal wiring layers 105 connected with the first conductive plugs 104. The first metal layer can be etched, for example, using a reactive ion etching method. The first medium layers 106 are formed above the first metal wiring layers 105 and in the gaps therebetween. The first medium layers 106 may be formed, for example, using a chemical vapor deposition method. The first medium layers 106 on the first metal wiring layers 105 are removed, for example, using a chemical mechanical polishing, to leave the first medium layers 106 in the gaps between the first metal wiring layers 105.

[0033] In an alternative embodiment, the first metal wiring layers 105 may comprise copper. The first medium layers 106 may be formed on the first insulation layer 102 using, for example, a chemical vapor deposition method. A photoresist layer is formed on the first medium layers 106 using, for example, a spin-coating method, and subjected to exposure and development processes to define the first metal wiring patterns on the photoresist layer (not shown). The first medium layers 106 are etched using the photoresist layer as a mask along the first metal wiring patterns until the first conductive plugs 104 and a part of the first insulation layer 102 are exposed to form first metal wiring openings. A first metal layer (not shown) comprised of copper is formed on the first medium layers 106 using, for example, an electroplating method, to fill up the first metal

wiring openings with the first metal layer. The first metal layer on the first medium layers 106 is removed using, for example, a chemical mechanical polishing method that leaves the first metal layer in the first metal wiring openings, thus forming the first metal wiring layers 105.

[0034] Figure 9 illustrates yet another step in the formation of a semiconductor device consistent with the first embodiment. As illustrated in Figure 9, a second insulation layer 107 is deposited on the first metal wiring layers 105 and the first medium layers 106. The second insulation layer 107 may have, for example, a thickness of less than 10000Å. Second conductive plugs 108 are formed in the second insulation layer 107 to connect second metal wiring layers 109 to the first metal wiring layers 105. The second metal wiring layers 109 are isolated by second medium layers 110. The number and arrangement of the second conductive plugs 108 is exemplary only. One or more conductive of the second conductive plugs 108 can be provided.

[0035] With further reference to Figure 9, the method of forming the second insulation layer 107 is described next. The second insulation layer 107 is etched using, for example, a dry etching method, to form therein second trenches, corresponding to the second conductive plugs 108, traversing the thickness thereof to expose the first metal wiring layers 105. A conductive substance is deposited (not shown) on the second insulation layer 107 using, for example, a chemical vapor deposition method, to fill up the second trenches with the conductive substance; and the conductive substance layer on the second insulation layer 107 is removed using, for example, a chemical mechanical polishing method, to leave only the conductive substance in the second trenches, thus forming the second conductive plugs 108 connected with the first metal wiring layers 105. The second metal wiring layers 109 comprising a material of tungsten, aluminum, or copper, etc., are deposited on the surface of the second insulation layer 107 to cover the second conductive plugs 108 with the second metal wiring layers 109 for connection with the first metal wiring layers 105 through the second conductive plugs 108. The second metal wiring layers 109 are isolated by the second medium layers 110, the second medium layers 110 having, for example, the same thickness as second metal wiring layers 109.

[0036] In the present embodiment, the second metal wiring layers 109 may be formed, for example, of tungsten. A process of formation consistent with such an embodiment follows. The second metal layer comprising tungsten is formed on the second insulation layer 107 using, for example, a physical vapor deposition method. A photoresist layer is provided on the surface of the second metal layer. Next the photoresist layer is exposed and developed to form second metal wiring patterns. Then the second metal layer is

etched using the photoresist layer as a mask along the second metal wiring pattern to form the second metal wiring layers 109 connected with the second conductive plugs 108. Tungsten can be etched in a reactive ion etching, for example. The second medium layers 110 are formed on the second metal wiring layers 109 and in the gaps therebetween in a chemical vapor deposition method, and the second medium layers 110 on the second metal wiring layers 109 are removed in the chemical mechanical polishing.

[0037] In an alternative embodiment, the second metal wiring layers 109 may be formed, for example, of copper. A process of formation consistent with such an embodiment follows. The second medium layers 110 are formed on the second insulation layer 107 using, for example, a chemical vapor deposition method. Next, a photoresist layer is formed on the second medium layers 110, using a spin-coating method, and subject to exposure and development processes to define the second metal wiring patterns on the photoresist layer. The second medium layers 110 are etched using the photoresist layer as a mask along the second metal wiring patterns until the second conductive plugs 108 and a part of the second insulation layer 107 are exposed to form second metal wiring openings. The second metal layer comprising copper is formed on the second medium layers 110 by an electroplating method to fill up the second metal wiring openings with the second metal layer; and the second metal layer on the second medium layers 110 is removed using, for example, a chemical mechanical polishing method, to leave the second metal layer in the second metal wiring openings.

[0038] Further to the embodiment, several insulation layers and metal wiring layers including conductive plugs can also be formed sequentially at an interval on the second metal wiring layers 109 and the second medium layers 110.

[0039] The respective metal wiring layers in the device area II are connected with the semiconductor substrate 100 through the first metal wiring layers 105 and the first conductive plugs 104 in the virtual area I. In such a configuration, the semiconductor substrate 100 has a grounding function, capable of timely release of charges accumulated in the metal wiring layers and the insulation layers during formation of the conductive plugs by etching, thus avoiding both a crystal lattice defect and a device damage due to the residual charges.

[0040] Figure 10 to Figure 13 are schematic diagrams of a second embodiment of forming an interconnection line structure. As illustrated in Figure 10, a semiconductor substrate 200, which may be either a logic structure with layers of metal lines or a metal line layer on the surface of a layer of logic structure, is provided. The semiconductor substrate 200 is divided into a device area II, and a virtual area I which is located at an

edge of the semiconductor substrate. A first insulation layer 202 is formed on the surface of the semiconductor substrate 200. The insulation layer 202 may be formed using, for example, a chemical vapor deposition method. The material of the first insulation layer 202 may be formed using, for example, a chemical vapor deposition method. The material of the first insulation layer 202 may be, for example, silicon oxide or doped silicon dioxide. First trenches 203 traversing the thickness of the first insulation layer 202 are formed in the device area II, and the first trenches 203 traversing the thickness of the first insulation layer 202 are also formed in the virtual area I. The number and arrangement of trenches 203 illustrated in Figure 10 is exemplary only. It will now be apparent to one of ordinary skill in the art that the substrate 200 may be provided with trenches 203 different in number and arrangement without departing from the scope of the discussion herein.

[0041] With reference to Figure 10, the insulation layer 202 provides electric isolation so that current of a resulting semiconductor product will flow only through an interconnection line. A formation process consistent with the above embodiment is as follows. A photoresist layer (not shown) is spin-coated on the first insulation layer 202 and subject to exposure and development processes to define corresponding first trench patterns, corresponding to the first trenches 203, in the virtual area I and the device area II. The first insulation layer 202 is etched using the photoresist layer as a mask along the trench patterns until the semiconductor substrate 200 is exposed. The first insulation layer 202 may be etched, for example, using a dry etching method. A corresponding etching gas may be selected based on the material of the first insulation layer 202. For example, C_4F_8 may be used if the first insulation layer is provided as silicon oxide. A dose of the etchant may depend upon the thickness of the first insulation layer 202.

[0042] Figure 11 illustrates another step in the formation of a semiconductor device consistent with the second embodiment. As illustrated in Figure 11, the first trenches 203 in the virtual area I are filled with a first conductive substance layer to form first conductive plugs 204; and the first trenches 203 in the device area II are filled with the conductive substance layer to form the first conductive plugs 204 therein. The first conductive plugs 204 provide an electrical connection to the substrate 200.

[0043] The material of the first conductive substance layer in the present embodiment may be tungsten or copper, etc. Tungsten may be deposited, for example, using a physical vapor deposition method, wherein a solid target of tungsten is bombarded using plasma, so that tungsten is deposited as a film in the first trenches 203. Then the first conductive substance layer on the first insulation layer is removed by, for example, a chemical mechanical polishing method to leave the first conductive substance layer in the

first trenches 203.

[0044] Figure 12 illustrates another step in the formation of a semiconductor device consistent with the second embodiment. As illustrated in Figure 12, first metal wiring layers 205 comprising, for example, a material of tungsten, aluminum or copper, etc., are deposited on the surface of the first insulation layer 202 to cover the first conductive plugs 204 with the first metal wiring layers 205. The first metal wiring layers 205 are isolated by first medium layers 206 with the same thickness. A part of the first metal wiring layers 205 covers the first conductive plugs 204 in the virtual area I.

[0045] Specific methods for forming the first metal wiring layers 205 of different materials have been described in the first embodiment, and repeated descriptions thereof will be omitted here.

[0046] Figure 13 illustrates yet another step in the formation of the semiconductor device consistent with the second embodiment. As illustrated in Figure 13, a second insulation layer 207 is formed on the first metal wiring layers 205 and the first medium layers 206. The second insulation layer 207 may be formed, for example, having a thickness of less than 10000Å. Second conductive plugs 208a and third conductive plugs 208b are provided in connection with second metal wiring layers 209. The second metal wiring layers 209 may comprise, for example, a material of tungsten, aluminum or copper, etc. The second metal wiring layers 209 are provided on the second insulating layer 207 with portions of the second metal wiring layers 209 provided in contact with the second conductive plugs 208a and the third conductive plugs 208b. The second metal wiring layers 209 in the device area II are connected with the first metal wiring layers 205 through the second conductive plugs 208a and the second metal wiring layers 209 in the virtual area I are connected with the semiconductor substrate 200 through the third conductive plugs 208b. The second conductive plugs 208a in the device area II are formed connected with the first metal wiring layers 205 and the third conductive plugs 208b in the virtual area I are formed connected with the semiconductor substrate 200. The second metal wiring layers 209 are isolated by second medium layers 210. The second metal wiring layers 209 and the second medium layers 210 may, for example, have the same thickness. It will now be apparent to one of ordinary skill in the art that although only one example of the third conductive plugs 208b is illustrated in Figure 13, other plugs 208b may also be provided in the virtual area I in other portions of the substrate 200.

[0047] With further reference to Figure 13, a formation process consistent with the above embodiment is as follows. The second insulating layer 207 is formed on the first

metal wiring layers 205 and the first medium layers 206. The second insulation layer 207 in the device area II is etched using, for example, a dry etching method to form therein second trenches, corresponding to the second conductive plugs 208a, traversing the thickness of the second insulating layer 207 to expose the first metal wiring layers 205. The second insulation layer 207, the first medium layers 206 and the first insulation layer 202 in the virtual area I are etched using, for example, the dry etching method until the semiconductor substrate 200 is exposed to form third trenches, corresponding to the third conductive plugs 208b. A conductive substance is deposited (not shown) on the second insulation layer 207 using, for example, a chemical vapor deposition method, to fill up the second and third trenches with the conductive substance. The conductive substance layer on the second insulation layer 207 is removed using, for example, a chemical mechanical polishing method, to leave only the conductive substance in the second and third trenches, thus forming the second conductive plugs 208a in the device area II connected with the first metal wiring layers 205 and the third conductive plugs 208b in the virtual area I connected with the semiconductor substrate 200.

[0048] Specific methods for forming the second metal wiring layers 209 of different materials have been described in the first embodiment, and repeated descriptions thereof will be omitted here.

[0049] The metal wiring layers 205 and 209 in the device area II are connected with the semiconductor substrate 200 through the first metal wiring layers 205 and the first conductive plugs 204 in the virtual area I, and also may be connected to the substrate 200 through the second metal wiring layers 209 and the third conductive plugs 208b in the virtual area I. The semiconductor substrate 200 has a function of grounding, thus releasing charges accumulated in the metal wiring layers and the insulation layers during formation of the conductive plugs through etching, and thereby avoids both a crystal lattice defect and a device damage due to the residual charges.

[0050] Further to this embodiment, several insulation layers including conductive plugs and metal wiring layers can also be formed sequentially at an interval on the second metal wiring layers 209 and the second medium layers 210. Each of the metal wiring layers 205 and 209 can be directly connected with the semiconductor substrate 200 through the conductive plugs.

[0051] Although the invention has been disclosed as above in the preferred embodiments thereof, the invention will not be limited thereto. Any skilled in the art can make various modifications and variations thereto without departing from the spirit and scope of the invention, and accordingly the claimed scope of the invention shall be

defined dependent upon the appended claims.

CLAIMS

1. A semiconductor device structure, comprising:

a semiconductor substrate having a device area and a virtual area, the virtual area being located at an edge of the semiconductor substrate;

a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in the virtual area and electrically connected to the substrate;

a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween;

wherein the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

2. The semiconductor device structure according to claim 1, wherein the metal layer is copper or aluminum.

3. The semiconductor device structure according to claim 1, further comprising:

an insulating layer provided between the first conductive plug and the second conductive plug,

wherein the insulation layer is formed of silicon dioxide or doped silicon oxide.

4. The semiconductor device structure according to claim 3, wherein the thickness of the insulation layer is less than 10000Å.

5. A method for manufacturing a semiconductor device structure, comprising:

forming a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in a virtual area located at an edge of a semiconductor substrate and electrically connected to the substrate;

forming a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween;

wherein the first conductive plug, the second conductive plug, and metal layer

form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

6. The method for manufacturing the semiconductor device structure according to claim 5, wherein the metal layer is copper or aluminum.

7. The method for manufacturing the semiconductor device structure according to claim 5 or 6, wherein the metal layer is formed using an electroplating method or a chemical vapor deposition method.

8. The method for manufacturing the semiconductor device structure according to claim 5, further comprising:

forming an insulating layer between the first conductive plug and the second conductive plug,

wherein the insulation layer is formed of silicon dioxide or doped silicon oxide.

9. The method for manufacturing the semiconductor device structure according to claim 8, wherein the thickness of the insulation layer is less than 10000Å.

10. The method for manufacturing the semiconductor device structure according to claim 9, wherein the insulation layer is formed using a chemical vapor deposition method.

11. A semiconductor device structure, comprising:

a semiconductor substrate having a device area and a virtual area, the virtual area being located at an edge of the semiconductor substrate;

a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in the virtual area and electrically connected to the substrate;

a first insulating layer provided on the substrate surface and between the first and second conductive plugs;

a metal layer disposed in contact with the first and second plugs to provide a

conductive path therebetween;

a second insulating layer formed on the metal layer;

wherein the first conductive plug passes through the first and second insulating layers to provide the electrical connection to the substrate, and

the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

12. The semiconductor device structure according to claim 11, wherein the metal layer is copper or aluminum.

13. The semiconductor device structure according to claim 11, wherein the first and second insulation layers are formed of silicon dioxide or doped silicon oxide.

14. The semiconductor device structure according to claim 13, wherein the thickness of the first and second insulation layers is less than 10000Å.

15. A method for manufacturing a semiconductor device structure, comprising:

forming a first conductive plug and a second conductive plug, wherein the first conductive plug is provided in a virtual area located at an edge of a semiconductor substrate and electrically connected to the substrate;

forming a first insulating layer provided on the substrate surface and between the first and second conductive plugs;

forming a metal layer disposed in contact with the first and second plugs to provide a conductive path therebetween;

forming a second insulating layer formed on the metal layer;

wherein the first conductive plug passes through the first and second insulating layers to provide the electrical connection to the substrate, and

the first conductive plug, the second conductive plug, and metal layer form an interconnection line structure electrically grounded through a portion of the substrate in the virtual area via the first conductive plug.

16. The method for manufacturing the semiconductor device structure according to claim 15, wherein the metal layer is copper or aluminum.

17. The method for manufacturing the semiconductor device structure according to claim 15 or 16, wherein the metal layer is formed using an electroplating method or a chemical vapor deposition method.

18. The method for manufacturing the semiconductor device structure according to claim 15, wherein the first and second insulation layers are formed of silicon dioxide or doped silicon oxide.

19. The method for manufacturing the semiconductor device structure according to claim 18, wherein the thickness of the first and second insulation layers is less than 10000Å.

20. The method for manufacturing the semiconductor device structure according to claim 19, wherein the first and second insulation layers are formed using a chemical vapor deposition method.

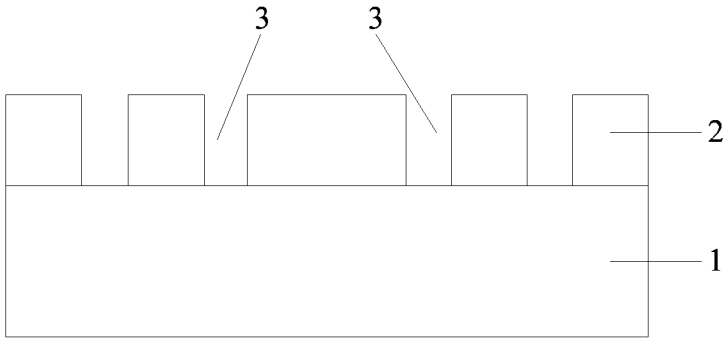

Figure 1

Prior Art

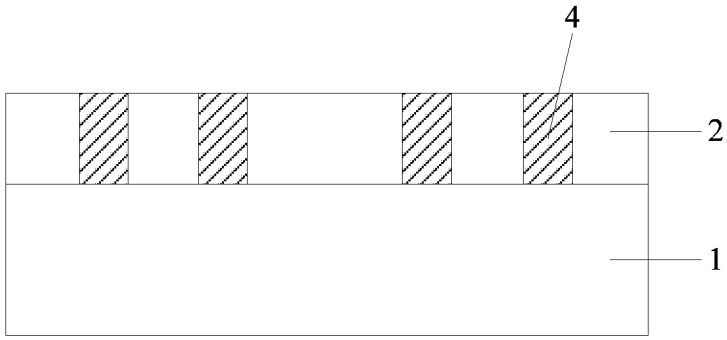

Figure 2

Prior Art

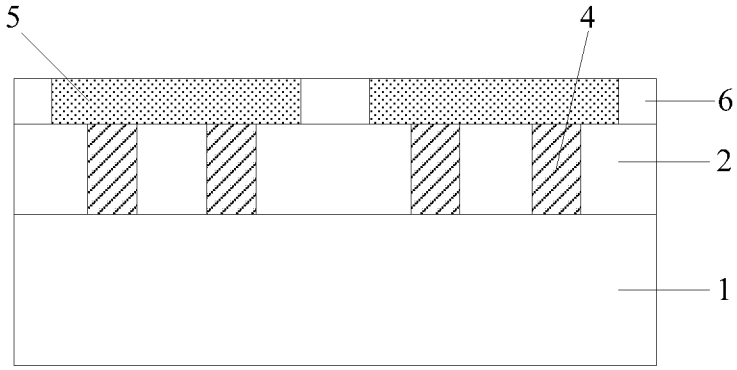

Figure 3

Prior Art

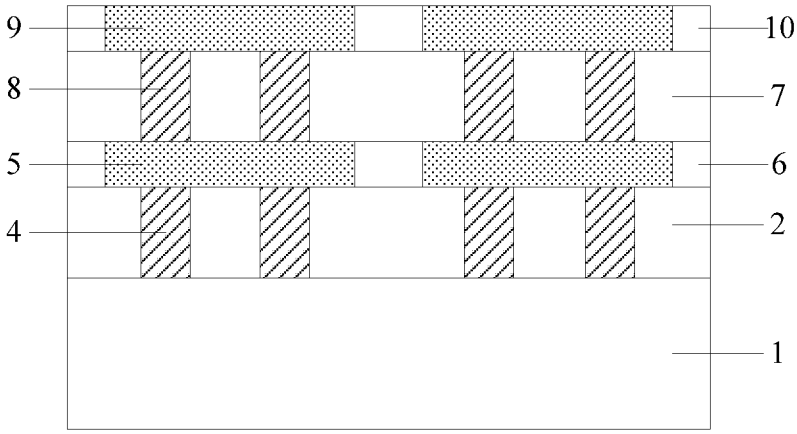

Figure 4

Prior Art

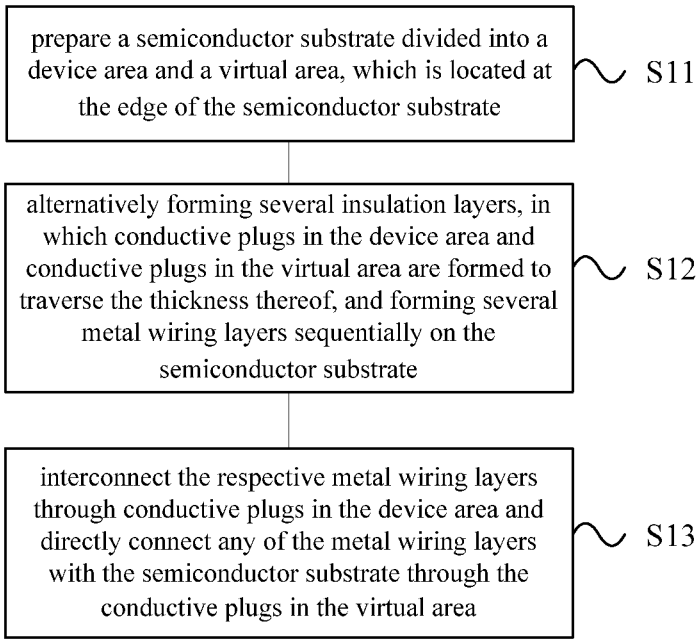

Figure 5

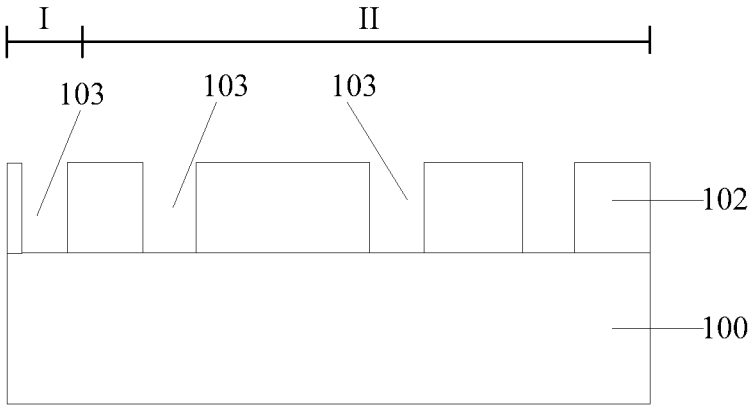

Figure 6

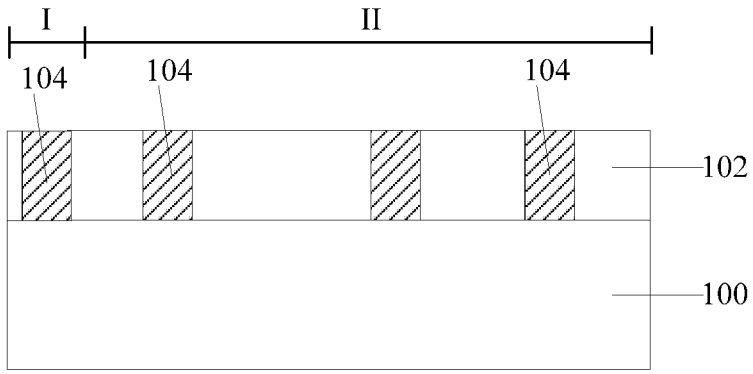

Figure 7

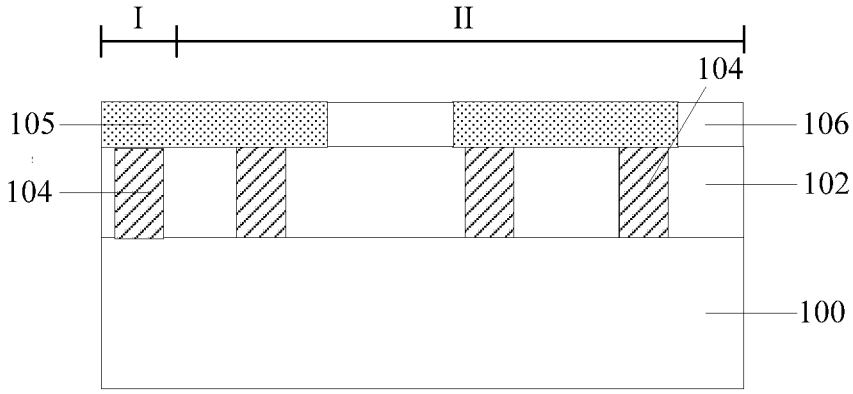

Figure 8

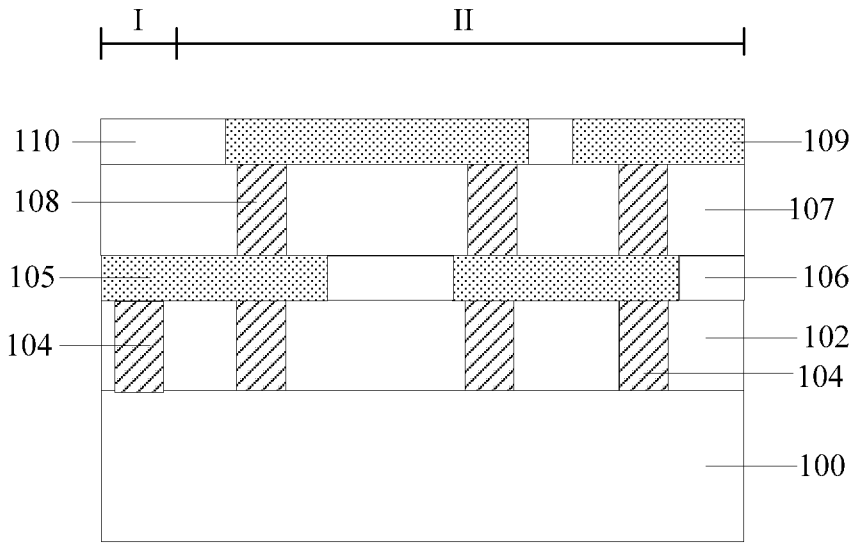

Figure 9

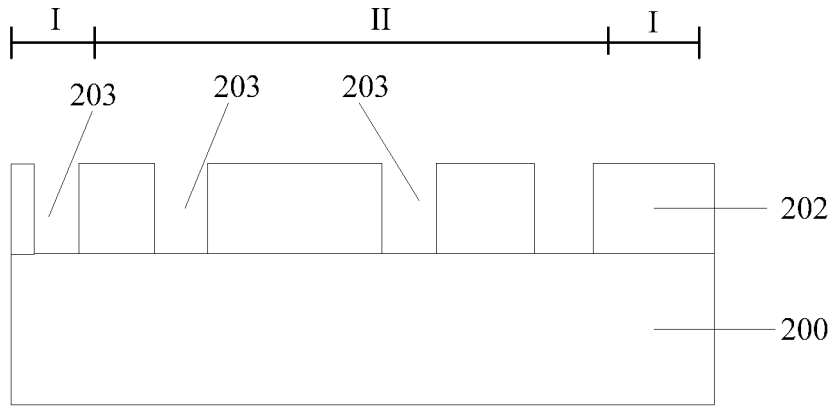

Figure 10

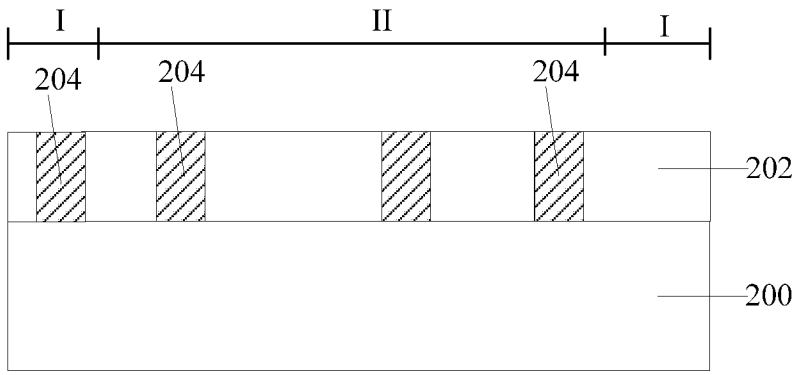

Figure 11

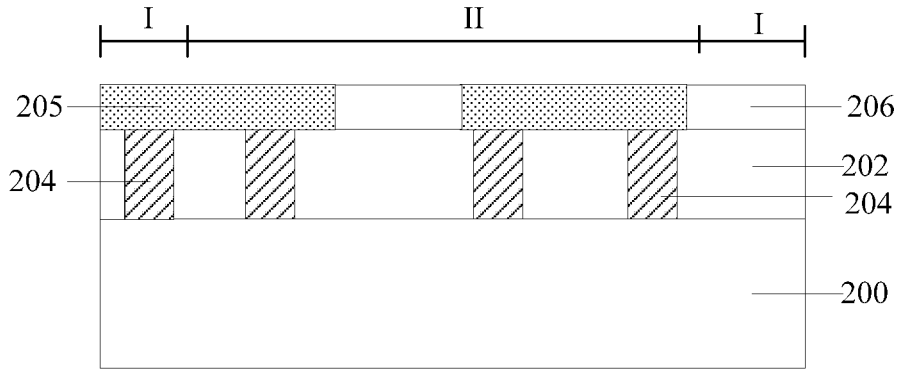

Figure 12

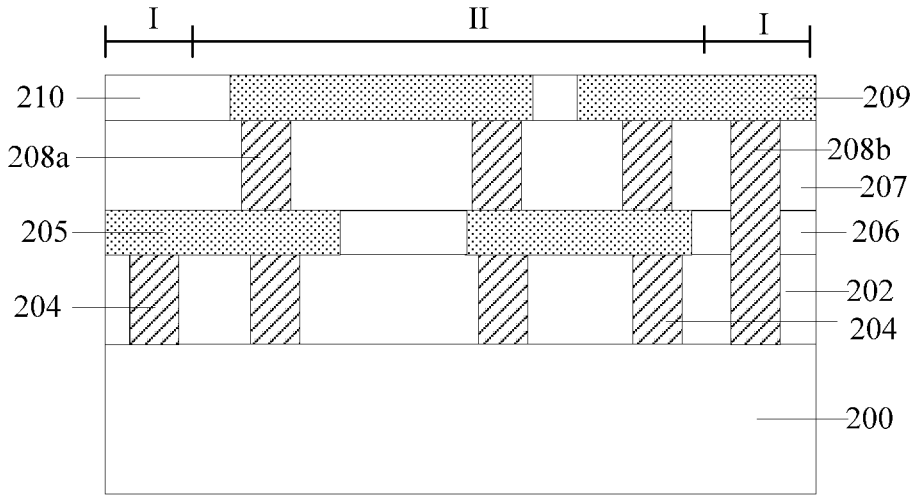

Figure 13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/077670

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L23/52, H01L23/522, H01L23/525, H01L23/528, H01L23/535

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, EPODOC, WPI: semiconductor device, plug, interconnect+, wiring, insulat+, substrate, metal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US2009/0039471A1(KATAGIRI, Haruyoshi)12 Feb.2009(12.02.2009) description paragraphs 34-51 and fig.1	1-10
Y		11-20
Y	US2004/0021224A1(FUKUYAMA, Shun-ichi et al.)05 Feb.2004(05.02.2004) description paragraphs 24-28 and fig.1	11-20
A	US2006/0163748A1(WATARAI, Masatoshi et al.)27 Jul.2006(27.07.2006) the whole document	1-20
A	US2007/0059885A1(HACHISUKA, Atsushi et al.)15 Mar.2007(15.03.2007) the whole document	1-20
A	JP9232429A(NEC CORP.)05 Sept.1997(05.09.1997) the whole document	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim (S) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&"document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 Nov. 2010(24.11.2010)	**23 Dec. 2010 (23.12.2010)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer CHEN, Yuan Telephone No. (86-10)62414081

Form PCT/ISA /210 (second sheet) (July 2009)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2010/077670

Patent Documents referred in the Report	Publication Date	Patent Family	Publication Date
US2009/0039471A1	12.02.2009	JP2009043779A	26.02.2009
US2004/0021224A1	05.02.2004	JP2004071705A	04.03.2004
		US6943431B2	13.09.2005
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		US7602064B2	13.10.2009
US2007/0059885A1	15.03.2007	US7563668B2	21.07.2009
JP9232429A	05.09.1997	KR970063677A	12.09.1997

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2010/077670

A. CLASSIFICATION OF SUBJECT MATTER

H01L23/52(2006.01)i

H01L23/522(2006.01)i