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(71) Applicant: MARS, INCORPORATED [US/US]; 6885 Elm Street, McLean, VA 22101-3883 (US).

(72) Inventor: HEIMAN, Frederic, P. ; 1 Bayview, No. 5, Los Gatos, CA 95030 (US).

(74) Agents: PRIEST, Peter, H. et al.; 45 Rockefeller Plaza, New York, NY 10111 (US).

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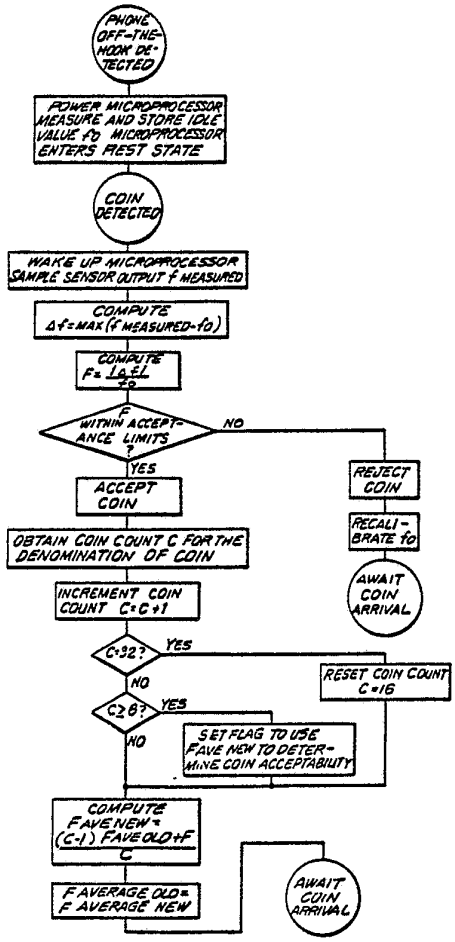
(57) Abstract

A self-tuning coin testing apparatus (10) having a coin sensor circuit (21, 22) which produces an output signal indicative of a parameter characteristic of the coins which are tested by the coin sensor and a programmed microprocessor (35) which stores an initial acceptance limit, determines whether the output signal from the coin sensor is indicative of a valid coin, stores a signal based on the output signal for each valid coin, calculates a statistical function based on the stored signal, and finally computes and stores a new acceptance limit based on the stored signals for a predetermined number of previously accepted coins. The statistical function is preferably weighted so that it is based upon values for only a predetermined number of the most recently accepted coins so that a recent average is maintained.



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Self-Tuning Coin Recognition System

Technical Field

The present invention relates to the examination of coins for authenticity and denomination, and more particularly to an adjustment-free self-tuning mechanism for coin testing.

Background Art

It has long been recognized in the coin examining art that the interaction of an object with a low frequency electromagnetic field can be used to indicate, at least in part, the material composition of the object and thus whether or not the object is an acceptable coin and, if acceptable, its denomination. See, for example, U.S. Patent No. 3,059,749. It has also been recognized that such low frequency tests are advantageously combined with one or more tests at a higher frequency. See, for

example, U.S. Patent No. 3,870,137 assigned to the assignee of the present application.

Most known electronic coin testing mechanisms require for each coin test included therein at least one tuning element and at least one tuning adjustment during the manufacturing process to compensate for components which have slightly different values within tolerance and for variations in component positioning which occur during the construction of the coin testing apparatus. For example, in low frequency coin test apparatus employing a bridge circuit, the bridge circuit is normally tuned in the factory by placing a known acceptable coin in the test position and balancing the bridge.

An additional problem long recognized in the coin testing art is the problem of how to compensate for component aging, for changes in the environment of the coin apparatus such as temperature and humidity changes, and for similar disruptive variations which result in undesirable changes in the operating characteristics of the electronic circuits employed in the electronic coin test apparatus.

Retuning of the test apparatus by a service person is one known response to the problem of component aging but such retuning is expensive and provides only a temporary solution to the problem. Discrete compensation circuitry has been developed to solve the environmental compensation problem. See, for example, U.S. Application No. 308,548 filed October 2, 1981 and assigned to the assignee of the present invention. Further, an improved transmit-receive method and apparatus has been developed which eliminates the need for tuning adjustments or discrete compensation circuitry. See U.S. Application No. 428,467 assigned to the assignee of the present invention.

Disclosure of Invention

The present invention relates to simple and cost effective method and apparatus for setting coin acceptance limits and eliminating compensation problems. The present invention can be applied to a wide range of electronic coin tests for measuring a parameter indicative of the acceptability of a coin. According to the present invention, the coin acceptance limits for a coin test are set and readjusted by the apparatus itself, based upon computed statistical function of the parameter measured by the coin test for a predetermined number of previously accepted coins.

The operation of an embodiment of the present invention may be summarized as follows. A standard set of initial acceptance limits for any coin which is to be tested, such as the U.S. 5-cent coin, is initially stored in all coin testing apparatuses made in accordance with the present invention. These initial limits are set rather wide so that virtually 100% acceptance of all genuine 5-cent coins is assured. During factory preparation of each individual coin test apparatus, acceptable coins are inserted into the apparatus and are tested by one or more sensors. A statistical function of the parameter measured by each sensor is computed. For example, a running average of the parameter can be computed. Once a predetermined number of acceptable coins have been accepted, a new acceptance limit is automatically established by the electronic coin testing apparatus. For example, the new acceptance limits can be set at the running average plus or minus a stored, preestablished constant or a stored, preestablished percentage of the running average. Alternatively, standard initial acceptance limits are not stored and

tuning is begun by transmitting an instruction signal that the apparatus is to be tuned for particular coin such as the 5-cent coin. Then, a predetermined number of valid 5-cent coins are inserted and tested. A single test coin representative of the average 5-cent coin may be used. A statistical function is computed and acceptance limits are set based thereon. Similarly, the process is repeated for additional denominations of coins which are to be accepted. In either case, the initial factory tuning is accomplished by merely inserting predetermined number of valid coins. Once the apparatus is commercially operational, the statistical function is continuously recomputed by the electronic coin testing apparatus as additional acceptable coins are inserted. In order to compensate for environmental changes such as a change of temperature or humidity after a large number of coins have been accepted, the coin testing apparatus reweights the computation so that the computation of the statistical function is based upon information for only a predetermined number of the most recently inserted and accepted coins.

The self-tuning feature of a coin testing apparatus according to the present invention has the advantage of significantly reducing the time and skill require to originally tune the coin testing apparatus in the factory, thereby reducing the costs of labor used in the manufacturing process. Further, such apparatus continuously retunes itself during normal operation thereby compensating for parameter drift and environmental changes.

Brief Description of Drawings

Fig. 1 is a schematic block diagram of an embodiment of electronic coin testing apparatus in accordance with the invention;

Fig. 2 is a detailed schematic diagram of circuitry suitable for the embodiment of Fig. 1;

Fig. 3 is a schematic diagram indicating suitable positions for the sensors of the embodiment of Fig. 1; and

Figs. 4A and B are a flowchart of the operation of the embodiment of Fig. 1.

Although the coin examining method and apparatus of this invention may be applied to a wide range of electronic coin tests for measuring a parameter indicative of a coin's acceptability and to the identification and acceptance of any number of coins from the coin sets of many countries, the invention will be adequately illustrated by explanation of its application to identifying the U.S. 5-cent coin. In particular, the following description concentrates on the details for setting the acceptance limits for a high frequency diameter test for U.S. 5-cent coins, but the application of the invention to other coin tests for U.S. 5-cent coins, such as a high frequency thickness test, and to other coins will be clear to those skilled in the art.

The figures are intended to be representational and are not necessarily drawn to scale. Throughout this specification, the term "coin" is intended to include genuine coins, tokens, counterfeit coins, slugs, washers, and any other item which may be used by persons in an attempt to use coin-operated devices. Furthermore, from time to time in this specification, for simplicity, coin movement is

described as rotational motion; however, except where otherwise indicated, translational and other types of motion also are contemplated. Similarly, although specific types of logic circuits are disclosed in connection with the embodiments described below in detail, other logic circuits can be employed to obtain equivalent results without departing from the invention.

Best Mode for Carrying Out the Invention

Fig. 1 shows a block schematic diagram of an electronic coin testing apparatus 10 in accordance with the present invention. The mechanical portion of the electronic coin testing apparatus 10 is shown in Fig. 3. The electronic coin testing apparatus 10 includes two principal sections: a coin examining and sensing circuit 20 including individuals sensor circuits 21, 22 and 23, and a processing and control circuit 30. The processing and control circuit 30 includes a programmed microprocessor 35, an analog to digital (A/D) converter circuit 40, a signal shaping circuit 45, a comparator circuit 50, a counter 55, and NOR-gates 61, 62, 63, 64 and 65.

Each of the sensor circuits 21, 22 includes two-sided inductive sensor 24, 25 having its series connected coils located adjacent opposing sidewalls of a coin passageway. As shown in Fig. 3, sensor 24 is preferably of a large diameter for testing coins of wideranging diameters. Sensor circuit 23 includes an inductive sensor 26 which is preferably arranged as shown in Fig. 3.

Sensor circuit 21 is a high frequency low power oscillator used to test coin parameters, such as diameter and material, and to "wake up" the microprocessor 35. As a coin passes the sensor 24,

the frequency and amplitude of the output of sensor circuit 21 change as a result of coin interaction with the sensor 24. This output is shaped by the shaping circuit 45 and fed to the comparator circuit 50. When the change in the amplitude of the signal from shaping circuit 45 exceeds a predetermined amount, the comparator circuit 50 produces an output on line 36 which is connected to the interrupt pin of microprocessor 35. A signal on line 36 directs the microprocessor 35 to "wake up" or in other words, to go from a low power idling or rest state to a full power coin evaluation state. In a preferred embodiment, the electronic coin testing apparatus 10 may be employed in a coin operated telephone or other environment in which low power operation is very important. In such environments, the above described wake up feature is particularly useful. The above described "wake up" is only one possible way for powering up upon detecting coin arrival. For example, a separate arrival detector could be used to detect coin arrival and wake up the microprocessor.

The output from shaping circuit 45 is also fed to an input of the A/D converter circuit 40 which converts the analog signal at its input to a digital output. This digital output is serially fed on line 42 to the microprocessor 35. The digital output is monitored by microprocessor 35 to detect the effect of a passing coin on the amplitude of the output of sensor circuit 21. In conjunction with frequency shift information, the amplitude information provides the microprocessor 35 with adequate data for particularly reliable testing of coins of wideranging diameters using a single sensor 21.

The output of sensor circuit 21 is also connected to one input of NOR gate 61 the output of

which is in turn connected to an input of NOR gate 62. NOR gate 62 is connected as one input of NOR gate 65 which has its output connected to the counter 55. Frequency related information for the sensor circuit 21 is generated by selectively connecting the output of sensor circuit 21 through the NOR gates 61, 62 and 65 to the counter 55. Frequency information for sensor circuits 22 and 23 is similarly generated by selectively connecting the output of either sensor circuit 22 or 23 through its respective NOR gate 63 or 64 and the NOR gate 65 to the counter 55. Sensor circuit 22 is also a high frequency low power oscillator and it is used to test coin thickness. Sensor circuit 23 is a strobe sensor commonly found in vending machines. As shown in Fig, 3, the sensor 26 is located after an accept gate 71. The output of sensor circuit 23 is used to control such functions as the granting of credit, to detect coin jams and to prevent customer fraud by methods such as lowering an acceptable coin into the machine with a string.

The microprocessor 35 controls the selective connection of the outputs from the sensor circuit 23 to counter 55 as described below. The frequency of the oscillation at the output of the sensor circuits 21, 22 and 23 is sampled by counting the threshold level crossings of the output signal occurring in a predetermined sample time. The counting is done by the counter circuit 55 and the length of the predetermined sample time is controlled by the microprocessor 35. One input of each of the NOR gates 62, 63 and 64 is connected to the output of its associated sensor circuit 21, 22 and 23. The output of sensor 21 is connected through the NOR gate 61 which is connected as an inverter amplifier. The other input of each of the NOR gates 62, 63 and 64 is

connected to its respective control line 37, 38 and 39 from the microprocessor 35. The signals on the control lines 37, 38 and 39 control when each of the sensor circuits 21, 22 and 23 is interrogated or sampled, or in other words, when the outputs of the sensor circuits 21, 22 and 23 will be fed to the counter 55. For example, if microprocessor 35 produces a high (logic "1") signal on lines 38 and 39 and a low signal (logic "0") on line 37, sensor circuit 21 is interrogated, and each time the output of the NOR gate 61 goes low, the NOR gate 62 produces a high output which is fed through NOR gate 65 to the counting input of and counted by the counter 55. Counter 55 produces an output count signal and this output of counter 55 is connected by line 57 to the microprocessor 35. Microprocessor 35 determines whether the output count signal from the counter 55 and the digital amplitude information from A/D converter circuit 40 are indicative of a coin of acceptable diameter or not by determining whether the outputs of counter 55 and A/D converter circuit 40 or a value or values computed therefrom are within stored acceptance limits. When sensor circuit 22 is interrogated, microprocessor 35 determines whether the counter output is indicative of a coin of acceptable thickness. Finally, when sensor circuit 23 is interrogated, microprocessor 35 determines whether the counter output is indicative of coin presence or absence. When both the diameter and thickness tests are satisfied, a high degree of accuracy in discrimination between genuine and false coins is achieved.

Fig. 2 is a detailed schematic diagram of circuitry suitable for the embodiment of Fig. 1 including the following components:

Resistors

R_1	820 k
R_2	330 k
R_3	43 k
R_4, R_9, R_{12}	3.9 k
$R_5, R_{13}, R_{28}, R_{36}$	1 k
$R_6, R_{14}, R_{18}, R_{21}$ $R_{27}, R_{29}, R_{30},$ R_{31}, R_{34}, R_{38}	100 k
R_7	510 k
R_8	680 k
R_{10}	470 k
R_{11}	620 k
R_{15}, R_{26}	47 k
R_{16}	180 k
R_{17}	10 k
R_{20}	390 k
R_{22}, R_{23}	150 k
R_{24}, R_{37}	6.8 k
R_{25}, R_{39}, R_{40}	1 M
R_{35}	1.5 k

Inductive Sensors

24	3.5 mH
25	400 uH
26	240 uH

Capacitors

$C_1, C_2, C_3, C_4, C_{15}$ $C_{16}, C_{17}, C_{22}, C_{23},$ C_{34}	.1uf
C_5	250 pf
C_6, C_{33}	510 pf
C_7, C_8	180 pf
C_9, C_{10}	100 pf

$C_{11}, C_{12}, C_{13}, C_{18}$	.01 uf
$C_{14}, C_{21},$	10 uf
C_{19}, C_{20}	30 pf

Diodes

D_1, D_2, D_3, D_4, D_5	
D_6, D_7, D_8, D_9	
$D_{11}, D_{12}, D_{13}, D_{14},$	
$D_{17}, D_{18}, D_{20}, D_{21},$	
$D_{22}, D_{23},$	1N4148
D_{15}, D_{16}	HSCH 1001

Zener Diode

Z	4.7v

Transistors

T_1, T_2, T_3	2N5089
T_4	2N3392
T_5, T_6	2N4356

Battery

LB	Saft LB2425 3 V Lithium

Oscillator

O	Murata 2MHz Ceramic Resonator

Comparators

$Comp_1$, $Comp_2$	LM2903

NOR Gates	
61,62,63,64	National Semiconductor 4001
65	National Semiconductor 4025
Counter	
55	National Semiconductor CD 4520B
Internal Memory	
58	74C244
59	27C16
60	74C373
Microprocessor	
35	Intel 80C39.

Circuit blocks and elements in Fig. 2 corresponding to blocks and elements in Fig. 1 have been similarly numbered. In the electronic coin testing apparatus 10 shown in detail in Fig. 2, the blocks 15, 16 and 17 provide an appropriate level of base current to the transistor T_1, T_2 and T_3 of sensor circuits 21, 22 and 23 respectively. Sensor circuit 21 is a low power oscillator circuit having an inductive sensor 24 comprising two coils connected in series and located on the opposing sidewalls 36 and 38 shown in Fig. 3. The two coils of sensor 24 have a combined inductance of approximately 3.5mH and the sensor circuit 21 oscillates at an idling frequency of approximately 170kHz. An oscillating output signal from sensor circuit 21 is taken from point A and connected through shaping circuit 45 to A/D converter 41 and comparator circuit 50. The signal at point B

is the envelope of the oscillation output signal of sensor circuit 21. When the sensor circuit 21 is unaffected by coins, the amplitude of the signal at the point B is approximately 3.5 volts. As a coin approaches and then passes sensor 24, the voltage at point B decreases until the coin as centered between the coils of sensor 24 and then increases again as the coin rolls away from the sensor 24. When the voltage level at point B changes by approximately .2 volts, the comparator circuit 50 produces an output on line 36 which is fed through a NOR gate and a diode to the interrupt port of microprocessor 35 and wakes up microprocessor 35. Amplitude and frequency information for diameter testing are then generated and evaluated as discussed above.

Sensor circuit 22 shown in detail in Fig. 2 is also an oscillator circuit and it produces frequency test information relating to the width of a coin passing sensor 25. The oscillator shown in Fig. 2 has an inductive sensor 25 comprising two coils connected in series and located on the opposing side walls 36 and 38 shown in Fig. 3. The two coils of sensor 25 have a combined inductance of approximately 400uH and the oscillator circuit has an idling frequency of approximately 750kHz.

The sensor circuit 23, the strobe sensor, has its inductive sensor 26 located after a coin routing gate 71 as shown in Fig. 3. The single coil of inductive sensor 26 has an inductance of approximately 240uH and sensor circuit 23 has an idling frequency of approximately 850Hz. The strobe sensor is used to detect coin passage, to prevent coin jamming and customer fraud.

The microprocessor 35 is a CMOS device with its RAM power supply 80 backed up by a 3 volt lithium

battery LB. This power arrangement provides for nonvolatile memory. Other devices including EEPROM and NOVRAM devices can be used to achieve the same result. As shown in Fig. 2, the three chips labeled 58, 59 and 60 constitute the external program memory. Where a microprocessor 35 is used which has sufficient internal memory, such as an Intel 80C49, the chips 58, 59 and 60 may be eliminated.

In a preferred embodiment, the electronic coin testing apparatus 10 is incorporated into a coin operated telephone. In this embodiment, the apparatus 10 is only powered up when the phone is off-the-hook. When the phone is lifted off the hook, each of the sensor circuits begins to oscillate. The microprocessor 35 samples and stores idling or no coin amplitude (A_o) and frequency (f_o) values for sensor circuit 21 and frequency values for sensor circuits 22 and 23. Then, the microprocessor "goes to sleep" or enters rest or standby mode. In this mode, it consumes very little power until an interrupt signal is produced on line 36 thereby indicating that a coin has been inserted and waking up microprocessor 35. Microprocessor 35 upon being awakened is fully powered and it evaluates the information from the sensor circuits 21 and 22 and determines whether or not the detected coin is an acceptable coin.

The method of the present invention will now be described in the context of setting coin acceptance limits based upon the frequency information from sensor circuit 21. As a coin approaches and passes inductive sensor 24, the frequency of its associated oscillator varies from the no coin idling frequency, f_o, and the output of sensor circuit 21 varies accordingly. Also, the amplitude of the envelope of this output signal varies. When this latter variation

exceeds a predetermined limit, the microprocessor 35 recognizes that a coin has been inserted and wakes up. Microprocessor 35 then computes a maximum change in frequency Δf, where Δf equals the maximum absolute difference between the frequency measured during coin passage and the idling frequency. $\Delta f = \max (f_{measured} - f_o)$. A dimensionless quantity $F = \Delta f / f_o$ is then computed and compared with stored acceptance limits to see if this value of F for the coin being tested lies within the acceptability range for a valid coin. As background to such measurements and computations, see U.S. Patent No. 3,918,564 assigned to the assignee of the present application. As discussed in that patent, this type of measurement technique also applies to parameters of a sensor output signal other than frequency, for example, amplitude. Similarly, while the present invention is specifically applied to the setting of coin acceptance limits for particular sensors providing amplitude and frequency outputs, it applies in general to the setting of coin acceptance limits derived from a statistical function for a number of previously accepted coins of the parameter or parameters measured by any sensor.

If the coin is determined to be acceptable, the F value is stored and added to the store of information used by microprocessor 35 for computing new acceptance limits. For example, a running average of stored F values is computed for a predetermined number of previously accepted coins and the acceptance limits are established as the running average plus or minus a stored constant or a stored percentage of the running average. Preferably, both wide and narrow acceptance limits are stored in the microprocessor 35. Alternatively these limits might be stored in RAM or ROM. In the embodiment shown, whether the new

acceptance limits are set to wide or narrow values is controlled by external information supplied to the microprocessor through its data communication bus. Alternatively, a selection switch connected to one input of the microprocessor 35 might be used. In the latter arrangement, microprocessor 35 tests for the state of the switch, that is, whether it is open or closed and adjusts the limits depending on the state of the switch. The narrow range achieves very good protection against the acceptance of slugs; however, the tradeoff is that acceptable coins which are worn or damaged may be rejected. The ability to select between wide and narrow acceptance limits allows the owner of the apparatus to adjust the acceptance limits in accordance with his operational experience.

Other ports of the microprocessor 35 are connected to a relay control circuit 70 for controlling the gate 71, shown in Fig. 3, a clock 75, a power supply circuit 80, interface lines 81, 82, 83 and 84, and debug line 85. The microprocessor 35 can be readily programmed to control relay circuit 70 which operates a gate to separate acceptable from unacceptable coins or perform other coin routing tasks. The particular details of controlling such a gate do not form a part of the present invention. For further details of typical gate operation, see for example, U.S. Patent No. 4,106,610 assigned to the assignee of the present invention. See also, Plesko, "Low Power Coin Routing Gate", U.S. Application No. 585,252 assigned to the assignee of the present invention and filed on even date herewith for details of a preferred gate suitable for use in conjunction with this invention.

The clock 75 and power supply 80 supply clock and power inputs required by the microprocessor 35.

The interface lines 81, 82, 83 and 84 provide a means for connecting the electronic coin testing apparatus 10 to other apparatus or circuitry which may be included in a coin operated vending mechanism which includes the electronic coin testing apparatus 10. The details of such further apparatus and the connection thereto do not form part of the present invention. Debug line 85 provides a test connection for monitoring operation and debugging purposes.

Fig. 3 illustrates the mechanical portion of the coin testing apparatus 10 and one way in which sensors 24, 25 and 26 may be suitably positioned adjacent a coin passageway defined by two spaced side walls 36, 38 and a coin track 33, 33a. The coin handling apparatus 11 includes a conventional coin receiving cup 31, two spaced sidewalls 36 and 38, connected by a conventional hinge and spring assembly 34, and coin track 33, 33a. The coin track 33, 33a and sidewalls 36, 38 form a coin passageway from the coin entry cup 31 past the coin sensors 24, 25. Fig. 3 also shows the sensor 26 located after the gate 71, which in Fig. 3 is shown for separating acceptable from unacceptable coins.

It should be understood that other positionings of sensors may be advantageous, that other coin passageway arrangements are contemplated and that additional sensors for other coin tests may be used.

Figs. 4A and 4B are a flowchart of the operation of the embodiment of Figs. 1-3. According to one embodiment of the method of the present invention, for each denomination of coin to be accepted, initial acceptance limits for each test are stored in the microprocessor 35 of the electronic coin testing apparatus 10. These initial limits are set quite wide guaranteeing almost 100% acceptance of

acceptable coins. These acceptance limits are used only in the original tuning. To tune the electronic coin testing apparatus 10, a predetermined number of known acceptable coins of each denomination are inserted. For example, eight acceptable 5-cent coins are inserted. The inserted coins are detected by the sensor circuit 21, microprocessor 35 is awakened, amplitude and frequency tests are conducted for each coin using sensor circuit 21, and a second frequency test is conducted using sensor circuit 22. Then, new acceptance limits are computed based on the test information for the eight acceptable coins. These new limits are used for testing additional coins which are inserted. By way of example, the frequency test using sensor circuit 21 will be further discussed, but it should be understood that similar processing is performed for each test undertaken in the coin validation process.

The flowchart of Figs. 4A and 4B illustrates the process involved in the coin telephone context. It will be understood that the method and apparatus of the present invention can be used in other contexts. The general method of Figs. 4A and 4B may be understood by taking all f variables as representing any function which might be tested, such as frequency, amplitude and the like, for any coin test. The specific discussion which follows will be in terms of frequency testing for United States 5-cent coins.

After a phone off-the-hook condition is detected, the microprocessor 35 is powered up, an idling frequency, f_o is measured and stored and the microprocessor 35 enters its low power rest state. For initial calibration and tuning, a phone off-the-hook signal may be artificially simulated.

Then, in one embodiment, a series of eight acceptable 5-cent coins are inserted to tune the apparatus for 5 cent-coins. Microprocessor 35 stays in its rest state until the first 5-cent coin is detected. The frequency of the output of sensor circuit 21 is repetitively sampled and the frequency values $f_{measured}$ are obtained. A maximum difference value, Δf, is computed from the maximum difference between $f_{measured}$ and f_o during passage of the first 5-cent coin. $\Delta f = \max(f_{measured} - f_o)$.

Next, a dimensionless quantity, F, is calculated by dividing Δf by f_o. $F = \Delta f / f_o$. The computed F for the first 5-cent coin is compared with the stored acceptance limits to see if it lies within those limits. Since the first 5-cent coin is an acceptable 5-cent coin, its F value is within the limits. The first 5-cent coin is accepted and microprocessor 35 obtains a coin count C for that coin.

For the first coin the coin count C equals zero. C=0. This coin count is then incremented by one. C=C+1. The coin count C=1 is now compared with the number 32. C=32? Since C is not equal 32, the next step is to compare C with 8 to see if C is greater than or equal to 8. $C \geq 8$? Since C is not greater than or equal to 8, the next step is to compute a new average F, $F_{AVE\ NEW}$, for 5-cent coins. $F_{AVE\ NEW} = (((C-1) \times F_{AVE\ OLD}) + F) / C$. $F_{AVE\ OLD}$ for the first coin equals 0. Consequently, $F_{AVE\ NEW} = F/C = F$. $F_{AVE\ NEW}$ is now stored as $F_{AVE\ OLD}$. $F_{AVE\ OLD} = F_{AVE\ NEW}$. This step completes the processing of the first 5-cent coin.

As additional 5-cent coins are inserted to tune the apparatus the process repeats until the eighth 5-cent coin is inserted. For the eighth 5-cent

coin the coin count C=7, when it is incremented by 1 it becomes equal to 8. When C is now compared with 8 it is found to equal 8. As a result, a flag is set to use the computed $F_{AVE\ NEW}$ to determine the acceptance limits. $F_{AVE\ NEW}$ is computed as before, but now it is used in determining the acceptance limits for subsequently inserted 5-cent coins. The originally stored limits are no longer used. The new limits may be $F_{AVE\ NEW}$ plus or minus a constant, that is, upper limit = $F_{AVE\ NEW} + X$, lower limit = $F_{AVE\ NEW} - X$; or $F_{AVE\ NEW}$ plus or minus a fixed percentage of $F_{AVE\ NEW}$, upper limit = $(F_{AVE\ NEW})(1+X)$, lower limit = $(F_{AVE\ NEW})(1-X)$; or computed from $F_{AVE\ NEW}$ in any logical manner. Once the apparatus is tuned as discussed above, it may be used in an actual operating environment.

As additional 5-cent coins are inserted, $F_{AVE\ NEW}$ and new acceptance limits are continually recomputed. If a coin other than an acceptable 5-cent coin is inserted, its F value will not be within the acceptance limits and that coin will be rejected. After that occurs, a new idling frequency, f_o, is measured and then microprocessor 35 returns to a rest state to await coin arrival.

The recomputation of $F_{AVE\ NEW}$ and the acceptance limits with each acceptable 5-cent coin after the eighth allows the system of the present invention to self-tune and recalibrate itself and thus to compensate for parameter drift, temperature and environmental shifts and the like. In order for this beneficial compensation to be achieved, it is important that $F_{AVE\ NEW}$ not become overly weighted by the previously accepted coins. Consequently, when the thirty-second 5-cent coin is inserted, the incremented count C=32 and the process branches

differently. When C=32, the coin count C is reset to 16. C=16. The coin count value C=16 is then used for computing $F_{AVE\ NEW}$. When the thirty third coin is received, the coin count C=16 is incremented for use in the later process steps. The above process continues indefinitely as additional 5-cent coins are inserted.

As discussed above, the method of the present invention is not limited to frequency based testing. Neither is the statistical function limited solely to a running average. Further, while the specific example of the flowchart discussed above uses the numbers 8, 16 and 32 in the computation process, other predetermined numbers may be used without departing from the present invention. The values 8, 16 and 32 were selected because: a) $F_{AVE\ NEW}$ is fairly well determined after eight coins have been accepted; b) $F_{AVE\ NEW}$ becomes heavily weighted after 32 coins have been inserted so that the insertion of additional acceptable coins has little effect; and c) the number 16 is between 8 and 32.

In the preferred embodiment, the microprocessor 35 is programmed according to the attached printout; however, the operation of the electronic coin testing apparatus 10 will be clear to one skilled in the art from the above discussion.

I claim:

1. A method of operating a coin testing apparatus having a coin sensor circuit and a processing and control circuit so that it is self-tuning comprising the steps of:

(a) inserting a first coin to be tested into the coin testing apparatus;

(b) determining a test value for the first coin characteristic of the first coin; and characterized by the further steps of:

(c) using the test value to set an acceptance limit; and

(d) testing a subsequently inserted coin using the acceptance limit.

2. A method of operating a coin testing apparatus having a coin sensor circuit and a processing and control circuit so that it is self-tuning comprising the steps of:

(a) testing a coin which is inserted into the coin testing apparatus with the coin sensor circuit and producing an output signal indicative of characteristic of the coin;

(b) determining if the output signal is indicative of an acceptable coin;

(c) storing a value related to the output signal if the coin was determined to be an acceptable coin; and characterized by the further steps of:

(d) computing a statistical function value from the stored value;

(e) using the computed statistical function value after a predetermined number of coins have been accepted for determining the acceptability of subsequently inserted coin; and

(f) repeating the steps (a)-(e) as additional coins are inserted into the test apparatus.

3. The method of claim 2 further characterized in that the step of using the computed statistical function value for determining the acceptability of subsequently inserted coins further comprises the steps of:

(a) computing acceptance limits for an acceptable coin from the statistical function value;

(b) storing the computed acceptance limits in the processing and control circuit; and

(c) comparing the value related to the output signal for a subsequently inserted coin with the stored acceptance limits.

4. A method of operating a coin testing apparatus having a coin sensor circuit and a processing and control circuit characterized by the steps of:

(a) inserting a predetermined number of coins of a single denomination which are known to be acceptable into the coin testing apparatus;

(b) testing the coins with the coin sensor circuit and producing output signals indicative of a characteristic of the coins;

(c) storing values related to the output signals;

(d) computing a statistical function value from the stored values; and

(e) storing the computed statistical function values in the processing and control means.

5. The method of claim 4 further characterized by the step of using the stored statistical function values in determining if subsequently inserted coins are acceptable.

6. The apparatus of claim 5 further characterized by the step of using the stored computed statistical function values to compute acceptance limits for the denomination of the coins which have been inserted.

7. A method for testing coins comprising the steps of:

(a) storing an initial set of test limits in a memory in a coin testing apparatus;

(b) inserting a first coin to be tested into the coin testing apparatus;

(c) determining a test value for the first coin characteristic of the first coin;

(d) comparing the test value with the initial set of test limits to see if the test value is within those limits;

(e) accepting the first coin if the test value is within the initial test limits; and characterized by the further steps of:

(f) using the test value to recompute the test limits if the first coin was accepted; and

(g) testing subsequently inserted coins using the recomputed test limits.

8. The method of claim 7 further characterized by the step of using the test value for each additional acceptable coin to recompute the test limits.

9. Apparatus for testing coins comprising a coin sensor circuit having a sensor located adjacent a coin path, said coin sensor circuit producing an output

signal indicative of a characteristic of an inserted coin on the coin path adjacent the sensor;

memory means for storing test limits;

means to derive a test value from the output signal; and characterized by

means to determine if the output signal from the coin sensor circuit is indicative of an acceptable coin by determining if the test value is within a set of test limits and to recompute the test limits used for subsequent coins if the inserted coin is found to be acceptable.

10. The apparatus of claim 9 further characterized in the coin sensor circuit being an oscillator circuit which produces an oscillating output signal.

11. The apparatus of claim 10 further characterized in the means to derive a test value from the output signal comprising in analog-to-digital converter circuit for producing a digital output signal related to the amplitude of the oscillating output signal.

12. The apparatus of claim 10 further characterized in the means to derive a test value from the output signal comprising a counter circuit for producing a digital output count related to the frequency of oscillation of the oscillating output signal.

13. The apparatus of claim 12 further characterized in the means to determine and to recompute comprising a programmed microprocessor.

14. The apparatus of claim 13 further characterized in the programmed microprocessor storing the recomputed test limits each time a coin is found to be acceptable.

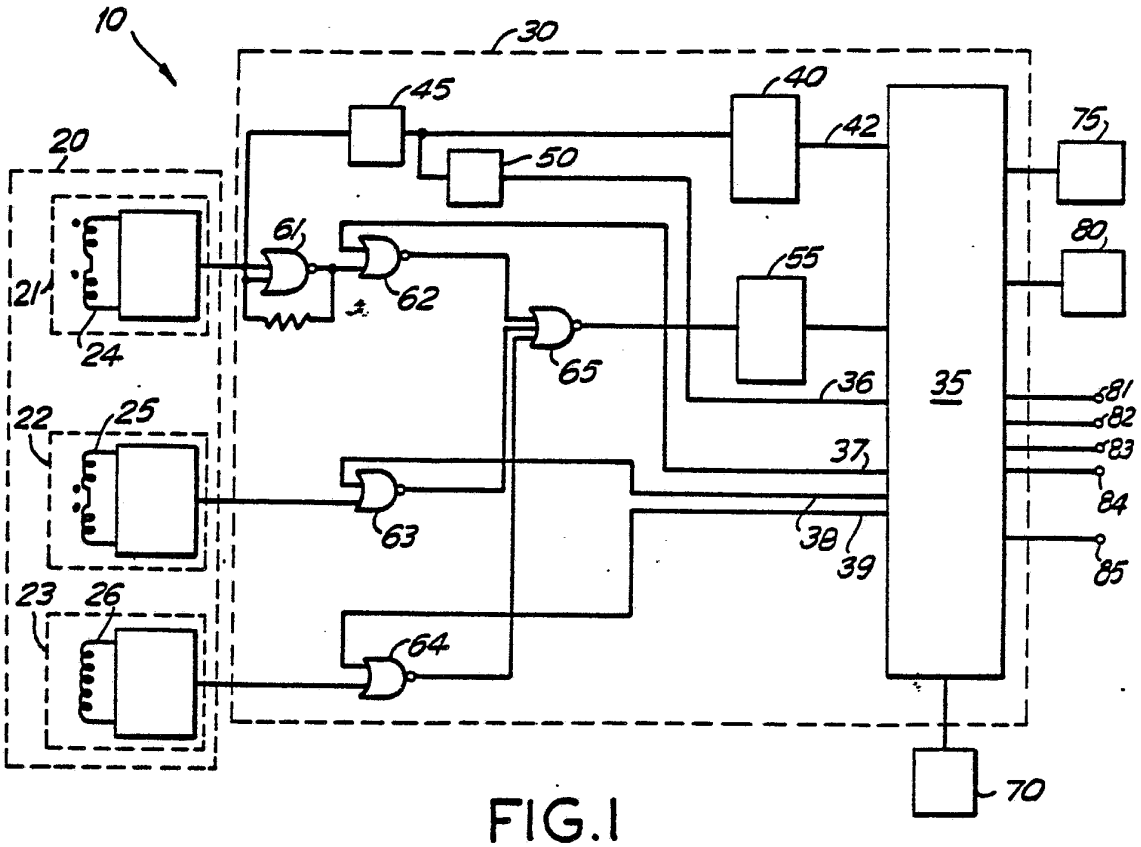
10
30
45
40
42
75
20
50
61
62
55
80
21
24
65
36
35
81
82
83
22
25
37
84
63
38
39
85
23
26
64
70

FIG.1

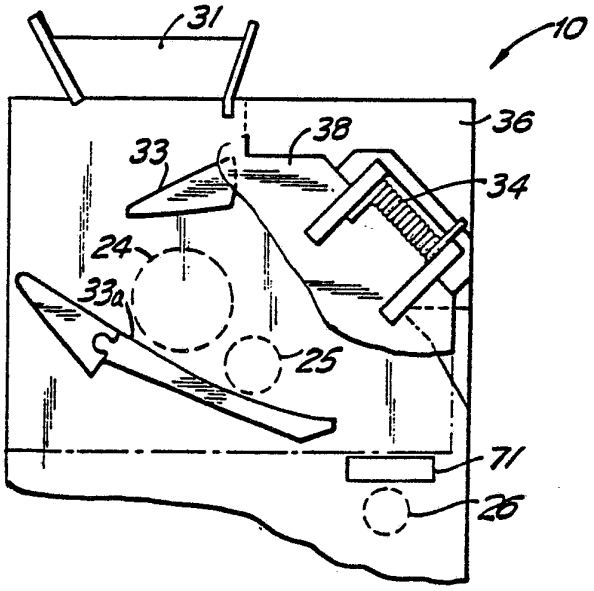
31
10
36
38
33
34
24
33a
25
71
26

FIG.3

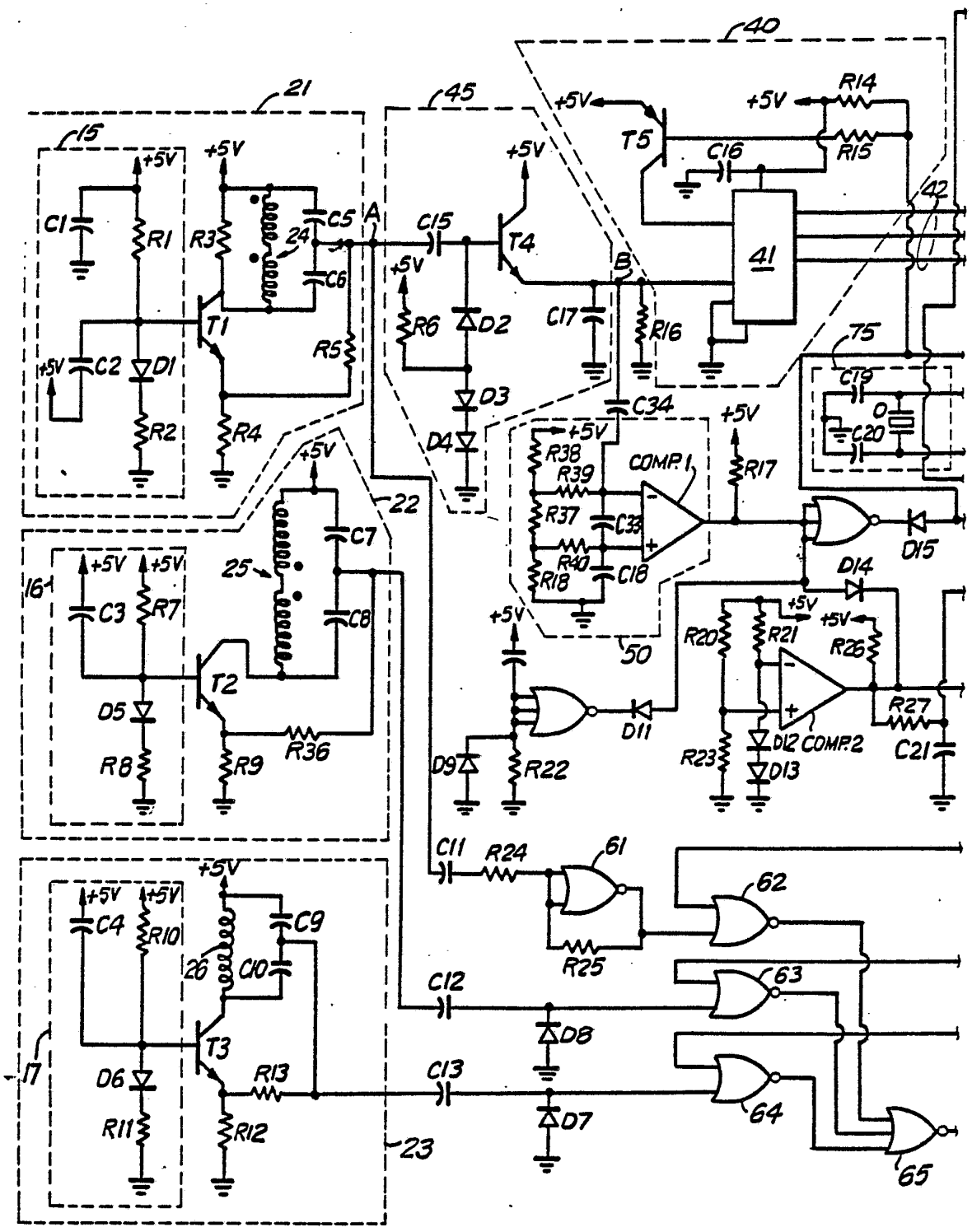
40
21
45
15
+5V
C1
R1
R3
24
C5
C6
A
C15
T4
T5
C16
R14
R15
42
41
B
T1
R5
R6
D2
C17
R16
75
D3
D4
C34
C19
C20
R38
R39
R37
C33
R40
R18
C18
COMP.1
R17
D15
D14
50
R20
R21
R26
R27
C21
D11
D9
R22
D12
D13
COMP.2
R23
22
C7
C8
25
16
C3
R7
T2
D5
R8
R9
R36
C11
R24
61
62
R25
63
C12
D8
64
C13
D7
65
17
C4
R10
C9
C10
26
T3
D6
R11
R12
R13
23

FIG.2A

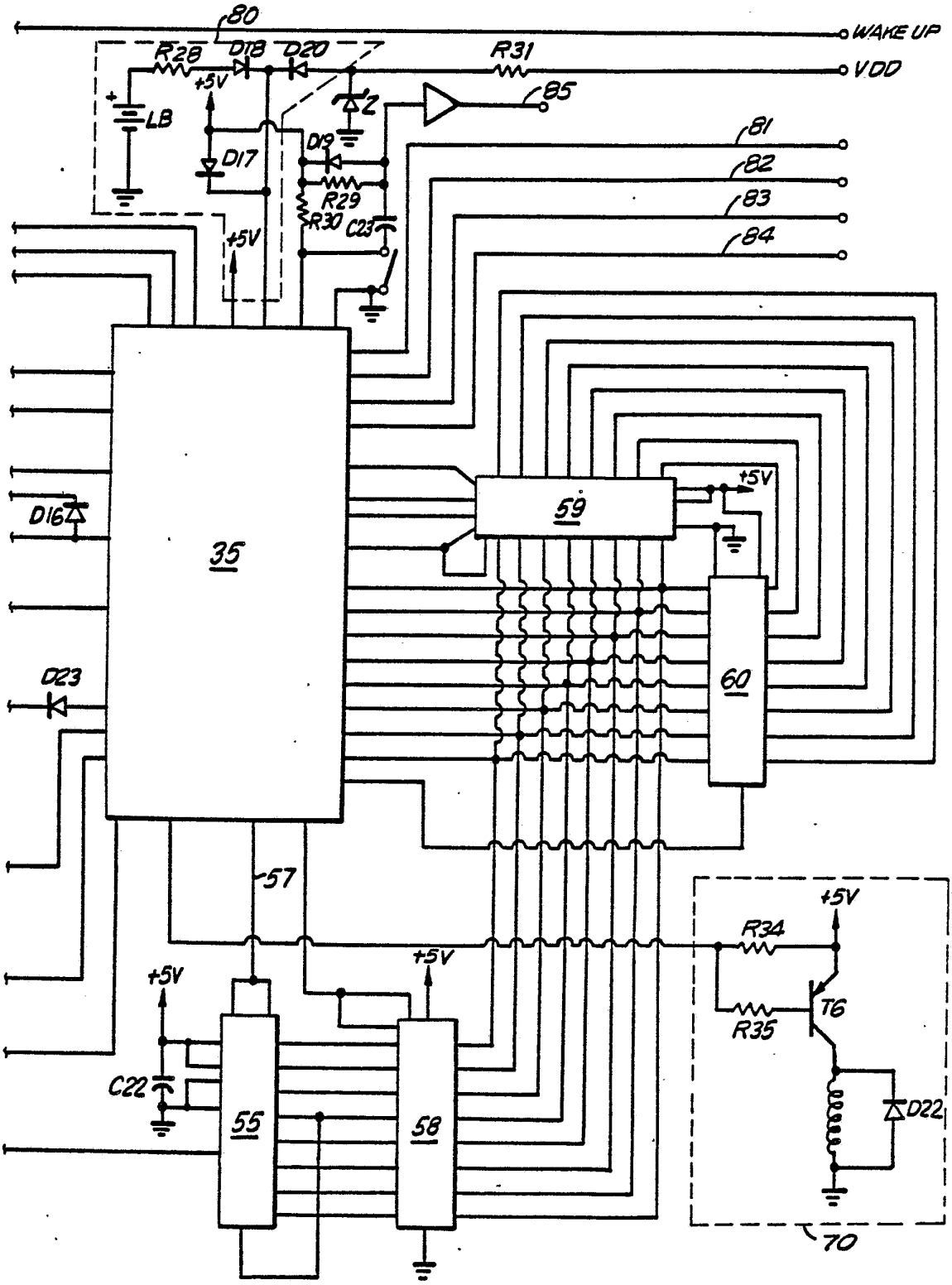
80
WAKE UP
R28
D18
D20
R31
VDD
+5V
LB
Z
85
D17
D19
81
82
R29
R30
C23
83
84
+5V
35
59
+5V
D16
60
D23
57
+5V
+5V
R34
+5V
T6
R35
C22
55
58
D22
70

FIG.2B

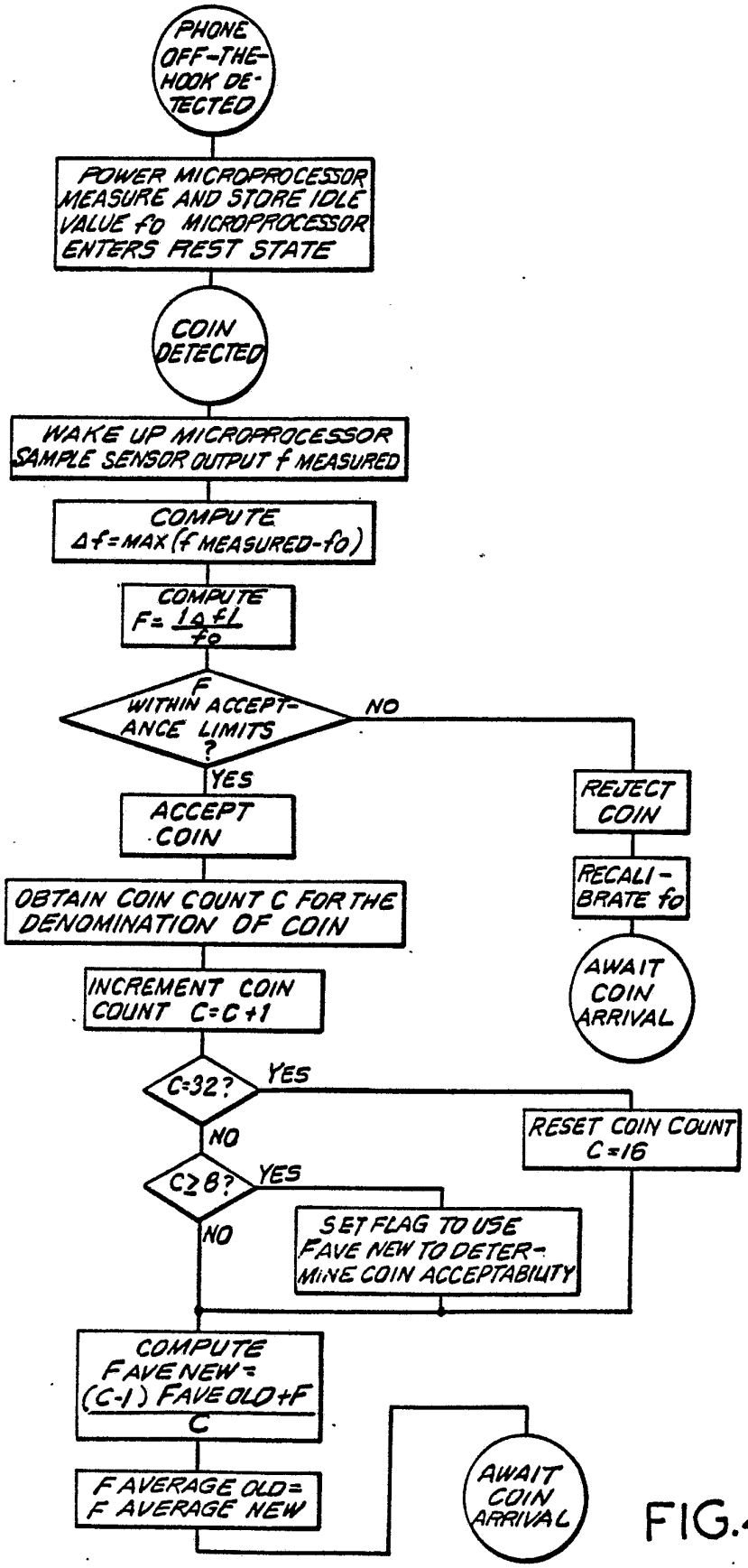
PHONE OFF-THE-HOOK DETECTED
POWER MICROPROCESSOR MEASURE AND STORE IDLE VALUE fo MICROPROCESSOR ENTERS REST STATE
COIN DETECTED
WAKE UP MICROPROCESSOR SAMPLE SENSOR OUTPUT f MEASURED
COMPUTE Δf=MAX (f MEASURED-fo)
COMPUTE F= |Δf| / fo
F WITHIN ACCEPTANCE LIMITS ?
NO
YES
REJECT COIN
RECALIBRATE fo
AWAIT COIN ARRIVAL
ACCEPT COIN
OBTAIN COIN COUNT C FOR THE DENOMINATION OF COIN
INCREMENT COIN COUNT C=C+1
C=32?
YES
NO
RESET COIN COUNT C=16
C≥8?
YES
NO
SET FLAG TO USE FAVE NEW TO DETERMINE COIN ACCEPTABILITY
COMPUTE FAVE NEW = (C-1) FAVE OLD+F / C
F AVERAGE OLD= F AVERAGE NEW
AWAIT COIN ARRIVAL

FIG.4

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/00369

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl.[4] G07F 3/02
U.S. Cl. 194/100A

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
US	194/99, 199R, 100A 364/551 73/163

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 3,956,692, (WEINBERG) 11 May 1976	1
Y	US, A, 4,353,453, (PARTIN ET AL) 12 October 1982	2-4

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
11 April 1985	29 APR 1985
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Stanley H. Tollberg Stanley H. Tollberg

Form PCT/ISA/210 (second sheet) (October 1981)