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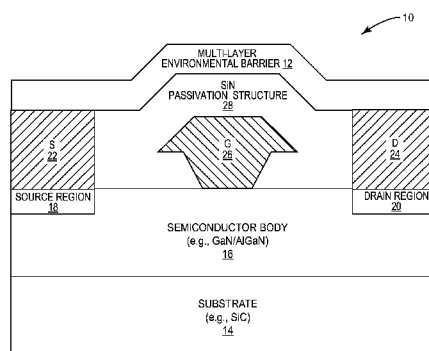
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IC LAYER DEPOSITION

FIG. 1

(57) Abstract: Embodiments of a multi-layer environmental barrier for a semiconductor device and methods of manufacturing the same are disclosed. In one embodiment, a semiconductor device is formed on a semiconductor die. The semiconductor die includes a semiconductor body and a passivation structure on the semiconductor body. A multi-level environmental barrier is provided on the passivation structure. The multi-layer environmental barrier is a low-defect multi-layer dielectric film that hermetically seals the semiconductor device from the environment. In one embodiment, the multi-layer environmental barrier has a defect density of less than 10 defects per square centimeter (cm²). By having a low defect density, the multi-layer environmental barrier serves as a robust barrier to the environment.

ENCAPSULATION OF SEMICONDUCTOR DEVICE WITH MULTILAYER BARRIER USING PECVD OR ATOMIC LAYER DEPOSITION

Government Support

- 5 **[0001]** This invention was made with government funds under contract number 11-D-5309 awarded by the Department of Defense. The U.S. Government may have rights in this invention.

Field of the Disclosure

- 10 **[0002]** The present disclosure relates to a semiconductor device and more particularly relates to an environmental barrier for a semiconductor device.

Summary

- [0003]** Embodiments of a multi-layer environmental barrier for a semiconductor device and methods of manufacturing the same are disclosed. In one embodiment, a semiconductor device is formed on a semiconductor die. The semiconductor die includes a semiconductor body and a passivation structure on the semiconductor body. A multi-level environmental barrier is provided on the passivation structure. The multi-layer environmental barrier is a low-defect multi-layer dielectric film that hermetically seals the semiconductor device from the environment. In one embodiment, the multi-layer environmental barrier has a defect density of less than 10 defects per square centimeter (cm²). Further, in one embodiment, the multi-layer environmental barrier has a pin hole density of less than 10 pin holes per cm². By having a low defect density and a low pin hole density, the multi-layer environmental barrier serves as a robust barrier to the environment.

- [0004]** In one embodiment, the multi-layer environmental barrier includes multiple Plasma Enhanced Chemical Vapor Deposition (PECVD) and/or Atomic Layer Deposition (ALD) layers of two or more different dielectric materials. In another embodiment, the multi-layer environmental barrier includes a first layer of a first dielectric material, a second layer of a second dielectric material, and a third layer of the first dielectric material. In another embodiment, the multi-layer

environmental barrier includes a repeating structure of a first layer of a first dielectric material and a second layer of a second dielectric material. In one embodiment, each of the layers in the repeating structure is formed by PECVD or ALD.

5 **[0005]** In one embodiment, the multi-layer environmental barrier includes a first silicon nitride layer on the passivation structure, a silicon dioxide layer on the first silicon nitride layer, and a second silicon nitride layer on the silicon dioxide layer. In another embodiment, the multi-layer environmental barrier includes a repeating structure of a silicon nitride layer and a silicon dioxide layer on the
10 silicon nitride layer. In one embodiment, each of the layers in the repeating structure is formed by PECVD or ALD.

[0006] In one embodiment, the multi-layer environmental barrier includes a first silicon nitride layer on the passivation structure, a polymer layer on the first silicon nitride layer, and a second silicon nitride layer on the polymer layer. In
15 another embodiment, the multi-layer environmental barrier includes a repeating structure of a silicon nitride layer and a polymer layer on the silicon nitride layer. In one embodiment, each of the layers in the repeating structure is formed by PECVD or ALD.

[0007] In one embodiment, the multi-layer environmental barrier includes a
20 silicon nitride layer on the passivation structure, a silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer. In another embodiment, the multi-layer environmental barrier includes a repeating structure of a silicon nitride layer, a silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer. In one
25 embodiment, each of the layers in the repeating structure is formed by PECVD or ALD.

[0008] In one embodiment, a method of fabricating a semiconductor die and, in particular a semiconductor device on a semiconductor die, includes providing a semiconductor body, providing a passivation structure on the semiconductor
30 body, and providing a multi-layer environmental barrier on the passivation structure. The multi-layer environmental barrier is a low-defect multi-layer

dielectric film that hermetically seals the semiconductor device from the environment. In one embodiment, the multi-layer environmental barrier has a defect density of less than 10 defects per square cm^2 . Further, in one embodiment, the multi-layer environmental barrier has a pin hole density of less than 10 pin holes per cm^2 . By having a low defect density and a low pin hole density, the multi-layer environmental barrier serves as a robust barrier to the environment.

[0009] In one embodiment, providing the multi-layer environmental barrier includes depositing multiple dielectric layers of two or more different dielectric materials via PECVD and/or ALD. In another embodiment, providing the multi-layer environmental barrier includes providing a first layer of a first dielectric material on the passivation structure, providing a second layer of a second dielectric material on the first layer, and providing a third layer of the first dielectric material on the second layer. In another embodiment, providing the multi-layer environmental barrier includes providing a repeating structure of a first layer of a first dielectric material and a second layer of a second dielectric material on the first layer of the first dielectric material. In one embodiment, each of the layers in the repeating structure is provided by PECVD or ALD.

[0010] In one embodiment, providing the multi-layer environmental barrier includes providing a first silicon nitride layer on the passivation structure, providing a silicon dioxide layer on the first silicon nitride layer, and providing a second silicon nitride layer on the silicon dioxide layer. In another embodiment, providing the multi-layer environmental barrier includes providing a repeating structure of a silicon nitride layer and a silicon dioxide layer on the silicon nitride layer. In one embodiment, each of the layers in the repeating structure is provided by PECVD or ALD.

[0011] In one embodiment, providing the multi-layer environmental barrier includes providing a first silicon nitride layer on the passivation structure, providing a polymer layer on the first silicon nitride layer, and providing a second silicon nitride layer on the polymer layer. In another embodiment, providing the multi-layer environmental barrier includes providing a repeating structure of a

silicon nitride layer and a polymer layer on the silicon nitride layer. In one embodiment, each of the layers in the repeating structure is provided by PECVD or ALD.

[0012] In one embodiment, providing the multi-layer environmental barrier includes providing a silicon nitride layer on the passivation structure, providing a silicon oxynitride layer on the silicon nitride layer, and providing a silicon dioxide layer on the silicon oxynitride layer. In another embodiment, providing the multi-layer environmental barrier includes providing a repeating structure of a silicon nitride layer, a silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer. In one embodiment, each of the layers in the repeating structure is provided by PECVD or ALD.

[0013] Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Brief Description of the Drawing Figures

[0014] The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.

[0015] Figure 1 illustrates a semiconductor device that includes a multi-layer environmental barrier according to one embodiment of the present disclosure;

[0016] Figure 2 is a more detailed illustration of the multi-layer environmental barrier of Figure 1 according to one embodiment of the present disclosure;

[0017] Figure 3 is a more detailed illustration of the multi-layer environmental barrier of Figure 1 according to another embodiment of the present disclosure;

[0018] Figure 4 is a more detailed illustration of the multi-layer environmental barrier of Figure 1 according to another embodiment of the present disclosure;

[0019] Figure 5 illustrates a semiconductor device that includes a multi-layer environmental barrier according to one embodiment of the present disclosure; and

[0020] Figure 6 illustrates a semiconductor device that includes a multi-layer environmental barrier according to one embodiment of the present disclosure.

Detailed Description

5 **[0021]** The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of
10 these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.

[0022] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited
15 by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

20 **[0023]** It will be understood that when an element such as a layer, region, or substrate is referred to as being "on" or extending "onto" another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being
25 "directly on" or extending "directly onto" another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being "over" or extending "over" another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast,
30 when an element is referred to as being "directly over" or extending "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or

"coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present.

5 **[0024]** Relative terms such as "below" or "above" or "upper" or "lower" or "horizontal" or "vertical" may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the
10 orientation depicted in the Figures.

[0025] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further
15 understood that the terms "comprises," "comprising," "includes," and/or "including" when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

20 **[0026]** Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the
25 relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0027] Semiconductor devices are often required to operate in high temperature and/or high humidity environments. If moisture is allowed to reach these semiconductor devices, then there will be corrosion of the semiconductor
30 devices which, of course, degrades the performance of the semiconductor devices. In some applications, semiconductor devices are hermetically sealed

within a package. In these applications, the semiconductor devices are protected from the environment. However, in other applications, the packages in which the semiconductor devices are incorporated do not provide a hermetic seal against the environment. In these applications, it is desirable to provide an

5 environmental barrier on the semiconductor devices (i.e., a die level environmental barrier) that protects the semiconductor devices from the environment.

[0028] Embodiments of a multi-layer environmental barrier for a semiconductor device and methods of manufacturing the same are disclosed.

10 Before discussing those embodiments in detail, a brief discussion of one conventional environmental barrier is beneficial. Commonly owned and assigned U.S. Patent No. 7,525,122, entitled PASSIVIATION OF WIDE BAND-GAP BASED SEMICONDUCTOR DEVICES WITH HYDROGEN-FREE SPUTTERED

15 Enhanced Chemical Vapor Deposition (PECVD) Silicon Nitride (SiN) layer as an environmental barrier for a semiconductor device. The inventors found that while a PECVD SiN layer serves as a suitable environmental barrier in many implementations, there is a need for an improved environmental barrier. In particular, the inventors found that a PECVD SiN layer, or film, is prone to
20 forming defects, namely, pin holes and columnar structures. These defects allow moisture to penetrate the PECVD SiN layer and reach the semiconductor device. As discussed below, the multi-layer environmental barrier is a low-defect material that provides an improved environmental barrier for a semiconductor device.

[0029] In this regard, Figure 1 illustrates a semiconductor device 10 that
25 includes a multi-layer environmental barrier 12 according to one embodiment of the present disclosure. In this embodiment, the semiconductor device 10 is a Metal-Semiconductor Field Effect Transistor (MESFET) and, as such, the semiconductor device 10 is also referred to herein as a MESFET 10. Notably, the multi-layer environmental barrier 12 is not limited to use with the MESFET 10.
30 Rather, the multi-layer environmental barrier 12 can be utilized as an environmental barrier for any suitable semiconductor device. Some examples of

additional semiconductor devices with which the multi-layer environmental barrier 12 can be used are described below. However, these additional examples are only examples and are not to be construed as an exhaustive list of semiconductor devices with which the multi-layer environmental barrier 12 can be used.

[0030] As illustrated in Figure 1, the MESFET 10 includes a substrate 14 and a semiconductor body 16 on a surface of the substrate 14. The substrate 14 is preferably formed of Silicon Carbide (SiC), but is not limited thereto. The substrate 14 may be formed of other materials such as, for example, Sapphire, Aluminum Nitride (AlN), Aluminum Gallium Nitride (AlGaN), Gallium Nitride (GaN), Silicon (Si), Gallium Arsenide (GaAs), Zinc Oxide (ZnO), and Indium Phosphide (InP). The semiconductor body 16 preferably includes one or more epitaxial layers of one or more wide bandgap materials such as, for example, one or more Group III nitrides. For example, the semiconductor body 16 may be formed of one or more layers of GaN or AlGaN. However, other Group III nitride materials may be used. As another example, both the substrate 14 and the semiconductor body 16 may be formed of SiC.

[0031] A source region 18 and a drain region 20 are formed in the semiconductor body 16 by, for example, implanting appropriate ions into a surface of the semiconductor body 16 to achieve a desired doping concentration. A source contact 22 is formed by one or more metallic layers on, and preferably directly on, the surface of the semiconductor body 16 over the source region 18. Likewise, a drain contact 24 is formed by one or more metallic layers on, and preferably directly on, the surface of the semiconductor body 16 over the drain region 20. The source and drain contacts 22 and 24 preferably provide low-resistance ohmic contacts to the source and drain regions 18 and 20, respectively. A gate contact 26 is formed by one or more metallic layers on, and preferably directly on, a surface of the semiconductor body 16 between the source region 18 and the drain region 20. The region within the semiconductor body 16 between the source and drain regions 18 and 20 is referred to as a channel region of the MESFET 10.

[0032] In this embodiment, an SiN passivation structure 28 is formed on the surface of the semiconductor body 16 between the source contact 22 and the gate contact 26 and between the drain contact 24 and the gate contact 26. Further, in this embodiment, the SiN passivation structure 28 extends over the gate contact 26. The SiN passivation structure 28 serves to passivate the surface of the semiconductor body 16 (i.e., passivate dangling bonds at the surface of the semiconductor body 16). While the details of the SiN passivation structure 28 are not essential to the understanding of the present disclosure, for more information regarding some exemplary embodiments of the SiN passivation structure 28, the interested reader is directed to U.S. Patent No. 7,525,122, which is mentioned above, as well as commonly owned and assigned U.S. Patent Application Serial No. 13/644,506, entitled HYDROGEN MITIGATION SCHEMES IN THE PASSIVATION OF ADVANCED DEVICES, which was filed on October 4, 2012, both of which are hereby incorporated herein by reference for their teachings regarding an SiN passivation structure. It should also be noted that while the SiN passivation structure 28 is illustrated as an SiN passivation structure, the SiN passivation structure 28 is not limited thereto.

[0033] Lastly, the semiconductor device 10 includes the multi-layer environmental barrier 12. As discussed below in detail, the multi-layer environmental barrier 12 includes multiple layers of two or more different dielectric materials. The inventors have found that, by using multiple layers of different dielectric materials, environmental barrier properties of the multi-layer environmental barrier 12 are substantially improved as compared to a similar single layer environmental barrier. While the inventors do not wish to be limited to any particular theory, the inventors believe that any defects in a first layer of the multi-layer environmental barrier 12 that is formed of a first dielectric material are disrupted by a second layer of the multi-layer environmental barrier 12 that is formed of a second dielectric material, and so on. As a result, the number of defects in the multi-layer environmental barrier 12 is very low, e.g., less than 10 defects per square centimeter (cm^2) or as low as or even less than 1 defect per cm^2 . One particular type of defect that is of concern is a pin hole. As a result of

the disruption of the defects, and in particular the pin holes, using layers of different dielectric materials, the number of pin holes in the multi-layer environmental barrier 12 is very low, e.g., less than 10 pin holes per cm^2 or as low as or even less than 1 pin hole per cm^2 . The low defect density and the low pin hole density is particularly beneficial for and is a substantial improvement for PECVD.

[0034] Figure 2 illustrates one embodiment of the multi-layer environmental barrier 12 of Figure 1. As illustrated, in this embodiment, the multi-layer environmental barrier 12 includes multiple SiN layers 30-1 through 30- N_{SiN} (more generally referred to herein collectively as SiN layers 30 and individually as SiN layer 30) and multiple Silicon Dioxide (SiO_2) layers 32-1 through 32- N_{SiO} (more generally referred to herein collectively as SiO_2 layers 32 and individually as SiO_2 layer 32) arranged in an alternating pattern. The number (N_{SiN}) of SiN layers 30 is greater than or equal to 2, and the number (N_{SiO}) of SiO_2 layers 32 is greater than or equal to 1. In this embodiment, the multi-layer environmental barrier 12 both begins and ends with an SiN layer, namely, the SiN layers 30-1 and 30- N_{SiN} , respectively. However, the multi-layer environmental barrier 12 may alternatively end with an SiO_2 layer (i.e., the SiO_2 layer 32- N_{SiO}).

[0035] In one embodiment, the number (N_{SiN}) of SiN layers 30 is 2 and the number (N_{SiO}) of SiO_2 layers 32 is 1 such that the multi-layer environmental barrier 12 includes only the SiN layer 30-1, the SiO_2 layer 32-1, and the SiN layer 30-2. However, in another embodiment, the multi-layer environmental barrier 12 includes a repeating structure of two or more SiN layers 30 and two or more SiO_2 layers 32 in an SiN/ SiO_2 pattern. Then, in the illustrated embodiment, the multi-layer environmental barrier 12 further includes the final SiN layer 30- N_{SiN} on the repeating structure formed by the SiN layers 30-1 through 30- $(N_{\text{SiN}}-1)$ and the SiO_2 layers 32-1 through 32- N_{SiO} . In other words, in the repeating structure, the structure of an SiN layer 30 and an SiO_2 layer 32 on the SiN layer 30 is repeated N_{SiO} times, and, in the illustrated embodiment, the repeating structure is then terminated by the final SiN layer 30- N_{SiN} .

[0036] The SiN layers 30-1 through 30-N_{SiN} and the SiO₂ layers 32-1 through 32-N_{SiO} are preferably formed using PECVD and/or Atomic Layer Deposition (ALD). In one particular embodiment, all of the SiN layers 30-1 through 30-N_{SiN} and all of the SiO₂ layers 32-1 through 32-N_{SiO} are formed using PECVD. In

5 another particular embodiment, all of the SiN layers 30-1 through 30-N_{SiN} and all of the SiO₂ layers 32-1 through 32-N_{SiO} are formed using ALD. In yet another embodiment, some of the layers 30-1 through 30-N_{SiN} and 32-1 through 32-N_{SiO} are formed using PECVD and the rest of the layers 30-1 through 30-N_{SiN} and 32-1 through 32-N_{SiO} are formed using ALD. In one embodiment, a total thickness
10 of the multi-layer environmental barrier 12 is in a range of and including 0.01 micrometers (μm) to 10 μm, and more preferably in a range of and including 0.1 μm to 5 μm. Thicknesses of each of the SiN layers 30-1 through 30-N_{SiN} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another embodiment.

15 Further, all of the SiN layers 30-1 through 30-N_{SiN} may have the same thickness or some or all of the SiN layers 30-1 through 30-N_{SiN} may have different thicknesses. Likewise, thicknesses of each of the SiO₂ layers 32-1 through 32-N_{SiO} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another
20 embodiment. Further, all of the SiO₂ layers 32-1 through 32-N_{SiO} may have the same thickness or some or all of the SiO₂ layers 32-1 through 32-N_{SiO} may have different thicknesses.

[0037] Figure 3 illustrates another embodiment of the multi-layer environmental barrier 12 of Figure 1. As illustrated, in this embodiment, the
25 multi-layer environmental barrier 12 includes multiple SiN layers 34-1 through 34-N_{SiN} (more generally referred to herein collectively as SiN layers 34 and individually as SiN layer 34) and multiple polymer layers 36-1 through 36-N_P (more generally referred to herein collectively as polymer layers 36 and individually as polymer layer 36) arranged in an alternating pattern. The number
30 (N_{SiN}) of SiN layers 34 is greater than or equal to 2, and the number (N_P) of polymer layers 36 is greater than or equal to 1. In this embodiment, the multi-

layer environmental barrier 12 both begins and ends with an SiN layer, namely, the SiN layers 34-1 and 34- N_{SiN} , respectively. However, the multi-layer environmental barrier 12 may alternatively end with a polymer layer (i.e., the polymer layer 36- N_{P}). The polymer layers 36 can be formed of any suitable polymer having a low dielectric constant (e.g., less than or approximately equal to that of SiN or less than or approximately equal to that of SiO_2). In one embodiment, the polymer used for the polymer layers 36 is an inorganic polymer but may alternatively be an organic polymer.

[0038] In one embodiment, the number (N_{SiN}) of SiN layers 34 is 2 and the number (N_{P}) of polymer layers 36 is 1 such that the multi-layer environmental barrier 12 includes only the SiN layer 34-1, the polymer layer 36-1, and the SiN layer 34-2. However, in another embodiment, the multi-layer environmental barrier 12 includes a repeating structure of two or more SiN layers 34 and two or more polymer layers 36 in an SiN/polymer pattern. Then, in the illustrated embodiment, the multi-layer environmental barrier 12 further includes the final SiN layer 34- N_{SiN} on the repeating structure formed by the SiN layers 34-1 through 34- $(N_{\text{SiN}}-1)$ and the polymer layers 36-1 through 36- N_{P} . In other words, in the repeating structure, the structure of an SiN layer 34 and a polymer layer 36 on the SiN layer 34 is repeated N_{P} times, and, in the illustrated embodiment, the repeating structure is then terminated by the final SiN layer 34- N_{SiN} .

[0039] The SiN layers 34-1 through 34- N_{SiN} and the polymer layers 36-1 through 36- N_{P} are preferably formed using PECVD and/or ALD. In one particular embodiment, all of the SiN layers 34-1 through 34- N_{SiN} and all of the polymer layers 36-1 through 36- N_{P} are formed using PECVD. In another particular embodiment, all of the SiN layers 34-1 through 34- N_{SiN} and all of the polymer layers 36-1 through 36- N_{P} are formed using ALD. In yet another embodiment, some of the layers 34-1 through 34- N_{SiN} and 36-1 through 36- N_{P} are formed using PECVD and the rest of the layers 34-1 through 34- N_{SiN} and 36-1 through 36- N_{P} are formed using ALD. In one embodiment, a total thickness of the multi-layer environmental barrier 12 is in a range of and including 0.01 μm to 10 μm , and more preferably in a range of and including 0.1 μm to 5 μm . Thicknesses of

each of the SiN layers 34-1 through 34-N_{SiN} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another embodiment. Further, all of the SiN layers 34-1 through 34-N_{SiN} may have the same thickness or some or all of the SiN layers 34-1 through 34-N_{SiN} may have different thicknesses. Likewise, thicknesses of each of the polymer layers 36-1 through 36-N_P may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another embodiment. Further, all of the polymer layers 36-1 through 36-N_P may have the same thickness or some or all of the polymer layers 36-1 through 36-N_P may have different thicknesses.

[0040] Figure 4 illustrates another embodiment of the multi-layer environmental barrier 12 of Figure 1. As illustrated, in this embodiment, the multi-layer environmental barrier 12 includes multiple SiN layers 38-1 through 38-N_{SiN} (more generally referred to herein collectively as SiN layers 38 and individually as SiN layer 38), multiple Silicon Oxynitride (SiO_XN_Y) layers 40-1 through 40-N_{SiON} (more generally referred to herein collectively as SiO_XN_Y layers 40 and individually as SiO_XN_Y layer 40) where X and Y are both greater than 0, and multiple SiO₂ layers 42-1 through 42-N_{SiO} (more generally referred to herein collectively as SiO₂ layers 42 and individually as SiO₂ layer 42) arranged in an SiN/SiO_XN_Y/SiO₂ pattern. The SiO_XN_Y layers 40-1 through 40-N_{SiON} are preferably formed of SiO_XN_Y having a refractive index measured at 632 nanometers (nm) in a range of 1.9 to 1.95. Notably, the refractive index of SiO_XN_Y at 632 nm ranges from approximately 1.4 for SiO₂ (i.e., Y=0) to approximately 2 for SiN (i.e., X=0). Thus, SiO_XN_Y having a refractive index measured at 632 nm in the range of 1.9 to 1.95 is a nitride-rich SiO_XN_Y.

[0041] The number (N_{SiN}) of SiN layers 38 is greater than or equal to 2, the number (N_{SiON}) of SiO_XN_Y layers 40 is greater than or equal to 1, and the number (N_{SiO}) of SiO₂ layers 42 is greater than or equal to 1. In this embodiment, the multi-layer environmental barrier 12 both begins and ends with an SiN layer, namely, the SiN layers 38-1 and 38-N_{SiN}, respectively. However, the multi-layer environmental barrier 12 may alternatively end with an SiO_XN_Y layer 40 or an

SiO₂ layer 42 (i.e., the SiO_xN_y layer 40-N_{SiON} or the SiO₂ layer 42-N_{SiO}). In one embodiment, the number (N_{SiN}) of SiN layers 38 is 2, the number (N_{SiON}) of SiO_xN_y layers 40 is 1, and the number (N_{SiO}) of SiO₂ layers 42 is 1 such that the multi-layer environmental barrier 12 includes only the SiN layer 38-1, the SiO_xN_y layer 40-1, the SiO₂ layer 42-1, and the SiN layer 38-2. However, in another embodiment, the multi-layer environmental barrier 12 includes a repeating structure of two or more SiN layers 38, two or more SiO_xN_y layers 40, and two or more SiO₂ layers 42 in an SiN/ SiO_xN_y/SiO₂ pattern. Then, in the illustrated embodiment, the multi-layer environmental barrier 12 further includes the final SiN layer 38-N_{SiN} on the repeating structure formed by the SiN layers 38-1 through 38-(N_{SiN}-1), the SiO_xN_y layers 40-1 through 40-N_{SiON}, and the SiO₂ layers 42-1 through 42-N_{SiO}. In other words, in the repeating structure, the structure of an SiN layer 38, an SiO_xN_y layer 40 on the SiN layer 38, and an SiO₂ layer 42 on the SiO_xN_y layer 40 is repeated N_{SiON} (or equivalently N_{SiO}) times, and, in the illustrated embodiment, the repeating structure is then terminated by the final SiN layer 38-N_{SiN}.

[0042] The SiN layers 38-1 through 38-N_{SiN}, the SiO_xN_y layers 40-1 through 40-N_{SiON}, and the SiO₂ layers 42-1 through 42-N_{SiO} are preferably formed using PECVD and/or ALD. In one particular embodiment, all of the SiN layers 38-1 through 38-N_{SiN}, all of the SiO_xN_y layers 40-1 through 40-N_{SiON}, and all of the SiO₂ layers 42-1 through 42-N_{SiO} are formed using PECVD. In another particular embodiment, all of the SiN layers 38-1 through 38-N_{SiN}, all of the SiO_xN_y layers 40-1 through 40-N_{SiON}, and all of the SiO₂ layers 42-1 through 42-N_{SiO} are formed using ALD. In yet another embodiment, some of the layers 38-1 through 38-N_{SiN}, 40-1 through 40-N_{SiON}, and 42-1 through 42-N_{SiO} are formed using PECVD and the rest of the layers 38-1 through 38-N_{SiN}, 40-1 through 40-N_{SiON}, and 42-1 through 42-N_{SiO} are formed using ALD. In one embodiment, a total thickness of the multi-layer environmental barrier 12 is in a range of and including 0.01 μm to 10 μm, and more preferably in a range of and including 0.1 μm to 5 μm. Thicknesses of each of the SiN layers 38-1 through 38-N_{SiN} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range

of and including 10 to 100 Angstroms in another embodiment. Further, all of the SiN layers 38-1 through 38-N_{SiN} may have the same thickness or some or all of the SiN layers 38-1 through 38-N_{SiN} may have different thicknesses. Likewise, thicknesses of each of the SiO_xN_y layers 40-1 through 40-N_{SiON} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another embodiment. Further, all of the SiO_xN_y layers 40-1 through 40-N_{SiON} may have the same thickness or some or all of the SiO_xN_y layers 40-1 through 40-N_{SiON} may have different thicknesses. In the same manner, thicknesses of each of the SiO₂ layers 42-1 through 42-N_{SiO} may, for example, be in a range of and including 5 to 1000 Angstroms in one embodiment or in a range of and including 10 to 100 Angstroms in another embodiment. Further, all of the SiO₂ layers 42-1 through 42-N_{SiO} may have the same thickness or some or all of the SiO₂ layers 42-1 through 42-N_{SiO} may have different thicknesses.

[0043] As discussed above, the applicability of the multi-layer environmental barrier 12 is not limited to the MESFET 10. For example, the multi-layer environmental barrier 12 may also be used with respect to a High Electron Mobility Transistor (HEMT) 44, as illustrated in Figure 5. In this example, the HEMT 44 is formed in a Group III nitride material system on a substrate 46. In particular, the HEMT 44 is formed in a GaN/AlGaN material system, and the substrate 46 is formed of SiC. The substrate 46 is a semi-insulating substrate. The term "semi-insulating" is used in a relative rather than an absolute sense. Alternative materials for the substrate 46 include Sapphire, AlN, AlGaN, GaN, Si, GaAs, ZnO, and InP. The substrate 46 is generally between 300 μm and 500 μm thick.

[0044] A channel layer 48 is formed on a surface of the substrate 46. Notably, as will be appreciated by one of ordinary skill in the art, a nucleation layer is typically formed between the substrate 46 and the channel layer 48 to provide an appropriate crystal structure transition between the substrate 46 and the channel layer 48. The channel layer 48 is formed by one or more epitaxial layers. For this example, the channel layer 48 is GaN. However, the channel

layer 48 may more generally be a Group III nitride such as GaN, $\text{Al}_x\text{Ga}_{1-x}\text{N}$ where $0 \leq x < 1$, Indium Gallium Nitride (InGaN), Aluminum Indium Gallium Nitride (AlInGaN), or the like. The channel layer 48 may be undoped, or at least unintentionally doped, and may be grown to a thickness of greater than about 20
5 Angstroms. In certain embodiments, the channel layer 48 may employ a multi-layer structure, such as a superlattice or alternating layers of different Group III nitrides, such as GaN, AlGaN, or the like.

[0045] A barrier layer 50 is formed on the channel layer 48. The barrier layer 50 may have a bandgap that is greater than a bandgap of the underlying channel
10 layer 48. Further, the barrier layer 50 may have a smaller electron affinity than the channel layer 48. In this illustrated embodiment, the barrier layer 50 is AlGaN; however, the barrier layer 50 may include AlGaN, AlInGaN, AlN, or various combinations of these layers. The barrier layer 50 is generally between 20 Angstroms and 400 Angstroms thick; however, the barrier layer 50 should not
15 be so thick as to cause cracking or substantial defect formation therein. The barrier layer 50 may be either undoped, or at least unintentionally doped, or doped with an n-type dopant to a concentration less than about $1 \times 10^{19} \text{ cm}^{-3}$. Notably, together, the channel layer 48 and the barrier layer 50 form a semiconductor body of the HEMT 44.

[0046] A source region 52 and a drain region 54 are formed in the semiconductor body by, for example, implanting appropriate ions into a surface of the barrier layer 50 to achieve a desired depth and doping concentration. The source and drain regions 52 and 54 extend just below the interface between the channel layer 48 and the barrier layer 50 where a two-dimensional electron gas
25 (2-DEG) plane is formed during operation and in which electron conductivity is modulated. A source contact 56 is formed by one or more metallic layers on, and preferably directly on, the surface of the barrier layer 50 over the source region 52. Likewise, a drain contact 58 is formed by one or more metallic layers on, and preferably directly on, the surface of the barrier layer 50 over the drain region 54.
30 The source and drain contacts 56 and 58 preferably provide low-resistance ohmic contacts to the source and drain regions 52 and 54, respectively. A gate

contact 60 is formed by one or more metallic layers on, and preferably directly on, a surface of the barrier layer 50 between the source region 52 and the drain region 54.

[0047] An SiN passivation structure 62 is formed on the surface of the semiconductor body, and specifically on the surface of the barrier layer 50, between the source contact 56 and the gate contact 60 and between the drain contact 58 and the gate contact 60. In this embodiment, the SiN passivation structure 62 extends over the gate contact 60. The SiN passivation structure 62 may be the same or substantially the same as the SiN passivation structure 28 of Figure 1. Lastly, the HEMT 44 includes the multi-layer environmental barrier 12 on the SiN passivation structure 62. The details of the multi-layer environmental barrier 12 are the same as described above and are therefore not repeated.

[0048] As another example, the multi-layer environmental barrier 12 may be used with respect to a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) 64, as illustrated in Figure 6. In this example, the MOSFET 64 includes a substrate 66 and a semiconductor body 68 on a surface of the substrate 66. The substrate 66 is preferably formed of SiC, but is not limited thereto. The substrate 66 may be formed of other materials such as, for example, Sapphire, AlN, AlGa_N, GaN, Si, GaAs, ZnO, and InP. The semiconductor body 68 preferably includes one or more epitaxial layers of one or more wide bandgap materials such as, for example, one or more Group III nitrides. For example, the semiconductor body 68 may be formed of one or more layers of GaN or AlGa_N. However, other Group III nitride materials may be used.

[0049] A source region 70 and a drain region 72 are formed in the semiconductor body 68 by, for example, implanting appropriate ions into a surface of the semiconductor body 68 to achieve a desired doping concentration. A source contact 74 is formed by one or more metallic layers on, and preferably directly on, the surface of the semiconductor body 68 over the source region 70. Likewise, a drain contact 76 is formed by one or more metallic layers on, and preferably directly on, the surface of the semiconductor body 68 over the drain region 72. The source and drain contacts 74 and 76 preferably provide low-

resistance ohmic contacts to the source and drain regions 70 and 72, respectively.

[0050] In this embodiment, an insulator layer 78 is formed on, and preferably directly on, a surface of the semiconductor body 68 between the source and drain contacts 74 and 76. The insulator layer 78 may be, for example, one or more oxide layers (e.g., SiO₂). A gate contact 80 is formed by one or more metallic layers on, and preferably directly on, a surface of the insulator layer 78. The region within the semiconductor body 68 between the source and drain regions 70 and 72 is referred to as a channel region of the MOSFET 64.

[0051] An SiN passivation structure 82 is formed on the surface of the semiconductor body 68, and more specifically on a surface of the insulator layer 78, between the source contact 74 and the gate contact 80 and between the drain contact 76 and the gate contact 80. In this embodiment, the SiN passivation structure 82 extends over the gate contact 80. The SiN passivation structure 82 may be the same or substantially the same as the SiN passivation structure 28 of Figure 1. Lastly, the MOSFET 64 includes the multi-layer environmental barrier 12 on the SiN passivation structure 82. The details of the multi-layer environmental barrier 12 are the same as described above and are therefore not repeated. Again, it should be noted that the MESFET 10, the HEMT 44, and the MOSFET 64 are only a few examples of semiconductor devices for which the multi-layer environmental barrier 12 can be used. The multi-layer environmental barrier 12 can be used for any semiconductor device for which an environmental barrier is desired.

[0052] Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

What is claimed is:

1. A semiconductor die on which a semiconductor device is fabricated,
5 comprising:
a semiconductor body;
a passivation structure on the semiconductor body; and
a multi-layer environmental barrier on the passivation structure.
- 10 2. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises multiple Plasma Enhanced Chemical Vapor Deposition (PECVD) layers of two or more different dielectric materials.
- 15 3. The semiconductor die of claim 2 wherein the multi-layer environmental barrier has less than 10 defects per square centimeter.
- 20 4. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises multiple Atomic Layer Deposition (ALD) layers of two or more different dielectric materials.
- 25 5. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a first layer of a first dielectric material on the passivation structure, a second layer of a second dielectric material on the first layer, and a third layer of the first dielectric material on the second layer.
- 30 6. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a repeating structure of a first layer of a first dielectric material and a second layer of a second dielectric material on the first layer of the first dielectric material.

7. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a first silicon nitride layer on the passivation structure, a silicon dioxide layer on the first silicon nitride layer, and a second silicon nitride layer on the silicon dioxide layer.

5

8. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a repeating structure of a silicon nitride layer and a silicon dioxide layer on the silicon nitride layer.

10 9. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a first silicon nitride layer on the passivation structure, a polymer layer on the first silicon nitride layer, and a second silicon nitride layer on the polymer layer.

15 10. The semiconductor die of claim 1 wherein the multi-layer environmental barrier comprises a repeating structure of a silicon nitride layer and a polymer layer on the silicon nitride layer.

11. The semiconductor die of claim 1 wherein the multi-layer environmental
20 barrier comprises a silicon nitride layer on the passivation structure, a silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer.

12. The semiconductor die of claim 1 wherein the multi-layer environmental
25 barrier comprises a repeating structure of a silicon nitride layer, a silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer.

13. A method comprising:
30 providing a semiconductor body;
providing a passivation structure on the semiconductor body; and

providing a multi-layer environmental barrier on the passivation structure.

14. The method of claim 13 wherein providing the multi-layer environmental barrier comprises depositing multiple dielectric layers of two or more different dielectric materials via Plasma Enhanced Chemical Vapor Deposition (PECVD).

15. The method of claim 13 wherein providing the multi-layer environmental barrier comprises depositing multiple dielectric layers of two or more different dielectric materials via Atomic Layer Deposition (ALD).

16. The method of claim 13 wherein providing the multi-layer environmental barrier comprises:

providing a first layer of a first dielectric material on the passivation structure;

providing a second layer of a second dielectric material on the first layer; and

providing a third layer of the first dielectric material on the second layer.

17. The method of claim 13 wherein providing the multi-layer environmental barrier comprises providing a repeating structure of a first layer of a first dielectric material and a second layer of a second dielectric material on the first layer of the first dielectric material.

18. The method of claim 17 wherein providing the repeating structure comprises providing each layer of the repeating structure via one of a group consisting of: Plasma Enhanced Chemical Vapor Deposition (PECVD) and Atomic Layer Deposition (ALD) layers.

19. The method of claim 13 wherein providing the multi-layer environmental barrier comprises:

providing a first silicon nitride layer on the passivation structure;

providing a silicon dioxide layer on the first silicon nitride layer; and
providing a second silicon nitride layer on the silicon dioxide layer.

20. The method of claim 13 wherein providing the multi-layer environmental
5 barrier comprises providing a repeating structure of a silicon nitride layer and a
silicon dioxide layer on the silicon nitride layer.

21. The method of claim 20 wherein providing the repeating structure
comprises providing each layer of the repeating structure via one of a group
10 consisting of: Plasma Enhanced Chemical Vapor Deposition (PECVD) and
Atomic Layer Deposition (ALD) layers.

22. The method of claim 13 wherein providing the multi-layer environmental
barrier comprises:
15 providing a first silicon nitride layer on the passivation structure;
providing a polymer layer on the first silicon nitride layer; and
providing a second silicon nitride layer on the polymer layer.

23. The method of claim 13 wherein providing the multi-layer environmental
20 barrier comprises providing a repeating structure of a silicon nitride layer and a
polymer layer on the silicon nitride layer.

24. The method of claim 23 wherein providing the repeating structure
comprises providing each layer of the repeating structure via one of a group
25 consisting of: Plasma Enhanced Chemical Vapor Deposition (PECVD) and
Atomic Layer Deposition (ALD) layers.

25. The method of claim 13 wherein providing the multi-layer environmental
barrier comprises:
30 providing a silicon nitride layer on the passivation structure;
providing a silicon oxynitride layer on the silicon nitride layer; and

providing a silicon dioxide layer on the silicon oxynitride layer.

26. The method of claim 13 wherein providing the multi-layer environmental barrier comprises providing a repeating structure of a silicon nitride layer, a
5 silicon oxynitride layer on the silicon nitride layer, and a silicon dioxide layer on the silicon oxynitride layer.

27. The method of claim 26 wherein providing the repeating structure comprises providing each layer of the repeating structure via one of a group
10 consisting of: Plasma Enhanced Chemical Vapor Deposition (PECVD) and Atomic Layer Deposition (ALD) layers.

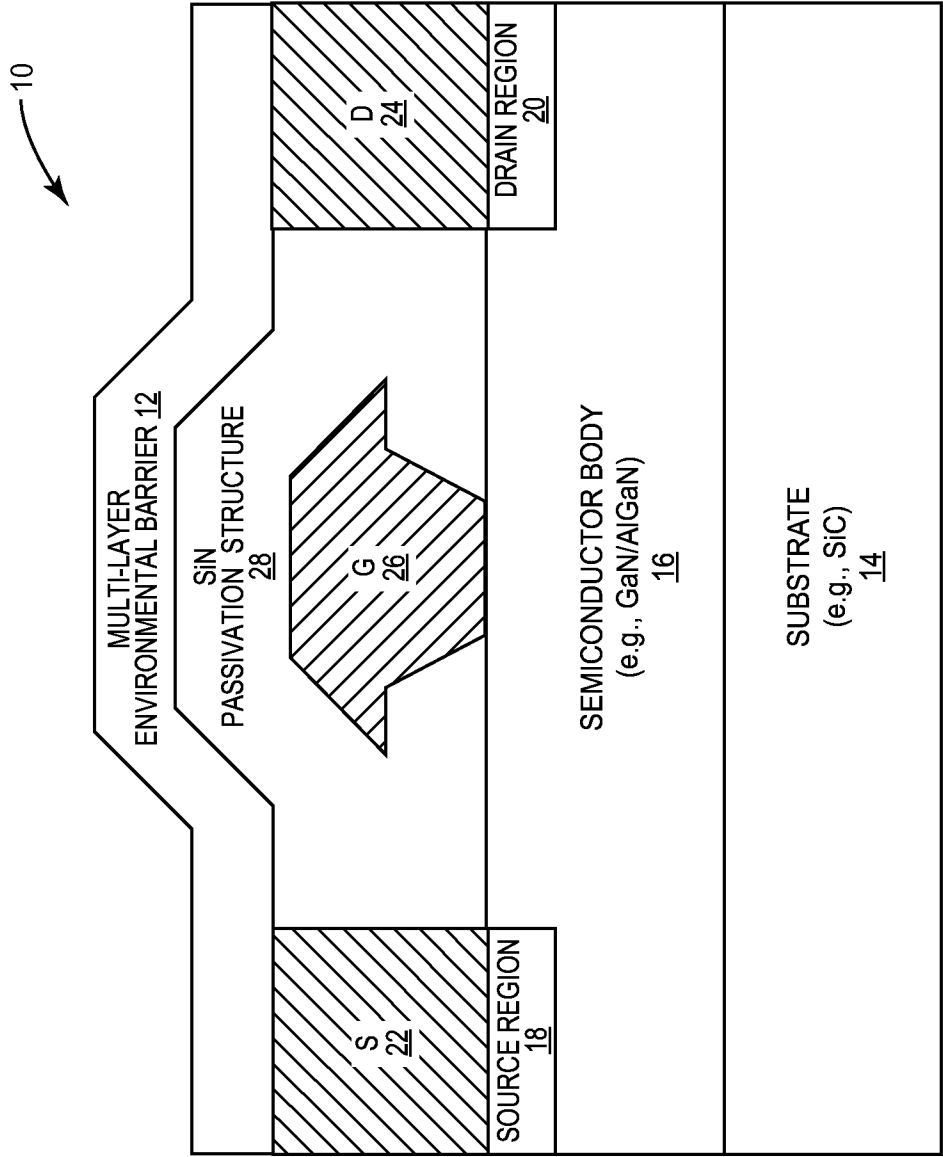


FIG. 1

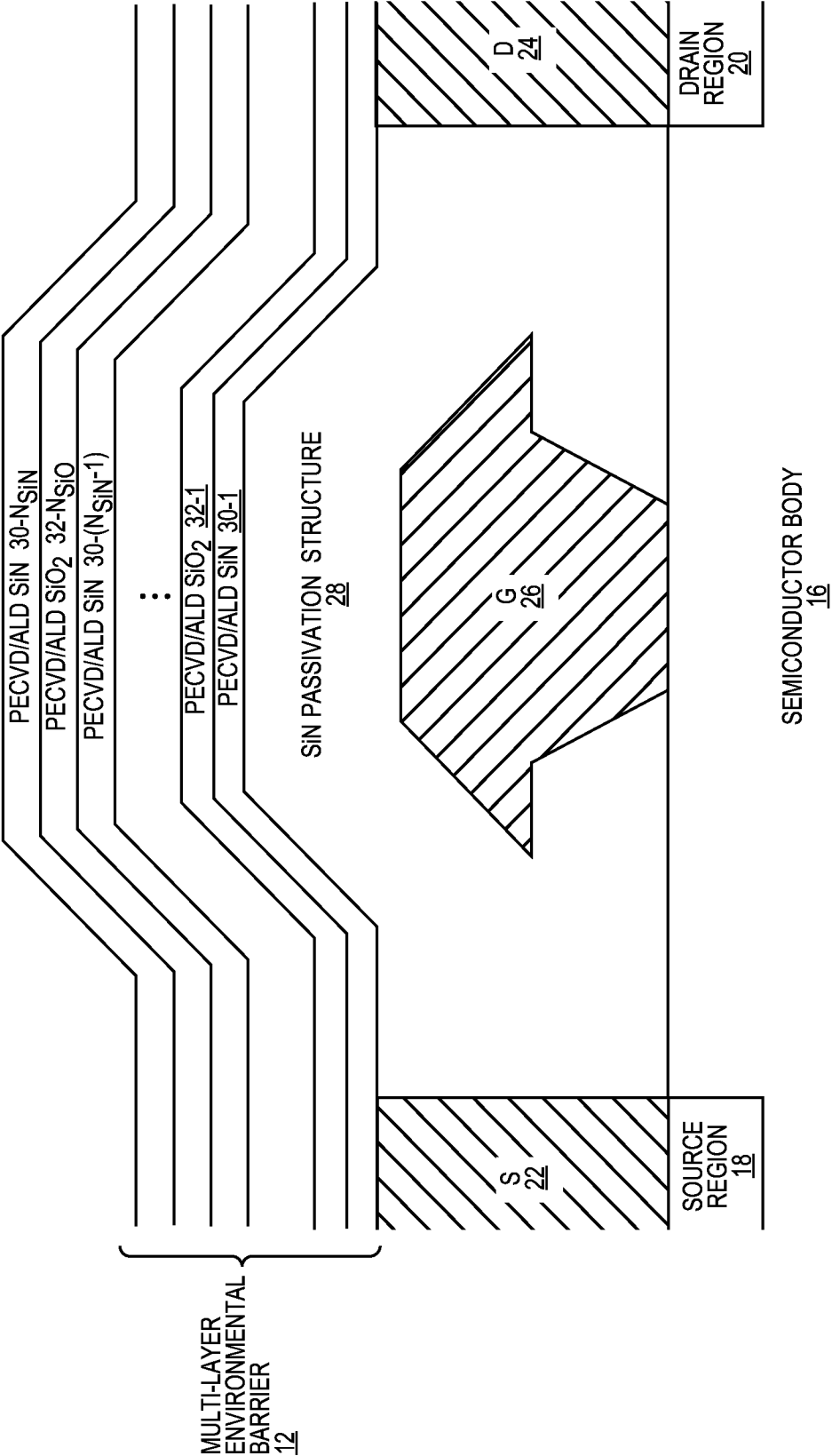


FIG. 2

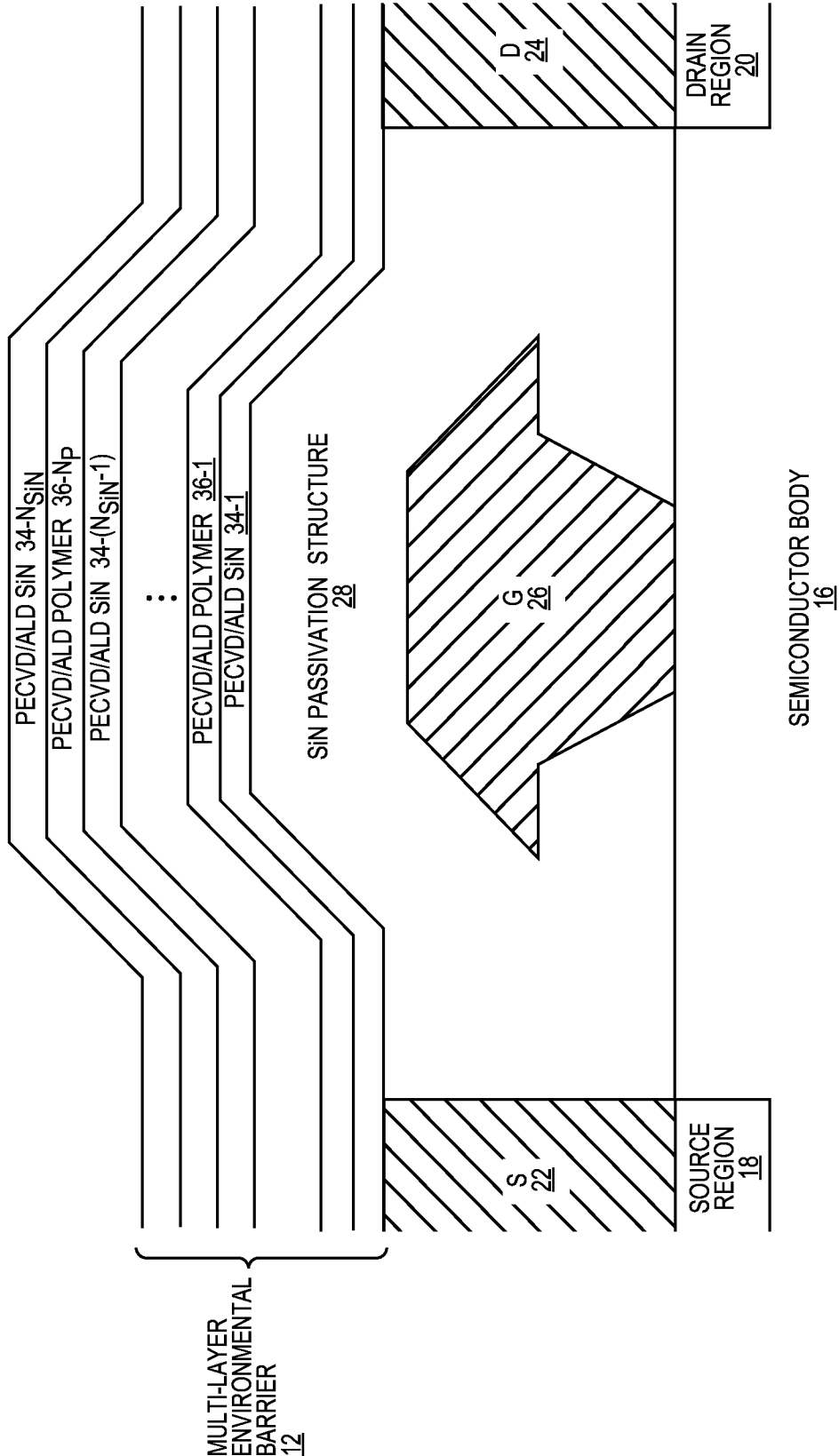


FIG. 3

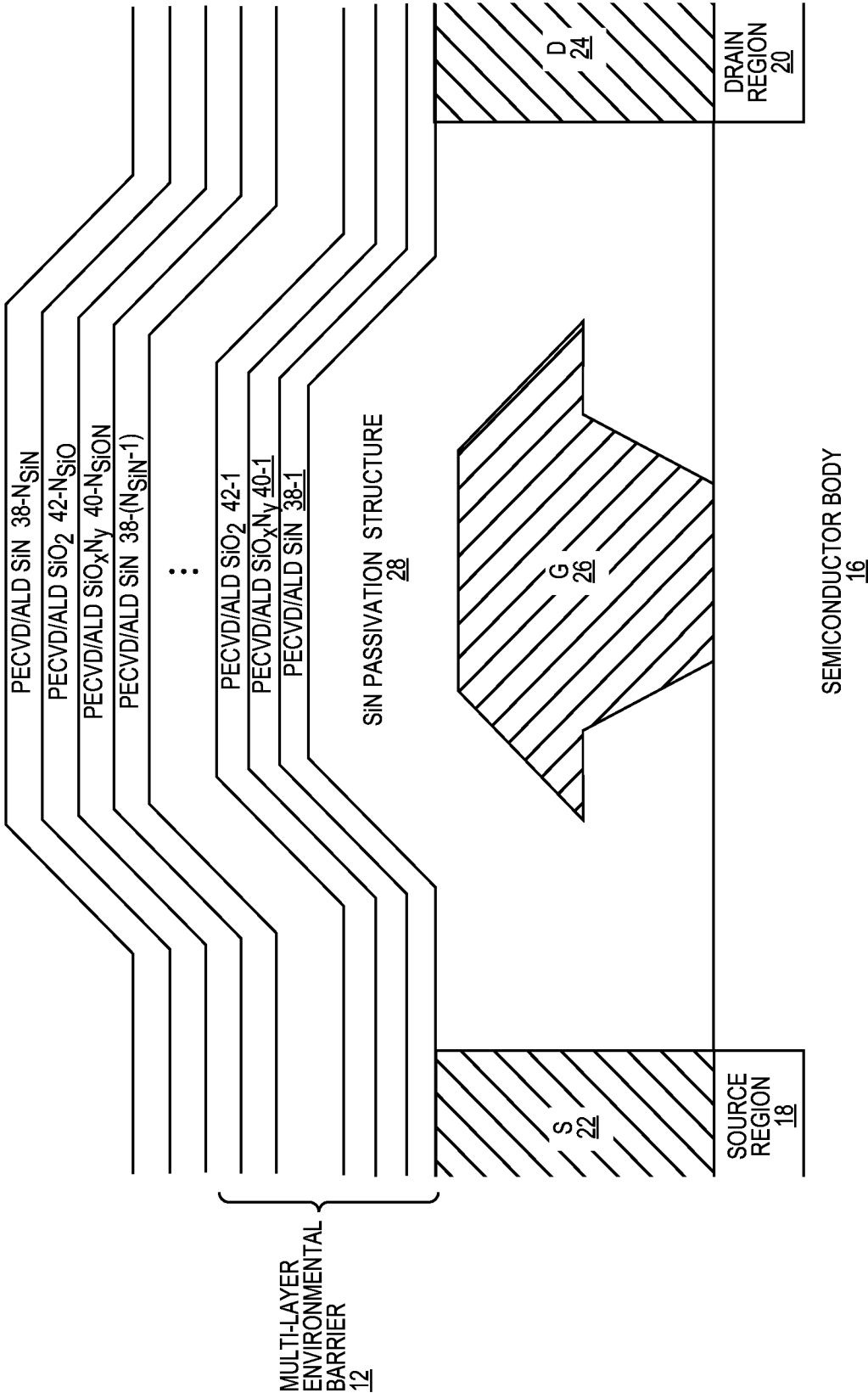


FIG. 4

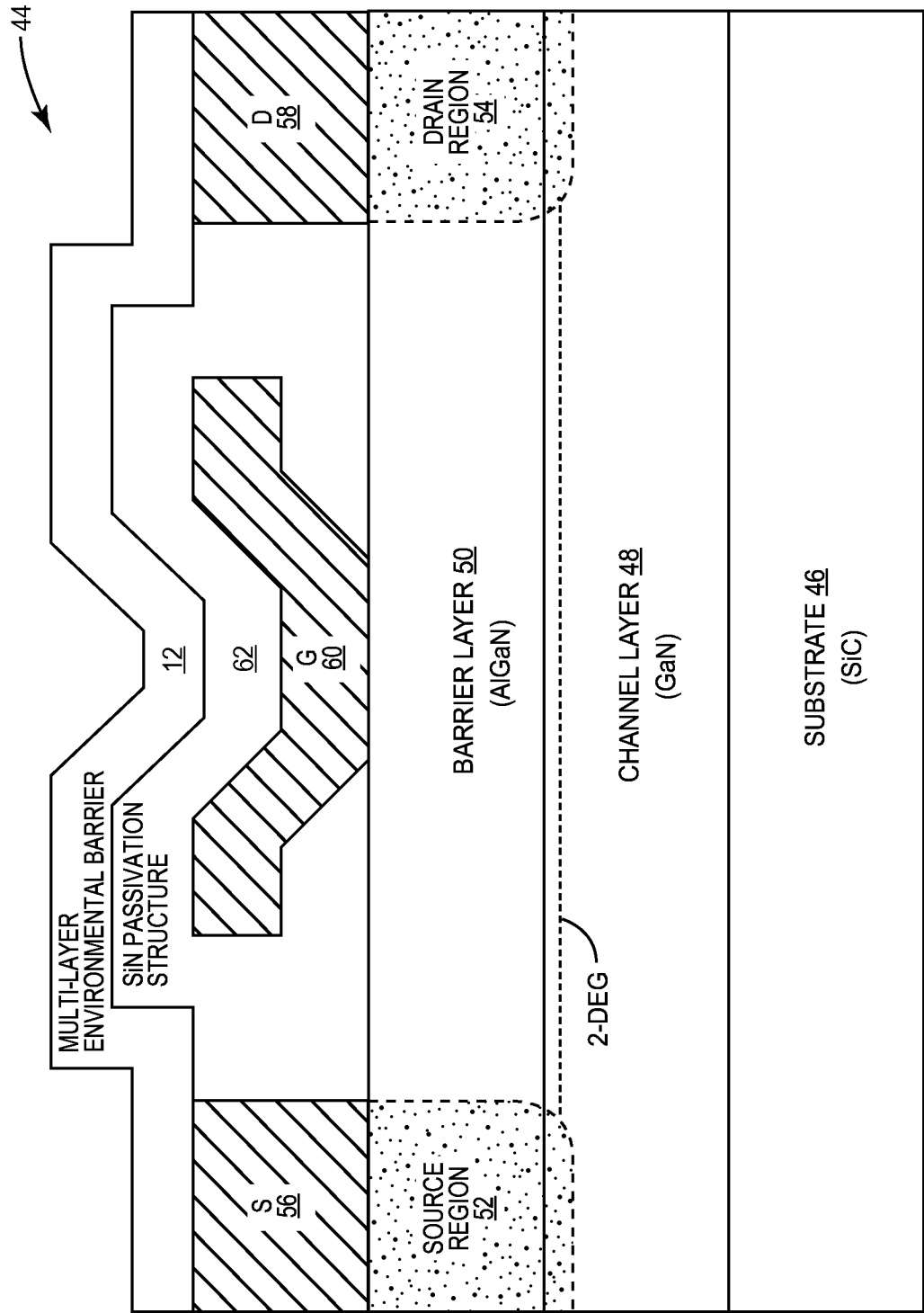


FIG. 5

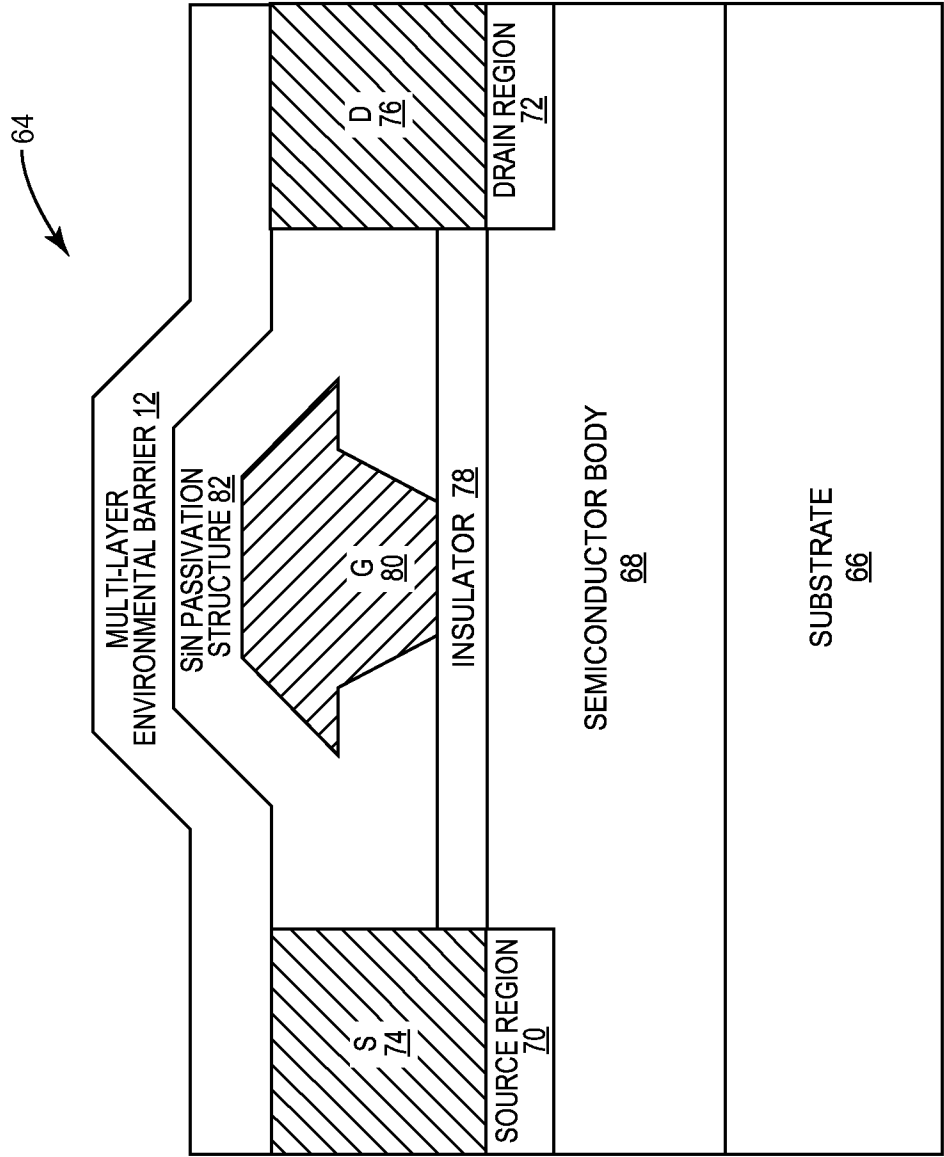


FIG. 6

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/011286

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L23/31

ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2001/019168 A1 (WILLER JOSEF [DE] ET AL) 6 September 2001 (2001-09-06) paragraphs [0007] - [0021]; figure 2 -----	1-8, 13-21
X	US 2002/011656 A1 (SWANSON LELAND S [US] ET AL) 31 January 2002 (2002-01-31) paragraphs [0028] - [0034]; figures 3,6 -----	1-3,13, 14
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Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

7 April 2014

Date of mailing of the international search report

17/06/2014

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INTERNATIONAL SEARCH REPORT

International application No

PCT/US2014/011286

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2011/151173 A1 (RAMADAS SENTHIL KUMAR [SG] ET AL) 23 June 2011 (2011-06-23) paragraphs [0005], [0019], [0030] - [0045], [0056] - [0057]; figure 3 -----	1,3-8, 11,12, 15-21, 25-27
X	US 2010/279092 A1 (HWANG JANG-YEON [KR] ET AL) 4 November 2010 (2010-11-04) paragraphs [0003], [0008], [0022] - [0088]; figures 6,7 -----	1,3,5,6, 13,16,17
A	US 2010/304047 A1 (YANG LIU [US] ET AL) 2 December 2010 (2010-12-02) the whole document -----	4,15,18, 21,27

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/011286

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-8, 11-21, 25-27

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-8, 11-21, 25-27

Semiconductor die and manufacturing method thereof, in which a multi-layer environmental barrier is provided, in particular comprising a stack of at least one set of silicon dioxide, silicon nitride, silicon oxynitride layers.

2. claims: 9, 10, 22-24

Semiconductor die and manufacturing method thereof, in which a multi-layer environmental barrier is provided comprising a stack of at least one set of silicon nitride and polymer layers.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/011286

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