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(71) Applicant (for all designated States except US): **EASTMAN KODAK COMPANY** [US/US]; 343 State Street, Rochester, New York 14650 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **COWDERY-CORVAN, Peter Jerome** [US/US]; 343 State Street, Rochester, New York 14650 (US). **LEVY, David Howard** [US/US]; 343 State Street, Rochester, New York 14650 (US). **PAWLIK, Thomas D.** [DE/US]; 343 State Street, Rochester,

New York 14650 (US). **FREEMAN, Diane Carol** [US/US]; 343 State Street, Rochester, New York 14650 (US).

(74) Common Representative: **EASTMAN KODAK COMPANY**; 343 State Street, Rochester, New York 14650 (US).

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(54) Title: PROCESS FOR MAKING DOPED ZINC OXIDE

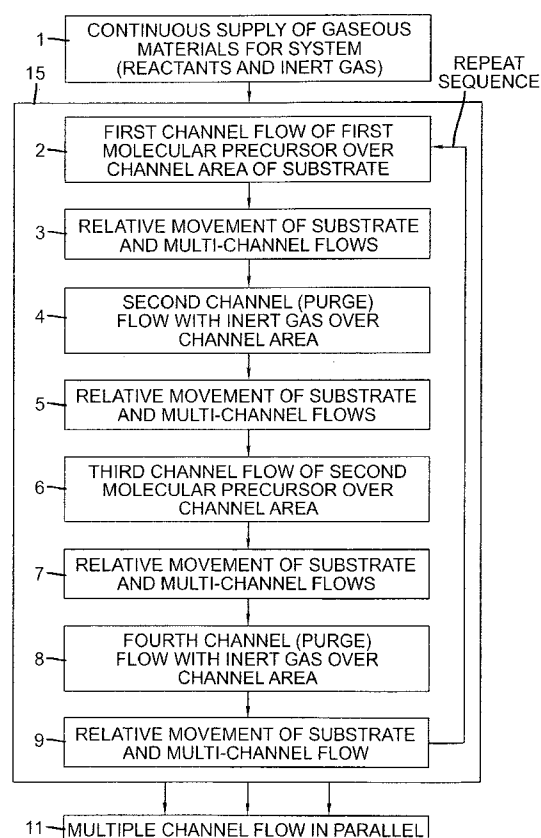


FIG. 1

(57) Abstract: The present invention relates to a process of making a zinc-oxide-based thin film semiconductor, for use in a transistor, comprising thin film deposition onto a substrate comprising providing a plurality of gaseous materials comprising first, second, and third gaseous materials, wherein the first gaseous material is a zinc-containing volatile material and the second gaseous material is reactive therewith such that when one of the first or second gaseous materials are on the surface of the substrate the other of the first or second gaseous materials will react to deposit a layer of material on the substrate, wherein the third gaseous material is inert and wherein a volatile indium-containing compound is introduced into the first reactive gaseous material or a supplemental gaseous material.

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PROCESS FOR MAKING DOPED ZINC OXIDE

FIELD OF THE INVENTION

This invention generally relates to the deposition of thin film zinc-oxide-based materials and, more particularly, to a process using atomic layer deposition. In particular, the present invention relates to a process of making a film of an indium-doped zinc-oxide-based semiconductor material for thin film transistors, which can be used in electronic devices, particularly in displays, the making of which at low temperature and near atmospheric pressure is advantageous.

BACKGROUND OF THE INVENTION

Thin film transistors (TFTs) are widely used as switching elements in electronics, for example, in active-matrix liquid-crystal displays, smart cards, and a variety of other electronic devices and components thereof. The thin film transistor (TFT) is an example of a field effect transistor (FET). The best-known example of an FET is the MOSFET (Metal-Oxide-Semiconductor-FET), today's conventional switching element for high-speed applications. For applications in which a transistor needs to be applied to a substrate, a thin film transistor is typically used. A critical step in fabricating the thin film transistor involves the deposition of a semiconductor onto the substrate. Presently, most thin film devices are made using vacuum deposited amorphous silicon as the semiconductor.

Amorphous silicon as a semiconductor for use in TFTs still has its drawbacks. The deposition of amorphous silicon, during the manufacture of transistors, requires relatively difficult or complicated processes such as plasma enhanced chemical vapor deposition and high temperatures (typically 360°C) to achieve the electrical characteristics sufficient for display applications. Such high processing temperatures disallow deposition on substrates made of certain plastics that might otherwise be desirable for use in applications such as flexible displays.

There is a growing interest in depositing thin film semiconductors on plastic or flexible substrates, particularly because these supports would be more mechanically robust, lighter weight, and potentially lead to cheaper manufacturing by allowing roll-to-roll processing. A useful example of a flexible substrate is

polyethylene terephthalate. Such plastics, however, limit device processing to below 200°C.

There is also interest in utilizing processes for deposition that do not involve the expense associated with vacuum processing. In typical vacuum
5 processing, a large metal chamber and sophisticated vacuum pumping systems are required in order to provide the necessary environment. These items increase the capital cost of systems and preclude the easy use of continuous web based systems.

In the past decade, various materials have received attention as a potential
10 alternative to amorphous silicon for use in semiconductor channels of thin film transistors. Semiconductor materials are desirable that are simpler to process, especially those that are capable of being applied to large areas by relatively simple processes. Semiconductor materials that can be deposited at lower temperatures would open up a wider range of substrate materials, including
15 plastics, for flexible electronic devices.

Thus, thin film transistors made of easily deposited semiconductor materials can be viewed as a potential key technology for circuitry in various electronic devices or components such as display backplanes, portable computers, pagers, memory elements in transaction cards, and identification tags, where ease
20 of fabrication, mechanical flexibility, and/or moderate operating temperatures are important considerations.

The discovery of practical inorganic semiconductors as a replacement for current silicon-based technologies has also been the subject of considerable research efforts. For example, metal oxide semiconductors are known that
25 constitute zinc oxide, indium oxide, gallium indium zinc oxide, tin oxide, or cadmium oxide deposited with or without additional doping elements including metals such as aluminum. Such semiconductor materials, which are transparent, can have an additional advantage for certain applications, as discussed below.

A semiconductor material useful in a TFT must display several
30 characteristics. In typical applications of a thin film transistor, the desire is for a switch that can control the flow of current through the device. As such, it is desired that when the switch is turned on a high current can flow through the

device. The extent of current flow is related to the semiconductor charge carrier mobility. When the device is turned off, it is desired that the current flow be very small. This is related to the native charge carrier concentration. Furthermore, it is desired that the device be weakly or not at all influenced by visible light to avoid a light-protection layer. In order for this to be true, the semiconductor band gap must be sufficiently large (> 3 eV) so that exposure to visible light does not cause an inter-band transition. Zinc oxide based materials are capable of delivering these features. Furthermore, in a real high volume web based atmospheric manufacturing scheme, it is highly desirable that the chemistries used in the process be both cheap and of low toxicity, which can be satisfied also by the use of ZnO-based materials and the majority of its precursors.

High on/off ratios result when the device in its off state has very low current flow, often referred to as current leakage. There are many applications in which low leakage is essential. In display applications, low leakage is required for the pixel select transistor. This select transistor is a switch that allows a charge to enter in and be stored in the pixel. In a perfect transistor without leakage, once the charge is stored in the pixel the transistor is switched to its off state and this charge cannot diminish by leakage through the select transistor. Too high of an off current in a transistor will cause a decay in stored charge in the pixel which results in poor display performance.

Another transistor characteristic that is relevant for useful operation is the steepness of the transistor turn on, represented by the subthreshold slope. As the gate voltage of a transistor is varied, the transistor will start in an off state, characterized by low current flow, and transition to an on state, characterized by high current flow. When the gate voltage reaches a point at which the transistor begins to turn on, there is a substantial increase in drain current with increasing gate voltage. This increase, called the subthreshold slope, is measured in volts of gate voltage per decade of drain current. This expression therefore represents the number of volts of gate voltage required to produce a 10-fold increase in drain current. Lower values of the subthreshold slope indicate faster device turn on and are desirable.

Various processes for making zinc oxide films have been disclosed, both high temperature and low temperature processes, including radio frequency magnetron sputtering or modified reactive planar magnetron sputtering.

Ohya et al. (Japanese Journal of Applied Physics, Part 1, January 2001, vol. 40, no.1, pages 297-8) disclose a thin film transistor of ZnO fabricated by chemical solution deposition.

Transparent conducting oxides are reviewed in the August 2000 issue of the Materials Research Bulletin, Volume 25 (8) 2000, devoted to materials and properties of transparent conducting oxide compounds.

One low temperature process for deposition of such oxide semiconductors is disclosed in US 2004/0127038 to Carcia et al. This publication discloses a semiconductor deposition process that uses magnetron sputtering of a metal oxide (ZnO, In₂O₃, SnO₂, CdO) or metal (Zn, In, Sn, Cd) target in an atmosphere with a controlled partial pressure of oxygen in an inert gas. This is a low temperature process that is compatible with temperature sensitive substrates and components, for example, drive circuits for displays on flexible, polymer substrates. The field effect transistors of Carcia et al. are based on a nominally undoped metal oxide semiconductor that must be deposited using physical vapor deposition or chemical vapor deposition, preferably rf (radio frequency) magnetron sputtering.

Steven K. Volkman et al., in "A novel transparent air-stable printable n-type semiconductor technology using ZnO nanoparticles," 2004 IEEE International Electron Device meeting Technical Digest, pp. 769, 2004, disclose a method for producing thin film transistors using organically stabilized zinc-oxide nanoparticles. The disclosed process involves an exposure to a temperature of 400°C.

Although successful zinc oxide based devices have been made with sputtering techniques, it is clear that very precise control over the reactive gas composition (such as oxygen content) is required to produce good quality devices. Chemical vapor deposition (CVD) techniques, in which two reactive gasses are mixed to form the desired film material, can be useful routes to achieving high quality film growth. Atomic layer deposition ("ALD") is yet another alternative film deposition technology that can provide improved thickness resolution and

conformal capabilities, compared to its CVD predecessor. The ALD process segments the conventional thin-film deposition process of conventional CVD into single atomic-layer deposition steps.

ALD can be used as a fabrication step for forming a number of types of thin-film electronic devices, including semiconductor devices and supporting electronic components such as resistors and capacitors, insulators, bus lines, and other conductive structures. ALD is particularly suited for forming thin layers of metal oxides in the components of electronic devices. General classes of functional materials that can be deposited with ALD include conductors, dielectrics or insulators, and semiconductors.

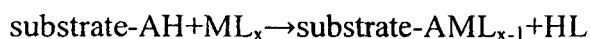
Examples of useful semiconducting materials are compound semiconductors such as gallium arsenide, gallium nitride, cadmium sulfide, zinc oxide, and zinc sulfide.

A number of device structures can be made with the functional layers described above. A capacitor results from placing a dielectric between two conductors. A diode results from placing two semiconductors of complementary carrier type between two conducting electrodes. There may also be disposed between the semiconductors of complementary carrier type a semiconductor region that is intrinsic, indicating that that region has low numbers of free charge carriers. A diode may also be constructed by placing a single semiconductor between two conductors, where one of the conductor/semiconductors interfaces produces a Schottky barrier that impedes current flow strongly in one direction. A transistor results from placing upon a conductor (the gate) an insulating layer followed by a semiconducting layer. If two or more additional conductor electrodes (source and drain) are placed spaced apart in contact with the top semiconductor layer, a transistor can be formed. Any of the above devices can be created in various configurations as long as the critical interfaces are created.

Advantageously, ALD steps are self-terminating and can deposit precisely one atomic layer when conducted up to or beyond self-termination exposure times. An atomic layer typically ranges from 0.1 to 0.5 molecular monolayers, with typical dimensions on the order of no more than a few Angstroms. In ALD, deposition of an atomic layer is the outcome of a chemical reaction between a

reactive molecular precursor and the substrate. In each separate ALD reaction-deposition step, the net reaction deposits the desired atomic layer and substantially eliminates "extra" atoms originally included in the molecular precursor. In its most pure form, ALD involves the adsorption and reaction of each of the precursors in the complete absence of the other precursor or precursors of the reaction. In practice in any process it is difficult to avoid some direct reaction of the different precursors leading to a small amount of chemical vapor deposition reaction. The goal of any process claiming to perform ALD is to obtain device performance and attributes commensurate with an ALD process while recognizing that a small amount of CVD reaction can be tolerated.

In ALD applications, typically two molecular precursors are introduced into the ALD reactor in separate stages. For example, a metal precursor molecule, ML_x , comprises a metal element, M that is bonded to an atomic or molecular ligand, L. For example, M could be, but would not be restricted to, Al, W, Ta, Si, Zn, etc. The metal precursor reacts with the substrate when the substrate surface is prepared to react directly with the molecular precursor. For example, the substrate surface typically is prepared to include hydrogen-containing ligands, AH or the like, that are reactive with the metal precursor. Sulfur (S), oxygen (O), and Nitrogen (N) are some typical A species. The gaseous precursor molecule effectively reacts with all of the ligands on the substrate surface, resulting in deposition of a single atomic layer of the metal:

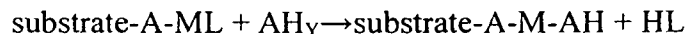


(1)

where HL is a reaction by-product. During the reaction, the initial surface ligands, AH, are consumed, and the surface becomes covered with AML_{x-1} ligands, which cannot further react with metal precursor ML_x . Therefore, the reaction self-terminates when all of the initial AH ligands on the surface are replaced with AML_{x-1} species. The reaction stage is typically followed by an inert-gas purge stage that eliminates the excess metal precursor and the HL by-product species from the chamber prior to the separate introduction of the other precursor.

A second molecular precursor then is used to restore the surface reactivity of the substrate towards the metal precursor. This is done, for example, by

removing the L ligands and re-depositing AH ligands. In this case, the second precursor typically comprises the desired (usually nonmetallic) element A (i.e., O, N, S), and hydrogen (i.e., H₂O, NH₃, H₂S). The next reaction is as follows:



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(2)

This converts the surface back to its AH-covered state. (Here, for the sake of simplicity, the chemical reactions are not balanced.) The desired additional element, A, is incorporated into the film and the undesired ligands, L, are eliminated as volatile by-products. Once again, the reaction consumes the reactive sites (this time, the L terminated sites) and self-terminates when the reactive sites on the substrate are entirely depleted. The second molecular precursor then is removed from the deposition chamber by flowing inert purge-gas in a second purge stage.

In summary, then, an ALD process requires alternating in sequence the flux of chemicals to the substrate. The representative ALD process, as discussed above, is a cycle having four different operational stages:

1. ML_x reaction;
2. ML_x purge;
3. AH_y reaction; and
4. AH_y purge, and then back to stage 1.

This repeated sequence of alternating surface reactions and precursor-removal that restores the substrate surface to its initial reactive state, with intervening purge operations, is a typical ALD deposition cycle. A key feature of ALD operation is the restoration of the substrate to its initial surface chemistry condition. Using this repeated set of steps, a film can be layered onto the substrate in equal metered layers that are all identical in chemical kinetics, deposition per cycle, composition, and thickness.

Self-saturating surface reactions make ALD insensitive to transport non-uniformities, which might otherwise impair surface uniformity, due either to engineering tolerances and the limitations of the flow process or related to surface topography (that is, deposition into three dimensional, high aspect ratio

structures). As a general rule, a non-uniform flux of chemicals in a reactive process generally results in different completion times at different areas.

However, with ALD, each of the reactions is allowed to complete on the entire substrate surface. Thus, differences in completion kinetics impose no penalty on
5 uniformity. This is because the areas that are first to complete the reaction self-terminate the reaction; other areas are able to continue until the full treated surface undergoes the intended reaction.

Typically, an ALD process deposits 0.1 - 0.2 nm of a film in a single ALD cycle (with numbered steps 1 through 4 as listed earlier). A useful and
10 economically feasible cycle time must be achieved in order to provide a uniform film thickness in a range of from 3 nm to 300 nm for many or most semiconductor applications, and even thicker films for other applications. Industry throughput standards dictate that substrates be processed in 2 minutes to 3 minutes, which means that ALD cycle times must be in a range from 0.6 seconds to 6 seconds.

15 An ALD process must be able to execute this sequencing efficiently and reliably for many cycles in order to allow cost-effective coating of many substrates. In an effort to minimize the time that an ALD reaction needs to reach self-termination, at any given reaction temperature, one approach has been to maximize the flux of chemicals flowing into the ALD reactor, using a so-called
20 "pulsing" process. In the pulsed ALD process, a substrate sits in a chamber and is exposed to the above sequence of gases by allowing a first gas to enter the chamber, followed by a pumping cycle to remove that gas, followed by the introduction of a second gas to the chamber, followed by a pumping cycle to remove the second gas. This sequence can be repeated at any frequency and
25 variations in gas type and/or concentration. The net effect is that the entire chamber experiences a variation in gas composition with time, and thus this type of ALD can be referred to as time dependent ALD. The vast majority of existing ALD processes are time dependent ALD.

In order to maximize the flux of chemicals into the ALD reactor, it is
30 advantageous to introduce the molecular precursors into the ALD reactor with minimum dilution of inert gas and at high pressures. However, these measures work against the need to achieve short cycle times and the rapid removal of these

molecular precursors from the ALD reactor. Rapid removal in turn dictates that gas residence time in the ALD reactor be minimized.

Existing ALD approaches have been compromised with the trade-off between the need to shorten reaction times and improve chemical utilization efficiency, and on the other hand, the need to minimize purge-gas residence and chemical removal times. One approach to overcome the inherent limitations of time dependent ALD systems is to provide each reactant gas continuously and to move the substrate through each gas in succession. In these systems a relatively constant gas composition exists, but is located to specific areas or spaces of the processing system. Therefore, these systems will be referred to as spatially dependent ALD systems.

For example, U.S. Patent No. 6,821,563 entitled "GAS DISTRIBUTION SYSTEM FOR CYCLICAL LAYER DEPOSITION" to Yudovsky describes a spatially dependent ALD processing system, under vacuum, having separate gas ports for precursor and purge gases, alternating with vacuum pump ports between each gas port. Each gas port directs its stream of gas vertically downward toward a substrate. The separate gas flows are separated by walls or partitions, with vacuum pumps for evacuating gas on both sides of each gas stream. A lower portion of each partition extends close to the substrate, for example, 0.5 mm or greater from the substrate surface. In this manner, the lower portions of the partitions are separated from the substrate surface by a distance sufficient to allow the gas streams to flow around the lower portions toward the vacuum ports after the gas streams react with the substrate surface.

A rotary turntable or other transport device is provided for holding one or more substrate wafers. With this arrangement, the substrate is shuttled beneath the different gas streams, effecting ALD deposition thereby. In one embodiment, the substrate is moved in a linear path through a chamber, in which the substrate is passed back and forth a number of times.

Another approach using continuous gas flow spatially dependent ALD is shown in U.S. Patent No. 4,413,022 entitled "METHOD FOR PERFORMING GROWTH OF COMPOUND THIN FILMS" to Suntola et al. A gas flow array is provided with alternating source gas openings, carrier gas openings, and vacuum

exhaust openings. Reciprocating motion of the substrate over the array effects ALD deposition, again, without the need for pulsed operation. In the embodiment of Figures 13 and 14, in particular, sequential interactions between a substrate surface and reactive vapors are made by a reciprocating motion of the substrate over a fixed array of source openings. Diffusion barriers are formed by a carrier gas opening between exhaust openings. Suntola et al. state that operation with such an embodiment is possible even at atmospheric pressure, although little or no details of the process, or examples, are provided.

While processes such as those described in the '563 Yudovsky and '022 Suntola et al. patents may avoid some of the difficulties inherent to pulsed gas approaches, these processes have other drawbacks. For example, it would be very difficult to maintain a uniform vacuum at different points in an array and to maintain synchronous gas flow and vacuum at complementary pressures, thus compromising the uniformity of gas flux that is provided to the substrate surface. Neither the gas flow delivery unit of the '563 Yudovsky patent nor the gas flow array of the '022 Suntola et al. patent can be used in closer proximity to the substrate than 0.5 mm.

U.S. Patent Publication No. 2005/0084610 to Selitser discloses an atmospheric pressure atomic layer chemical vapor deposition process. Selitser states that extraordinary increases in reaction rates are obtained by changing the operating pressure to atmospheric pressure, which will involve orders of magnitude increase in the concentration of reactants, with consequent enhancement of surface reactant rates. The embodiments of Selitser involve separate chambers for each stage of the process, although Figure 10 shows an embodiment in which chamber walls are removed. A series of separated injectors are spaced around a rotating circular substrate holder track. Each injector incorporates independently operated reactant, purging, and exhaust gas manifolds and controls and acts as one complete mono-layer deposition and reactant purge cycle for each substrate as it passes there under in the process. Little or no specific details of the gas injectors or manifolds are described by Selitser, although it is stated that spacing of the injectors is selected so that cross-

contamination from adjacent injectors is prevented by purging gas flows and exhaust manifolds incorporated in each injector.

A spatially dependent ALD process can be accomplished with other apparatus or systems described in more detail in commonly assigned US Application No. 11/392,007, US Application No. 11/392,006, US Application No. 11/620,744, and US Application No. 11/620,740. These systems attempt to overcome one of the difficult aspects of a spatial ALD system, which is undesired intermixing of the continuously flowing mutually reactive gases. In particular, US Application No. 11/392,007 employs a novel transverse flow pattern to prevent intermixing, while US Application No. 11/620,744 and US Application No. 11/620,740 employ a coating head partially levitated by the pressure of the reactive gases of the process to accomplish improved gas separation.

Scientists have theorized in recent years that amorphous films are more robust than poly-crystalline or crystalline films. The advantages over polycrystalline films are a decreased surface roughness and an absence of grain boundaries that act as both charge trapping sites and diffusion pathways. While single crystalline films would generally have the highest mobilities, the deposition of a film that is single crystalline over a large area is very difficult, especially if flexibility in the choice of substrate is desired. Amorphous zinc oxide-based semiconductors are especially advantaged because the penalty in carrier mobility going from the crystalline to the amorphous state is much less compared to crystalline and amorphous silicon. This is due to the fact that the conduction band of ZnO is comprised of s-type wave functions that are spherically symmetric, whereas p-type wave functions make up the conduction band of Si.

Indium-doped zinc-oxide films and indium zinc oxides (IZOs) have received attention both as conductive transparent oxides and as transparent semiconducting materials for use in devices such as thin film transistors (TFTs). As noted above, these types of films are typically made by vacuum processes such as rf magnetron sputtering. Song et al. reported in 2007 on amorphous indium zinc oxide TFTs formed at room temperature by rf magnetron sputtering (Song et al., Applied Physics Letters 90, 022106 (2007)). In order to control the carrier

concentration of the active channel, the partial pressure of oxygen in the sputtering chamber had to be controlled.

Studies on indium-doped zinc-oxide films formed by chemical spray pyrolysis were done by Joseph, et al. (Joseph et al., Bull.Mater. Sci. 28, 5, (2005)).

5 Joseph, et al. were able to form low resistivity IZO films which, however, were polycrystalline in nature. Additionally, the spray pyrolysis technique used requires substrate temperatures of 723 K or approximately 450°C.

A common approach to chemically modifying the nature of a semiconductor is to include in the matrix of the semiconductor other atoms or
10 molecules which vary the electrical properties of the semiconductor. These additional atoms typically operate by accepting or donating mobile charge to the system. In the case of a semiconductor like zinc oxide, acceptor dopants can be used to trap electrons, thus driving the semiconductor to have increased hole concentration and toward a p-type semiconductor. Alternatively, donor dopants
15 tend to release electrons and in a semiconductor like zinc oxide this can produce high numbers of conduction band electrons, a desirable effect for applications requiring conductivity. Indium is a donor dopant for a zinc-oxide-based material.

In some instances, incorporating both donor and acceptor dopants into a zinc-oxide-based material can increase the control one has in selecting carrier type
20 and concentration. Chen et al. found that for zinc oxide films co-doped with indium and nitrogen they could vary the films from p-type to n-type by controlling the substrate temperature (Chen, et al., Applied Physics Letters 89, 252113 (2006)). Chen et al. used direct current (DC) reactive magnetron sputtering for their experiments, varying the substrate temperatures between 440°C and 600°C.

25 It is, thus, known that indium incorporation in zinc-oxide-based films can provide the benefit of decreased coating crystallinity and increased conductivity. There remains a need to provide a useful and cost effective process for producing indium-doped a zinc-oxide-based films.

SUMMARY OF THE INVENTION

30 In the material produced by a spatial ALD process, defects in the materials may lead to two deleterious effects. First, such materials may tend to have too high a concentration of native charge carrier, leading to high off currents.

Secondly, such materials may tend to contain defect sites that can cause bulk charging effects, leading to poor subthreshold slope. The present invention provides doping methods that permit zinc-oxide-based semiconductor materials produced in a spatially dependent ALD system to effectively work in practice and perform more robustly.

Accordingly, the present invention relates to a process of making an indium-doped n-type zinc-oxide-based thin film semiconductor by depositing a thin film material on a given surface area of a substrate (either an entire surface area or a selected portion thereof) wherein the deposition process is an atomic layer deposition process that is carried out substantially at or above atmospheric pressure, wherein the temperature of the substrate during deposition is under 300°C, and wherein the atomic layer deposition process comprises simultaneously directing a series of gas flows along elongated substantially parallel channels comprising, in order, at least a first reactive gaseous material containing a zinc-containing compound, an inert purge gas, and a second reactive gaseous material through a plurality of output openings spaced apart from the substrate, and transporting the substrate in a direction relative to the plurality of output openings, such that any point on the surface area of the substrate experiences a sequence of the first, second and third gaseous materials, whereby the sequence causes a thin film to be formed by atomic layer deposition on the surface area of the substrate, wherein a volatile indium-containing compound is introduced into the first reactive gaseous material or a supplemental gaseous material such that the indium-containing compound has a molar flow at a level of greater than 20 percent of the molar flow of the zinc-containing compound.

During the process, the substrate or deposition device for the gaseous materials, or both, is capable of providing relative movement between the output face of the deposition device and the substrate while maintaining close proximity.

In a preferred embodiment, the process can be operated with continuous movement of a substrate being subjected to thin film deposition, wherein the process is capable of conveying the support on or as a web past the deposition device, preferably in an unsealed environment to ambient at substantially atmospheric pressure.

It is an advantage of the present invention that it provides an advantageous process for atomic layer deposition of indium doped zinc-oxide-based thin film onto a substrate, well suited to a number of different types of substrates and deposition environments.

5 It is yet a further advantage of the present invention that it is adaptable for deposition on a web or other moving substrate, including deposition onto a large area substrate.

It is a further advantage of the present invention that it allows operation, in preferred embodiments, under atmospheric pressure conditions.

10 It is still a further advantage of the present invention that it can be employed in low temperature processes at atmospheric pressures, which processes may be practiced in an unsealed environment, open to ambient atmosphere.

The invention is also directed to a transistor comprising a zinc-oxide-based semiconductor, preferably on a flexible substrate, made by the present process.

15 Semiconductor films made by the present method are capable of exhibiting, in the film form, excellent field-effect electron mobilities of greater than $0.1 \text{ cm}^2/\text{Vs}$ and on-off ratios of greater than 10^4 , in which performance properties are sufficient for use in a variety of relevant technologies, including active matrix display backplanes.

20 A TFT structure includes, in addition to the zinc-oxide-based semiconductor, conducting electrodes, commonly referred to as a source and a drain, for injecting a current into the zinc-oxide-based semiconductor. The n-channel semiconductor films made by the present invention can be used in thin film transistors each comprising spaced apart first and second contact means
25 connected to an n-channel semiconductor film. A third contact means can be spaced from said semiconductor film by an insulator, and adapted for controlling, by means of a voltage applied to the third contact means, a current between the first and second contact means through said film. The first, second, and third contact means can correspond to a drain, source, and gate electrode in a field
30 effect transistor.

The objects, features, and advantages of the present invention will become apparent to those skilled in the art upon a reading of the following detailed

description when taken in conjunction with the drawings wherein there is shown and described an illustrative embodiment of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

While the specification concludes with claims particularly pointing out and distinctly claiming the subject matter of the present invention, it is believed that the invention will be better understood from the following description when taken in conjunction with the accompanying drawings, wherein:

Figure 1 is a flow chart describing the steps of the present process;

Figure 2 is a cross-sectional side view of one embodiment of a deposition device for atomic layer deposition that can be used in the present process;

Figure 3 is a cross-sectional side view of an embodiment, for one exemplary system of gaseous materials, of the distribution of gaseous materials to a substrate that is subject to thin film deposition;

Figures 4A and 4B are cross-sectional side views of one embodiment of the distribution of a system of gaseous materials, schematically showing the accompanying deposition operation;

Figure 5 is a perspective view, from the output face side, of a portion of one embodiment of a deposition device, showing the orientation of output channels relative to the substrate and reciprocating motion, which can be used for deposition on the substrate;

Figure 6 is a perspective view as in Figure 5, showing one exemplary arrangement of gas flow in the deposition device;

Figures 7A, 7B, 7C, and 7D are cross-sectional views taken orthogonally to the cross-sectional views of previous Figures 2-4B, showing gas flow directions for output channels in various embodiments;

Figures 8A and 8B are cross-sectional views showing the impact of reduced distance from the output face, of a deposition device for providing gaseous materials, to the substrate surface;

Figure 9 is a plan view of the output face of a deposition device such as shown in Figure 3 that can be used in the present process, showing movement of gaseous materials through an arrangement of output channels according to one embodiment of the invention;

Figure 10 is a perspective view of one embodiment of a deposition device formed from stacked plates that can be used in the present process;

Figures 11A and 11B are exploded views of the construction of a deposition device that employs the stacked-plate structure shown in Figure 10, the exploded views showing two different output channels for different gases used in the process;

Figure 12 is a perspective view showing an embodiment using an enveloping shroud of inert gas directed along the perimeter of the deposition device;

Figure 13 is a schematic diagram showing an alternative motion pattern for reciprocating and orthogonal movement;

Figure 14 is a block diagram of one embodiment of a deposition system that uses the process according to the present invention;

Figure 15 is a block diagram showing one embodiment of a deposition system applied to a moving web in accordance with the present process;

Figure 16 is a block diagram showing another embodiment of a deposition system applied to a moving web in accordance with the present process, with the deposition device stationary;

Figure 17 is a cross-sectional side view of one embodiment of a deposition device with an output face having curvature that can be used in the present process;

Figure 18 is a block diagram of the source materials for a thin film deposition process according to the Examples;

Figure 19 is a cross-sectional side view of a deposition device used in the present process, showing the arrangement of gaseous materials provided to a substrate that is subject to the thin film deposition process of the Examples;

Figure 20 illustrates a cross-sectional view of a typical thin film transistor having a bottom-gate/bottom-contact configuration;

Figure 21 illustrates a cross-sectional view of a typical thin film transistor having a bottom-gate/top-contact configuration;

Figure 22 illustrates a cross-sectional view of a typical thin film transistor having a top-gate/bottom-contact structure;

Figure 23 illustrates a cross-sectional view of a typical thin film transistor having a top-gate/top-contact structure;

Figure 24 illustrates a typical active matrix pixel design comprising a select transistor and capacitor representing the capacitance due to display design;

5 Figure 25 illustrates a typical pixel layout comprising data lines, control lines, thin film transistors, and pixel conductor pads;

Figure 26 shows overlaid X-ray diffraction spectra of a series of Indium-doped ZnO films made using the atmospheric pressure ALD process herein at a range of Indium dopant levels, wherein at the highest Indium dopant levels the
10 peak intensity is diminished as the crystallinity of the ZnO film approaches an amorphous state, as described in the Examples; and

Figure 27 shows comparative changes in the CESR spectra of a series of Indium-doped ZnO layers as the Indium level was varied from zero to a higher level, as described in the Examples.

15 **DETAILED DESCRIPTION OF THE INVENTION**

The semiconductor films made according to the present method exhibit a field effect electron mobility that is greater than $0.01 \text{ cm}^2/\text{Vs}$, preferably at least $0.1 \text{ cm}^2/\text{Vs}$, more preferably greater than $1 \text{ cm}^2/\text{Vs}$. In addition, n-channel semiconductor devices made according to the present invention are capable of
20 providing on/off ratios of at least 10^4 , advantageously at least 10^5 or 10^6 .

Furthermore, it is desired that the device be weakly or not at all influenced by visible light. In order for this to be true, the semiconductor band gap must be sufficiently large ($> 3 \text{ eV}$) so that exposure to visible light does not cause an inter-band transition.

25 Zinc-oxide-based materials are capable of yielding a high mobility, low carrier concentration, and high band gap. Furthermore, in a real high volume web based atmospheric manufacturing scheme, it is highly desirable that the chemistries used in the process be both cheap and of low toxicity, which can be satisfied by the use of ZnO-based materials and the majority of its precursors.

30 The present invention employs an n-type zinc-oxide-based thin film semiconductor that is deposited as a thin film material on a surface area of a substrate, either an entire surface area or a selected portion thereof, by an atomic

layer deposition process. The atomic layer deposition process comprises simultaneously directing a series of gas flows along elongated substantially parallel channels comprising, in order, at least a first reactive gaseous material containing a zinc-containing compound, an inert purge gas, and a second reactive
5 gaseous material through a plurality of output openings spaced apart from the substrate, and transporting the substrate in a direction relative to the plurality of output openings, such that any point on the surface area of the substrate experiences a sequence of the first, second and third gaseous materials. In particular, a volatile indium-containing compound is introduced into the first
10 reactive gaseous material or a supplemental gaseous material such that the indium-containing compound has a molar flow at a level of greater than 20 percent of the molar flow of the zinc-containing compound.

Preferably, the weight ratio of zinc to indium in the zinc-oxide-based thin film semiconductor is 0.05 to 0.7, preferably 0.2 to 0.5.

15 In the preferred embodiment, the introduction of the indium results in the crystallinity of the zinc-oxide-based film being less than 85 percent as measured by x-ray diffraction. The volatile indium-containing compound suitably can be a trialkylindium compound, such as trimethylindium, or cyclopentadienylindium(I), wherein the alkyl has 1 to 4 carbon atoms, preferably 1 to 2 carbon atoms.

20 As a consequence of introducing indium into the zinc-oxide-based film during the process, the resistivity of the zinc oxide based film can be reduced relative to the resistivity of a similar film not containing indium. The presence of incorporated indium dopant derived from an indium-containing compound or precursor can provide a decrease in resistivity by a factor of at least 10 in the thin
25 film material. Consequently, the zinc-oxide-based thin film semiconductor can effectively serve as the channel layer of a thin film transistor or as one or more conductive electrodes of a thin film transistor such as a gate material. The zinc-oxide-based thin film semiconductor can also serve as an electrical conduit in an electronic circuit in some applications such as displays. The zinc-oxide-based
30 semiconductor material can contain minor amounts of other metals capable of forming semiconducting oxides such as tin or cadmium, and combinations thereof. For example, Chiang, H.Q. et al., "High mobility transparent thin-film transistors

with amorphous zinc tin oxide channel layer,” Applied Physics Letters **86**, 013503 (2005) discloses zinc tin oxide materials.

Accordingly, the term “zinc-oxide-based” refers to a composition comprising mostly zinc and indium as the metal, but (excluding oxygen) allowing
5 up to 20 percent by weight of other elements or dopants, as will be appreciated by the skilled artisan. The highest In/Zn ratio in the coated indium-doped zinc oxide layer herein is 45 weight % (mass of In atoms to Zn atoms). The Indium-doped zinc oxide may have a different preferable concentration of Indium, depending on whether the material is used as a conductive material or a semiconductive
10 material, for example, a conductive electrode or the semiconductor of a transistor. In one embodiment, the preferable In/Zn ratio by weight for a semiconductor in a transistor is 10 weight % Indium, and the preferable In/Zn ratio for a conductive material, for example a gate electrode, is 30 weight %. Overall, the preferable range of In/Zn weight ratio is between 5% and 60%, more preferably from 10 to
15 50 percent.

Nominally undoped zinc oxide shows n-type conductivity because of the presence of shallow donors. Lattice imperfections due to a deviation from stoichiometry are thought to play a role in the creation of shallow donor states, although unintentionally incorporated hydrogen is also considered as a source of
20 shallow donor states. See D. C. Look, J. R. Sizelove and J. W. Hemsky, Phys. Rev. Lett. **82**, 2552 - 2555 (1999); C. G. Van de Walle, Phys. Rev. Lett. **85** 1012 (2000). These shallow donors have in common that they introduce occupied energy levels that are less than 100 meV below the conduction band edge of zinc oxide. Electrons occupying these shallow donor states can be promoted into the
25 conduction band via thermal excitation and lead to intrinsic conductivity.

In order to improve off currents, the zinc oxide based semiconductor must have low numbers of native charge carriers, leading to a high resistivity. According to one embodiment, therefore, the resistivity of the ZnO can be enhanced by substitutional doping with an acceptor dopant made from a volatile
30 organic compound, for example, volatile compounds comprising an acceptor dopant such as N, P, As, Li, Na, K, Cu, Ag, or mixtures thereof. Preferably, the acceptor dopant comprises a Group V element, more preferably nitrogen, for

example, using an acceptor dopant precursor comprises nitrogen in the form of NO, N₂O, NO₂, or ammonia.

Typically, an acceptor dopant has fewer valence electrons than the atom it replaces, whether a Group (V) element substituting for oxygen or a Group (IA) or
5 (IB) element substituting for zinc.

In preferred embodiments of the invention, the on-off ratio of the semiconductor without an acceptor dopant is less than 1.0×10^6 . Also, the presence of the acceptor dopant provides an increase in resistivity of at least 10^2 wherein the resistivity of the semiconductor without the acceptor dopant is less
10 than 500 ohm*cm. In preferred embodiments, the presence of an acceptor dopant also provides an increase in mobility of at least 25 percent, more preferably at least 50 percent.

Volatile compounds used in the present invention are defined as compounds that can exist to some extent in the vapor phase at room temperature,
15 so that they may be delivered to a reaction chamber in the form of a gas. In order for such a gas to contain sufficient volatile materials to usefully affect the deposition process, the volatile compound must have a vapor pressure at room temperature of greater than 0.1 mmHg, preferably greater than 1 mmHg. Dopants such as nitrogen, for example are preferably present in the final semiconductor in
20 the amount of 0.001% to 5%, more preferably 0.01% to 1%.

An acceptor dopant is typically an impurity that introduces an energy level within the band-gap of ZnO-based materials that is below the energy level of shallow donors and is able to accept an electron. Such an acceptor dopant can be an impurity atom that has fewer valence electrons than the atom it replaces.
25 Examples for ZnO-based materials are group (V) elements substituting for oxygen, e.g., nitrogen, phosphorous or arsenic or Group (I) and (IB) elements substituting for zinc, e.g. lithium, sodium, potassium, copper or silver. See Ü. Özgür, Ya. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Doan, V. Avrutin, S.-J. Cho, and H. Morkoç, J. Appl. Phys. **98** 041301 (2001).

30 In addition, minor amounts of still other conventional dopants, preferably less than 10 weight percent, can optionally also be included in the zinc-oxide-based semiconductor during or after deposition. The thickness of the channel

layer may vary, and according to particular examples it can range from 5 nm to 500 nm, 10 nm to 50 nm.

The length and width of the channel is determined by the pixel size and the design rules of the system under construction. Typically, the channel width may
5 vary from 10 to 1000 μm . The channel length may vary, and according to particular examples it can range from 1 to 100 μm .

The entire process of making the thin film transistor or electronic device of the present invention, or at least the production of the thin film semiconductor, can be carried out below a maximum support temperature of 300° C, more
10 preferably below 250° C, or even at temperatures around room temperature (25° C to 70°C). The temperature selection generally depends on the support and processing parameters known in the art, once one is armed with the knowledge of the present invention contained herein. These temperatures are well below traditional integrated circuit and semiconductor processing temperatures, which
15 enables the use of any of a variety of relatively inexpensive supports, such as flexible polymeric supports. Thus, the invention enables production of relatively inexpensive circuits containing thin film transistors with significantly improved performance.

For the description that follows, the term “gas” or “gaseous material” is
20 used in a broad sense to encompass any of a range of vaporized or gaseous elements, compounds, or materials. Other terms used herein, such as: reactant, precursor, vacuum, and inert gas, for example, all have their conventional meanings as would be well understood by those skilled in the materials deposition art. The figures provided are not drawn to scale but are intended to show overall
25 function and the structural arrangement of some embodiments of the present invention.

The process of the present invention offers a significant departure from conventional approaches to making a film of zinc-oxide-based n-type semiconductor, employing a system for delivery of gaseous materials to a
30 substrate surface that can be adaptable to deposition on larger and web-based substrates and capable of achieving a highly uniform thin-film deposition at improved throughput speeds. The process of the present invention employs a

continuous spatially dependent ALD (as opposed to pulsed or time dependent ALD) gaseous material distribution. The process of the present invention allows operation at atmospheric or near-atmospheric pressures and is capable of operating in an unsealed or open-air environment.

5 Figure 1 is a generalized step diagram of one embodiment of a process for making a film of zinc-oxide-based n-type semiconductor according to an embodiment of the present invention, in which two reactive gases are used, a first molecular precursor and a second molecular precursor. Gases are supplied from a gas source and can be delivered to the substrate, for example, via a deposition
10 device. Metering and valving apparatus for providing gaseous materials to the a deposition device can be used.

 As shown in Step 1, a continuous supply of gaseous materials for the system is provided for depositing a thin film of material on a substrate. The Steps in Sequence 15 are sequentially applied. In Step 2, with respect to a given area of
15 the substrate (referred to as the channel area), a first molecular precursor or reactive gaseous material is directed to flow in a first channel over the channel area of the substrate and reacts therewith. In Step 3 relative movement of the substrate and the multi-channel flows in the system occurs, which sets the stage for Step 4, in which second channel (purge) flow with inert gas occurs over the
20 given channel area. Then, in Step 5, relative movement of the substrate and the multi-channel flows sets the stage for Step 6, in which the given channel area is subjected to atomic layer deposition in which a second molecular precursor now (in this particular embodiment, transversely and substantially parallel to the surface of the substrate) over the given channel area of the substrate and reacts
25 with the previous layer on the substrate to produce (theoretically) a monolayer of a desired material. A first molecular precursor is a zinc-containing compound in gas form, and the material deposited is a zinc-containing compound, for example, an organozinc compound such as diethylzinc. In such an embodiment, the second molecular precursor can be, for example, a non-metallic oxidizing compound. A
30 volatile acceptor doping compound can be supplied to the system in any way in which allows it to react to sites in the growing film. Thus, it can be delivered with the first or second molecular precursors, or with the purge gas. Preferably

the volatile acceptor is delivered in common with the oxidizing molecular precursor.

In Step 7, relative movement of the substrate and the multi-channel flows then sets the stage for Step 8 in which again an inert gas is used, this time to sweep excess second molecular precursor from the given channel area from the previous Step 6. In Step 9, relative movement of the substrate and the multi-channels occurs again, which sets the stage for a repeat sequence, back to Step 2. The cycle is repeated as many times as is necessary to establish a desired film. In the present embodiment of the process, the steps are repeated with respect to a given channel area of the substrate, corresponding to the area covered by a flow channel. Meanwhile the various channels are being supplied with the necessary gaseous materials in Step 1. Simultaneous with the sequence of box 15 in Figure 1, other adjacent channel areas are being processed, which results in Multiple channel flows in parallel, as indicated in overall Step 11. Parallel flow can be either substantially orthogonal or substantially parallel to the output face of the deposition device.

The primary purpose of the second molecular precursor is to condition the substrate surface back toward reactivity with the first molecular precursor. The second molecular precursor also provides material from the molecular gas to combine with metal at the surface, forming an oxide with the freshly deposited zinc-containing precursor.

This particular embodiment does not need to use a vacuum purge to remove a molecular precursor after applying it to the substrate. Purge steps are expected by most researchers to be the most significant throughput-limiting step in ALD processes.

Assuming that, for the two reactant gases in Figure 1, AX and BY are used, for example. When the reaction gas AX flow is supplied and flowed over a given substrate area, atoms of the reaction gas AX are chemically adsorbed on a substrate, resulting in a layer of A and a surface of ligand X (associative chemisorptions) (Step 2). Then, the remaining reaction gas AX is purged with an inert gas (Step 4). Then, the flow of reaction gas BY, and a chemical reaction between AX (surface) and BY (gas) occurs, resulting in a molecular layer of AB

on the substrate (dissociative chemisorptions) (Step 6). The remaining gas BY and by-products of the reaction are purged (Step 8). The thickness of the thin film can be increased by repeating the process cycle (steps 2-9) many times.

Because the film can be deposited one monolayer at a time it tends to be
5 conformal and have uniform thickness.

Oxides that can be made using the process of the present invention include, but are not limited to: ZnO, indium oxide, tin oxide. Mixed structure oxides that can be made using the process of the present invention can include, for example, InZnO. Doped materials that can be made using the process of the
10 present invention can include, for example, ZnO:Al, $Mg_xZn_{1-x}O$, and LiZnO doped with indium.

It will be apparent to the skilled artisan that alloys of two, three, or more metals may be deposited, compounds may be deposited with two, three, or more constituents, and such things as graded films and nano-laminates may be produced
15 as well.

These variations are simply variants using particular embodiments of the invention in alternating cycles. There are many other variations within the spirit and scope of the invention, so the invention is limited only by the claims that follow.

For various volatile zinc-containing precursors, precursor combinations, and reactants useful in ALD thin film processes, reference is made to the Handbook of Thin Film Process Technology, Vol. 1, edited by Glocker and Shah, Institute of Physics (IOP) Publishing, Philadelphia 1995, pages B1.5:1 to B1.5:16, cited herein; and Handbook of Thin Film Materials, edited by Nalwa, Vol.1, pages
20 103 to 159, cited herein, including Table V1.5.1 of the former reference.

Although oxide substrates provide groups for ALD deposition, plastic substrates can be used by suitable surface treatment.

Referring now to Figure 2, there is shown a cross-sectional side view of one embodiment of a deposition device 10 that can be used in the present process
30 for atomic layer deposition of a zinc-oxide-based semiconductor onto a substrate 20 according to the present invention. Deposition device 10 has a gas inlet port 14 for accepting a first gaseous material, a gas inlet port 16 for accepting a second

gaseous material, and a gas inlet port 18 for accepting a third gaseous material. These gases are emitted at an output face 36 via output channels 12, having a structural arrangement described subsequently. The arrows in Figure 2 and subsequent Figures 3-4B refer to the diffusive transport of the gaseous material, and not the flow, received from an output channel. In this particular embodiment, the flow is substantially directed out of the page of the figure, as described further below.

In one embodiment, gas inlet ports 14 and 16 are adapted to accept first and second gases that react sequentially on the substrate surface to effect ALD deposition, and gas inlet port 18 receives a purge gas that is inert with respect to the first and second gases. Deposition device 10 is spaced a distance D from substrate 20, provided on a substrate support, as described in more detail subsequently. Reciprocating motion can be provided between substrate 20 and deposition device 10, either by movement of substrate 20, by movement of deposition device 10, or by movement of both substrate 20 and deposition device 10. In the particular embodiment shown in Figure 2, substrate 20 is moved across output face 36 in reciprocating fashion, as indicated by the arrow R and by phantom outlines to the right and left of substrate 20 in Figure 2. It should be noted that reciprocating motion is not always required for thin-film deposition using deposition device 10. Other types of relative motion between substrate 20 and deposition device 10 could also be provided, such as movement of either substrate 20 or deposition device 10 in one or more directions, as described in more detail subsequently.

The cross-sectional view of Figure 3 shows gas flows emitted over a portion of output face 36 of deposition device 10. In this particular arrangement, each output channel 12, separated by partitions 22, is in gaseous flow communication with one of gas inlet ports 14, 16 or 18 seen in Figure 2. Each output channel 12 delivers typically a first reactant gaseous material O, or a second reactant gaseous material M, or a third inert gaseous material I.

Figure 3 shows a relatively basic or simple arrangement of gases. It is envisioned that a plurality of non-metal deposition precursors (like material O) or a plurality of metal-containing precursor materials, including at least a zinc-

containing precursor (like material M) may be delivered sequentially at various ports in a thin-film single deposition. Alternately, a mixture of reactant gases, for example, a mixture of metal precursor materials or a mixture of metal and non-metal precursors may be applied at a single output channel when making complex thin film materials, for example, having alternate layers of metals or having lesser amounts of dopants admixed in a metal oxide material. The inter-stream labeled I separates any reactant channels in which the gases are likely to react with each other. First and second reactant gaseous materials O and M react with each other to effect ALD deposition, but neither reactant gaseous material O nor M reacts with inert gaseous material I. The nomenclature used in Figure 3 and following suggests some typical types of reactant gases. For example, first reactant gaseous material O could be an oxidizing gaseous material; second reactant gaseous material M could be a metallic zinc-containing compound. Inert gaseous material I could be nitrogen, argon, helium, or other gases commonly used as purge gases in ALD processes. Inert gaseous material I is inert with respect to first or second reactant gaseous materials O and M. Reaction between first and second reactant gaseous materials could form a metal oxide or other binary compound, such as zinc oxide ZnO, in one embodiment. Reactions between more than two reactant gaseous materials could form other zinc-oxide-based materials such as a ternary compound, for example, ZnAlO.

The cross-sectional views of Figures 4A and 4B show, in simplified schematic form, the ALD coating operation performed as substrate 20 passes along output face 36 of deposition device 10 when delivering reactant gaseous materials O and M. In Figure 4A, the surface of substrate 20 first receives an oxidizing material from output channels 12 designated as delivering first reactant gaseous material O. The surface of the substrate now contains a partially reacted form of material O, which is susceptible to reaction with material M. Then, as substrate 20 passes into the path of the metal compound of second reactant gaseous material M, the reaction with M takes place, forming a metallic oxide or some other thin film material that can be formed from two reactant gaseous materials.

As Figures 4A and 4B show, inert gaseous material I is provided in every alternate output channel 12, between the flows of first and second reactant gaseous materials O and M. Sequential output channels 12 are adjacent, that is, share a common boundary, formed by partitions 22 in the embodiments shown.

5 Here, output channels 12 are defined and separated from each other by partitions 22 that extend at a perpendicular to the surface of substrate 20.

As mentioned above, in this particular embodiment, there are no vacuum channels interspersed between the output channels 12, that is, no vacuum channels on either side of a channel delivering gaseous materials to draw the gaseous materials around the partitions. This advantageous, compact arrangement is possible because of the innovative gas flow that is used. Unlike gas delivery arrays of earlier processes that apply substantially vertical (that is, perpendicular) gas flows against the substrate and must then draw off spent gases in the opposite vertical direction, deposition device 10 directs a gas flow (preferably substantially laminar in one embodiment) along the surface for each reactant and inert gas and handles spent gases and reaction by-products in a different manner, as described subsequently. The gas flow used in the present invention is directed along and generally parallel to the plane of the substrate surface. In other words, the flow of gases is substantially transverse to the plane of a substrate rather than perpendicular to the substrate being treated.

Figures 5 and 6 show perspective views of one embodiment of a deposition device 10 that can be used in the present process, from the output face 36 (that is, from the underside with respect to Figures 2 - 4B). Partitions 22 that define and separate the adjacent output channels 12 in this embodiment are represented as partially cut away, to allow better visibility for the gas flows flowing from gas outlet ports 24. Figures 5 and 6 also show reference x, y, z coordinate axis assignments used in the figures of this disclosure. Output channels 12 are substantially in parallel and extend in a length direction that corresponds to the x coordinate axis. Reciprocating motion of substrate 20, or motion relative to substrate 20, is in the y coordinate direction, using this coordinate assignment.

Figure 6 shows the gas flows F_I , F_O , and F_M for the various gaseous materials delivered from deposition device 10 with this embodiment. Gas flows F_I , F_O , and F_M are in the x -direction, that is, along the length of elongated output channels 12.

5 The cross-sectional views of Figures 7A, 7B, 7C, and 7D are taken orthogonally to the cross-sections of Figures 2 - 4B and show gas flows in one direction from this view. Within each output channel 12, the corresponding gaseous material flows from a gas output port 24, shown in phantom in the views of Figures 7A, 7B, 7C, and 7D. In the embodiment of Figure 7A, gas flow F_1
10 directs the gaseous material along the length of output channel 12 and across substrate 20, as was described with reference to Figures 5 and 6. Flow F_1 continues past the edge of deposition device 10 in this arrangement, flowing outward into the environment or, if desirable, to a gas collection manifold (not shown). Figure 7B shows an alternative embodiment for gas flow F_2 in which
15 output channel 12 also provides an exhaust port 26 for redirection or drawing off of the gas flow. Figure 7C shows an alternative embodiment for gas flow F_3 , in which gas output port 24 is centrally located within output channel 12 and directs gaseous material in gas flows along the channel in both directions. Figure 7D
20 shows an alternate embodiment for gas flow F_4 , in which gas output port 24 is also centrally positioned, with multiple exhaust ports 26 suitably placed near the extreme ends of output channel 12. Although unidirectional flows are preferred, some degree of mixing can occur and even may be beneficial to some extent, depending on the flow rates and other circumstances involved in a particular application.

25 A particular deposition device 10 may use output channels 12 configured using any one of the gas flow configurations or combinations thereof, either the F_1 flow of Figure 7A, the F_2 flow of Figure 7B, the F_3 flow of Figure 7C, the F_4 flow of Figure 7D, or some other variation in which gaseous material is directed to flow across substrate 20 along output channel 12, preferably in a substantially
30 laminar or smooth fashion with controlled mixing. In one embodiment, one or more exhaust ports 26 are provided for each output channel 12 that delivers a reactant gaseous material. For example, referring to Figure 6, output channels 12

for first and second reactant gaseous materials, labeled O and M, are configured with exhaust ports 26 to vent or draw off the reactant substances, following the pattern of flow F2 (Figure 7B). This allows some recycling of materials and prevents undesirable mixing and reaction near the end of the manifold. Output channels 12 for inert gaseous material, labeled I, do not use exhaust ports 26 and thus follow the pattern of flow F1 (Figure 7A). Although laminar flows are preferred in some embodiments, some degree of mixing can occur and even may be beneficial to some extent, depending on the flow rates and other circumstances involved in a particular application.

Exhaust port 26 is not a vacuum port, in the conventional sense, but is simply provided to draw off the gaseous flow in its corresponding output channel 12, thus facilitating a uniform gas flow pattern within the channel. A negative draw, just slightly less than the opposite of the gas pressure at gas output port 24, can help to facilitate an orderly gas flow. The negative draw can, for example, operate at a pressure of between 0.9 and 1.0 atmosphere, whereas a typical vacuum is, for example, below 0.1 atmosphere. An optional baffle 58, as shown in dotted outline in Figures 7B and 7D may be provided to redirect the flow pattern into exhaust port 26.

Because no gas flow around partition 22 to a vacuum exhaust is needed, output face 36 can be positioned very closely, to within 1 mil (approximately 0.025 mm) of the substrate surface. By comparison, an earlier approach such as that described in the US Patent No. 6,821,563 to Yudovsky, cited earlier, required gas flow around the edges of channel sidewalls and was thus limited to 0.5 mm or greater distance to the substrate surface. Positioning the deposition device 10 closer to the substrate surface is preferred in the present invention. In a preferred embodiment, distance D from the surface of the substrate can be 0.4 mm or less, preferably within 0.3 mm, more preferably within 0.25 mm of the output face of the deposition device or the bottom of the guide walls that provide the flow channels.

The cross-sectional views of Figures 8A and 8B show why it is desirable to have the distance D relatively small, consistent with the operation of the invention. In these figures, deposition device 10 is moving over substrate 20 from

left to right, as the arrow indicates. As output channel 12 carrying a reactive gaseous material M moves to the right over an area, it encounters a diffusion layer 72 from the next adjacent (previous-in-time) output channel that is primarily inert gaseous material I. In order to react on the surface of substrate 20, reactive

5 gaseous material M must diffuse through diffusion layer 72, which has a thickness proportional to distance D. By comparison, Figure 8B shows what happens when distance D is reduced: diffusion layer 72 is reduced proportionately. Diffusion through diffusion layer 72 happens more quickly and more efficiently, allowing less waste and reducing the overall amount of time needed for reaction on the

10 surface of substrate 20. The lower partition walls 22 also prevent less gas to remain from the previous-in time output channel gas. It should be noted that the flow of the gases in the channels are perpendicular to the page of the Figures 8A and 8B, as shown by the back of the arrow, which flow maintains a concentration gradient that aids the diffusion through the thin diffusion layer 72 to the surface of

15 the substrate 20. The surface is exposed to the gas flow of M for sufficient time for diffusion and any mixing to replace the previous-in-time output channel gas. In this particular embodiment, the flow of gas is across the surface rather than directly into the surface so that it limits the undesirable mixing of reactant gases between outlet channels, which might otherwise be exacerbated by relative

20 oscillation of the manifold and/or substrate.

In order to provide smooth flow along the length of output channel 12, gas output port 24 may be inclined at an angle away from normal, as indicated in Figures 7A and 7B. Optionally, some type of gas flow redirecting structure may also be employed to redirect a downward flow from gas output port 24 so that it

25 forms a gas flow that runs substantially in parallel to output face 36.

The plan view of Figure 9 shows output face 36 of a portion of a deposition device 10 that can be used in one embodiment. For optimizing directional gas flow in this particular embodiment, redirecting plates 38 may be positioned in each of the output channels 12 for directing reactant gaseous

30 materials. In the embodiment shown, only output channels 12 that deliver reactant gaseous materials are provided with redirecting plates 38 and exhaust ports 26. This particular arrangement may be advantageous in some applications, where it is

advantageous to surround deposition device 10 with inert gas, such as to reduce unwanted intake of ambient gases. However, redirecting plates 38 could be used on all output channels 12. Also, exhaust ports 26 could be used on some or all output channels 12. In another possible embodiment, redirecting plates can be
5 used on all channels, but the outlet edge of the redirecting plate may be at a different x-axis position depending upon which channel is considered. In particular, it may be desirable to have the outlet edge position of the baffles 58 (as shown in Figures 7B and 7D) for the inert flows to be at lower x-axis positions than those of the reactant gases so that the inert purge flows can serve as
10 mentioned above to isolate the various channels.

Figure 9 also shows the pattern of output channels in one embodiment. Here, it has been found to be particularly advantageous to provide inert gas channels I as the outermost channels of deposition device 10. Oxidation channels with first reactant gaseous material O are next to the outermost channels, since
15 these condition the surface for ALD reaction with the metallic component of second reactant gaseous material M.

Figure 10 shows one embodiment of a deposition device 10 that can be used in the present process in which the channels of width W, length L, and height H are formed from stacked metal plates 42 and 44 having apertures 40 forming
20 ducts 46a,b,c. Figure 11A shows an exploded view of a single output channel 12 section of deposition device 10 formed in this way, showing an arrangement of apertures 40 in alternating partition plates 42 and delivery plates 44. Figure 11B shows a similar exploded view for an adjacent output channel 12. Ducts 46a, 46b, and 46c, formed by alignment of apertures 40, extend through deposition device
25 10 and provide input conduits for gaseous flow communication, accepting the different reactant and inert gaseous materials from external sources and providing the redirecting structures that provide gas flows along output face 36 described earlier. Baffles and other redirecting structures are not shown in these figures, but could be provided using stacked plates suitably structured, or applied after the
30 device is assembled.

The exploded views of Figures 11A and 11B each show a single output channel 12 formed from stacked plates 42 and 44. In the example of Figure 11A,

output channel 12 provides gaseous material provided from duct 46b. Ducts 46a and 46c conduct other gases past this channel in the embodiment shown in Figure 11A. Delivery plate 44, dimensioned and apertured differently than the partition plates 42 that bound output channel 12, contains a redirecting chamber 48 that
5 redirects a portion of the gas in duct 46b into gas flow F1. In the example of Figure 11B, output channel 12 provides gaseous material provided from duct 46a. Ducts 46b and 46c conduct other gases past this channel in the embodiment shown in Figure 11B. Plates 42 and 44 should be of a suitable metal for conducting the reactive gaseous materials, such as stainless steel or other metal for
10 example.

It is desirable that when a large number of plates are assembled for such an embodiment, the gas flow delivered to the substrate is uniform across all of the channels delivering a particle flow (I, M, or O). This can be accomplished by proper design of the plates, such as having restrictions in some part of the flow
15 pattern for each plate which are accurately machined to provide a reproducible pressure drop for each channel.

Although the method of stacking plates is a particularly useful way of constructing a deposition device for use in this invention, there are a number of other methods to build such structures and may be useful in alternate
20 embodiments of deposition devices that can be used in the present process. For example, the deposition device for use in the present process may be constructed by direct machining of a metal block, or of several metal blocks adhered together. Furthermore, molding techniques involving internal mold features can be employed, as will be understood by the skilled artisan. A deposition device can
25 also be constructed using any of a number stereolithography techniques.

As can be seen from the example embodiment of Figures 10, 11A, and 11B, deposition device 10 can be constructed of very small size, with each output channel 12 having the width of a sheet of metal plating. For example, in one embodiment using the arrangement of Figures 10, 11A, and 11B, output channel
30 12 is 0.034 inches (0.86 mm) in width W. Output channels 12 for different materials could be fabricated at different thicknesses to obtain width W ranges, preferably from 0.01 inches (0.25 mm) to 0.1 inches (2.5 mm) for a compact

arrangement. The length L of output channel 12 can vary, depending on the needed uniformity and desired gas pressure. In one embodiment, output channel length L is 3 inches (75 mm). The height H of output channels 12 formed from extending portions of stacked plates 42 is 0.1 inches in one embodiment.

5 Because gas flow can inadvertently draw ambient gases, due to low-pressure zones that are created, it may be useful to provide additional protection barrier from an inert layer. Referring to Figure 12, there is shown an envelopment gas flow F_E by which an additional flow of inert gas is used on one or more sides of deposition device 10 to prevent ambient gases from contaminating the process
10 gases.

 As was particularly described with reference to Figures 4A and 4B, deposition device 10 requires movement relative to the surface of substrate 20 in order to perform its deposition function. This relative movement can be obtained in a number of ways, including movement of either or both deposition device 10
15 and substrate 20, such as by movement of a process that provides a substrate support. Movement can be oscillating or reciprocating or could be continuous movement, depending on how many deposition cycles are needed. Rotation of a substrate can also be used, particularly in a batch process, although continuous processes are preferred.

20 Typically, ALD requires multiple deposition cycles, building up a controlled film depth with each cycle. Using the nomenclature for types of gaseous materials given earlier, a single cycle can, for example in a simple design, provide one application of first reactant gaseous material O and one application of second reactant gaseous material M.

25 The distance between output channels for O and M reactant gaseous materials determines the needed distance for reciprocating movement to complete each cycle. For the example deposition device 10 of Figure 9, having a nominal channel width of 0.034 inches in width W for each output channel 12, reciprocating motion (along the y axis as used herein) of at least 0.20 inches
30 would be required. For this example, an area of substrate 20 would be exposed to both first reactant gaseous material O and second reactant gaseous material M with movement over this distance. In some cases, consideration for uniformity

may require a measure of randomness to the amount of reciprocating motion in each cycle, such as to reduce edge effects or build-up along the extremes of reciprocation travel.

5 A deposition device 10 may have only enough output channels 12 to provide a single cycle. Alternately, deposition device 10 may have an arrangement of multiple cycles, enabling it to cover a larger deposition area or enabling its reciprocating motion over a distance that allows two or more deposition cycles in one traversal of the reciprocating motion distance.

10 In one embodiment, a given area of the substrate is exposed to a gas flow in a channel for less than 500 milliseconds, preferably less than 100 milliseconds. The relative movement of the substrate to a channel during oscillation is at a speed of at least 0.1 cm/sec, and the gas flow in the channels is at least 1 cm/sec. Preferably, the temperature of the substrate during deposition is under 300°C, more preferably under 250°C.

15 For example, in one particular application, it was found that each O-M cycle formed a layer of one atomic diameter over $\frac{1}{4}$ of the treated surface. Thus, four cycles, in this case, are needed to form a uniform layer of 1 atomic diameter over the treated surface. Similarly, to form a uniform layer of 10 atomic diameters in this case, then, 40 cycles would be required.

20 An advantage of the reciprocating motion used for a deposition device 10 used in one embodiment of the present process is that it allows deposition onto a substrate 20 whose area exceeds the area of output face 36. Figure 13 shows schematically how this broader area coverage can be effected, using reciprocating motion along the y axis as shown by arrow R and also movement orthogonal or
25 transverse to the reciprocating motion, relative to the x axis. Again, it must be emphasized that motion in either the x or y direction, as shown in Figure 13, can be effected either by movement of deposition device 10, or by movement of substrate 20 provided with a substrate support 74 that provides movement, or by movement of both deposition device 10 and substrate 20.

30 In Figure 13 the relative motion of the deposition head and the substrate are perpendicular to each other. It is also possible to have this relative motion in parallel. In this case, the relative motion needs to have a nonzero frequency

component that represents the oscillation and a zero frequency component that represents the displacement of the substrate. This combination can be achieved by: an oscillation combined with displacement of the deposition device over a fixed substrate; an oscillation combined with displacement of the substrate relative to a fixed substrate deposition device; or any combinations wherein the oscillation and fixed motion are provided by movements of both substrates.

As indicated above, the present ALD process can be performed at or near atmospheric pressure and over a broad range of ambient and substrate temperatures, preferably at a temperature of under 300°C. Preferably, a relatively clean environment is needed to minimize the likelihood of contamination; however, full “clean room” conditions or an inert gas-filled enclosure would not be required for obtaining good performance when using preferred embodiments of the process of the present invention.

Figure 14 shows an Atomic Layer Deposition (ALD) process, for making a zinc-oxide-based semiconductor, having a chamber 50 for providing a relatively well-controlled and contaminant-free environment. Gas supplies 28a, 28b, and 28c provide the first, second, and third gaseous materials to deposition device 10 through supply lines 32. The optional use of flexible supply lines 32 facilitates ease of movement of deposition device 10. For simplicity, an optional vacuum vapor recovery process and other support components are not shown in Figure 13 but could also be used. A transport subsystem 54 provides a substrate support that conveys substrate 20 along output face 36 of deposition device 10, providing movement in the x direction, using the coordinate axis system employed in the present disclosure. Motion control, as well as overall control of valves and other supporting components, can be provided by a control logic processor 56, such as a computer or dedicated microprocessor assembly, for example. In the arrangement of Figure 14, control logic processor 56 controls an actuator 30 for providing reciprocating motion to deposition device 10 and also controls a transport motor 52 of transport subsystem 54.

Figure 15 shows an alternate embodiment of an Atomic Layer Deposition (ALD) process 70 for thin film deposition of zinc-oxide-based semiconductor onto a web substrate 66 that is conveyed past deposition device 10 along a web

conveyor 62 that acts as a substrate support. A deposition device transport 64 conveys deposition device 10 across the surface of web substrate 66 in a direction transverse to the web travel direction. In one embodiment, deposition device transport 64 uses a lead screw that traverses the width of web substrate 66. In
5 another embodiment, multiple deposition devices 10 are used, at suitable positions along web 62.

Figure 16 shows another Atomic Layer Deposition (ALD) system 70 for depositing a zinc-oxide-based semiconductor in a web arrangement, using a stationary deposition device 10 in which the flow patterns are oriented
10 orthogonally to the configuration of Figure 14. In this arrangement, motion of web conveyor 62 itself provides the movement needed for ALD deposition. Reciprocating motion could also be used in this environment, such as by repeatedly reversing the direction of rotation of a web roller to move substrate 66 forward and backwards relative to deposition device 10. Reciprocation motion
15 can also be obtained by allowing a reciprocating motion of the deposition device across an arc whose axis coincides with the roller axis, while the web is moved in a constant motion. Referring to Figure 17, an embodiment of a portion of deposition device 10 is shown in which output face 36 has an amount of curvature, which might be advantageous for some web coating applications.
20 Convex or concave curvature could be provided.

Optionally, the present process can be accomplished with other apparatus or systems described in more detail in commonly assigned US Application No. 11/392,007, US Application No. 11/392,006, US Application No. 11/620,744, and US Application No. 11/620,740.

25 In the embodiments in the latter three applications, a delivery device having an output face for providing gaseous materials for thin-film material deposition onto a substrate comprises elongated emissive channels in at least one group of elongated emissive channels, of the three groups of elongated emissive channels (namely, at least one group of: (i) one or more first elongated emissive
30 channels, (ii) one or more second elongated channels, and (iii) a plurality of third elongated channels) that is capable of directing a flow, respectively, of at least one of the first gaseous material, second gaseous material, and the third gaseous

material substantially orthogonally with respect to the output face of the delivery device, which flow of gaseous material is capable of being provided, either directly or indirectly from each of the elongated emissive channels in the at least one group, substantially orthogonally to the surface of the substrate.

5 In one embodiment, apertured plates are disposed substantially in parallel to the output face, and apertures on at least one of the apertured plates form the first, second, and third elongated emissive channels. In an alternative embodiment, the apertured plates are substantially perpendicularly disposed with respect to the output face.

10 In one such embodiment, the deposition device comprises exhaust channels, for example, a delivery device for thin-film material deposition of a zinc-oxide-based semiconductor onto a substrate comprising: (a) a plurality of inlet ports comprising at least a first inlet port, a second inlet port, and a third inlet port capable of receiving a common supply for a first reactive gaseous material, a
15 second reactive gaseous material, and a third (inert purge) gaseous material, respectively; (b) at least one exhaust port capable of receiving exhaust gas from thin-film material deposition and at least two elongated exhaust channels, each of the elongated exhaust channels capable of gaseous fluid communication with the at least one exhaust port; and (c) at least three pluralities of elongated output
20 channels, (i) a first plurality of first elongated output channels, (ii) a second plurality of second elongated output channels, and (iii) a third plurality of third elongated output channels,, each of the first, second, and third elongated output channels capable of gaseous fluid communication, respectively, with one of the corresponding first inlet port, second inlet port, and third inlet port; wherein each
25 of the first, second, and third elongated output channels and each of the elongated exhaust channels extend in a length direction substantially in parallel; wherein each first elongated output channel is separated on at least one elongated side thereof from a nearest second elongated output channel by a relatively nearer elongated exhaust channel and a relatively less near third elongated output
30 channel; and wherein each first elongated emissive channel and each second elongated emissive channel is situated between relatively nearer elongated exhaust channels and between relatively less nearer elongated emissive channels.

The delivery head has elongated output openings in the output face of the delivery head for providing the gaseous materials to the substrate. In some cases, each elongated output opening can be connected to a corresponding elongated output/emissive channel and optionally, in some embodiments, can form the opening thereof in the output face.

Further embodiments can comprise a gas diffuser associated with at least one group of the three groups of elongated emissive channels such that at least one of the first, second, and third gaseous material, respectively, is capable of passing through the gas diffuser prior to delivery from the delivery device to the substrate, during thin-film material deposition onto the substrate, and wherein the gas diffuser maintains flow isolation of the at least one of first, second, and third gaseous material downstream from each of the elongated emissive channels in the at least one group of elongated emissive channels.

In one embodiment such a gas diffuser is capable of providing a friction factor for gaseous material passing there through that is greater than 1×10^2 , thereby providing back pressure and promoting equalization of pressure where the flow of the at least one first, second and third gaseous material exits the delivery device. In one embodiment of the invention, the gas diffuser comprises a porous material through which the at least one of the first, second, and third gaseous material passes. In a second embodiment of the invention, the gas diffuser comprises a mechanically formed assembly comprising at least two elements comprising interconnected passages, for example, in which nozzles are connected to a flow path provided by a thin space between parallel surface areas in the two elements.

In one embodiment, the one or more of the gas flows from the deposition devices provides a pressure that at least contributes to the separation of the surface of the substrate from the face of the delivery head, thereby providing a "floating head" or "air bearing" type deposition head, which can help to stabilize the gas flows and limit intermixing of the gas flows.

The process of the present invention is advantaged in its capability to perform deposition onto a substrate over a broad range of temperatures, including room or near-room temperature in some embodiments. The process of the present

invention can operate in a vacuum environment, but is particularly well suited for operation at or near atmospheric pressure.

The production of thin film transistors and electronic devices from the ALD deposited semiconductor materials can be accomplished by conventional techniques known to the skilled artisan. In one embodiment, a substrate is provided, a film or layer of the semiconductor material as described above can be applied to the substrate, and electrical contacts made to the layer. The exact process sequence is determined by the structure of the desired semiconductor component. Thus, in the production of a field effect transistor, for example, a gate electrode can be first deposited on a substrate, for example a vacuum or solution deposited metal or organic conductor. The gate electrode can then be insulated with a dielectric and then source and drain electrodes and a layer of the n-channel semiconductor material can be applied on top. The structure of such a transistor and hence the sequence of its production can be varied in the customary manner known to a person skilled in the art. Thus, alternatively, a gate electrode can be deposited first, followed by a gate dielectric, then the semiconductor can be applied, and finally the contacts for the source electrode and drain electrode deposited on the semiconductor layer. A third structure could have the source and drain electrodes deposited first, then the semiconductor, with dielectric and gate electrode deposited on top.

The skilled artisan will recognize other structures can be constructed and/or intermediate surface modifying layers can be interposed between the above-described components of the thin film transistor. In most embodiments, a field effect transistor comprises an insulating layer, a gate electrode, a semiconductor layer comprising a ZnO material as described herein, a source electrode, and a drain electrode, wherein the insulating layer, the gate electrode, the semiconductor layer, the source electrode, and the drain electrode are in any sequence as long as the gate electrode and the semiconductor layer contact opposite sides of the insulating layer, and the source electrode and the drain electrode both contact the semiconductor layer.

As previously mentioned, Song et al. reported on amorphous indium zinc oxide TFTs formed at room temperature, although the TFTs were prepared by rf

magnetron sputtering (Song, et al. Applied Physics Letters 90, 022106 (2007)).

Song et al. reported on the preparation of conductive gate and source/drain electrodes made using this sputtered indium zinc oxide. In order to achieve the higher conductivity necessary for the electrodes, it was necessary to control the partial pressure of oxygen in the sputtering chamber to within a narrow range of concentration. Techniques for fabricating these structures include selective deposition, sequential masking, photolithography, laser, and/or other means known to the skilled artisan.

A thin film transistor (TFT) is an active device, which is the building block for electronic circuits that switch and amplify electronic signals. Attractive TFT device characteristics include a high ratio of the on current to the off current, and a steep subthreshold slope. In the operation of such a TFT device, a voltage applied between the source and drain electrodes establishes a substantial current flow only when the control gate electrode is energized. That is, the flow of current between the source and drain electrodes is modulated or controlled by the bias voltage applied to the gate electrode. The relationship between material and device parameters of the zinc-oxide-based semiconductor TFT can be expressed by the approximate equation (see Sze in *Semiconductor Devices—Physics and Technology*, John Wiley & Sons (1981)):

$$I_d = \frac{W}{2L} \mu C_{ox} (V_g - V_{th})^2$$

where I_d is the saturation source-drain current, C is the geometric gate capacitance, associated with the insulating layer, W and L are physical device dimensions, μ is the carrier (hole or electron) mobility in the zinc-oxide-based semiconductor, and V_g is the applied gate voltage, and V_{th} is the threshold voltage. Ideally, the TFT allows passage of current only when a gate voltage of appropriate polarity is applied. However, with zero gate voltage, the "off" current between source and drain will depend on the intrinsic conductivity σ of the zinc-oxide-based semiconductor,

$$\sigma = nq\mu$$

where n is the charge carrier density and q is the charge, so that

$$(I_{sd}) = \sigma(Wt/L) V_{sd} @ V_g=0$$

- 5 wherein t is the zinc-oxide-based semiconductor layer thickness and V_{sd} is the voltage applied between source and drain. Therefore, for the TFT to operate as a good electronic switch, e.g. in a display, with a high on/off current ratio, the semiconductor needs to have high carrier mobility but very small intrinsic conductivity, or equivalently, a low charge carrier density. On/off ratios $>10^4$ are
10 desirable for practical devices.

The TFT structure described herein includes a transparent zinc-oxide-based semiconductor with conducting electrodes, commonly referred to as a source and a drain, for injecting a current into the zinc-oxide-based semiconductor and a capacitance charge injection scheme for controlling and/or modulating the
15 source-drain current. One particularly attractive application of zinc-oxide-based semiconductor TFT's is in the drive circuits for displays on flexible, polymer substrates. Zinc oxide semiconductor transistors and/or transistor arrays are useful in applications including, but not limited to, flat panel displays such as active matrix imagers, sensors, rf price labels, electronic paper systems, rf
20 identification tags and rf inventory tags. The inclusion of indium doping in these transistors can be effective for both improving the robustness of the semiconductor layer when used as the channel material and the conductivity of the electrodes when used as a conducting electrode.

The present invention is preferably used for making an "enhancement-mode transistor" which means a transistor in which there is negligible off-current flow, relative to on-current flow, between a source and a drain at zero gate voltage. In other words, the transistor device is "normally off." (In contrast, a depletion-mode transistor is "normally on" meaning that more than a substantially negligible current flows between a source and a drain at zero gate voltage.
25 Enhancement-mode devices are typically preferred.)

Turning now to Figures 20 to 25, with reference to these particular Figures, the terms "over," "above," "under," and the like, with respect to layers in

the thin film transistor, refer to the order of the layers, wherein the thin film semiconductor layer is above the gate electrode, but do not necessarily indicate that the layers are immediately adjacent or that there are no intermediate layers. Also the descriptors "top" and "bottom" refer to the disposition of the contact with respect to the semiconductor, with bottom representing closer to the substrate and top representing further from the substrate. "Vertical" means substantially perpendicular to the surface of a substrate.

Described in the embodiments of Figures 20 to 25 are enhancement-mode, field effect transistors wherein at least a portion of the transistor structure may be substantially transparent. Accordingly, an optional characteristic of a transistor structure made using the present invention is that selected embodiments of the construct, or a subset thereof that include the semiconductor channel layer and the gate insulator layer, may exhibit an optical transmission of at least 90%, more particularly at least 95%, across the visible portion (and/or infrared portion in certain variants) of the electromagnetic spectrum. Each of the additional components of the structure (i.e., substrate, gate electrode, source/drain terminals) may be optionally opaque or substantially transparent depending upon the desired end use of the transistor. In certain embodiments, the transistor structure as a whole (and/or individual components of the transistor) may exhibit an optical transmission of at least 50%, more particularly at least 70%, and most particularly at least 90%, across the visible portion (and/or infrared portion in certain variants) of the electromagnetic spectrum. Because of the optional transparency, transistors made according to the present invention may be advantageously included in optoelectronic display devices as switches coupled to at least one display element, as described in greater detail below.

Cross-sectional views of typical deposited thin film transistors are shown in Figures 20 - 25. For example, Figure 20 illustrates a typical bottom contact configuration, and Figure 21 illustrates a typical top contact configuration.

Each thin film transistor (TFT) in the embodiments of Figures 20 and 21 contains a source electrode 120, a drain electrode 130, a gate electrode 144, a gate dielectric 156, a substrate 128, and the semiconductor 170 of the invention in the form of a film connecting the source electrode 120 to drain electrode 130. When

the TFT operates in an enhancement-mode, the charges injected from the source electrode into the semiconductor are mobile and a current flows from source to drain, mainly in a thin channel region within 100 Angstroms of the semiconductor-dielectric interface. See A. Dodabalapur, L. Torsi H. E. Katz,
5 *Science* 1995, 268, 270. In the configuration of Figure 20, the charge need only be injected laterally from the source electrode 120 to form the channel. In the absence of a gate field the channel ideally has few charge carriers; as a result there is ideally no source-drain conduction when the device is in off mode.

The off current is defined as the current flowing between the source
10 electrode 120 and the drain electrode 130 when charge has not been intentionally injected into the channel by the application of a gate voltage. This occurs for a gate-source voltage more negative, assuming an n-channel, than a certain voltage known as the threshold voltage. See Sze in *Semiconductor Devices--Physics and Technology*, John Wiley & Sons (1981), pages 438-443. The on current is defined
15 as the current flowing between the source electrode 120 and the drain electrode 130 when charge carriers have been accumulated intentionally in the channel by application of an appropriate voltage to the gate electrode 144, and the channel is conducting. For an n-channel accumulation-mode TFT, this occurs at gate-source voltage more positive than the threshold voltage. It is desirable for this threshold
20 voltage to be zero, or slightly positive, for n-channel operation. Switching between on and off is accomplished by the application and removal of an electric field from the gate electrode 144 across the gate dielectric 156 to the semiconductor-dielectric interface, effectively charging a capacitor.

The specific examples of transistor configurations described herein are for
25 illustrative purposes and should not be considered as limiting the scope of the appended claims. For example, a further (third) specific transistor structure is shown in Figure 22, in which a third variation of a TFT structure includes an insulating substrate 128 upon which is disposed a source electrode 120 and a drain electrode 130. A semiconductor film 170 is provided such that contact between
30 the source and drain electrodes is made. A gate electrode 144 is disposed on the top surface (from a vertical perspective) of the gate dielectric 156. In other words,

the gate electrode 144 and the semiconductor film 170 are provided on opposing surfaces of the gate dielectric 156.

The TFT structure of Figure 22 may be fabricated, for example, by depositing and patterning a film that defines the source electrode 120 and the drain electrode 130. For instance, a 500 Angstrom ITO source/drain electrode film may be sputtered onto the glass substrate 128. The source and drain patterning may be accomplished via shadow masking or photolithography. The source/drain electrode film could optionally be annealed. The semiconductor film 170 may then be deposited and patterned over the source electrode 120, the drain electrode 130, and the substrate 128. For example, a ZnO-based film may be deposited, and then patterned via photolithography or patterning during deposition.

Subsequently, the gate dielectric 156 may then be deposited and patterned over the semiconductor film 170. For example, a 2000-Angstrom Al_2O_3 film may be sputter deposited, and then patterned via shadow masking or photolithography. Vias (not shown) may be formed through the gate dielectric 156 to electrically connect to the source electrode 120 and the drain electrode 130. The Al_2O_3 film could optionally be annealed. The gate electrode 144 may then be deposited and patterned over the gate dielectric 156. For example, a 2000 Angstrom ITO film may be sputter deposited, and then patterned via shadow masking or photolithography. The ITO film could optionally be annealed.

Yet a fourth variation of a TFT structure is shown in Figure 23. This TFT structure includes a substrate 128 upon which is disposed a semiconductor channel layer 170. A source electrode 120 and a drain electrode 130 are provided on a surface of the semiconductor channel layer 170 opposing the surface that is adjacent to the glass substrate 128. A gate dielectric 156 is disposed over the semiconductor channel layer 170, the source electrode 120, and the drain electrode 130. A gate electrode 144 is disposed on the top surface (from a vertical perspective) of the gate dielectric 156. In other words, the gate electrode 144 and the semiconductor channel layer 170 are provided on opposing surfaces of the gate dielectric 156.

The TFT structure of Figure 23 may be fabricated, for example, by the deposition and patterning of a film that defines the semiconductor channel layer 170. For instance, a 500-Angstrom ZnO-based film may be deposited, and patterned via photolithography. The source electrode 120 and the drain electrode 130 may then be deposited and patterned. For example, a 500-Angstrom Aluminum or Silver, or other metal source/drain electrode film may be deposited in the desired pattern. Subsequently, the gate dielectric 156 may then be deposited and patterned over the semiconductor channel layer 170, the source electrode 120, and the drain electrode 130. For example, a 2000 Ångstrom dielectric may be deposited and patterned or selectively deposited. Vias (not shown) may be formed through the gate dielectric 156 to electrically connect to the source electrode 120 and the drain electrode 130. The gate electrode 144 may then be deposited and patterned over the gate dielectric 156. For example, a 2000 Ångstrom ITO or metal film may be deposited and/or patterned.

Alternatively, the contacts in the above configuration of Figure 23 may be made by selectively doping the ends of the semiconductor channel layer with In, Al, or any other suitable n-type dopant.

A substrate for supporting the TFT during manufacturing, testing, and/or use can include organic or inorganic materials. For example, the support may comprise inorganic glasses, ceramic foils, polymeric materials, filled polymeric materials, coated metallic foils, acrylics, epoxies, polyamides, polycarbonates, polyimides, polyketones, poly(oxy-1,4- phenyleneoxy-1,4-phenylenecarbonyl-1,4-phenylene) (sometimes referred to as poly(ether ether ketone) or PEEK), polynorbornenes, polyphenyleneoxides, poly(ethylene naphthalenedicarboxylate) (PEN), poly(ethylene terephthalate) (PET), poly(ether sulfone) (PES), poly(phenylene sulfide) (PPS), and fiber-reinforced plastics (FRP). Flexible substrates can also be thin metal foils such as stainless steel provided they are coated with an insulating layer to electrically isolate the thin film transistor. A flexible support, in some embodiments of the present invention, allows for roll processing, which may be continuous, providing economy of scale and economy of manufacturing over flat and/or rigid supports. The flexible support chosen preferably is capable of wrapping around the circumference of a cylinder of less

than 50 cm diameter, more preferably 25 cm diameter, most preferably 10 cm diameter, without distorting or breaking, using low force as by unaided hands. The preferred flexible support may be rolled upon itself. However, if flexibility is not a concern, then the substrate may be a wafer or sheet made of materials including glass and silicon. The thickness of the substrate may vary, and according to particular examples it can range from 100 μm to 1 cm.

In some embodiments of the invention, the support may be optional. For example, in a top construction as in Figure 21, when the gate electrode and/or gate dielectric provides sufficient support for the intended use of the resultant TFT, the support is not required. In addition, the support may be combined with a temporary support. In such an embodiment, a support may be detachably adhered or mechanically affixed to the support, such as when the support is desired for a temporary purpose, e.g., manufacturing, transport, testing, and/or storage. For example, a flexible polymeric support may be adhered to a rigid glass support, from which support could be removed.

The gate electrode can be any useful conductive material. A variety of gate materials known in the art, are also suitable, including metals, degenerately doped semiconductors, conducting polymers, and printable materials such as carbon ink, silver-epoxy, or sinterable metal nanoparticle suspensions. For example, the gate electrode may comprise doped silicon, or a metal, such as aluminum, chromium, gold, silver, nickel, copper, tungsten, palladium, platinum, tantalum, and titanium. Gate electrode materials can also include transparent conductors such as indium-tin oxide (ITO), ZnO, SnO₂, or In₂O₃. Conductive polymers also can be used, for example polyaniline, poly(3,4-ethylenedioxythiophene)/poly(styrene sulfonate) (PEDOT:PSS). In addition, alloys, combinations, and multilayers of these materials may be useful.

The thickness of the gate electrode may vary, and according to particular examples it can range from 50 to 1000 nm. The gate electrode may be introduced into the structure by chemical vapor deposition, sputtering, evaporation and/or doping, or solution processing.

The same material can provide the gate electrode function and also provide the support function of the support. For example, doped silicon can function as the gate electrode and support the TFT.

The gate dielectric is provided in contact with the gate electrode. This gate dielectric electrically insulates the gate electrode from the balance of the TFT device. Thus, the gate dielectric comprises an electrically insulating material. The gate dielectric should have a suitable dielectric constant that can vary widely depending on the particular device and circumstance of use. For example, a dielectric constant from 2 to 100 or even higher is known for a gate dielectric. Useful materials for the gate dielectric may comprise, for example, an inorganic electrically insulating material. The gate dielectric may comprise a polymeric material, such as polyvinylidenedifluoride (PVDF), cyanocelluloses, polyimides, etc. The gate dielectric may comprise a plurality of layers of different materials having different dielectric constants.

Specific examples of materials useful for the gate dielectric include strontiates, tantalates, titanates, zirconates, aluminum oxides, silicon oxides, tantalum oxides, titanium oxides, silicon nitrides, barium titanate, barium strontium titanate, barium zirconate titanate, zinc selenide, and zinc sulfide. In addition, alloys, combinations, and multilayers of these examples can be used for the gate dielectric. Of these materials, aluminum oxides, silicon oxides, and zinc selenide are preferred. In addition, polymeric materials such as polyimides, polyvinyl alcohol, poly(4-vinylphenol), polyimide, and poly(vinylidene fluoride), polystyrene and substituted derivatives thereof, poly(vinyl naphthalene) and substituted derivatives, and poly(methyl methacrylate) and other insulators having a suitable dielectric constant.

The gate dielectric can be provided in the TFT as a separate layer, or formed on the gate such as by oxidizing the gate material to form the gate dielectric. The dielectric layer may comprise two or more layers having different dielectric constants. Such insulators are discussed in U.S Patent No. 5,981,970 and copending US Patent Publication No. 2006/0214154, both cited herein. Gate insulator materials typically exhibit a band-gap of greater than 5 eV.

The thickness of the gate insulator layer may vary, and according to particular examples it can range from 10 to 300 nm. The gate dielectric layer may be introduced into the structure by techniques such as chemical vapor deposition, sputtering, atomic layer deposition, or evaporation, solution.

5 Source/drain terminals refer to the terminals of a TFT, between which conduction occurs under the influence of an electric field. Designers often designate a particular source/drain terminal to be a "source" or a "drain" on the basis of the voltage to be applied to that terminal when the TFT is operated in a circuit.

10 The source electrode and drain electrode are separated from the gate electrode by at least the gate dielectric, while the zinc-oxide-based semiconductor layer can be over or under the source electrode and drain electrode. The source and drain electrodes can be any useful conductive material. Useful materials include most of those materials described above for the gate electrode, for
15 example, aluminum, barium, calcium, chromium, gold, silver, nickel, palladium, platinum, titanium, copper, tungsten, polyaniline, PEDOT:PSS, other conducting polymers, alloys thereof, combinations thereof, and multilayers thereof. Other illustrative materials include transparent, n-type conductors such as indium-tin oxide (ITO), ZnO, SnO₂, or In₂O₃. Preferred electrodes are silver, gold,
20 PEDOT:PSS, or aluminum.

 The source electrode and drain electrode can be provided by any useful means such as chemical or physical vapor deposition (e.g., thermal evaporation, sputtering), evaporation, ink jet printing, or doping of the semiconductor channel layer material via diffusion or ion implantation and solution deposition. The
25 patterning of these electrodes can be accomplished by known methods such as shadow masking, additive photolithography, subtractive photolithography, printing, microcontact printing, and pattern coating. The source and drain terminals may be fabricated such that they are geometrically symmetrical or non-symmetrical.

30 Electrical contact to the gate electrode, source, drain and substrate may be provided in any manner. For example, metal lines, traces, wires, interconnects, conductors, signal paths, and signaling mediums may be used for providing the

desired electrical connections. The related terms listed above, are generally interchangeable, and appear in order from specific to general. Metal lines, generally aluminum (Al), copper (Cu), or an alloy of Al and Cu, are typical conductors that provide signal paths for coupling or interconnecting, electrical
5 circuitry. Conductors other than metal may also be utilized.

In cases where another layer covers the electrical contact of interest, connection to the electrical contact can be made by creating a “via” that penetrates to the contact. Such vias can be made by convenient patterning operations such as lithography, etching, or laser based processes.

10 An illustrative n-channel operation of the transistor involves applying a positive voltage to the gate electrode, grounding the source, and applying a positive voltage to the drain. For example, a voltage of 5 to 40 V may be applied to the gate electrode and the drain during operation. The threshold voltage may range from -minus 10 to 20 V, although devices can operate with larger ranges.
15 Electrons flow from the source, along the semiconductor thin film, and out of the transistor through the drain. The effective mobility of the electrons may vary depending upon the specific structure, but typically should be greater than $0.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for useful practical applications. Simply by removing the positive voltage applied to the gate electrode turns the transistor off when the transistor is an
20 enhancement-mode transistor.

Electronic devices in which TFTs and other devices are useful include, for example, more complex circuits, e.g., shift registers, integrated circuits, logic circuits, smart cards, memory devices, radio-frequency identification tags, backplanes for active matrix displays, active-matrix displays (e.g. liquid crystal or
25 OLED), solar cells, ring oscillators, and complementary circuits, such as inverter circuits, for example, in combination with other transistors made using available p-type organic semiconductor materials such as pentacene. In an active matrix display, a transistor according to the present invention can be used as part of voltage hold circuitry of a pixel of the display. In devices containing the TFTs,
30 such TFTs are operatively connected by means known in the art.

One example of a microelectronic device is an active-matrix liquid-crystal display (AMLCD). One such device is an optoelectronic display that includes

elements having electrodes and an electro-optical material disposed between the electrodes. A connection electrode of the transparent transistor may be connected to an electrode of the display element, while the switching element and the display element overlap one another at least partly. An optoelectronic display element is
5 here understood to be a display element whose optical properties change under the influence of an electrical quantity such as current or voltage such as, for example, an element usually referred to as liquid crystal display (LCD). The presently detailed transistor has sufficient current carrying capacity for switching the display element at such a high frequency that the use of the transistor as a
10 switching element in a liquid crystal display is possible. The display element acts in electrical terms as a capacitor that is charged or discharged by the accompanying transistor. The optoelectronic display device may include many display elements each with its own transistor, for example, arranged in a matrix. Certain active matrix pixel designs, especially those supplying a display effect that
15 is current driven, may require several transistors and other electrical components in the pixel circuit.

One specific example of a basic AMLCD cell circuit is depicted in Figure 24. The AMLCD cell circuit includes a transistor 100 as presently described, and an LCD pixel 102 electrically coupled thereto. The transistor 100 and the LCD
20 pixel 102 together form a transistor/pixel cell 104. In the arrangement shown, the transistor 100 is electrically coupled to the LCD pixel 102 via the drain electrode 130. The gate electrode 144 of the transistor 100 is electrically coupled to a row or control line 108 (also referred to as a select or gate line) that receives on/off input for the transistor 100. The source electrode 120 of the transistor 100 is
25 electrically coupled to a column or data line 106 that receives a signal for controlling the LCD pixel 102. Each LCD pixel 102 can also be viewed as a capacitor representing the capacitance according to display design.

Figure 25 shows a typical pixel layout in which data lines 106 lead to individual source electrodes 120, control lines 108 lead to individual gate
30 electrodes 144, semiconductors 170, and drain electrodes 130 each forming a pixel conductor pad.

EXAMPLES

Description of the Coating Apparatus

All of the following thin film examples employ a flow setup as indicated in Figure 18. The flow setup is supplied with nitrogen gas flow 81 that has been purified to remove oxygen and water contamination to below 1 ppm. The gas is diverted by a manifold to several flow meters which control flows of purge gases and of gases diverted through bubblers to select the reactive precursors. In addition to the nitrogen supply, air flow 90 is also delivered via flow meter 91 to the apparatus. The air is pretreated with molecular sieves to remove moisture.

The following flows are delivered to the ALD coating apparatus: metal (zinc) precursor flow 92 containing metal precursors diluted in nitrogen gas; oxidizer-containing flow 93 containing non-metal precursors or oxidizers diluted in nitrogen gas; and nitrogen purge flow 95 composed only of the inert gas. The composition and flows of these streams are controlled as described below.

Gas bubbler 82 contains liquid diethylzinc. Gas bubbler 83 contains liquid trimethylaluminum. Both bubblers are kept at room temperature. Gas bubbler 99 contains solid trimethylindium. This bubbler is heated by means of a water bath to 60°C, in order to increase the vapor pressure of the trimethylindium. Flow meters 85, 86, and 100 deliver flows of pure nitrogen to the diethylzinc bubbler 82, trimethylaluminum bubbler 83, and trimethylindium bubbler 99, respectively. The output of the bubblers now contains nitrogen gas saturated with the respective precursor solutions. These output flows are mixed with a nitrogen gas dilution flow delivered from flow meter 87 to yield the overall flow of metal precursor flow 92. In the following examples, the flows will be as follows:

Flow meter 85:	To Diethylzinc Bubbler Flow
Flow meter 100:	To Trimethylindium Bubbler Flow
Flow meter 86:	To Trimethylaluminum Bubbler Flow
Flow meter 87:	To Metal Precursor Dilution Flow

Gas bubbler 84 contains pure water for the control (or ammonia in water) at room temperature. Flow meter 88 delivers a flow of pure nitrogen to gas bubbler 84, the output of which represents a stream of saturated water vapor. The water bubbler output and nitrogen streams are mixed with dilution stream from flow meter 89 to produce the overall flow of oxidizer-containing flow 93 which has a variable water vapor composition, ammonia composition, nitrogen composition, and total flow. In the following examples, the flows will be as follows:

Flow meter 88:	To Water Bubbler
Flow meter 89:	To Oxidizer Dilution Flow

Flow meter 94 controls the flow of pure nitrogen that is to be delivered to the coating apparatus. Streams or Flows 92, 93, and 95 are then delivered to an atmospheric pressure coating head where they are directed out of the channels or microchamber slots as indicated in Figure 19. A gap 96 of approximately 30 microns exists between the elongated channels and the substrate 97. The microchambers are approximately 2.5 mm tall, 0.86 mm wide, and run the length of the coating head, which is 76 mm. The reactant materials in this configuration are delivered to the middle of the slot and flow out of the front and back.

In order to perform a deposition, the coating head is positioned over a portion of the substrate and then moved in a reciprocating fashion over the substrate, as represented by the arrow 98. The length of the reciprocation cycle was 32 mm. The rate of motion of the reciprocation cycle is 30 mm/sec.

The following characterization is used:

Description of Transistor Measurement and Analysis

Transistor characterization of the fabricated devices fabricated using the present invention was performed with a Hewlett Packard HP 4156 parameter analyzer. Device testing was done in air in a dark enclosure.

The results were typically averaged from several devices. For each device, the drain current (I_d) was measured as a function of source-drain voltage (V_d) for various values of gate voltage (V_g). Furthermore, for each device the drain current was measured as a function of gate voltage for various values of source-

drain voltage. For most devices, V_g was swept from -10 V to 30 V for each of the drain voltages measured, typically 10 V, 20 V, and 30 V. Mobility measurements were taken from the 30 V sweep.

Parameters extracted from the data include field-effect mobility (μ),
5 threshold voltage (V_{th}), and the ratio of I_{on}/I_{off} for the measured drain current. These measurements can be taken without any protective film on the semiconductor thin film, yielding substantially the same results with or without the protective film. The field-effect mobility was extracted in the saturation region, where $V_d > V_g - V_{th}$. In this region, the drain current is given by the
10 equation (see Sze in *Semiconductor Devices—Physics and Technology*, John Wiley & Sons (1981)):

$$I_d = \frac{W}{2L} \mu C_{ox} (V_g - V_{th})^2$$

where, W and L are the channel width and length, respectively, and C_{ox} is the
15 capacitance of the dielectric layer, which is a function of dielectric thickness and dielectric constant of the material. Given this equation, the saturation field-effect mobility was extracted from a straight-line fit to the linear portion of the $\sqrt{I_d}$ versus V_g curve. The threshold voltage, V_{th} , is the x-intercept of this straight-line fit.

20 The log of the drain current as a function of gate voltage was plotted. Parameters extracted from the log I_d plot include the I_{on}/I_{off} ratio. The I_{on}/I_{off} ratio is simply the ratio of the maximum to minimum drain current. For the purpose of the claimed invention, the on/off ratio is measured by the ratio of the on current, defined as the drain current at a gate voltage of 10 V in excess of the threshold
25 voltage, to the off current, defined as the drain current at a gate voltage for which the transistor is in an off state. The measurements in the present examples were taken in excess of 10 V, which would result in minor changes to the measurement.

Materials Used:

(1) Conductive ITO substrate (100 nm thick ITO on soda lime glass,
30 commercially available from MBC, product #255)

(2) Me_3Al (commercially available from Aldrich Chemical Co.)

- (3) Et_2Zn (commercially available from Aldrich Chemical Co.)
 (4) Me_3In (commercially available from Strem Chemical Co.)
 (5) Ammonium Hydroxide [aqueous ammonia], (reagent grade, ~29
 5 weight % ammonia, commercially available from J. T. Baker Chemical Co.)

EXAMPLE 1

This example demonstrates that indium oxide (In_2O_3 when alone) has been incorporated into the zinc oxide (ZnO when alone) semiconductor layer as an indium-zinc-oxide material. Samples prepared using the above apparatus were
 10 analyzed employing X-ray fluorescence spectroscopy on a purified, fused quartz substrate (GM electronics 63x63-040p). Table 1 below shows the flow rates of the zinc and indium precursors as well as the level of zinc and indium detected.

TABLE 1

Sample	Diethyl zinc Gas Flow Rate, sccm	Trimethyl indium Gas Flow Rate, sccm	Molar Flow Ratio, In/Zn, percentage basis	Zn Detected ($\mu\text{g}/\text{cm}^2$)*	In Detected ($\mu\text{g}/\text{cm}^2$)**	Weight Ratio In/Zn
Comparative 1A	13	0	0	83.7	0	-----
1B	13	20	23%	85.3	None Detected Less than 1.4	-----
1C	13	40	46%	66.4	6.6	0.10
1D	13	80	92%	46.2	12.9	0.28
1E	13	160	185%	32.7	14.8	0.45

*XRF measurement error (1σ) for Zn values is 0.3%

15 **XRF measurement error (1σ) for In values is 1-2 %

The data in Table 1 indicate that substantial amounts of In_2O_3 have been doped into the ZnO host using this experimental approach and that it is possible to achieve a ratio of In/Zn, between 0 and 0.50 by controlling the respective metal
 20 precursor flow rates.

EXAMPLE 2

This example shows the change in crystallinity of the ZnO based semiconductor layer with increased incorporation of In_2O_3 . X-ray diffraction was used to determine the relative crystallinity of the same coatings used in the
 25 previous Example 1. X-ray diffraction analysis is capable of determining if a material is non-crystalline (amorphous), since a perfectly amorphous material would generate no lattice peaks. In order to quantify the crystallinity of these

InZnO samples, profile fitting summed the relative areas of the lattice peaks in each trace. The results are tabulated in Table 2 below. Figure 26 is an overlaid plot of the X-ray diffraction spectra of the series in Table 2. It may easily be seen that the intensities of the peaks of the ZnO trace having zero doped In (Sample 1A) are drastically diminished in relative intensity and broadened as the In is introduced into the ZnO lattice at the highest level (Sample 1E), the latter of which is seen to be approaching a completely amorphous morphology.

TABLE 2

Sample	Diethylzinc Flow Rate, (sccm)	Trimethylindium Flow Rate, sccm	Relative Crystallinity*
Comparative 1A	13	0	100%
1B	13	20	84%
1C	13	40	62%
1D	13	80	39%
1E	13	160	18%

* Cu-K α radiation used

Table 2 shows that as In₂O₃ content in the film is increased, the degree of crystallinity is significantly lowered. Because crystal regions in semiconductor films can be a source of film non-uniformity, a lower degree of crystallinity is associated with more uniform, robust films.

COMPARATIVE EXAMPLE 3

Preparation of Undoped ZnO thin film transistor.

This example describes the preparation of a thin film transistor device (TFT) that is comprised of a glass substrate, an ITO (indium tin oxide) gate electrode, a 1100 Å thick Al₂O₃ dielectric layer, and a 200 Å thick, undoped ZnO layer having evaporated Al metal source/drain contacts. The device used to prepare the Al₂O₃ and ZnO layers has been described in detail in Figures 5 to 12 herein. A 2.5 X 2.5 inch square (62.5 mm square) piece of ITO coated glass was positioned on the platen of this device, held in place by a vacuum assist, and heated to 200°C. The platen with the glass substrate was positioned under the coating head that directs the flow of the active precursor gasses. The spacing

between the ITO substrate and the coating head was adjusted using a micrometer to 30 microns.

The coating head has isolated channels through which flow: (1) inert nitrogen gas; (2) a mixture of nitrogen, and water vapor; and (3) a mixture of active metal alkyl vapor (Me_3Al or Et_2Zn) in nitrogen. The flow rate of the active metal alkyl vapor was controlled by bubbling nitrogen through the pure liquid (Me_3Al or Et_2Zn) contained in an airtight bubbler by means of individual mass flow control meters. The flow of water vapor was controlled by adjusting the bubbling rate of nitrogen passed through pure water in a bubbler. The temperature of the coating head was maintained at 40°C . Adjusting the flow rates of the individual gasses to the settings shown in Table 3 below, the coating process was initiated by oscillating the coating head across the substrate for the number of cycles specified. For the Samples Comparative 3A, Inventive 4A, Comparative 3B, and Inventive 4B, a common layer of Al_2O_3 dielectric was deposited on the ITO substrate using the process parameters for layer A in Table 3 below.

EXAMPLE 4

Preparation of Indium-Doped ZnO Thin film transistor

The preparation of the indium-doped ZnO layer in sample 4 is identical to that in sample 3 except that a flow of trimethylindium vapor is added to the flow of diethyl zinc, at the concentration specified in Table 3 below.

TABLE 3

Sample	Layer	Me_3Al^*	Et_2Zn^*	Me_3In^*	Water	Water/ Ammonia**	N_2 carrier with Metal Alkyl	N_2 carrier for water	N_2 Inert Purge	Cycles	Substrate Temp. ($^\circ\text{C}$)
A	Al_2O_3	4	0	0	15	0	45	90	644	330	200
Comp. 3A	ZnO 200 Å	0	13	0	15	0	45	90	644	62	240
4A	In-Doped ZnO 200 Å	0	13	40	15	0	45	90	644	62	240
Comp. 3B	N-Doped ZnO 200 Å	0	13	0	0	15	45	90	644	62	240
4B	In and N-Doped ZnO 200 Å	0	13	40	0	15	45	90	644	62	240

*Flow values in sccm (standard cubic centimeters/min)

** 29% NH_3 by weight in water

Aluminum source and drain contacts were evaporated onto samples Comparative 3A, Comparative 3B, Inventive 4A, and Inventive 4B through a shadow mask, yielding thin film transistors with channel lengths of 50, 100 or 150 μm and a channel width of 500 μm . A photolithographic process was used to isolate devices on the substrate, producing islands of ZnO. Electrical test results for the above devices are shown below in Table 4:

TABLE 4

Sample	Average Mobility (cm^2/Vs)	Average $I_{\text{on}}/I_{\text{off}}$
3A (comparative)	6.67	3×10^5
4A	6.22	4×10^5
3B (comparative)	12.74	2×10^9
4B	14.88	1×10^9

Table 4 shows that the In-doping of the ZnO semiconductor layer provides a similar or increased mobility relative to samples that do not contain indium, while providing increased robustness due to the lower crystallinity of the layers as indicated in Example 2

EXAMPLE 5

This example describes the preparation of devices made using a range of In_2O_3 levels in the ZnO semiconductor layer. This experiment is similar to that described in Example 4 except that the flow rate of trimethylindium in bubbler 99 was varied from 0 to 160 sccm. The trimethylindium flow rates used varied as in Table 5.

TABLE 5

Sample	Trimethylindium Flow Rates, in sccm	Average Mobility, $\text{cm}^2/\text{V}\cdot\text{s}$	Average Threshold Voltage, V	Average Ion/Ioff
5A	0	12.74	7.73	2×10^9
5B	20	13.37	7.17	1×10^9
5C	40	14.88	7.40	1×10^9
5D	80	10.71	7.59	1×10^9
5E	160	8.52	8.96	5×10^7

The data in Table 5 above show that as the trimethylindium flow rate is increased during the ZnO deposition that there is an increase in the mobilities up to a point (Sample 5C), and then there is a decrease in mobility at the highest trimethyl indium flow levels. On/off current ratios and average threshold voltages do not significantly shift within this series except at the highest trimethylindium flow rate.

EXAMPLE 6

Resistivity measurements were carried out on a Lucas SIGNATONE QuadPro 4-point probe instrument. Measured resistivity values for the undoped and N- and/or In-doped Samples 5A – 5D, all having 200Å thickness of the ZnO layer, ranged over 6 orders of magnitude. It is clear from the resistivity data in Table 6 that N-doping ZnO greatly increases the sample resistivity and that In-doping ZnO greatly reduces sample resistivity. Sample 5B, which had only In-doped ZnO, was too conductive for use as a good semiconductor layer. However, Sample 5D, which contains both In and N-doped ZnO is resistive enough to be a good semiconductor layer, plus because of the In-doping, has much reduced crystallinity.

TABLE 6

Sample	N-Doped	In-Doped	Resistivity ohm*cm
5A	No	0	1.1
5B	No	80	1.0×10^{-2}
5C	Yes	0	6.0×10^4
5D	Yes	80	4.8×10^1

Electron Paramagnetic Resonance (EPR) has been used as a technique to study donor states in ZnO based semiconductors. To our knowledge, there is no EPR data in the literature on either thin films of ZnO or mixed phases of $\text{In}_x\text{Zn}_{1-x}\text{O}$. Therefore, our interpretation of the EPR data is based on prior publications on shallow donor states in ZnO single crystals and nanoparticles. In the ZnO system, EPR can detect the conduction electron spin resonance (CESR) signal originating from shallow donor states of various intrinsic and extrinsic dopants. A highly n-doped ZnO matrix typically exhibits a CESR signal in the dark. We have conducted EPR experiments on sample set 4A-E using a Bruker ESP 300E X-Band EPR spectrometer. The measurements were conducted at 15 K. The CESR signal intensity was quantified using a calibrated EPR spin standard ($\text{Al}_2\text{O}_3\text{:Cr}$ NIST Standard SRM-2601P). Due to the low measurement temperature, the microwave power had to be reduced in order to avoid saturation of the EPR spin standard. Table 7 shows the EPR parameters of the CESR signal measured in the dark.

Table 7

Sample	Integrated CESR signal species /cm ³	g-value	EPR line width (mT)	Optical bandgap (eV)	Resistivity (ohm*cm)
2A	1.03×10^{18}	1.967	1.27	3.28	7.9×10^{-01}
2B	1.99×10^{18}	1.967	2.88	3.28	7.7×10^{-01}
2C	3.18×10^{18}	1.975	7.56	3.35	1.5×10^{-02}
2D	4.09×10^{18}	1.973	5.71	3.31	1.1×10^{-02}
2E	6.81×10^{18}	1.970	6.35	3.25	2.3×10^{-02}
6A	Not detected	N/A	N/A	3.34	5.4×10^{-01}

We observe that the CESR signal intensity increases monotonically with the trimethylindium flow rate as shown in Figure 27. This increase is concomitant with a decrease in resistivity of the samples as measured with the 4-point probe technique. Changes in the spectral characteristics of the EPR spectrum with increasing In content are: A substantial increase in the EPR line-width and a slight increase in the g-value towards the value of the free electron. The former could be due to the fact that In, at the center of a shallow donor state, will exhibit hyperfine interaction between the donor electron and the In nucleus. The increase in g-value coincides with an increase in the optical band-gap of the In-doped ZnO layer. Both effects could be manifestations of an increase in free carrier concentration, which according to the Burstein-Moss shift lead to an increase in the semiconductor bandgap. A larger bandgap in turn reduces the deviation of the EPR signal position of an effective mass donor from the value of the free electron. Sample 6A was prepared similarly to sample 4D, however the co-doping with indium was increased to 160 sccm flow rate while maintaining the ammonia flow rate (for N-doping) the same. In this sample, the resistivity is increased compared to the corresponding In-only sample 4D and the CESR signal is absent. This suggests that nitrogen co-doping either passivates or compensates the shallow donors introduced by In doping. The result is a semiconductor layer with a resistivity high enough to form a thin film transistor but with a desirable lesser degree of crystallinity compared to Indium-free ZnO.

EXAMPLE 7

The purpose of this example was to prepare a TFT device that had a transparent, conductive gate electrode prepared from a coating of In-doped ZnO. The devices on the sample had the following cross-sectional composition: glass substrate/In-doped ZnO gate electrode/ Al_2O_3 dielectric/ZnO semiconductor/Al source and drain electrodes. The In-doped ZnO gate electrode, layer 7A, was prepared in a similar fashion to sample 4A. The resistivity of the In-doped ZnO gate electrode layer was measured to be 3.3×10^{-02} ohm*cm. An Al_2O_3 dielectric layer (7B) and a ZnO semiconductor layer (7C) were then coated onto the top of layer 7A using the settings specified in Table 8. Aluminum source and drain contacts were evaporated onto the top of layer 7C through a shadow mask,

yielding thin film transistors with channel lengths of 50, 100 or 150 μm and a channel width of 500 μm . A photolithographic process was used to isolate devices on the substrate, producing islands of ZnO. Electrical test results for the above device (Sample 7) having the In-doped ZnO gate electrode are shown below in Table 9 and are compared to a check sample (3B) which was identical except that it had an ITO gate electrode.

TABLE 8

Sample Layer	Layer	Me ₃ Al	Et ₂ Zn	Me ₃ In	Water	Water/Ammonia**	N ₂ carrier with Metal Alkyl	N ₂ carrier for water	N ₂ Inert Purge	Number of Cycles	Substrate Temperature, C
7A	In-Doped ZnO gate electrode	0	13	80	15	0	45	90	644	300	240
7B	Al ₂ O ₃	4	0	0	15	0	45	90	644	330	200
7C	ZnO 200 Å	0	13	0	0	15	45	90	644	62	200

All flow values in sccm (standard cubic centimeters/min)

** 29% NH₃ by weight in water

10

TABLE 9

Sample	Average Mobility (cm ² /Vs)	Average I _{on} /I _{off}
7 (Devices with In-doped ZnO gate electrode)	5.19	5 x 10 ⁸
3B (Devices with ITO gate electrode)	12.74	2 x 10 ⁹

The data in Table 9 demonstrate that the In-doped ZnO layer produced on the atmospheric pressure atomic layer deposition device in this work is sufficiently conductive so that it functions well as a gate electrode in a TFT device.

15

PARTS LIST

1	continuous supply of gaseous materials for system
2	first channel flow of first molecular precursor over channel area of substrate
3	relative movement of substrate and multi-channel flows
4	second channel flow with inert gas over channel area
5	relative movement of substrate and multi-channel flows
6	third channel flow of second molecular precursor over channel area
7	relative movement of substrate and multi-channel flows
8	fourth channel flow with inert gas over channel area
9	relative movement of substrate and multi-channel flow
10	deposition device
11	multiple channel flow in parallel
12	output channel
14, 16, 18	gas inlet port
15	sequence
20	substrate
22	partition
24	gas output port
26	exhaust port
28a, 28b, 28c	gas supply
30	actuator
32	supply line
36	output face
38	redirecting plate
40	aperture
42	partition plate
44	delivery plate
46a, 46b, 46c	duct
48	redirecting chamber
50	chamber
52	transport motor
54	transport subsystem

Parts List – continued

56	control logic processor
58	baffle
60	Atomic Layer Deposition (ALD) process
62	web conveyor
64	deposition device transport
66	web substrate
70	Atomic Layer Deposition (ALD) process
72	diffusion layer
74	substrate support
81	nitrogen gas flow
82, 83, 84	gas bubblers
85, 86, 87	flow meter
88, 89, 91, 94	flow meter
90	air flow
92	metal precursor flow
93	oxidizer-containing flow
95	nitrogen purge flow
96	gap
97	example substrate
98	arrow
99	gas bubbler
100	flow meter
102	LCD pixel
103	transistor
104	transistor/pixel cell
106	column or data line
108	row or control line
120	source electrode
128	substrate
130	drain electrode
144	gate electrode
156	gate dielectric

Parts List – continued

170	semiconductor
175	protective layer
D	distance
F1, F2, F3, F4	gas flow
F _I , F _O , F _M , F _E	gas flow
H	channel height
I	inert gaseous material
L	channel length
M	second reactant gaseous material
O	first reactant gaseous material
R	arrow
W	channel width

CLAIMS:

1. A process of making an n-type zinc-oxide-based thin film semiconductor by depositing a thin film material on a surface area of a substrate,
5 either an entire surface area or a selected portion thereof, wherein deposition is by an atomic layer deposition process that is carried out substantially at or above atmospheric pressure, wherein the temperature of the substrate during deposition is under 300°C, and wherein the atomic layer deposition process comprises simultaneously directing a series of gas flows along elongated substantially parallel
10 channels comprising, in order, at least a first reactive gaseous material containing a zinc-containing compound having a molar flow during deposition, an inert purge gas, and a second reactive gaseous material through a plurality of output openings spaced apart from the substrate, and transporting the substrate in a direction relative to the plurality of output openings, such that any point on the surface area of the substrate
15 experiences a sequence of the first, the second and the third gaseous materials, whereby the sequence causes a thin film to be formed by atomic layer deposition on the surface area of the substrate,
wherein a volatile indium-containing compound is introduced into the first reactive gaseous material or a supplemental gaseous material such that the indium-
20 containing compound has a molar flow at a level of greater than 20 percent of the molar flow of the zinc-containing compound.
2. The process of claim 1 wherein the zinc-oxide-based thin film semiconductor is used in a thin film transistor.
25
3. The process of claim 1 wherein the crystallinity of the zinc-oxide-based thin film semiconductor is less than 85 percent as measured by x-ray diffraction.
- 30 4. The process of claim 1 wherein the volatile indium-containing compound is a trialkylindium compound or cyclopentadienylindium(I), wherein the alkyl has 1 to 4 carbon atoms.

5. The process of claim 1 wherein the resistivity of the zinc-oxide-based thin film semiconductor is reduced relative to the resistivity of a similar film not containing indium.

5 6. The process of claim 5 wherein the presence of incorporated Indium dopant derived from the indium-containing compound as a precursor provides a decrease in resistivity by a factor of at least 10 in the thin film material.

7. The process of claim 1 wherein the weight ratio of zinc to indium in
10 the zinc-oxide-based thin film semiconductor is 0.05 to 0.7.

8. The process of claim 1, wherein a volatile acceptor dopant precursor is introduced in the second reactive gaseous material, the inert purge gas, or an additional gas flow of a supplemental gaseous material.

15

9. The process of claim 8 wherein the volatile acceptor dopant precursor comprises an element selected from the group consisting of N, P, As, Li, Na, K, or mixtures thereof.

20 10. The process of claim 8 wherein the volatile acceptor dopant precursor is NO, NO₂, or ammonia.

11. The process of claim 1 wherein the zinc-oxide-based thin film semiconductor serves as a channel layer of a thin film transistor.

25

12. The process of claim 1 wherein the zinc-oxide-based thin film semiconductor serves as one or more conductive electrodes of a thin film transistor.

13. The process of claim 1 wherein the zinc-oxide-based thin film
30 semiconductor serves as an electrical conduit in an electronic circuit.

14. The process of claim 1 wherein the series of gas flows are provided by a deposition device comprising, facing the substrate in plan view, a series of elongated output openings, substantially in parallel, positioned over the substrate in

close proximity thereto, in an output face of the deposition device, spaced within 1 mm from the surface of the substrate subject to deposition.

15. The process of claim 14 wherein there are no exhaust channels
5 between the series of elongated output openings for the first reactive gaseous material and the second reactive gaseous material.

16. The process of claim 14 wherein the deposition device further
comprises exhaust channels between substantially parallel elongated output openings
10 for the first and the second reactive gaseous materials.

17. The process of claim 14 wherein the flows of one or more of the
gaseous materials to the substrate surface for thin film deposition provides at least
part of a force separating the depositing output face of the deposition device from the
15 surface of the substrate.

18. The process of claim 14 wherein the surface area of the substrate for
atomic layer deposition of the thin film semiconductor exceeds total surface area of
the output face of the deposition device.
20

19. The process of claim 1 wherein the substrate or a support for the
substrate comprises a moving web.

20. The process of claim 1 wherein the process is in unsealed relationship
25 to ambient atmosphere.

21. The process of claim 1 wherein the atomic layer deposition process is
carried out in a deposition system sequentially comprising:

(A) an entrance section;

30 (B) a coating section comprising:

(i) a plurality of sources for, respectively, a plurality of gaseous
materials comprising at least the first reactive gaseous material, the second reactive
gaseous material, and the inert purge gas, respectively;

(ii) at least one delivery head for delivering the plurality of gaseous materials to the substrate receiving thin film deposition, the delivery head comprising:

(a) a plurality of inlet ports comprising at least a first, a second, and a third inlet port for receiving the first reactive gas material, the second reactive gaseous material, and the inert purge gas, respectively; and

(b) a depositing output face separated a distance from the substrate and comprising a plurality of substantially parallel elongated output openings for each of the first reactive gaseous material, the second reactive gaseous material, and the inert purge gas, wherein the delivery head is designed to deliver the first reactive gaseous material, the second reactive gaseous material, and the inert purge gas simultaneously from the elongated output openings in the depositing output face;

(C) an exit section;

(D) means for moving the substrate in a unidirectional passage through the coating section; and

(E) means for maintaining a substantially uniform distance between the depositing output face of the delivery head and a surface of the substrate during deposition of the thin film, wherein the delivery head in the coating section is designed to provide flows of one or more of the gaseous materials to the substrate surface for thin film deposition that also provides at least a part of a force separating the depositing output face of the delivery head from the surface of the substrate, wherein optionally the entrance section and/or the exit section each comprises a non-depositing output face having a plurality of non-depositing output openings designed to provide gas flow of non-reactive gas to the surface of the substrate during at least part of the passage through the deposition system.

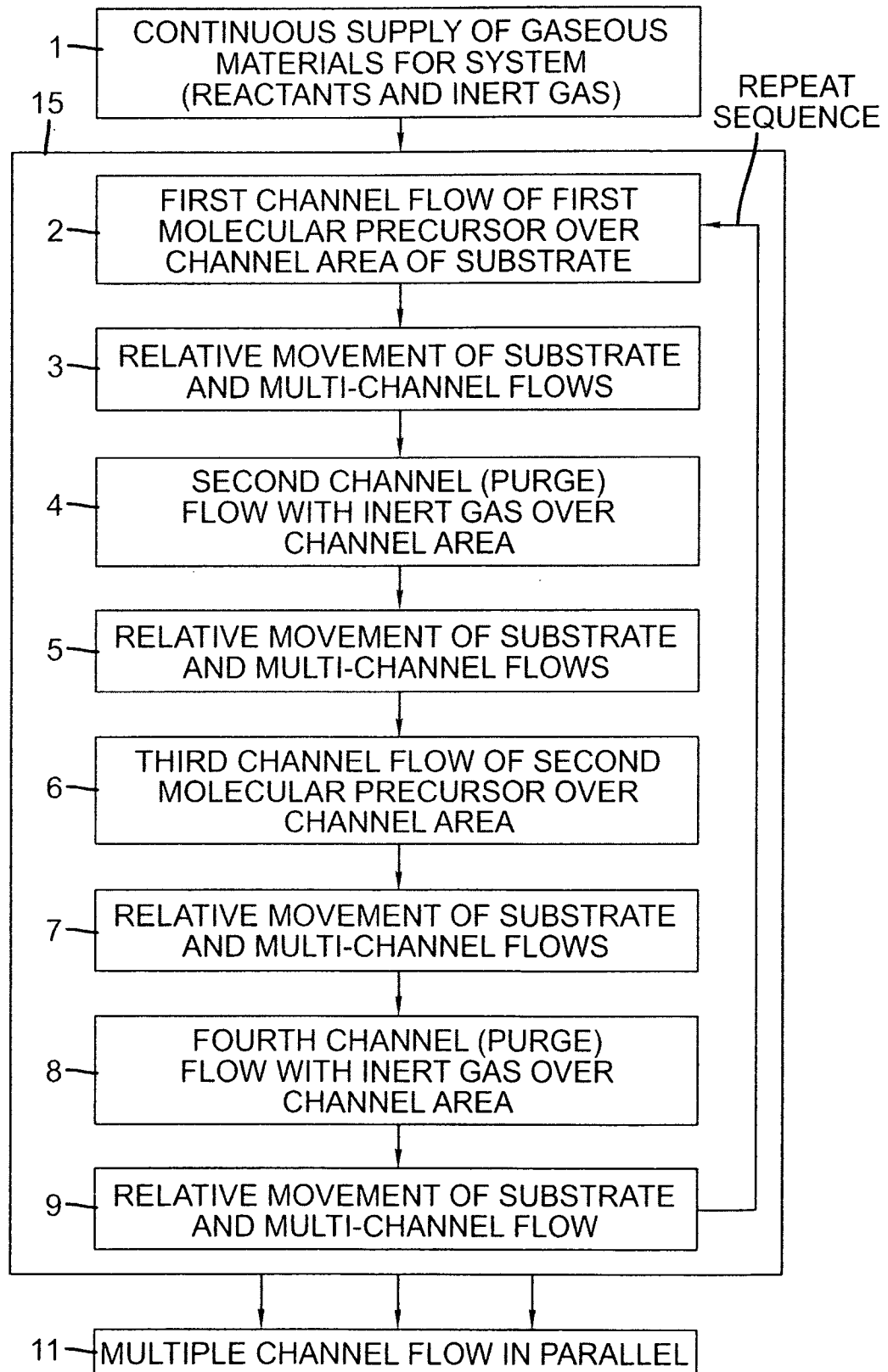
22. The process of claim 21 wherein the surface area of the substrate is exposed to a gas flow in a channel for less than 100 milliseconds.

23. The process of claim 21 wherein relative movement of the substrate to the deposition head is at a speed at least 0.1 cm/sec.

24. The process of claim 21 wherein the process is used to make a multiplicity of thin film transistors in an electronic device, each thin film transistor comprising said n-type zinc-oxide-based thin film semiconductor, wherein the first
5 reactive gaseous material comprises an organo-zinc precursor compound and the second reactive gaseous material comprises a reactive oxygen-containing gaseous material.

25. The process of claim 24, wherein the process further comprises
10 forming, for each of the multiplicity of thin film transistors, a spaced apart source electrode and drain electrode, wherein the source electrode and the drain electrode are separated by, and electrically connected with, the n-type zinc-oxide-based thin film semiconductor; and forming a gate electrode spaced apart from the n-type zinc-oxide-based thin film semiconductor, wherein the electronic device is selected from a group
15 consisting of an integrated circuit, active-matrix display, solar cell, active-matrix imager, sensor, and rf price, identification, or inventory label.

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**FIG. 1**

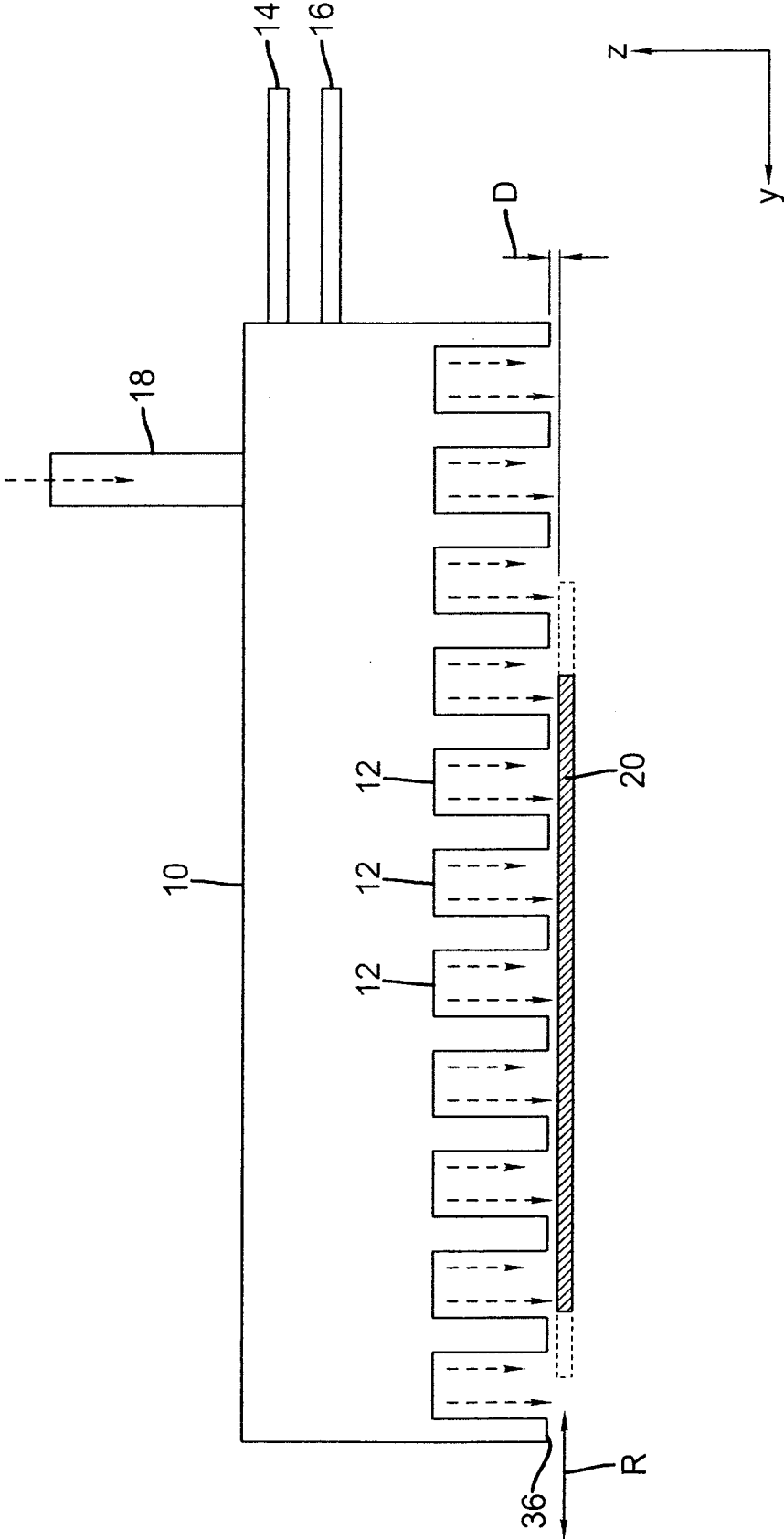


FIG. 2

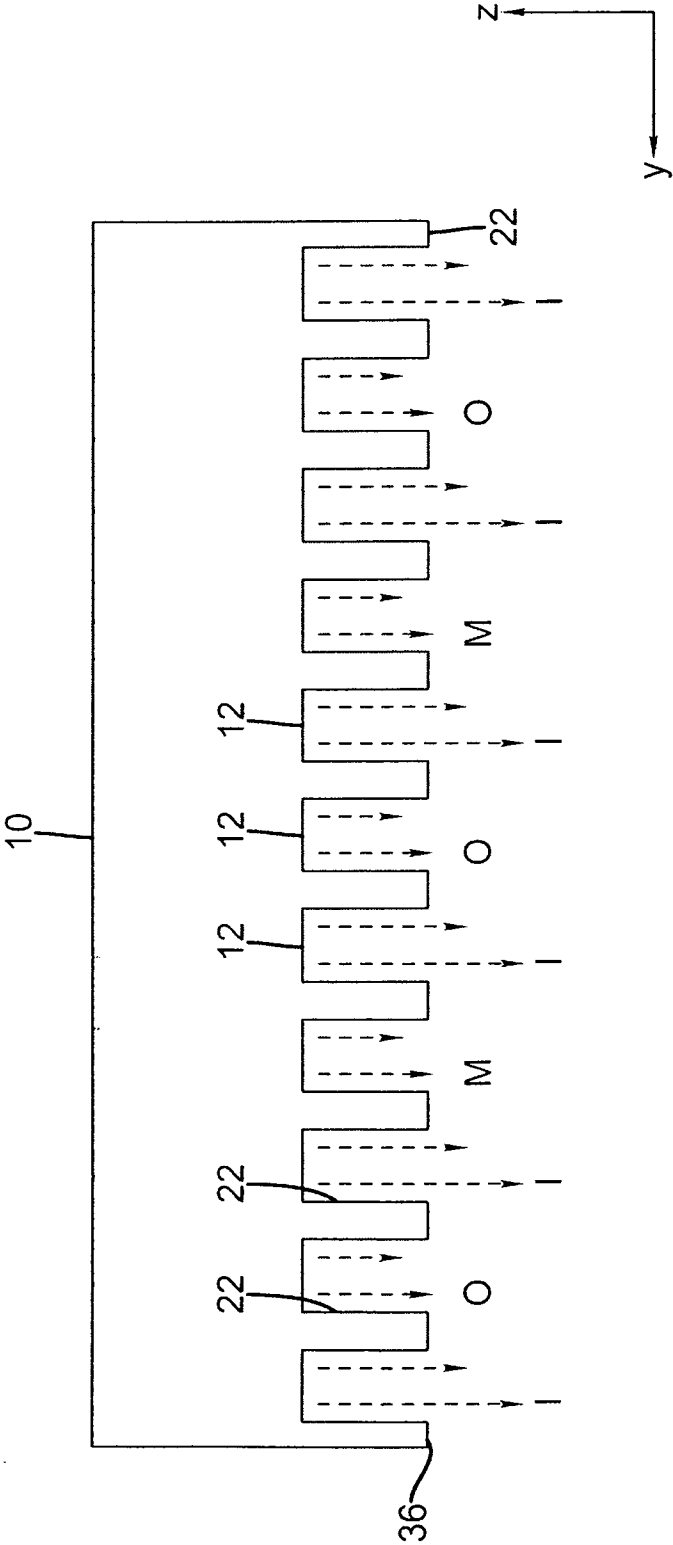


FIG. 3

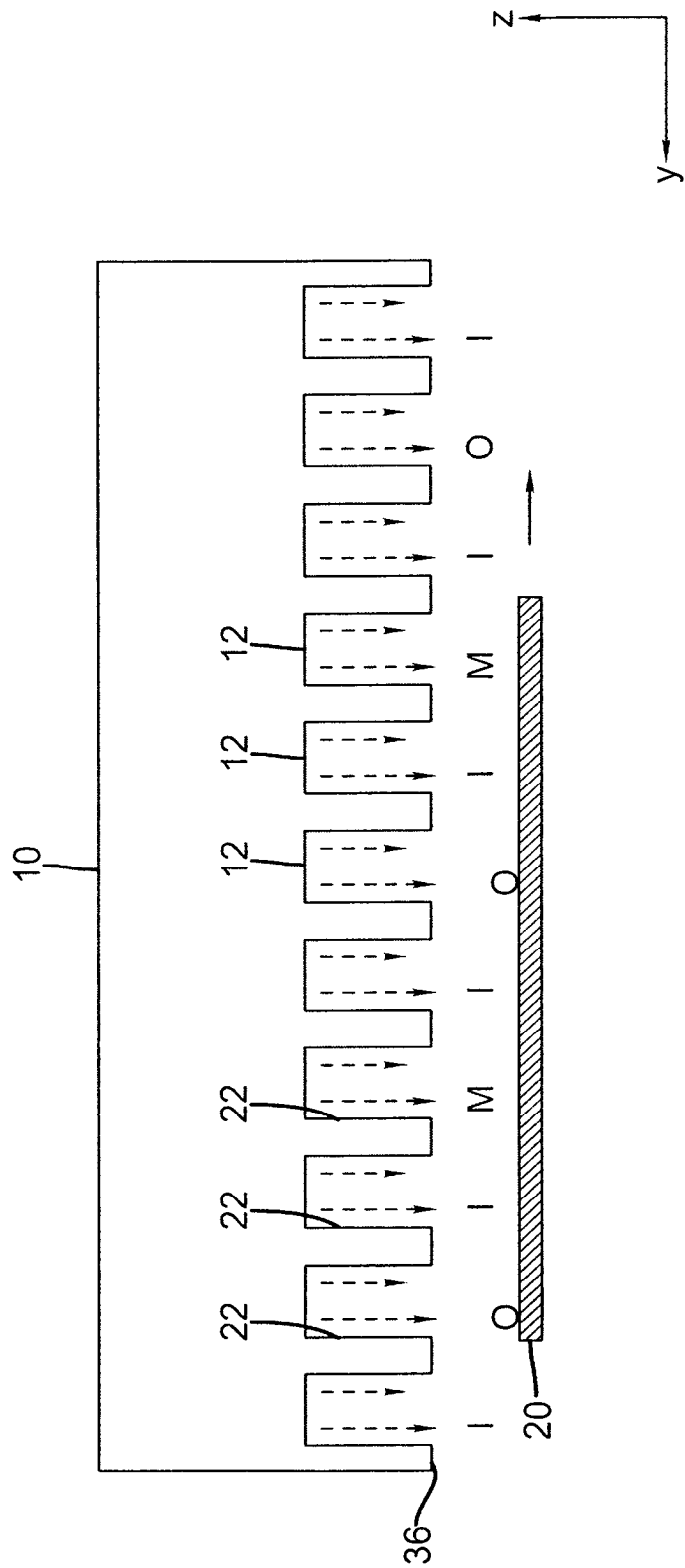


FIG. 4A

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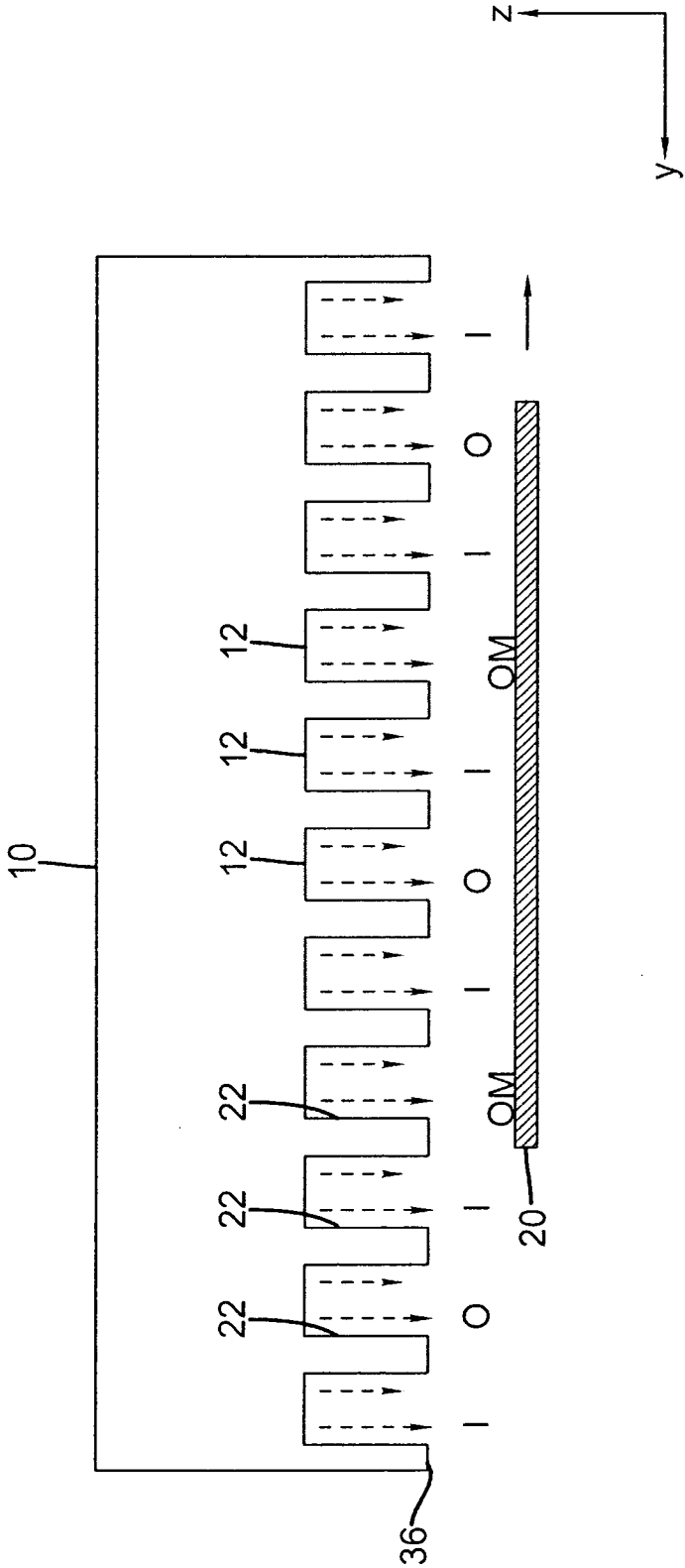


FIG. 4B

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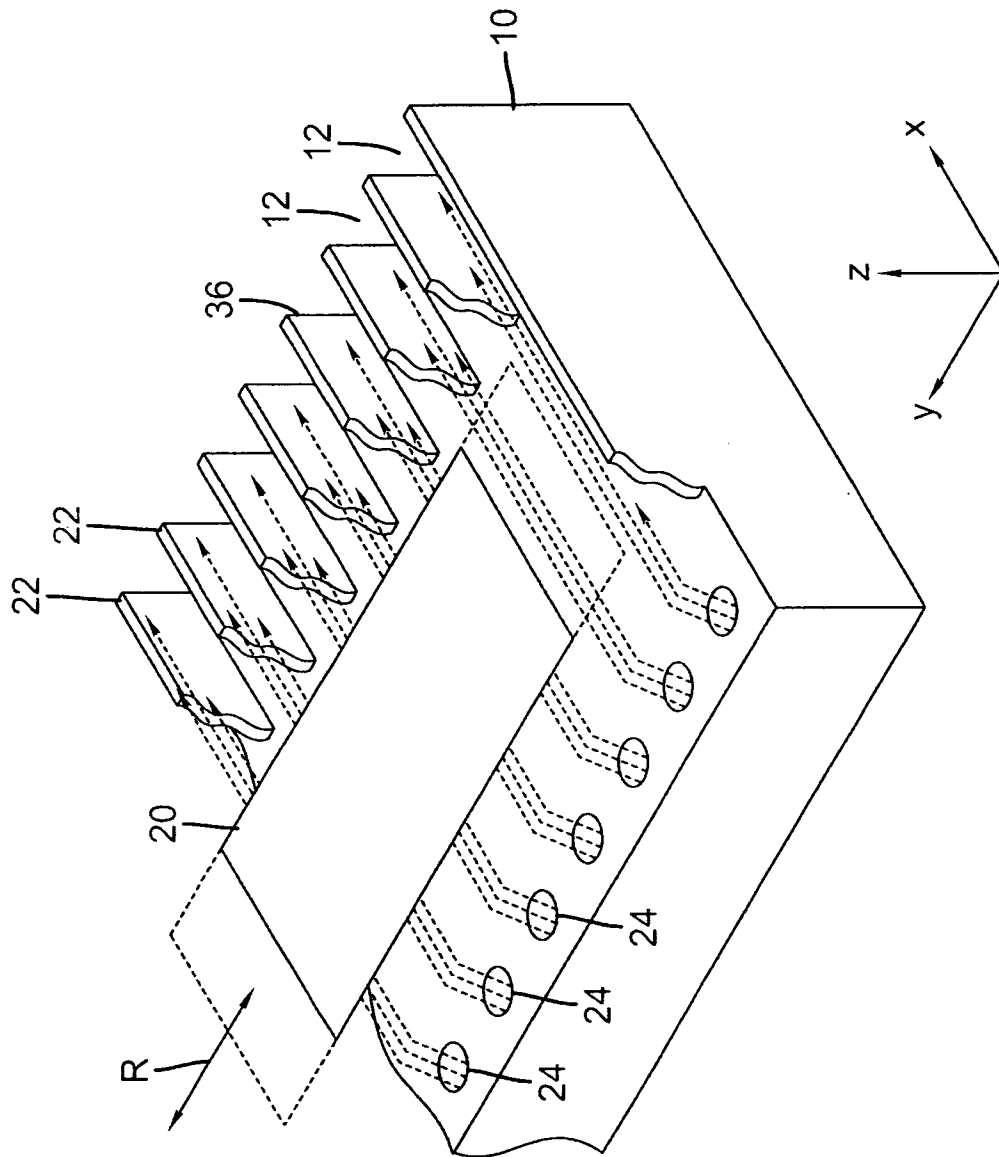


FIG. 5

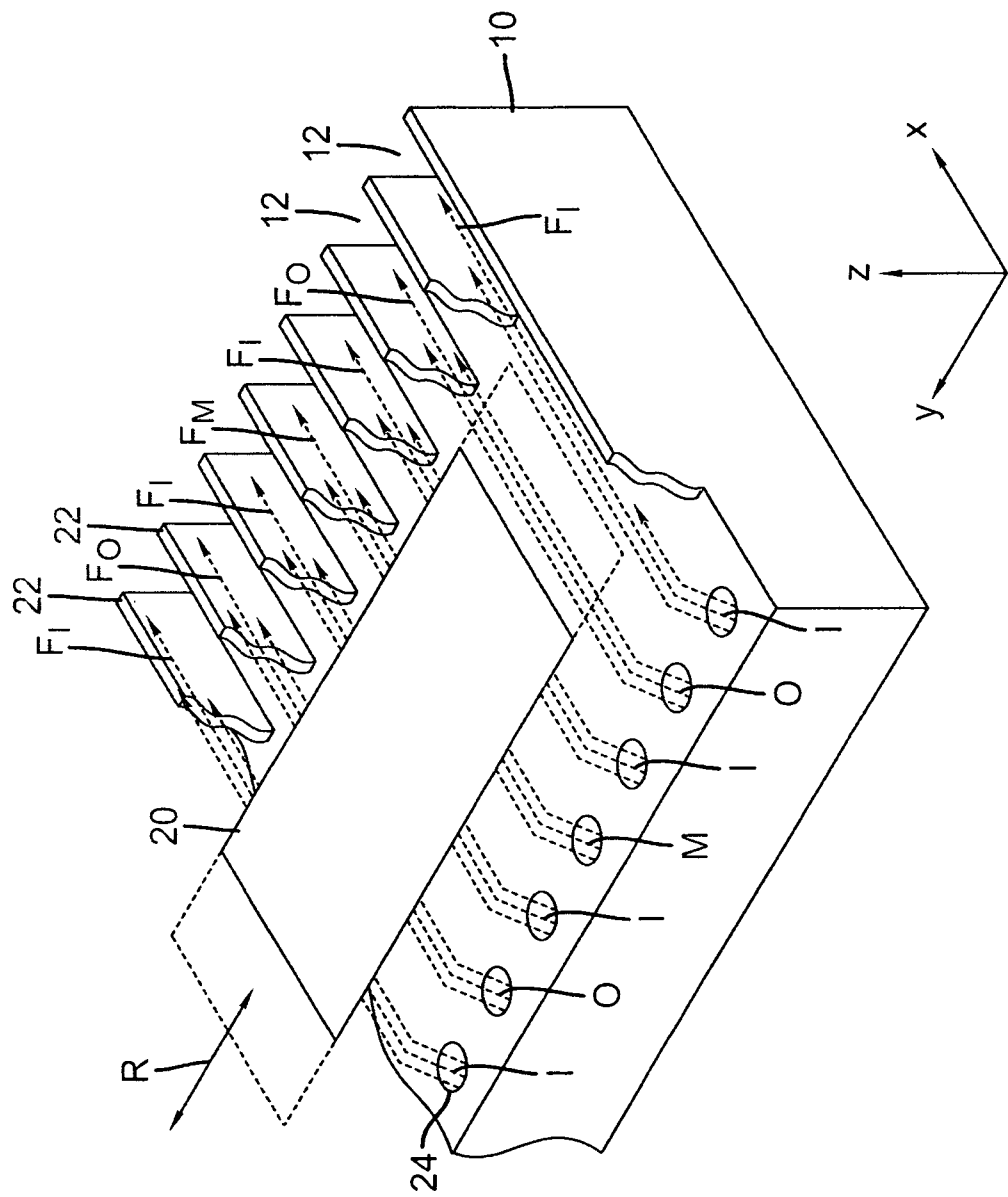
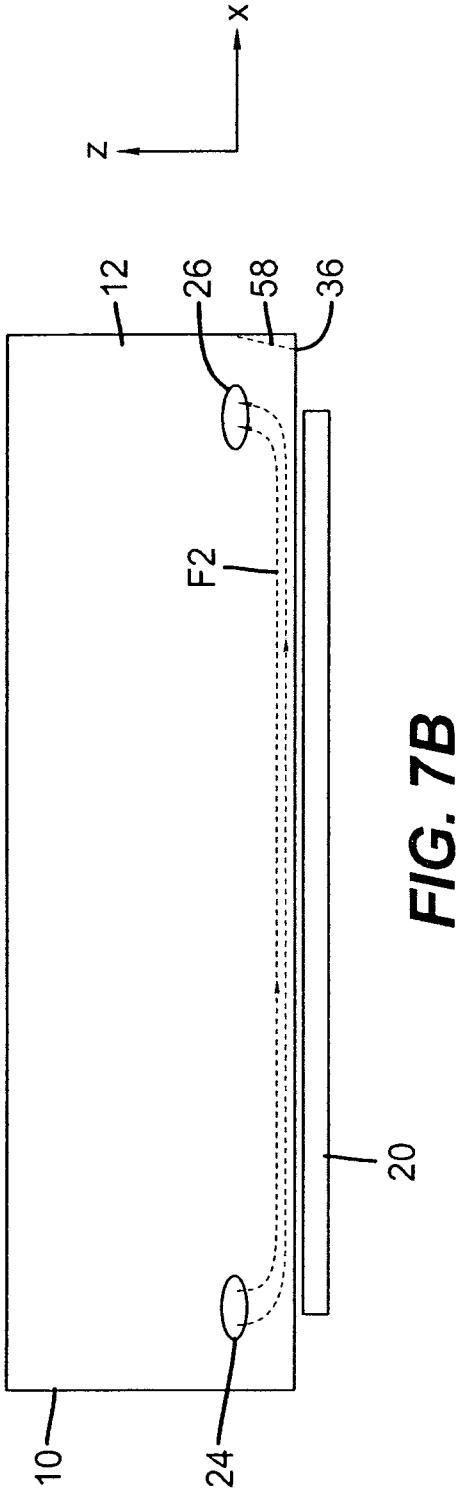
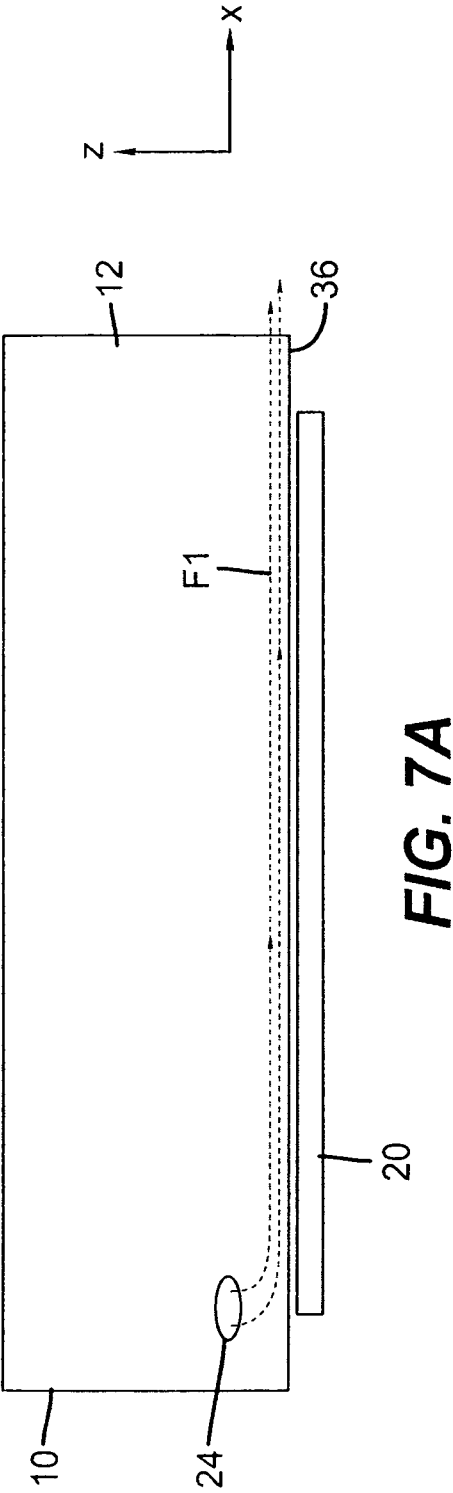
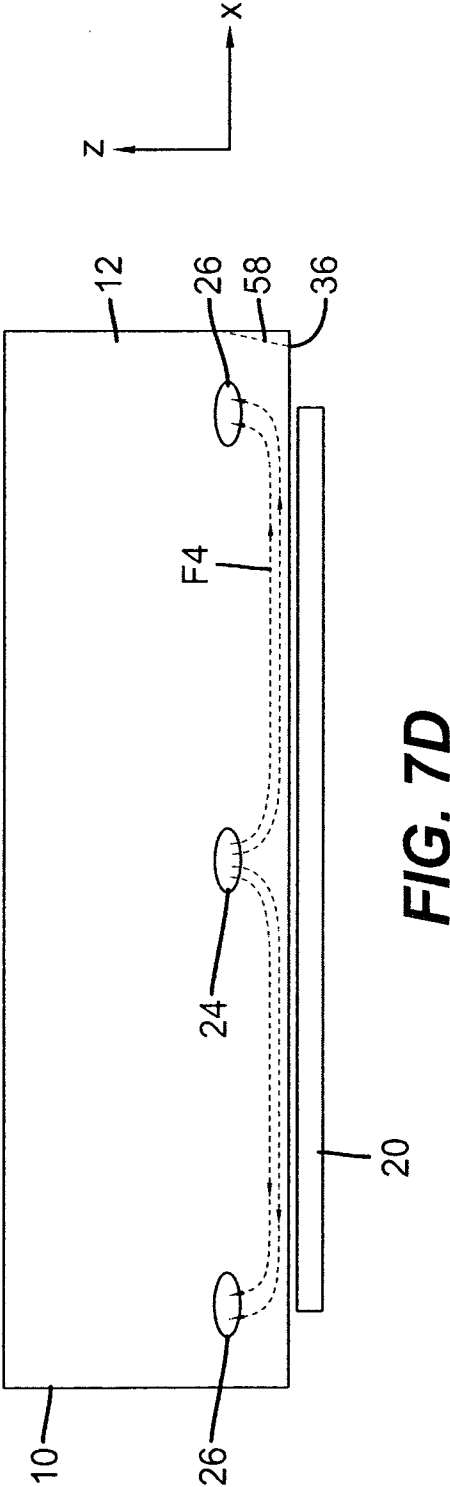
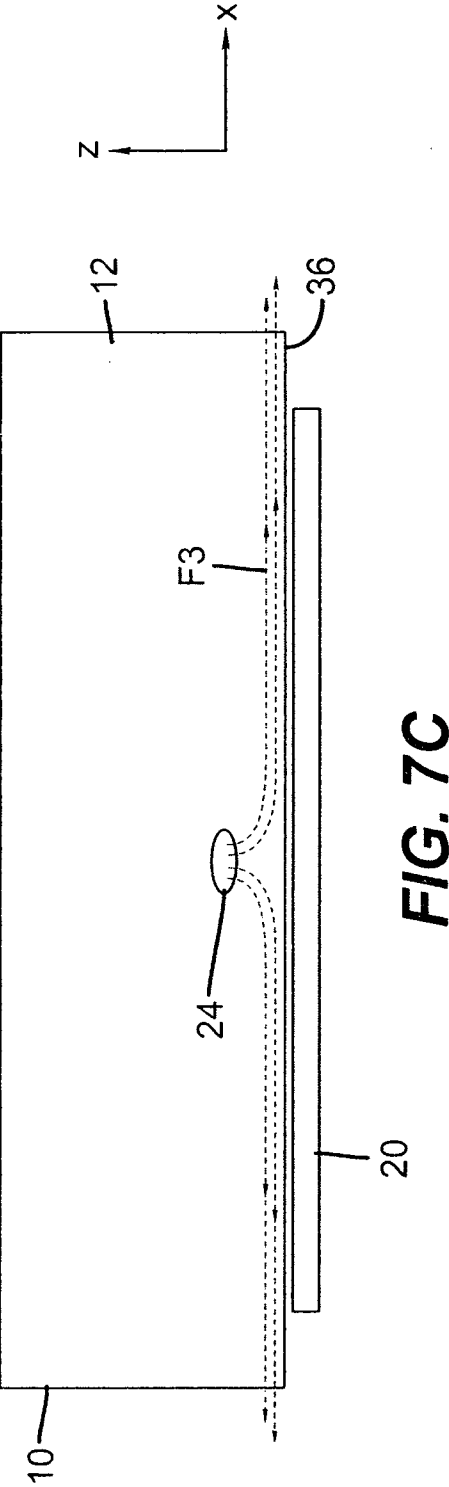


FIG. 6



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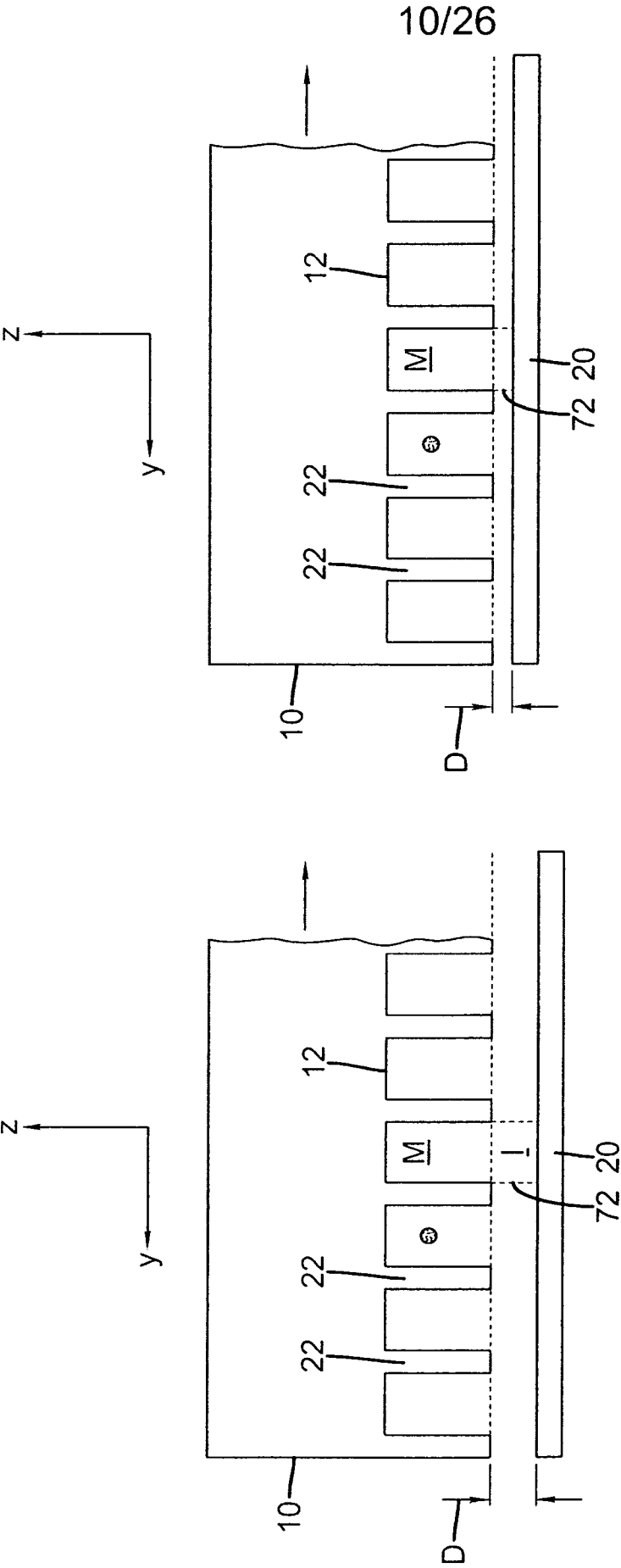


FIG. 8B

FIG. 8A

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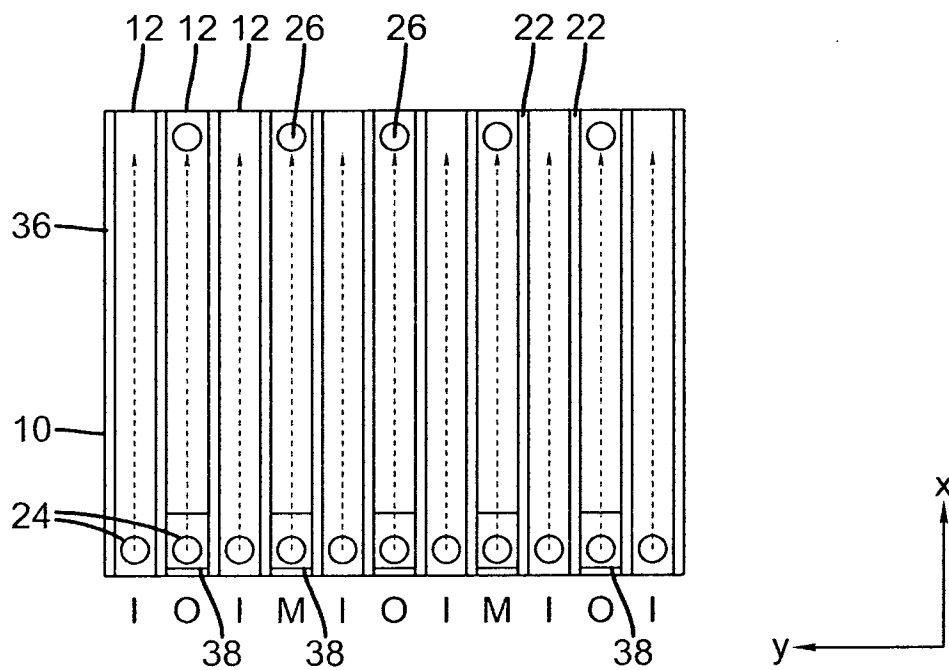


FIG. 9

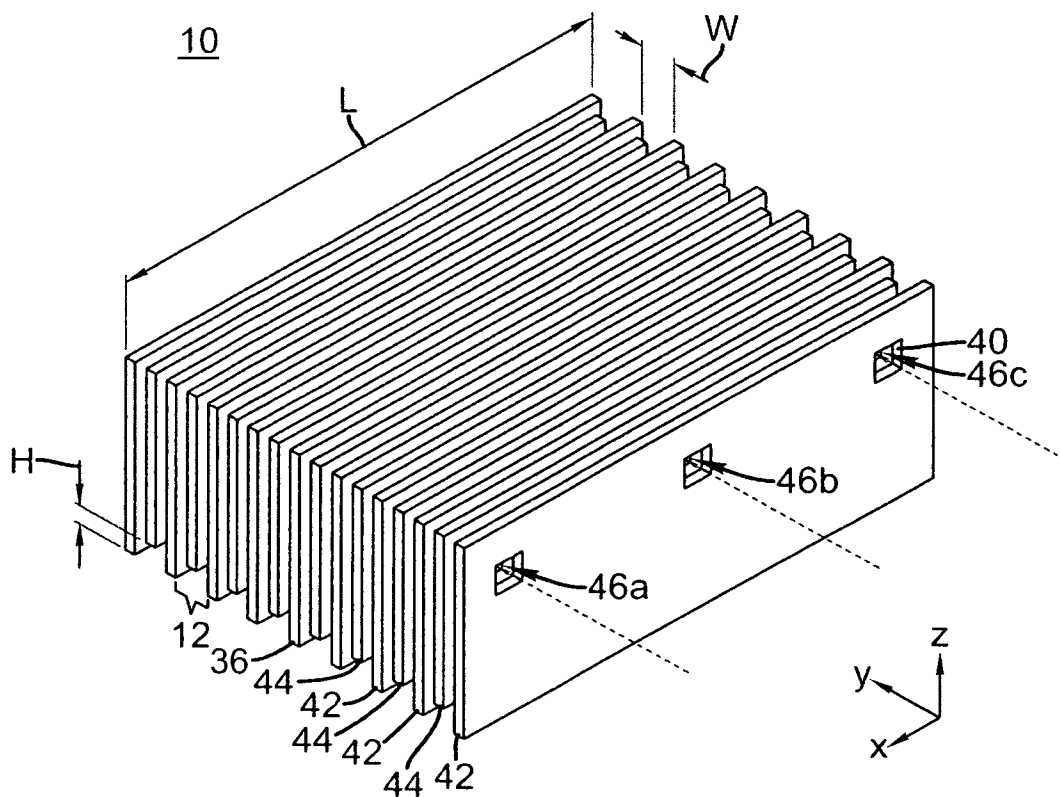


FIG. 10

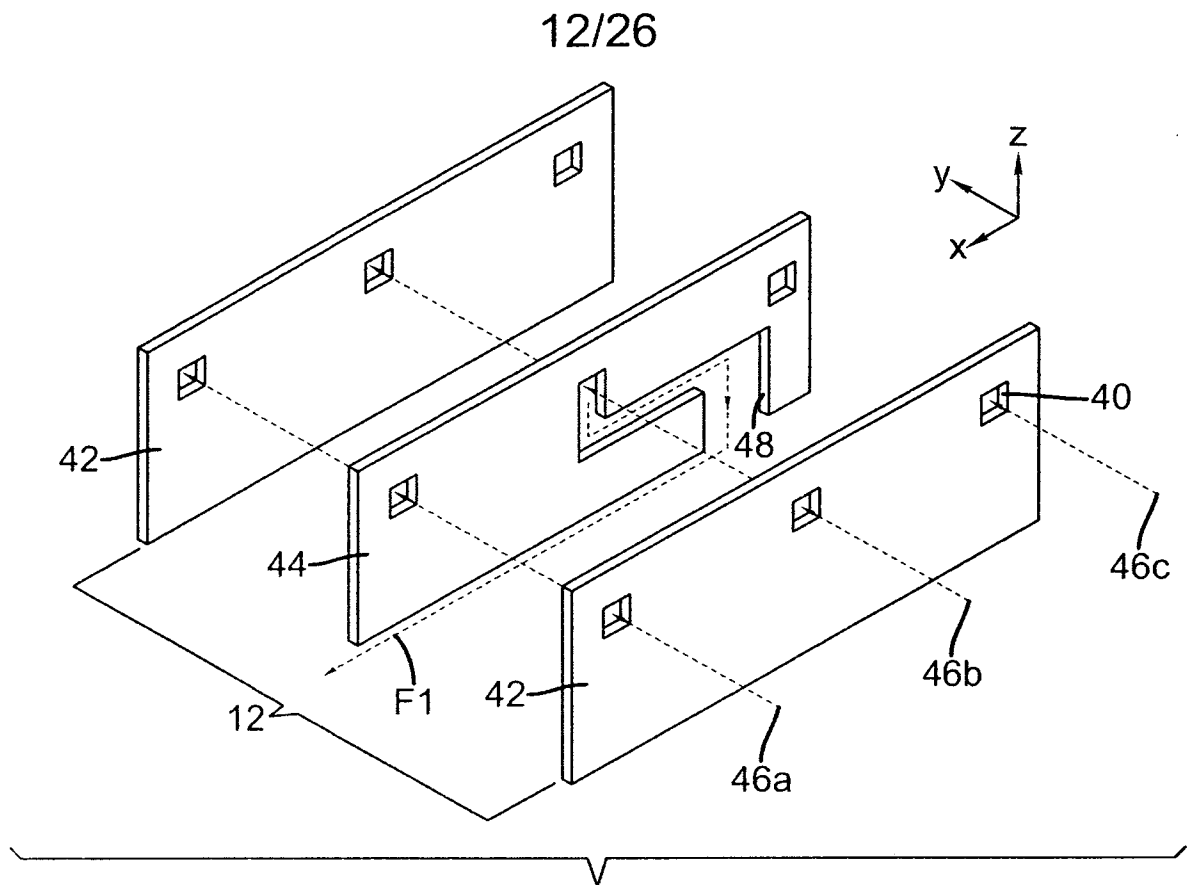


FIG. 11A

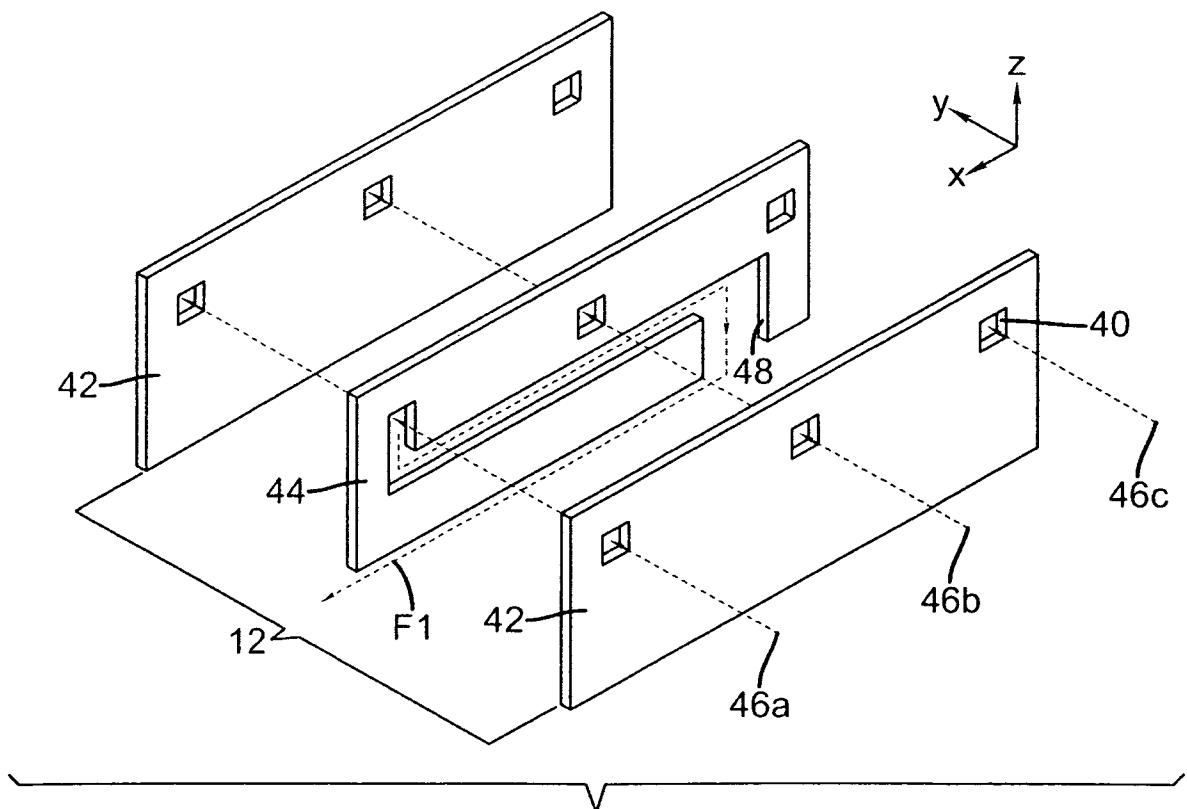
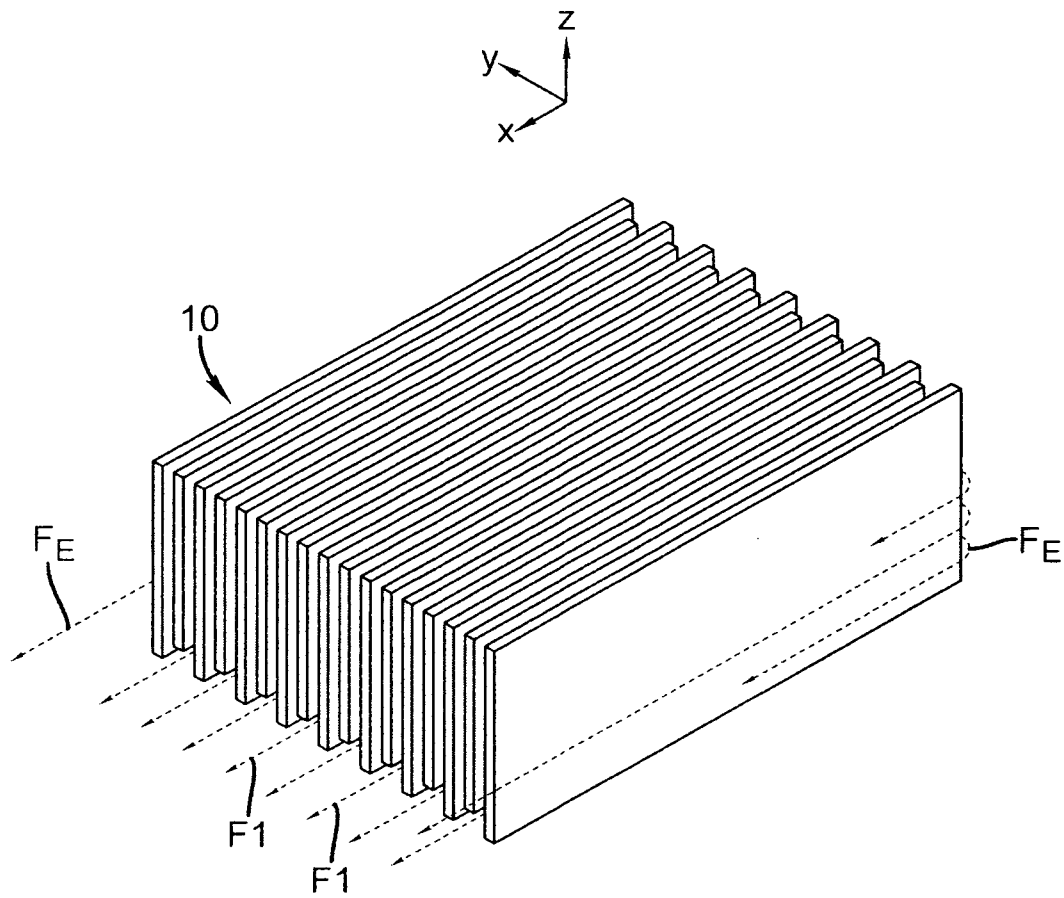
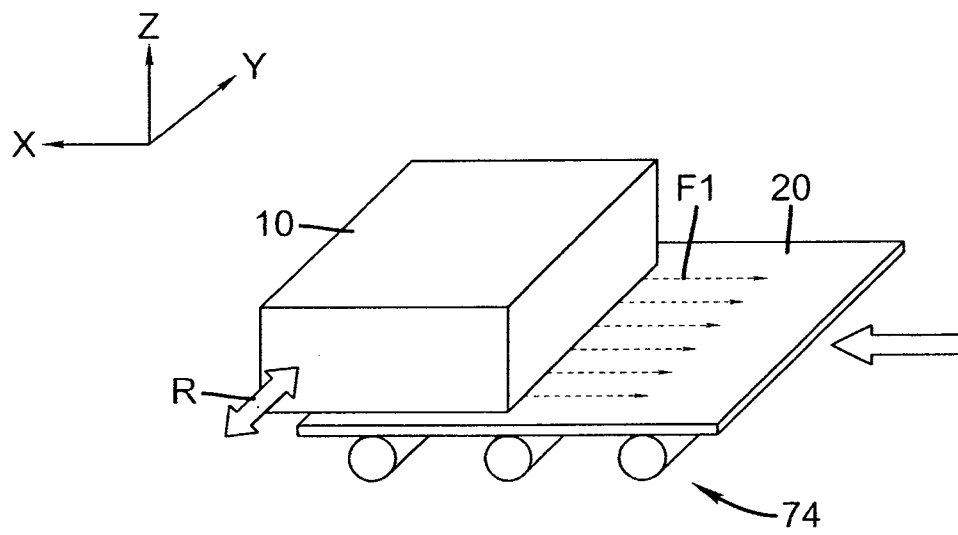


FIG. 11B

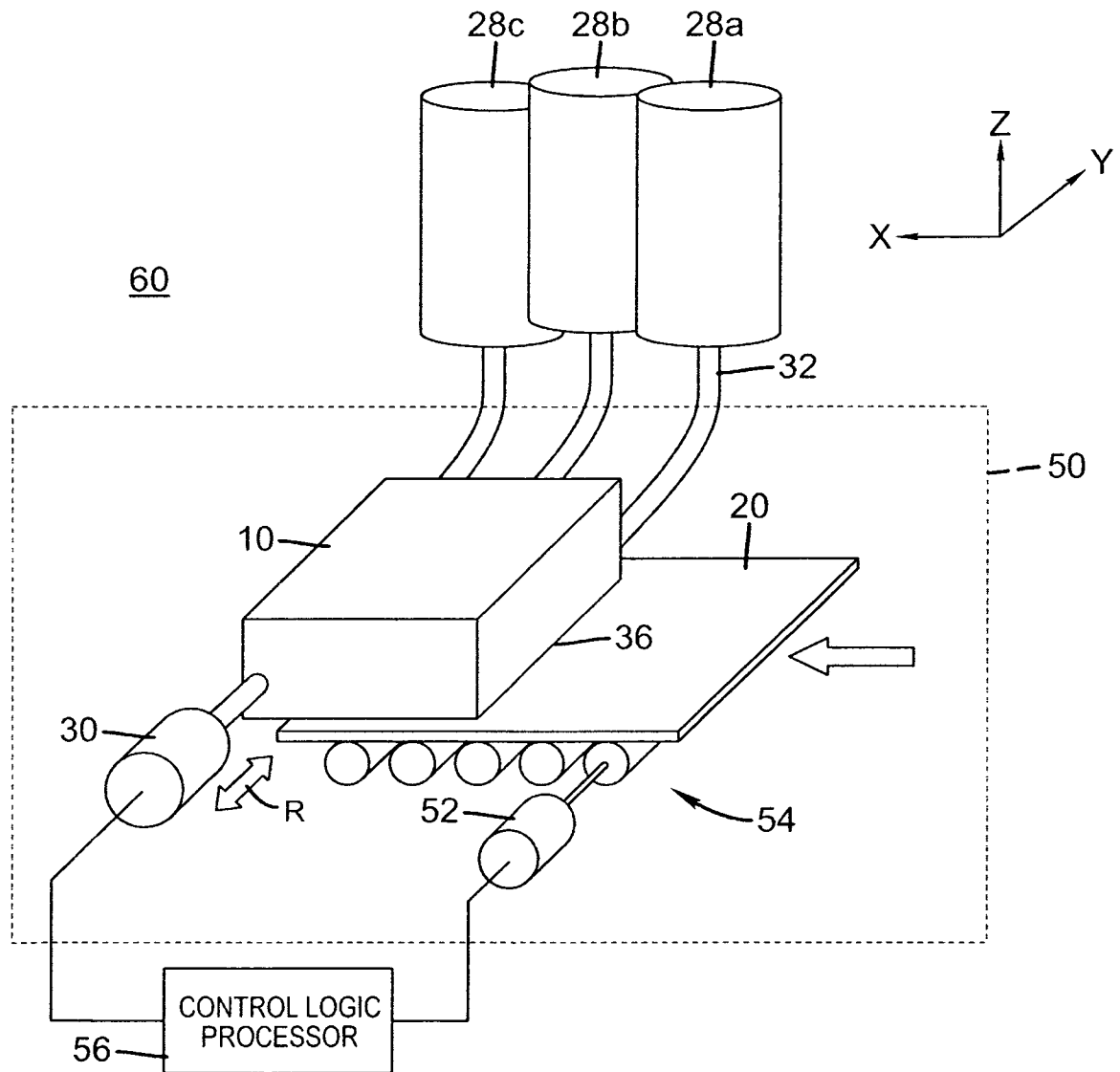
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**FIG. 12**

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**FIG. 13**

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**FIG. 14**

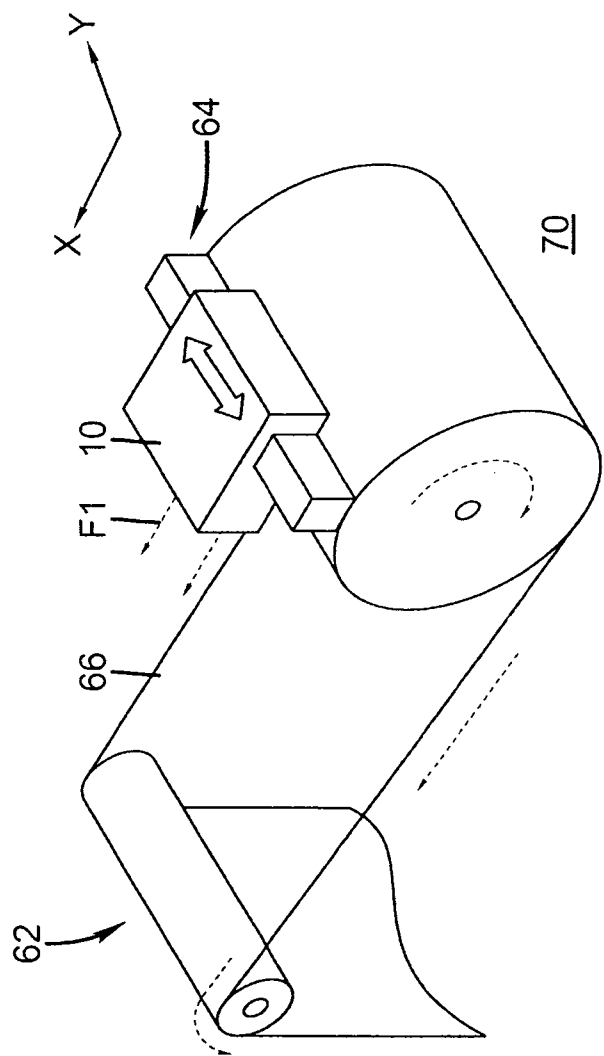


FIG. 15

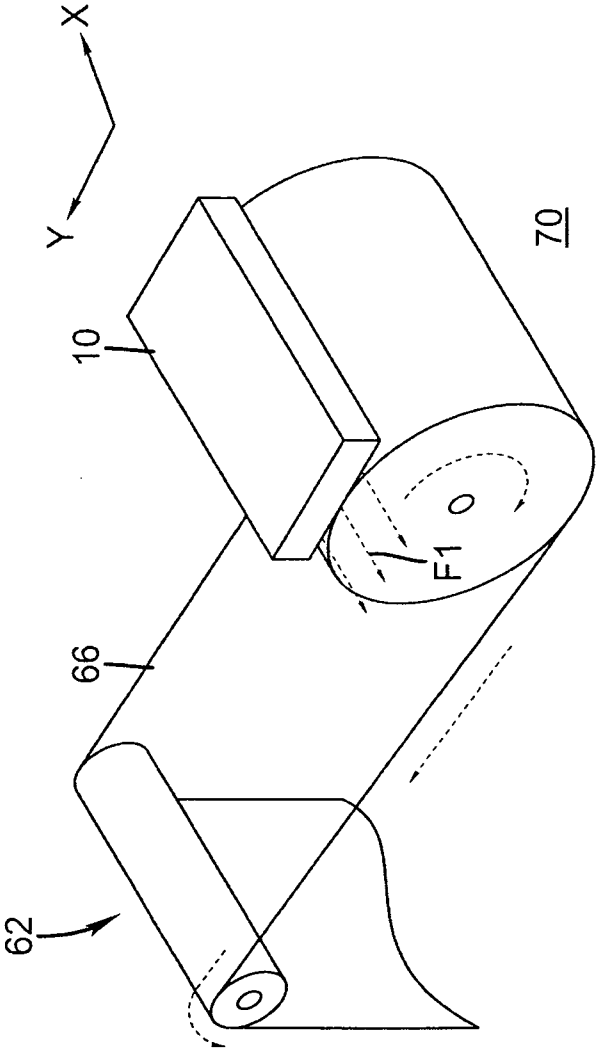


FIG. 16

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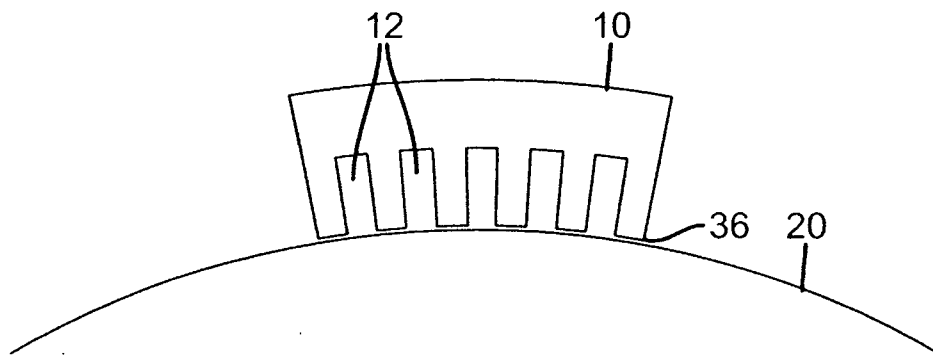
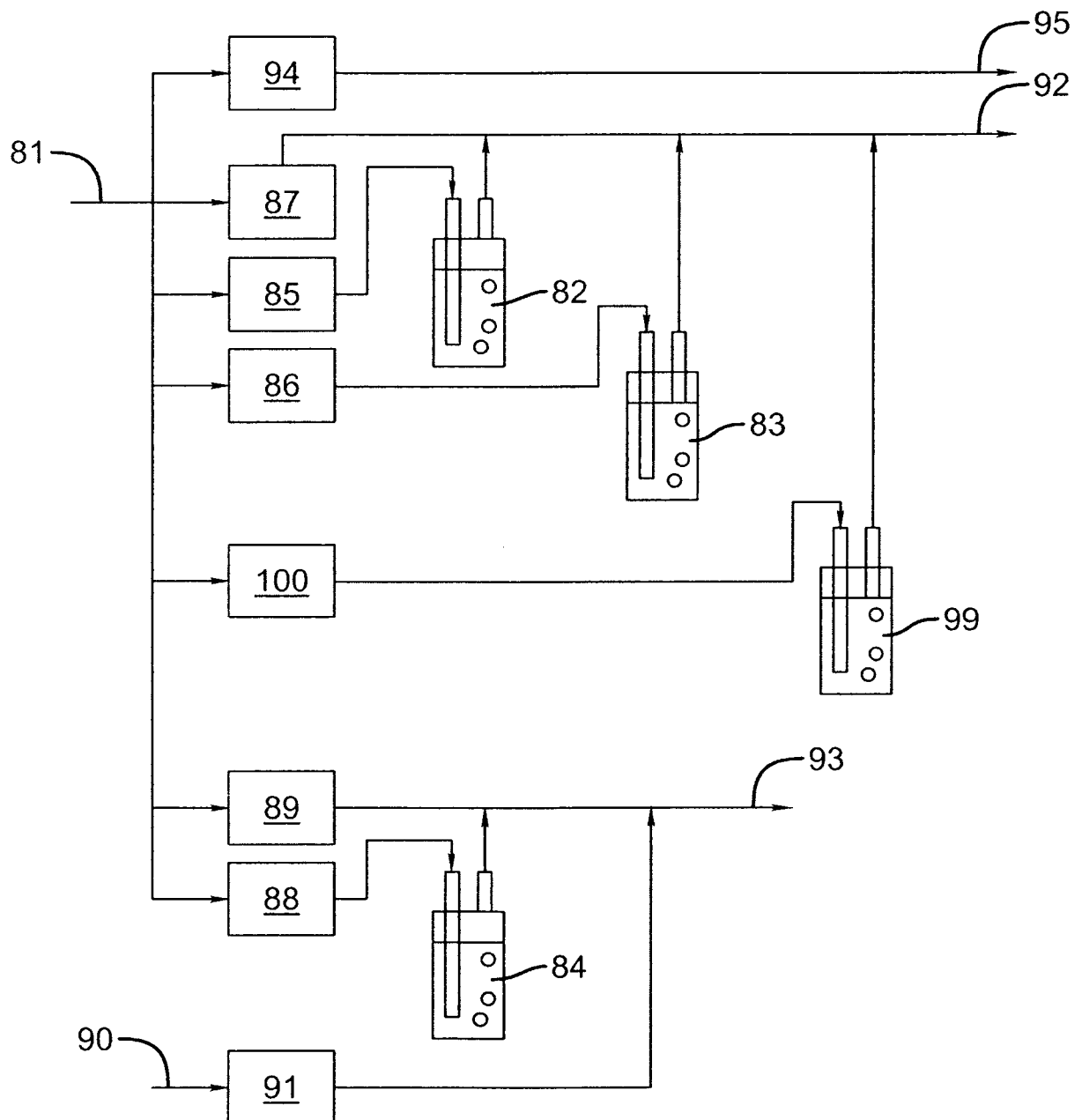


FIG. 17

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**FIG. 18**

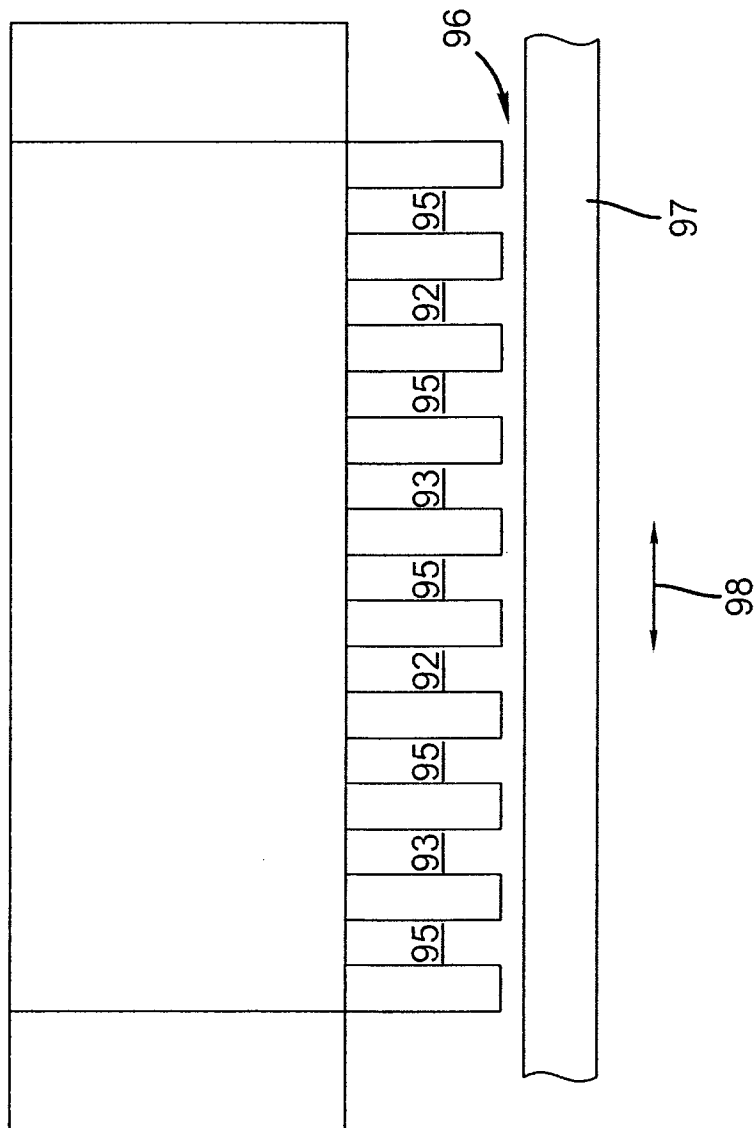


FIG. 19

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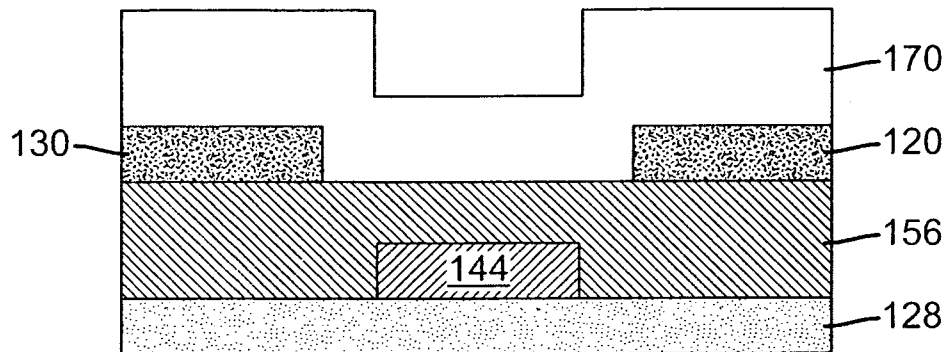


FIG. 20

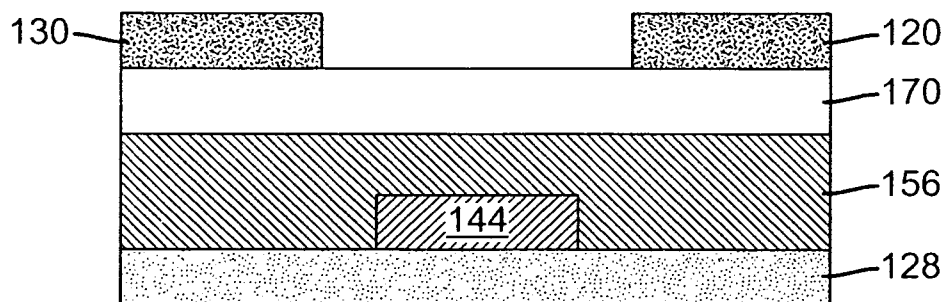


FIG. 21

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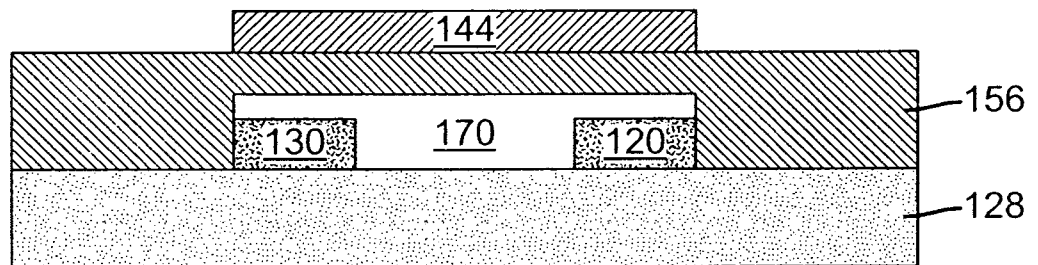


FIG. 22

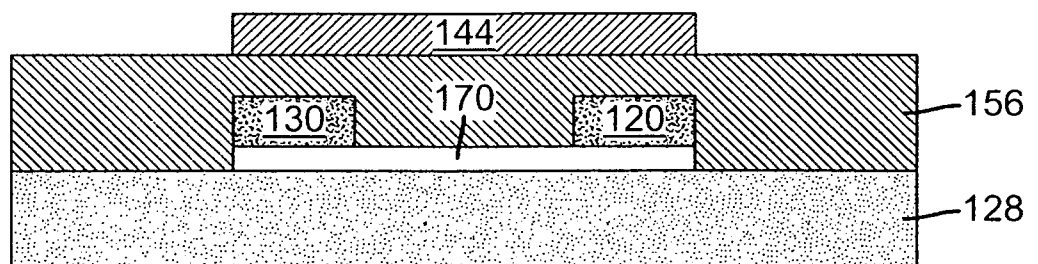
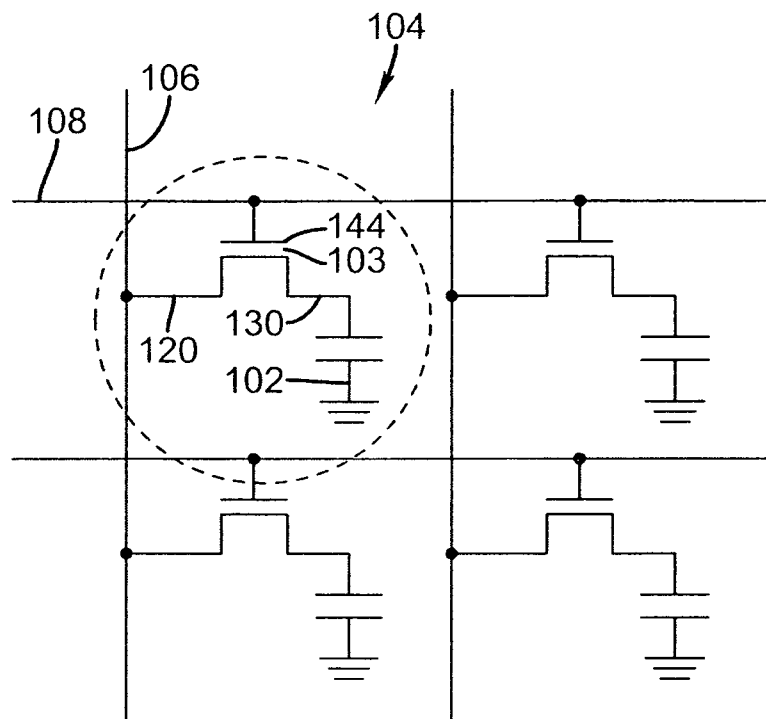


FIG. 23

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**FIG. 24**

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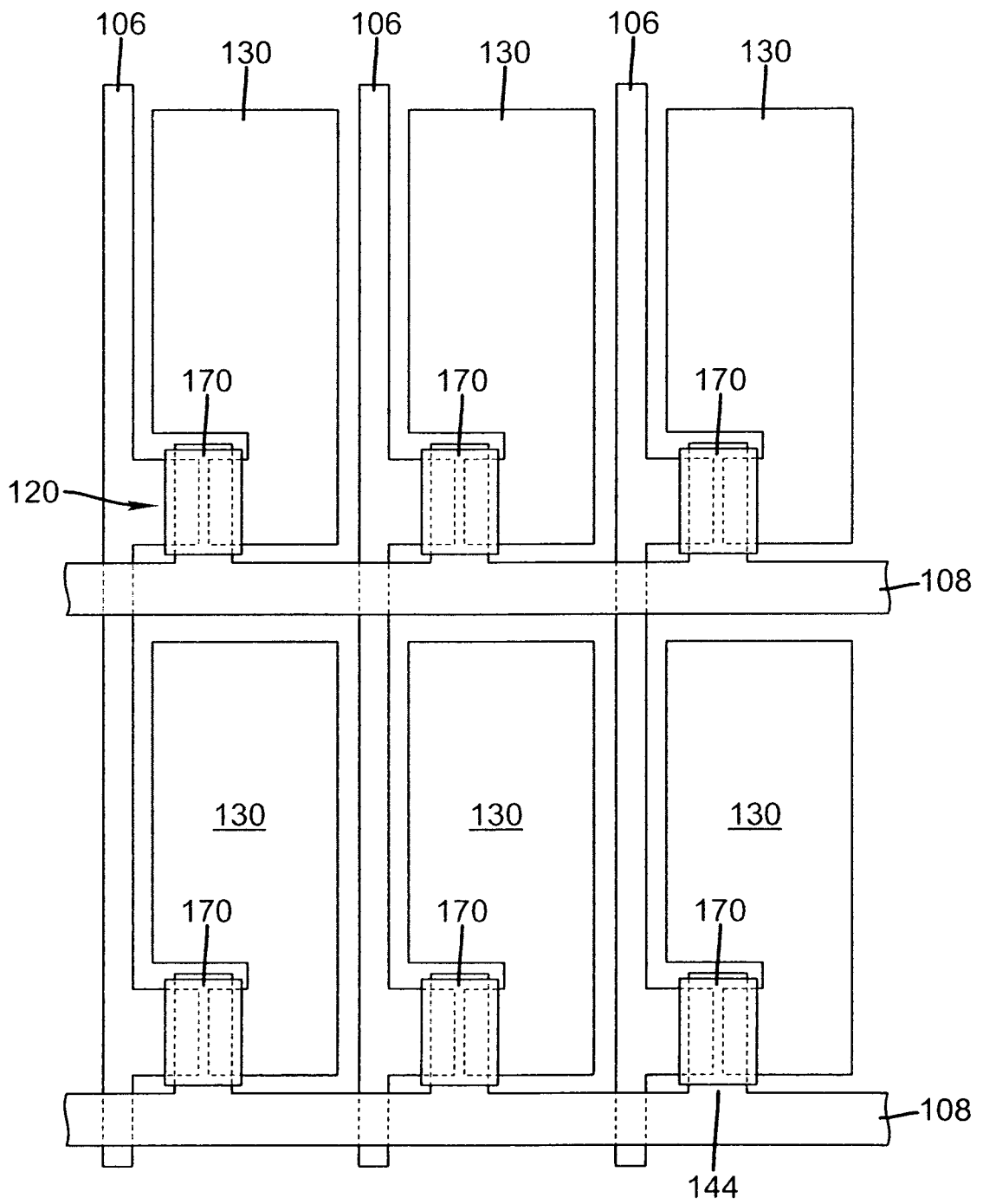
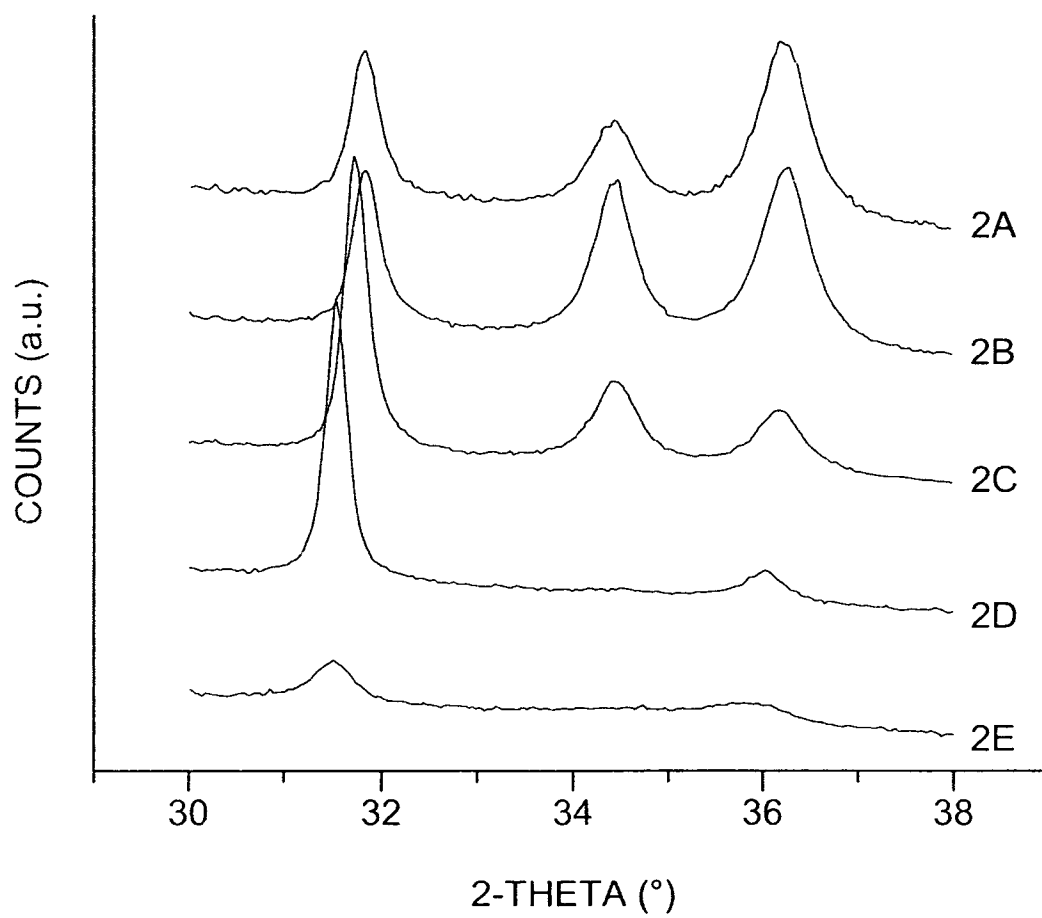
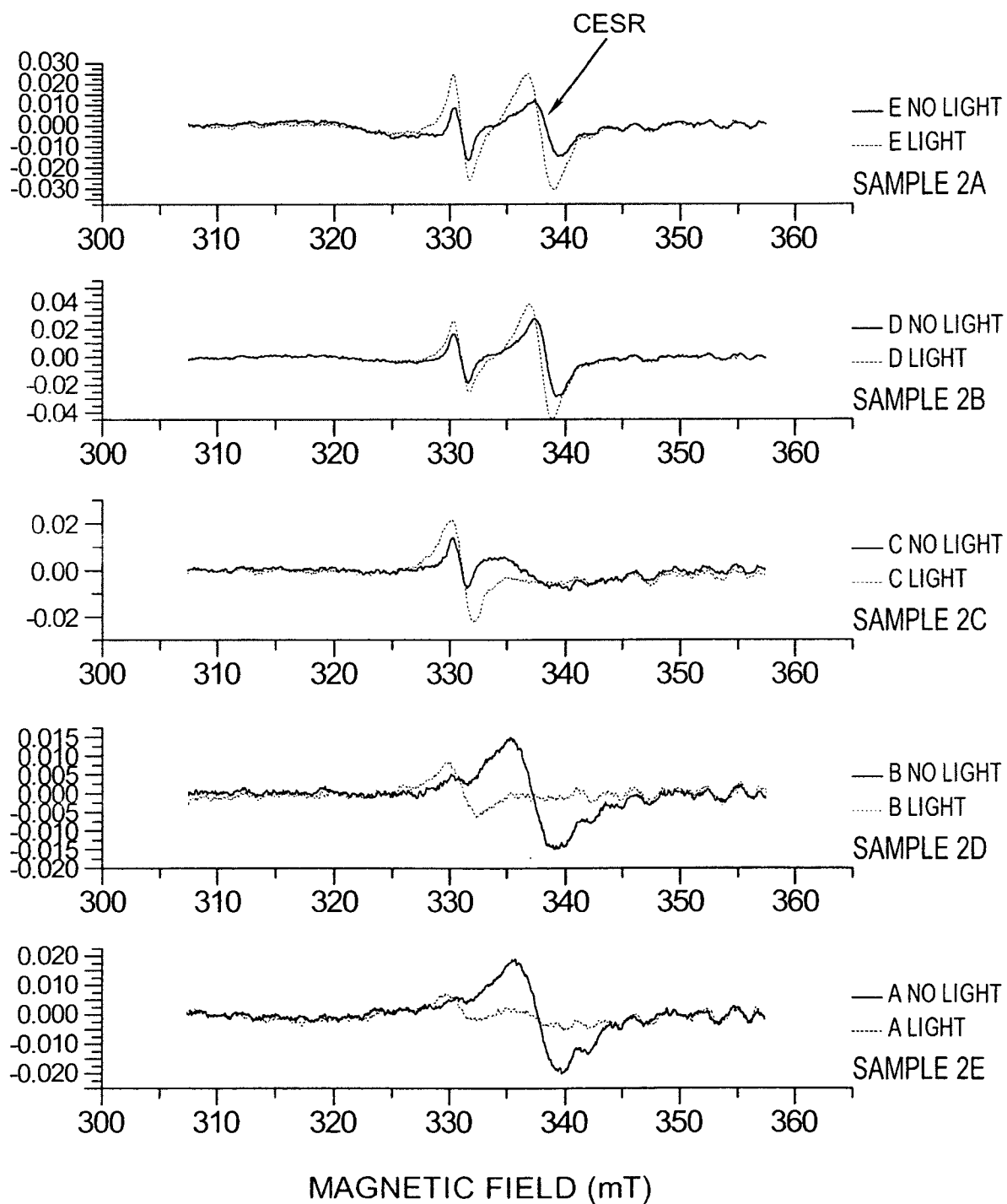


FIG. 25

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**FIG. 26**

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**FIG. 27**