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(54) Title: BANDGAP AND RECOMBINATION ENGINEERED EMITTER LAYERS FOR SI-GE HBT PERFORMANCE OPTIMIZATION

(57) Abstract: A method for fabricating a heterojunction bipolar transistor (HBT) is provided. The method includes providing a substrate including a collector region; forming a compound base region over the collector region; and forming an emitter region over the compound base region including forming a first emitter layer within the emitter region and doping the first emitter layer with a pre-determined percentage of at least one element associated with the compound base region. In one implementation, an emitter region is formed including multiple emitter layers to enhance a surface recombination surface area within the emitter region.



WO 2007/056017 A2

BANDGAP AND RECOMBINATION ENGINEERED EMITTER LAYERS FOR SI-GE HBT PERFORMANCE OPTIMIZATION

FIELD OF THE INVENTION

The present invention relates generally to heterojunction bipolar transistors (HBTs), and methods for fabricating HBTs.

5 BACKGROUND OF THE INVENTION

Bipolar transistors are important components in, for example, logic circuits, communication systems, and microwave devices. One type of bipolar transistor is a silicon germanium (SiGe) heterojunction bipolar transistor (HBT). An SiGe HBT can typically handle signals of very high frequencies, e.g., up to several hundred GHz.

10 Strained SiGe is typically the film of choice for application in NPN HBTs. The SiGe is pseudomorphically grown to match the silicon lattice beneath the SiGe and is, therefore, in a compressively strained state. Subsequent to the pseudomorphic growth process (and in the same reactor) a silicon cap layer can be grown. The silicon cap layer is conventionally doped n-type during the same process using either arsenic (As) or
15 phosphorus (P) – e.g., arsine (AsH₃) and phosphine (PH₃) are typical dopant gases. The silicon cap layer maintains the SiGe in a strained condition during thermal anneal processes.

After formation of the silicon cap layer, an emitter region is typically formed within an SiGe HBT. The emitter region typically comprises an amorphous,
20 poly-crystalline or mono-crystalline film type. The emitter region is conventionally doped with arsenic (As), phosphorus (P), or another group V element. The emitter region can further include germanium (Ge) to form a polySiGe emitter layer. Conventional SiGe HBTs with a polySiGe emitter layer, however, typically include an oxide interface (or oxide layer) that is formed between the silicon cap layer and the
25 polySiGe emitter layer.

Common device performance metrics of an SiGe HBT include a measurement of a current gain and a breakdown voltage (e.g., the collector-to-emitter breakdown (BVCE0)) associated with the SiGe HBT. Various device parameters that can affect the current gain and/or the breakdown voltage include, for example, a collector current, a
30 base current, emitter resistance, and the like. A common goal of designers is to seek new

ways to add device-tuning capability to conventional SiGe HBTs that can affect one or more of these device parameters to reduce current gains and increase breakdown voltages of an SiGe HBT.

Accordingly, what is needed are methods of material engineering that will reduce current gains and increase the breakdown voltages, e.g., the BV_{CE0} , of an SiGe HBT without adverse affect to device speed and power requirements. The present invention addresses such a need.

BRIEF SUMMARY OF THE INVENTION

In general, in one aspect, this specification describes a method for fabricating a heterojunction bipolar transistor (HBT). The method includes providing a substrate including a collector region; forming a compound base region over the collector region; and forming an emitter region over the compound base region including forming a first emitter layer within the emitter region and doping the first emitter layer with a pre-determined percentage of at least one element associated with the compound base region.

Particular implementations can include one or more of the following features. Forming a first emitter layer can further include doping the first emitter layer with a diffusion modulating impurity. Doping the first emitter layer with a diffusion modulating impurity can include doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O). Doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O) includes doping the first emitter layer such that carbon (C), nitrogen (N), fluorine (F), or oxygen (O) levels are substantially in the range of $5E17$ atoms/cc to $5E21$ atoms/cc. Forming an emitter region can further include forming one or more second emitter layers within the emitter region. Each of the first emitter layer and the one or more second emitter layers can be each doped with a different percentage of at least one element within the compound base region relative to one another. At least one of the first emitter layer and the one or more second emitter layers can include 0% of the at least one element to enhance a surface recombination surface area within the emitter region. Forming a first emitter layer can further include performing an HF last clean and a hydrogen pre-bake prior to forming the first emitter layer to create an oxide free interface between the first emitter layer and an adjacent layer. Forming a first emitter layer can include forming the first emitter layer at a temperature substantially

ranging from 550°C to 850°C.

In general, in another aspect, this specification describes a method for fabricating a heterojunction bipolar transistor (HBT) including providing a substrate including a collector region; depositing silicon germanium (SiGe) to form a base region over the collector region; and forming an emitter region over the base region including forming a first emitter layer within the emitter region and doping the first emitter layer with a pre-determined percentage of germanium (Ge).

Particular implementations can include one or more of the following features. The method can further include forming a base/collector spacer between the base region and the collector region, and forming a base/emitter spacer between the base region and the emitter region. Forming a first emitter layer can further include doping the first emitter layer with a diffusion modulating impurity. Doping the first emitter layer with a diffusion modulating impurity can include doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O). Doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O) can include doping the first emitter layer such that carbon (C), nitrogen (N), fluorine (F), or oxygen (O) levels are substantially in the range of 5×10^{17} atoms/cc to 5×10^{21} atoms/cc. Doping the first emitter layer with a pre-determined percentage of germanium (Ge) can include doping the first emitter layer such that a percentage of germanium (Ge) within the first emitter layer is substantially in the range of 0% to 65%. Forming an emitter region can further include forming one or more second emitter layers within the emitter region. Each of the first emitter layer and the one or more second emitter layers can be each doped with a different percentage of germanium (Ge) relative to one another. At least one of the first emitter layer and the one or more second emitter layers can include 0% of germanium (Ge) to enhance a surface recombination surface area within the emitter region.

In general, in another aspect, this specification describes a heterojunction bipolar transistor (HBT) including a substrate including a collector region, and a base region formed over the collector region. The base region includes silicon germanium (SiGe). The heterojunction bipolar transistor (HBT) further includes an emitter region formed over the silicon cap layer, in which the emitter region includes a first emitter layer being doped with a pre-determined percentage of germanium (Ge).

Implementations may provide one or more of the following advantages. The addition of germanium (Ge) and/or diffusion limiting impurities – e.g., carbon (C),

nitrogen (N), fluorine (F) and/or oxygen (O) – to one or more emitter layers within an emitter region of an SiGe HBT will add additional device-tuning capability to the SiGe HBT, while maintaining the benefits of conventional SiGe HBTs. The addition of germanium (Ge) to an emitter layer can reduce the rate of dopant diffusion for phosphorus (P) and increase the rate of dopant diffusion for arsenic (As). The emitter layer (including germanium (Ge)) is also formed without an oxide interface between the emitter layer and a silicon cap layer – i.e., an SiGe HBT is provided that includes an oxide-free growth interface for polySiGe emitter nucleation and growth. In addition, an SiGe HBT is provided that includes an emitter having multiple polySiGe/polySi surface recombination interfaces. The multiple polySiGe/polySi interfaces enhance a surface recombination current of the SiGe HBT due to increased surface area for recombination provided by the multiple polySiGe/polySi interfaces. Additionally, diffusion modulating impurities can be added to the emitter layer to allow engineering and control of the formation of the base-emitter metallurgical junction within an SiGe HBT.

Additionally, poly-SiGe possesses enhanced hole mobilities and activation as compared to poly-silicon, and similar electron activation and mobility for germanium (Ge) fractions up to approximately 40%. Additionally, a bandgap associated with an SiGe HBT can be tailored through control of the amount of germanium (Ge) incorporated (or doped) into the emitter region. The addition of germanium (Ge) into the emitter region further adds additional device parameter tuning to affect the collector current and base current, which also affects current gains and breakdown voltages associated with an SiGe HBT. This additional tuning capability occurs because of increased surface recombination velocity at the polySiGe/mono-silicon interface (i.e., the polySiGe/silicon cap interface).

The details of one or more implementations are set forth in the accompanying drawings and the description below. Other features and advantages will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a schematic cross-sectional view of an SiGe HBT.

FIG. 2 is a schematic cross-sectional view of the emitter region of the SiGe HBT of FIG. 1.

FIG. 3 is a flow diagram illustrating a process for fabricating an SiGe HBT.

FIGS. 4A-4F illustrate the process of fabricating an SiGe HBT according to the process of FIG. 3.

FIG. 5 illustrates a digital circuit including the SiGe HBT of FIG. 1.

Like reference symbols in the various drawings indicate like elements.

5

DETAILED DESCRIPTION OF THE INVENTION

The present invention relates generally to heterojunction bipolar transistors (HBTs), and methods for fabricating HBTs. The following description is presented to enable one of ordinary skill in the art to make and use the invention and is provided in the context of a patent application and its requirements. Various modifications to the preferred implementations and the generic principles and feature described herein will be readily apparent to those skilled in the art. Thus, the present invention is not intended to be limited to the implementations shown but is to be accorded the widest scope consistent with the principles and features described herein.

In addition, manufacturing steps are described below with enough detail to show relationships between elements of the completed device. Many fabrication details are omitted from this description, with the understanding that those skilled in the art may employ as many of those details as are called for in any particular design. Moreover, when description is given in this application of fabrication steps, those skilled in the art will realize that each such step may actually comprise one or more discrete steps and that other steps, not described herein, may be necessary to achieve specific applications of the invention.

FIG. 1 illustrates a cross-sectional view of an SiGe HBT 100. SiGe HBT 100 includes a collector region 102, a base region 104, and an emitter region composed of a plurality of emitter layers 106A-106B. Though two emitter layers are illustrated in FIG. 1, the emitter region of SiGe HBT 100 can include any number of emitter layers.

Collector region 102 is formed within a substrate 108. In one implementation, collector region 102 is n-type. Base region 104 is a compound layer that can include, e.g., p-type SiGe or SiGeC. Base region 104 can be formed as described in contemporaneously filed U.S. patent application – "Method and System For Providing a Heterojunction Bipolar Transistor Having Controlled Oxygen Incorporation" by Darwin Enicks and John Chaffee, attorney docket no. 3506P, which is incorporated by reference in its entirety.

A silicon base electrode 110 at least partially overlies base region 104, and a contact 112 connects base region 104 to silicon base electrode 110. In one implementation, base region 104 includes a base/collector spacer 114 and a base/emitter spacer 116. Base/collector spacer 114 separates base region 104 from collector region 102. Base/emitter spacer 116 separates base region 104 from the emitter region 106.

Base region 104 further includes a mono-crystalline silicon cap layer 118. Though a single silicon cap layer 118 is shown, more than one silicon cap layer can be implemented within SiGe HBT 100. In one implementation, silicon cap layer 118 is doped n-type using either arsenic (As) or phosphorus (P). Silicon cap layer 118 (and any other silicon cap layers (not shown)) can also be formed as described in contemporaneously filed U.S. patent application – "Bandgap Engineered Mono-Crystalline Silicon Cap Layers for SiGe HBT Performance Enhancement" by Darwin Enicks and Damian Carver, attorney docket no. 3508P, which is incorporated by reference in its entirety.

In one implementation, emitter layers 106A-106B of the emitter region are doped n-type. Emitter layers 106A-106B can be doped with arsenic (As), phosphorous (P), or any other group V element. Emitter layers 106A-106B are further doped to include a pre-determined amount (or percentage) of germanium (Ge). In one implementation, each emitter layer 106A-106B contains a different percentage of germanium (Ge) relative to one another (as described in greater detail below). The addition of germanium (Ge) to an emitter layer (e.g., emitter layers 106A-106B) enhances the surface recombination velocity of holes at the polySiGe/silicon cap layer interface.

Additionally, emitter layers 106A-106B can be doped with carbon (C) or oxygen (O) (or other diffusion modulating impurities such as nitrogen (N) and fluorine (F)) to tailor the base-emitter metallurgical junction profile, carrier recombination rates, surface recombination velocities at contact 112 and the emitter/silicon cap layer interface, dopant diffusion rates (through the emitter region), and dopant profiles within the emitter region.

FIG. 2 illustrates a schematic cross-sectional view of the emitter region of SiGe HBT 100 of FIG. 1, including emitter layers 106A-106n, where "n" represents an integer number. Though multiple emitter layers are shown in FIG. 2, the emitter region can include only a single emitter layer. Emitter layer 106A is formed over silicon cap layer 118. In one implementation, each emitter layer 106A-106n contains a different percentage of germanium (Ge) relative to one another. For example, as shown in FIG. 2,

emitter layer 106A is doped to contain X% of germanium (Ge), emitter layer 106B is doped to contain Y% of germanium (Ge), and emitter layer 106n is doped to contain Z% of germanium (Ge). In one implementation, the percentage of germanium (Ge) within an emitter layer 106A-106n is substantially in the range of 0% to 65%. It should be noted that by alternating emitter layers (including some percentage of germanium (Ge)) with adjacent layers of poly-Si (having 0% germanium (Ge)), the emitter resistance and recombination current due to hole recombination can be tailored. The recombination tailoring is accomplished by the addition of multiple polySiGe/poly-Si interfaces, where the surface recombination velocity is enhanced. In one implementation, the growth of the polySiGe and or poly-Si emitter layers occurs at temperatures substantially in the range of 550°C to 700°C, with gases of SiH₄, GeH₄, and an H₂ ambient.

The polySiGe/silicon cap layer interface is an oxide free interface, unlike in conventional SiGe HBTs. In one implementation, the oxide free interface between the polySiGe emitter layer and the silicon cap layer is accomplished by performing an HF last clean prior to growth of the polySiGe layer, and then (within the same process) performing a hydrogen (H₂) pre-bake at temperatures substantially at or above 600°C just before growth of the polySiGe layer. In conventional processes, temperatures greater than 900°C are typically utilized for oxide removal, however, implementing the low oxygen fabrication methods discussed below, temperatures below 900°C are effective for fabricating an SiGe HBT in accordance with the invention.

The oxide free interface avoids hot electron injection effects, which inhibits surface recombination. Hot electron injection is a tunneling phenomenon that typically occurs during tunneling of carriers through an oxide layer. In one implementation, in addition to performing an HF last clean followed by a subsequent hydrogen (H₂) pre-bake, the oxide free interface is formed through oxygen reduction methods as described in U.S. patent application – "System, Apparatus and Method for Contamination Reduction in Semiconductor Device Fabrication Equipment Components", application number 10/801,435, and in U.S. patent application – "Very Low Moisture O-Ring and Method For Preparing The Same", U.S. application publication number 20040117968, both of which are incorporated by reference herein.

FIG. 3 illustrates a process 300 of fabricating an SiGe HBT (e.g., SiGe HBT 100). Although process 300 is presented as a series of numbered steps for the purposes of clarity, no order should be inferred from the numbering.

Process 300 begins with providing a substrate including a collector region (step 302). The substrate can be a p-type substrate or an n-type substrate. In one implementation, the collector region is doped n-type. Referring to the example of FIG. 4A, an n-type substrate 400 is provided including an n-type collector region 402. An n-type silicon and/or SiGe seed layer can further be formed over collector region 402 (not shown). A base/collector spacer is deposited over the collector region (step 304). The base/collector spacer can be n-type and/or undoped SiGe. As shown in FIG. 4B, a base/collector spacer 404 is deposited over collector region 402. A compound base region is formed over the base/collector spacer (step 306). In one implementation, a p-type silicon germanium (SiGe) base region is formed. Referring to FIG. 4C, a p-type SiGe base region 406 is deposited over base/collector spacer 404. A base/emitter spacer is deposited over the SiGe base region (step 308). As with the base/collector spacer, the base/emitter spacer can be n-type and/or undoped SiGe. A base/emitter spacer 408 is deposited over SiGe base region 406 (FIG. 4D).

A mono-crystalline silicon cap layer is formed over the base/emitter spacer (step 310). In one implementation, an n-type region of the silicon cap layer is doped (in-situ) with phosphorus (P) or Arsenic (A). Accordingly, as shown in FIG. 4E, a silicon cap layer 410 is formed over base/emitter spacer 408.

An emitter region is formed, including one or more emitter layers, over the silicon cap layer (step 312). In one implementation, each emitter layer is formed with process temperatures substantially ranging from 550°C to 850°C. Each emitter layer can be doped (in-situ) with phosphorus (P) or arsenic (A), during chemical vapor deposition (CVD) or through ion implantation. In one implementation, arsenic (A) and/or phosphorus (P) doping levels are substantially in the range of 5×10^{17} atoms/cc to 5×10^{21} atoms/cc. Each emitter layer can also be doped (in-situ) during chemical vapor deposition (CVD) or through ion implantation with diffusion modulating impurities, e.g., carbon (C) or oxygen (O). In one implementation, carbon and/or oxygen levels are substantially in the range of 5×10^{17} atoms/cc to 5×10^{21} atoms/cc. As discussed above, the percentage of germanium (Ge) within an emitter layer is substantially in the range of 0% to 65%. In one implementation, 0% germanium is used within an emitter layer where a poly-Si (emitter) layers are desired in order to create multiple "surface recombination layers" (as discussed above) to enhance hole current. Further, doping profiles within each emitter layer can be graded for optimum device parameter control.

Gas sources that can be used during the growth process of an emitter layer include: SiH_4 – silicon source, GeH_4 – germanium source, CH_3SiH_3 – carbon source, AsH_3 – arsenic source, PH_3 – phosphorus source, and hydrogen or helium can be used as the carrier gas. Accordingly, as shown in FIG. 4E, an emitter region is formed including emitter layers 412A-412B over silicon cap layer 410.

An SiGe HBT according to the present invention (e.g., SiGe HBT 100) can be implemented within any type of digital circuit – e.g., digital circuit 500 as shown in FIG. 5. Digital circuit 500 can be associated with one or more of microcontrollers, memories, logic circuits, radio frequency (RF) components, sensors, communication systems, microwave devices, and the like.

Various implementations for fabricating an SiGe HBT have been described. Nevertheless, one of ordinary skill in the art will readily recognize that there that various modifications may be made to the implementations, and any variation would be within the spirit and scope of the present invention. For example, as discussed above, poly-Si emitter layers (having 0% germanium (Ge)) can be sandwiched between polySiGe emitter layers to further enhance surface recombination. Additionally, emitter layers in accordance with the invention can be formed according to methods disclosed in contemporaneously filed U.S. patent application – "A Semiconductive Film With Dopant Diffusion Barrier and Tunable Work Function" by Darwin Enicks, which is incorporated by reference herein. Accordingly, many modifications may be made by one of ordinary skill in the art without departing from the spirit and scope of the following claims.

CLAIMS

We Claim:

1. A method for fabricating a heterojunction bipolar transistor (HBT), the method comprising:

providing a substrate including a collector region;

forming a compound base region over the collector region; and

5 forming an emitter region over the compound base region including forming a first emitter layer within the emitter region and doping the first emitter layer with a pre-determined percentage of at least one element associated with the compound base region.

10 2. The method of claim 1, wherein forming a first emitter layer further includes doping the first emitter layer with a diffusion modulating impurity.

3. The method of claim 2, wherein doping the first emitter layer with a diffusion modulating impurity includes doping the first emitter layer with carbon (C),
15 nitrogen (N), fluorine (F), or oxygen (O).

4. The method of claim 3, wherein doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O) includes doping the first emitter layer such that carbon (C), nitrogen (N), fluorine (F), or oxygen (O) levels are substantially in the
20 range of $5E17$ atoms/cc to $5E21$ atoms/cc.

5. The method of claim 1, wherein forming an emitter region further includes forming one or more second emitter layers within the emitter region, wherein each of the first emitter layer and the one or more second emitter layers are each doped
25 with a different percentage of at least one element within the compound base region relative to one another.

6. The method of claim 5, wherein at least one of the first emitter layer and the one or more second emitter layers includes 0% of the at least one element to enhance
30 a surface recombination surface area within the emitter region.

7. The method of claim 1, wherein forming a first emitter layer further includes performing an HF last clean and a hydrogen pre-bake prior to forming the first emitter layer to create an oxide free interface between the first emitter layer and an adjacent layer.

5

8. The method of claim 1, wherein forming a first emitter layer includes forming the first emitter layer at a temperature substantially ranging from 550°C to 850°C.

10

9. A method for fabricating a heterojunction bipolar transistor (HBT), the method comprising:

providing a substrate including a collector region;

depositing silicon germanium (SiGe) to form a base region over the collector region; and

15

forming an emitter region over the base region including forming a first emitter layer within the emitter region and doping the first emitter layer with a pre-determined percentage of germanium (Ge).

20

10. The method of claim 9, further comprising:

forming a base/collector spacer between the base region and the collector region;

and

forming a base/emitter spacer between the base region and the emitter region.

25

11. The method of claim 9, wherein forming a first emitter layer further includes doping the first emitter layer with a diffusion modulating impurity.

30

12. The method of claim 11, wherein doping the first emitter layer with a diffusion modulating impurity includes doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O).

13. The method of claim 12, wherein doping the first emitter layer with carbon (C), nitrogen (N), fluorine (F), or oxygen (O) includes doping the first emitter layer such that carbon (C), nitrogen (N), fluorine (F), or oxygen (O) levels are

substantially in the range of 5×10^{17} atoms/cc to 5×10^{21} atoms/cc.

14. The method of claim 9, wherein doping the first emitter layer with a pre-determined percentage of germanium (Ge) includes doping the first emitter layer such that a percentage of germanium (Ge) within the first emitter layer is substantially in the range of 0% to 65%.

15. The method of claim 9, wherein forming an emitter region further includes forming one or more second emitter layers within the emitter region, wherein each of the first emitter layer and the one or more second emitter layers are each doped with a different percentage of germanium (Ge) relative to one another.

16. The method of claim 15, wherein at least one of the first emitter layer and the one or more second emitter layers includes 0% of germanium (Ge) to enhance a surface recombination surface area within the emitter region.

17. A heterojunction bipolar transistor (HBT) comprising:
a substrate including a collector region;
a base region formed over the collector region, the base region including silicon germanium (SiGe); and
an emitter region formed over the silicon cap layer, the emitter region including a first emitter layer being doped with a pre-determined percentage of germanium (Ge).

18. The transistor of claim 17, further comprising:
a base/collector spacer formed between the base region and the collector region;
and
a base/emitter spacer formed between the base region and the emitter region.

19. The transistor of claim 17, wherein the first emitter layer is doped with a diffusion modulating impurity.

20. The transistor of claim 19, wherein the diffusion modulating impurity includes carbon (C), nitrogen (N), fluorine (F), or oxygen (O), wherein a level of the

carbon (C), nitrogen (N), fluorine (F), or oxygen (O) is substantially in the range of 5×10^{17} atoms/cc to 5×10^{21} atoms/cc..

21. The transistor of claim 17, wherein the emitter region further includes one or more second emitter layers, wherein each of the first emitter layer and the one or more second emitter layers are each doped with a different percentage of germanium (Ge) relative to one another.

22. A digital circuit including the transistor of claim 17.

23. The digital circuit of claim 22, wherein the digital circuit comprises digital circuitry associated with one or more of a microcontroller, memory, logic circuit, radio frequency (RF) component, sensor, communication system, or microwave device.

1/5

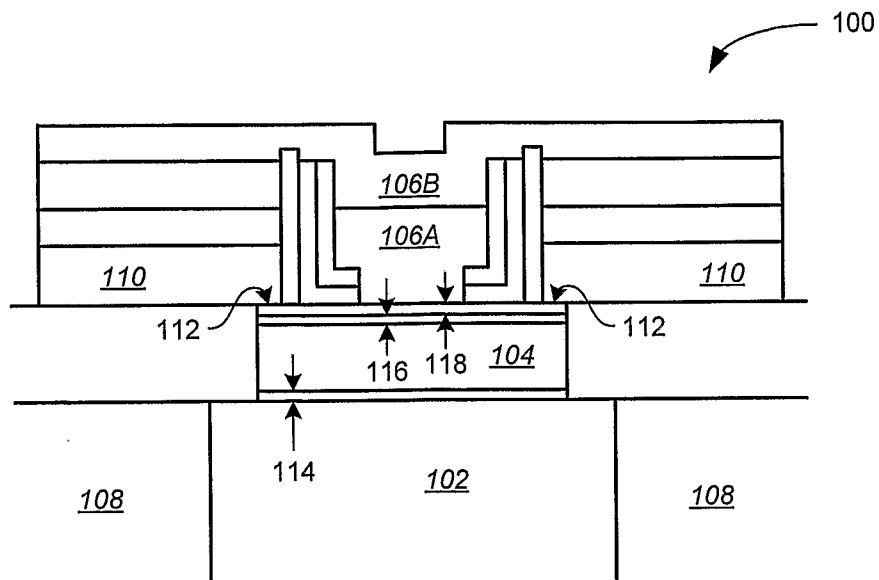


FIG. 1

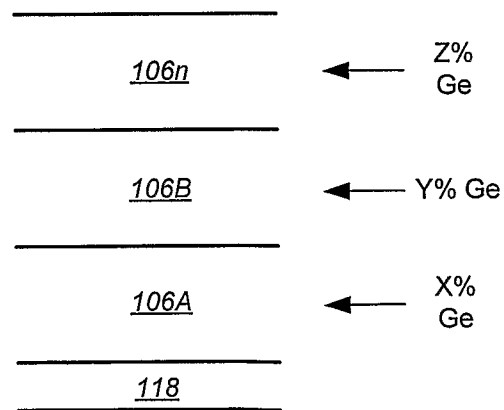
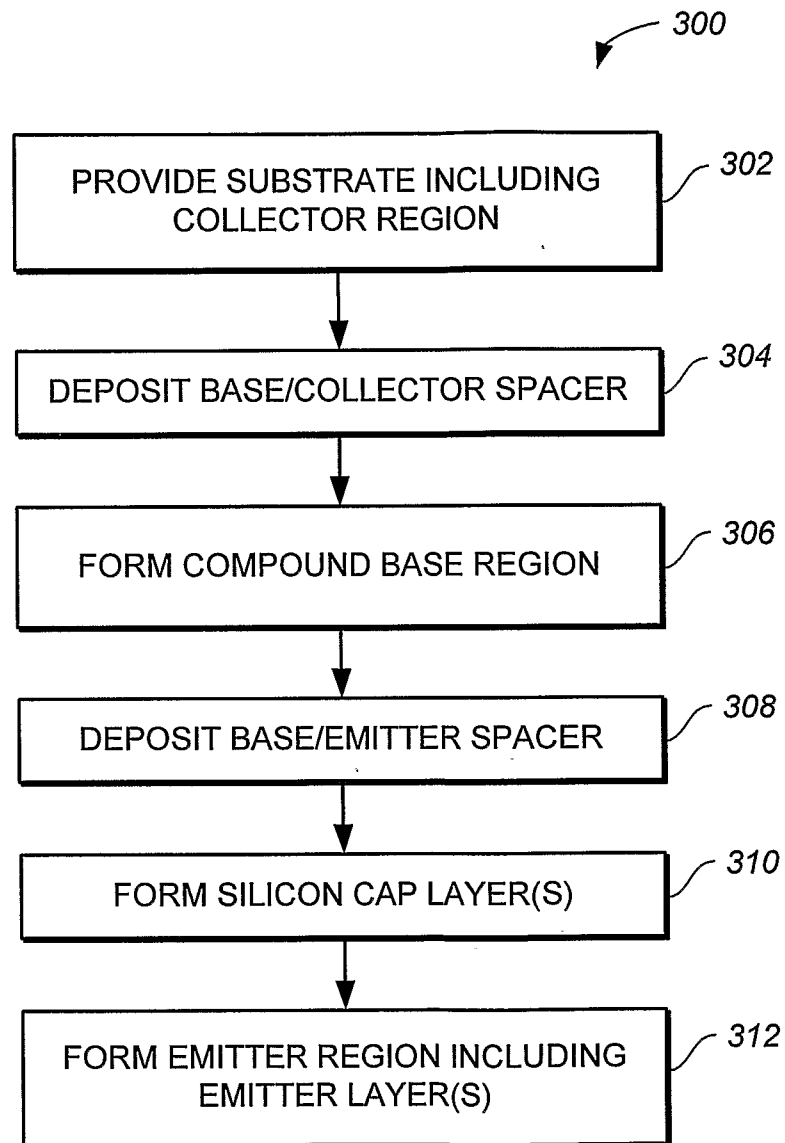


FIG. 2

2/5

**FIG. 3**

3/5

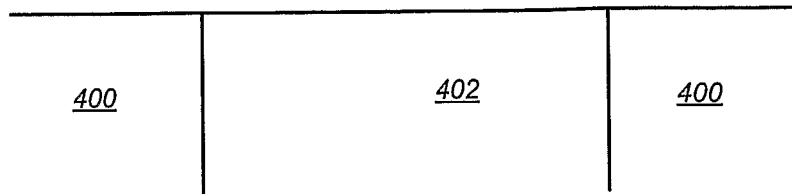


FIG. 4A

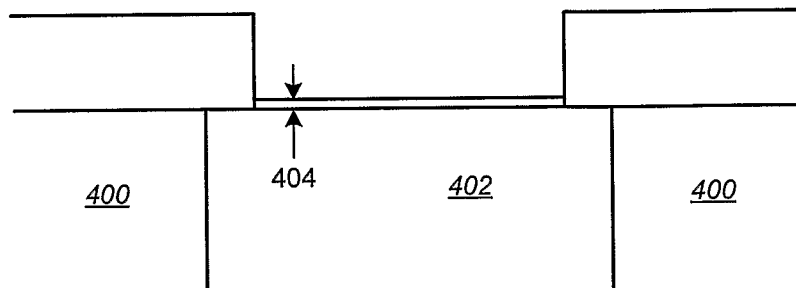


FIG. 4B

4/5

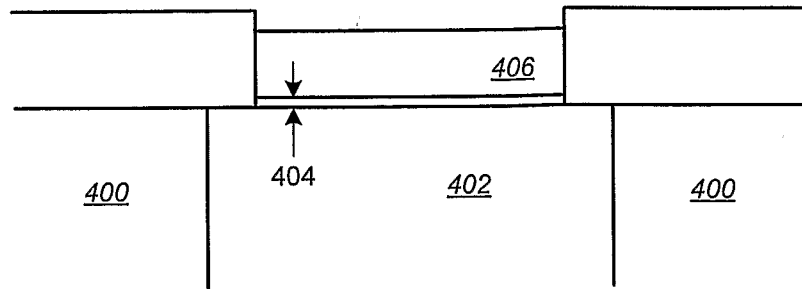


FIG. 4C

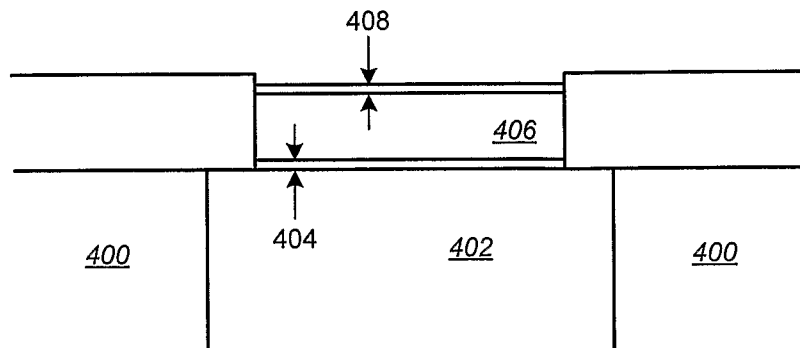


FIG. 4D

5/5

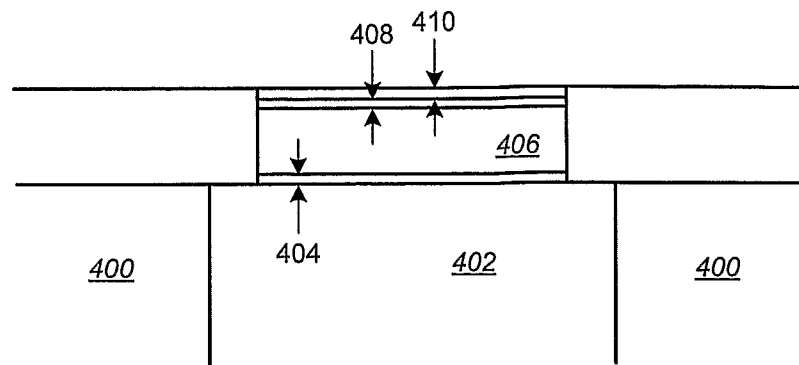


FIG. 4E

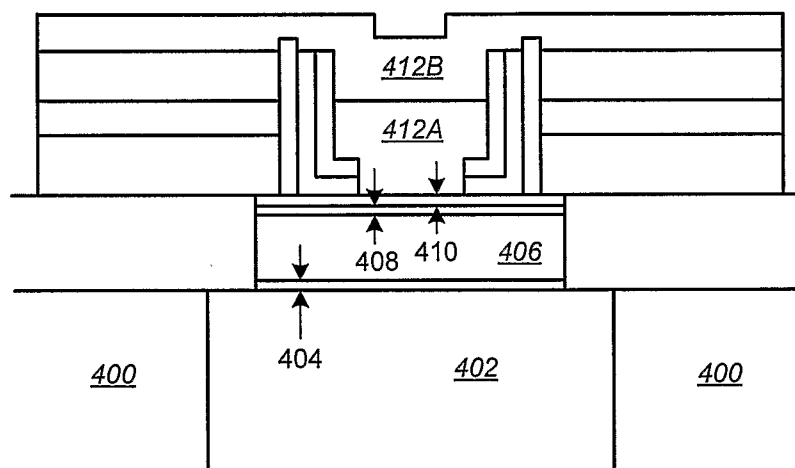


FIG. 4F

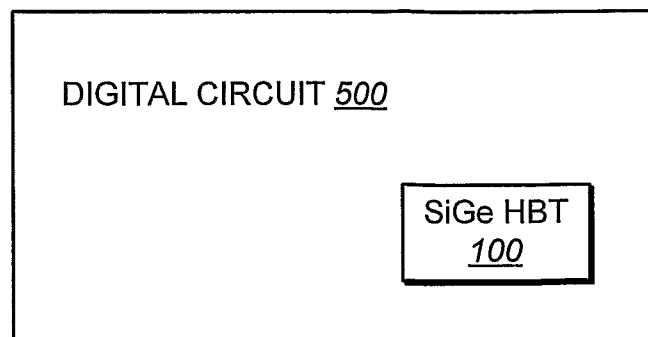


FIG. 5