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(54) **CHEMICAL MECHANICAL POLISHING METHOD AND APPARATUS**

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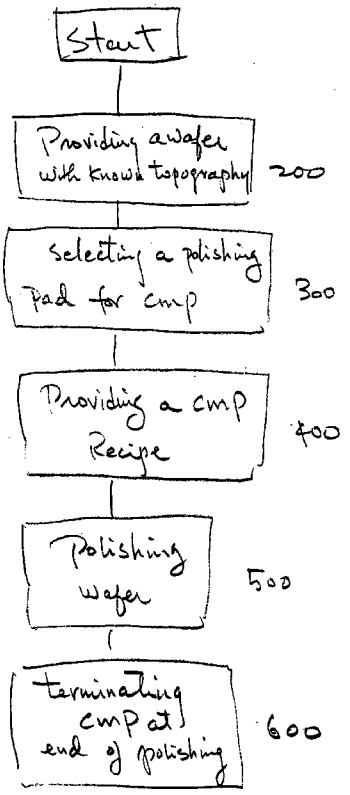
(57) **ABSTRACT**

A method for removing material from the surface of a semiconductor wafer with a chemical mechanical polishing process is described. The method uses a polishing pad on which a line-pattern of grooves is formed. The pattern comprises orderly spaced grooved-area and area without grooves. The method combines information of the surface topography of the wafer, the nature of the material to be removed, and the available groove pattern on the surface of the polishing pad to generate a process recipe in which the resident time of portions of the semiconductor wafer spends at the grooved and un-grooved areas of the polishing pad during the chemical mechanical polishing process is pre-determined.



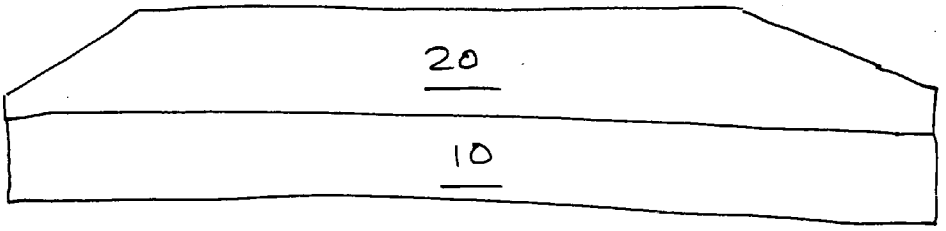


Fig. 1

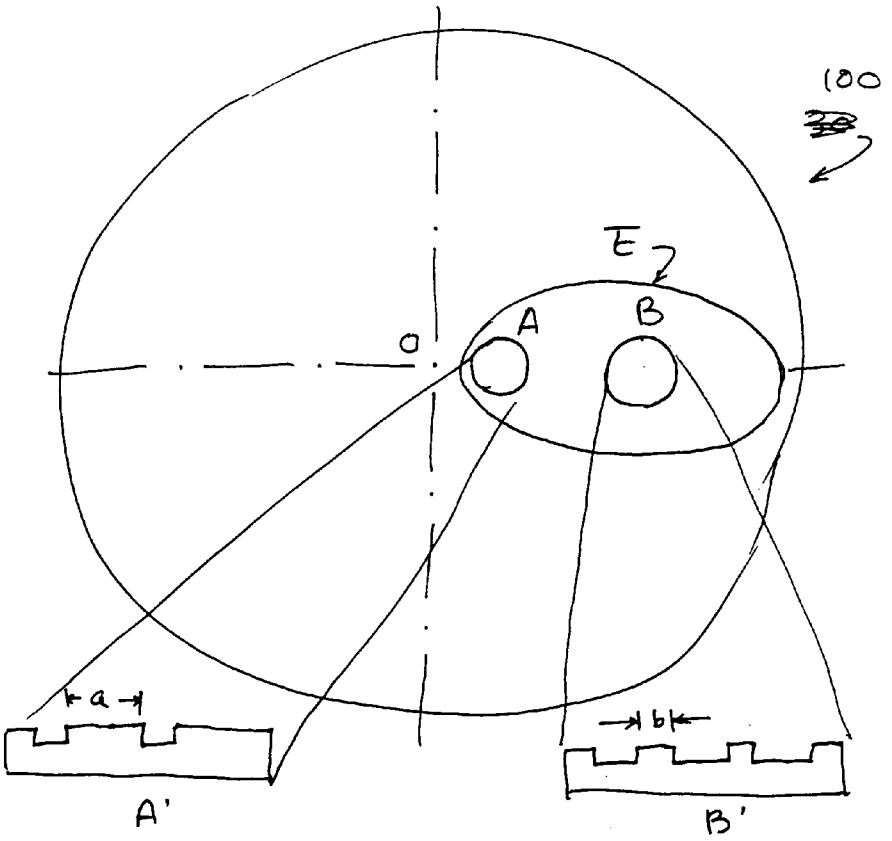


Fig. 2

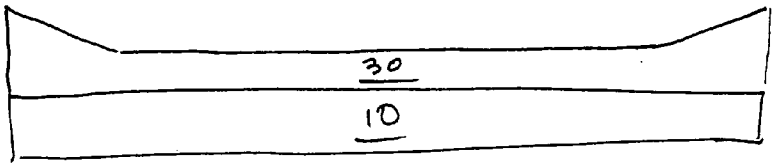


Fig. 3

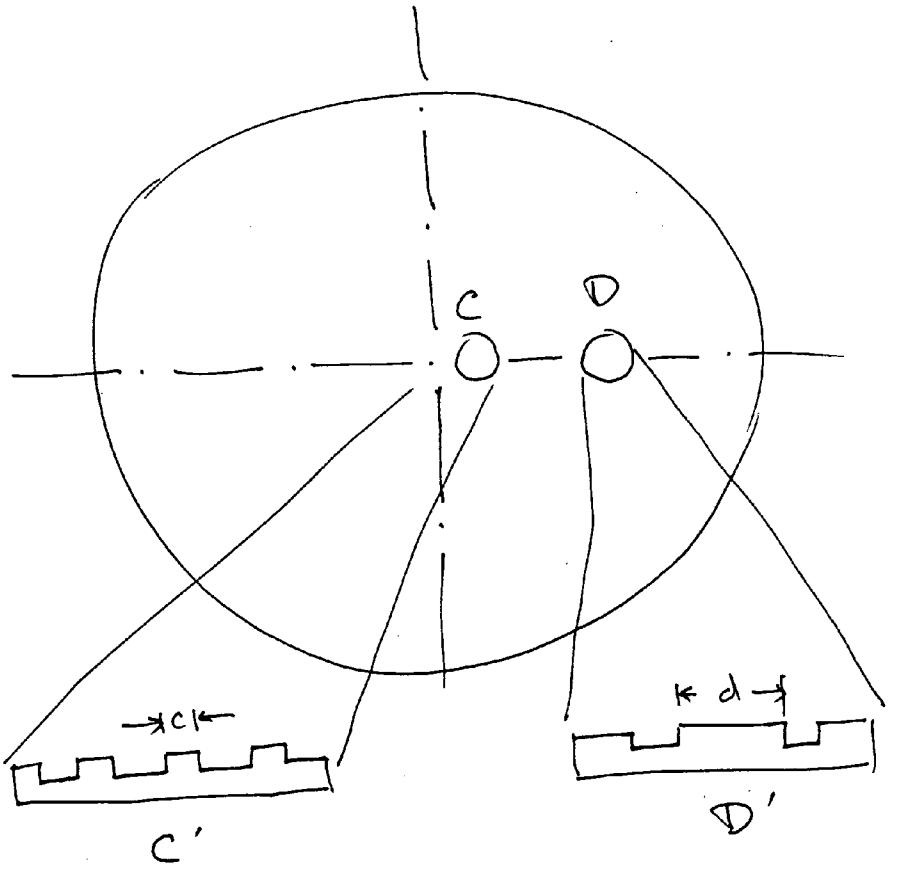


Fig 4

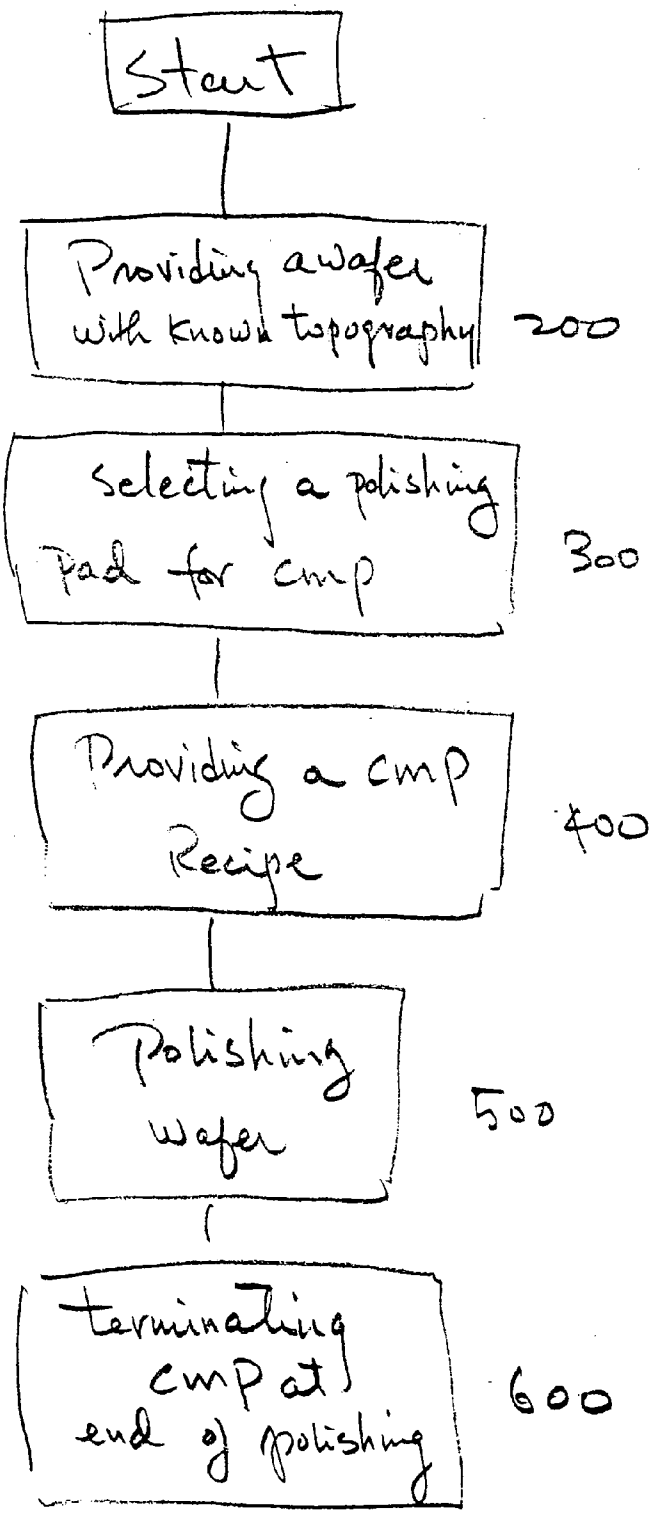

Start
Providing a wafer with known topography
200
Selecting a polishing pad for cmp
300
Providing a cmp Recipe
400
Polishing wafer
500
terminating cmp at end of polishing
600

Fig. 5

CHEMICAL MECHANICAL POLISHING METHOD AND APPARATUS

[0001] This is a continuation of application Ser. No. 10/697,676 **[text missing or illegible when filed]** which is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] This invention relates to semiconductor processing, particularly to a chemical mechanical polishing method and apparatus with which to achieve superior global and local wafer planarity control.

[0003] Modern integrated-circuit technology is capable of packing a large number of circuit-components at near the surface of a semiconductor wafer by scaling down the feature size of the circuit-components and connects the components with a large number of metal lines imbedded in a matrix of multiple layers of metal and dielectric material. Beneath the silicon wafer surface, the circuit-elements are isolated from each other by regions of silicon dioxide in shallow trenches to prevent unwanted electrical current passage between the circuit-elements.

[0004] Because of the downward scaling of the feature size and the increasing complexity of interconnecting scheme, the wafer process requires a high degree of wafer surface planarization. Specifically, the wafer surface must be planarized locally as well as globally after the formation of the shallow trenches and at all interconnect levels. Currently the technique of chemical mechanical polishing is the only satisfactory technique with which the necessary degree of planarization can be achieved.

[0005] In a chemical mechanical polishing operation, a semiconductor wafer is mounted upside down on a wafer-carrier, and the carrier is pressed downward against a polishing pad, which is motion with respect to the rotating wafer-carrier. Slurry comprised of silica or cerium oxide particles, for example, suspended in alkaline to slightly acid solution drips onto the polishing pad that has flow channels machined to transport the slurry beneath the rotating wafer carrier where it polishes the wafer surface.

[0006] The most popular type of chemical mechanical polisher is the rotary polisher in which both a platen and the wafer-carrier rotate. The carrier holds the wafer face down, and applies a downward force against the surface of the pad. The pad is mounted on a rotating platen by waterproof adhesive. The wafer-carrier rotates about the center point of the wafer and it oscillates along a radius of the platen such that the entire wafer surface contacts the polishing pad during the polishing operation.

[0007] Some types of the polishing pads are made of materials that absorb the slurry; other types are made of materials that do not have the ability to absorb the slurry.

[0008] The rate of removal of the target material is a function of the pressure that the pad exerts on the wafer surface, the relative speed between the pad and the wafer surface, and the nature of the slurry.

BRIEF DESCRIPTION OF DRAWINGS

[0009] **FIG. 1** depicts a cross section of a semiconductor wafer.

[0010] **FIG. 2** depicts a polishing pad with a flow-channel pattern of the present invention.

[0011] **FIG. 3** depicts a cross section of another semiconductor wafer.

[0012] **FIG. 4** depicts another polishing pad with a flow-channel pattern of the present invention.

[0013] **FIG. 5** depicts a flowchart of a chemical mechanical polishing process of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

[0014] The applicants recognize that with today's rotary chemical mechanical polisher, different portions of the wafer experience different relative speed with respect to the polishing pad during the polishing operation. The applicants also recognize that different processes that deposit the target material on the wafer surface may effects different built-in non-planarity on the wafer surface. In certain instances, the target material coating on the wafer may be thicker at the center while in other instances the coating is thicker at the edges.

[0015] The applicants further recognize that the rate of removing the target material depends on the presence of the slurry at the point where the wafer contacts the polishing pad. With a polishing pad made of material such as polyurethane, polycarbonate, nylon, acrylic polymer, or polyester, the slurry is transported to the contact point by the flow channels machined onto the polishing pad. Therefore, the rate of target material removal is a function of the dimension and density of the flow channels—a wafer gliding over an area on the polishing pad that has more densely placed flow channels will have more of the target material removed than over an area that has more sparsely placed flow channels.

[0016] Therefore, the applicants discovered that with a properly designed flow-channel pattern, desired planarity can be achieved even when the surface topography of the target material as formed is highly non-planar. The following exemplary embodiments are for the purpose of describing this invention.

[0017] **FIG. 1** depicts the cross-section view of a silicon wafer **10** with a deposited layer of silicon dioxide **20**. The dioxide layer may be formed following the formation of shallow trench isolation.

[0018] In **FIG. 1**, the silicon dioxide layer **20** is outwardly tapered—its thickness at the center of the wafer is greater than at the edge of the wafer. In order to compensate for this outward-tapering, it is advantageous to use a polishing pad that has a pattern of flow channels as depicted in **FIG. 2**.

[0019] **FIG. 2** depicts a polishing pad **100**, which may be made of material such as polyurethane. **FIG. 2** also depicts two areas A and B of the polishing pad and the enlargements A' and B' of the two areas, and the flow channels in the areas. Note that the spacing between the flow channels in area A is 'a' and the spacing between the flow channels in area B is 'b'. To polish an outwardly tapered wafer, the more favorable flow-channel pattern for polishing pad should be such that 'a' is wider than 'b'—in some cases, area A may be free of any flow-channels. It is applicants' observation that during the polishing operation, the wafer and the wafer carrier oscillates along a line OP while rotating. As a result,

the edge of the wafer travels along the edge of an ellipse E while the center portion of the wafer is confined in the interior of the ellipse E. A flow channel pattern such as depicted in **FIG. 2** will achieve a polishing rate lower at the edge of the wafer because of the more sparsely spaced flow channels at the location A.

[**0020**] **FIG. 3** depicts the cross-section view of another silicon wafer **30** with a layer **40** coated on the top surface. In this case, the layer **40** is inwardly tapered so that it is thinner at the center than at the edge of the wafer. Layer **30** may be deposited on the silicon with a spin-on process. In order to compensate for inward-tapering, it is advantageous to use a polishing pad that has a pattern of flow channels as depicted in **FIG. 4**.

[**0021**] **FIG. 4** depicts another polishing pad and two areas C and D on the polishing pad. Also depicted in **FIG. 4** are the enlargements C' and D' of the two areas and the flow channels in the areas. The spacing between the flow channels in area C is 'c' and the spacing between the flow-channels in area D is 'd'. To polish an inwardly-tapering wafer, the more favorable flow-channel pattern should be such that 'd' is wider than 'c'—in some cases D may be free of any flow-channels. A polishing pad having a flow-channel pattern as depicted in **FIG. 4** removes the target material more slowly at the center of the wafer because of the more sparsely spaced flow-channels.

[**0022**] **FIG. 5** is a flowchart for a chemical mechanical polishing process of the present invention. The process starts by providing a wafer having a coating of target material with a known surface topography to be polished **200**. This topography may be ascertained by scanning the top surface of each wafer or by sample-scanning a representative wafer in a wafer-lot. As explained earlier, the topography of the coating is generally a function of how the coating is formed and the nature of the coating material. In case of a spin-on film such as a spin-on-glass, the film tends to be inwardly tapered as the spun-on material gets pushed outwardly by the centrifugal force of spinning operation to the edge of the wafer. In case of electro-plating, the location of the electrode and the current path in the wafer surface may cause the film to be outwardly tapered.

[**0023**] The next step is to select a polishing pad of a proper flow-channel pattern **300**. As explained in the previous paragraphs, for a given relative polishing speed, an area of denser flow-channel usually removes target material at a higher rate.

[**0024**] The next step is to provide a recipe for the CMP operation **400**. The recipe may include the rotational speed for the platen—polishing pad and the rotational speed for the wafer-carrier, the frequency of the wafer carrier oscillating along a radius of the platen, the slurry feeding rate, and endpoint detection data or a predetermined polishing time.

[**0025**] The next step is the actual polishing **500** of the wafer according to the recipe **400**. When the predetermined polishing time is reached or when the endpoint detection mechanism triggers, the CMP operation is terminated **600**.

[**0026**] The present invention may be applied to semiconductor wafer other than silicon. For example, the CMP method is applicable on compound semiconductor material. It is applicable on SiGe material. The target film may comprise other material such as silicon, tungsten or copper. The flow-channel may be of more than one width and one depth.

1-13. (canceled)

14. A method for removing a predetermined amount of a material from a surface of a semiconductor wafer, comprising the steps of:

a. providing a semiconductor wafer having a top surface and a substantially flat bottom surface, the top surface having a center portion and a edge portion;

b. providing a chemical-mechanical-polishing (CMP) apparatus including a polishing pad that has a polishing surface and a backing surface, the backing surface attaching to a platen, the polishing surface having a center point, an edge, and a plurality of regions radially distant from the center point and patterned with slurry channels of various densities;

c. providing a CMP recipe for polishing the top surface of the semiconductor wafer on the polishing surface such that the edge portion of the wafer comes in contact with each of the plurality of regions of the polishing surface;

d. commencing the polishing process based on the process recipe;

and

e. terminating the polishing process when the predetermined amount of material is removed from the top surface of the semiconductor wafer.

15. The method of claim 14, in which a region on the polishing surface having a high density of slurry channels situates approximately half-way between the center point and the edge.

16. The method of claim 14, in which a region on the polishing surface having a low density of slurry channels situates adjacent the center point.

17. The method of claim 16, in which the region adjacent the center point has zero density of slurry channels.

18. The method of claim 14, in which a region on the polishing surface having a low density of slurry channels situates adjacent the edge.

19. The method of claim 18, in which the region adjacent the edge point has zero density of slurry channels.

20. The method of claim 14, in which the slurry channels are con-centric rings.

21. The method of claim 14, in which the slurry channels are spiral.

22. The method of claim 14, in which the slurry channels are con-centric rings.

23. The method of claim 20, in which the rings are evenly spaced in each region.

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