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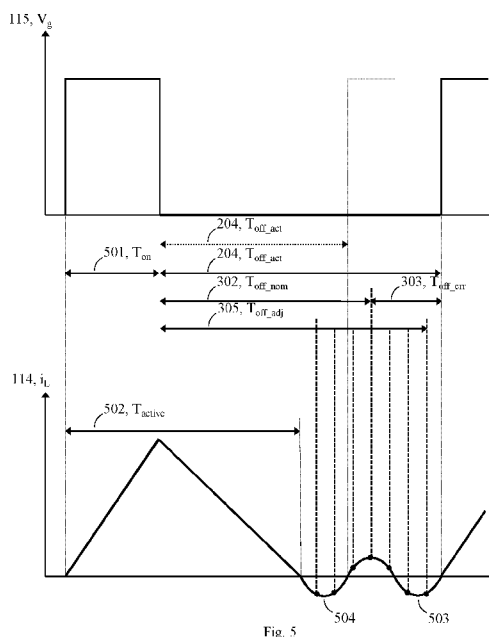


Fig. 5

(57) Abstract: A converter (1) for operating an LED load is provided. The converter (1) comprises an actively switched power factor correction, PEC, circuitry (104-112), having a control circuitry (2-4) for controlling a switch (105) of the PEC circuitry (104-112). The control circuitry (2-4) is configured to control a switch-on timing of the switch (105) such that an output voltage (113, V_{bus}) of the PEC circuitry (104-112) is feedback-controlled in accordance with a nominal value (201). In a discontinuous conduction mode, DCM, the control circuitry (2-4) is configured to control an actual value (204, T_{off_act}) of the switch-on timing of the switch (105) in one or more switching cycles to be a time of a valley of a voltage across the switch (105) succeeding a nominal value (302, T_{off_nom}) of the switch-on timing of a control algorithm implemented by the control circuitry (2-4).

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The control circuitry (2-4) is further configured to control the actual value (204, T_{off_act}) of the switch-on timing of the switch (105) in one or more subsequent switching cycles being subsequent to the one or more switching cycles to be a time of a valley of the voltage across the switch (105) preceding the nominal value (302, T_{off_nom}) of the switch-on timing. This reconciles valley switching and avoidance of visible light flicker.

CONVERTER FOR OPERATING AN LED LOAD, AND LIGHTING SYSTEM**Description:****Technical Field**

5 The present invention relates to operation of light emitting diode (LED) based light sources in a discontinuous conduction mode, and in particular, to a converter for operating an LED load and a lighting system comprising such a converter.

Background Art

10 Converters for LED-based light sources turn electrical power from a source, such as a mains grid, to a direct current (DC) parameter of the LED load, such as a DC voltage or DC current.

The DC parameter is typically regulated in accordance with a nominal/reference value by manipulating a duty cycle of a switch of the converter using pulse-width modulation (PWM).

15 Depending on the implementation of the converter, this may involve different modes of operation, such as Discontinuous Conduction Mode (DCM). In this mode of operation, the switching cycles of the switch comprise a period in which all stored energy of an inductor of the converter has dissipated and the inductor current is floating or ringing due to resonant oscillations until a subsequent switching cycle begins. A switching performance is optimized by commencing the subsequent switching cycle
20 using so-called valley switching, by closing the switch in a depression or valley of the voltage across it.

As such, an actual switch-on timing of the switch may depart from a nominal switch-on timing
25 determined by a control circuitry of the converter, resulting in a regulation error in each switching cycle of the switch.

If a regulation of the DC parameter is relatively slow, a large amount of error may accumulate over a plurality of switching cycles. As a result, a low-frequency instability of the DC parameter may
30 emerge, which becomes visible as light flicker.

Summary of the Invention

The object of the present invention is to provide a converter and a lighting system reconciling valley switching and avoidance of visible light flicker.

- 5 The invention is defined by the appended independent claims. Preferred embodiments are set forth in the dependent claims and in the following description and drawings.

According to a first aspect, a converter for operating an LED load is provided. The converter comprises an actively switched power factor correction, PFC, circuitry, having a control circuitry for
10 controlling a switch of the PFC circuitry. The control circuitry is configured to control a switch-on timing of the switch such that an output voltage V_{bus} of the PFC circuitry is feedback-controlled in accordance with a nominal value. In a discontinuous conduction mode, DCM, the control circuitry is configured to control an actual value T_{off_act} of the switch-on timing of the switch in one or more switching cycles to be a time of a valley of a voltage across the switch succeeding a nominal value
15 T_{off_nom} of the switch-on timing of a control algorithm implemented by the control circuitry. The control circuitry is further configured to control the actual value T_{off_act} of the switch-on timing of the switch in one or more subsequent switching cycles being subsequent to the one or more switching cycles to be a time of a valley of the voltage across the switch preceding the nominal value T_{off_nom} of the switch-on timing.

20 Preferably, the one or more switching cycles comprise consecutive switching cycles.

Preferably, the one or more subsequent switching cycles comprise consecutive subsequent switching cycles.

25 Preferably, the switch comprises a power field effect transistor, FET.

Preferably, the control circuitry is configured to calculate the nominal value T_{off_nom} of the switch-on timing of the switch in dependence of a constant duration of closure T_{on} of the switch and a magnified
30 constant duration of conductance T_{active} of a diode of the PFC circuitry.

Preferably, the control circuitry is configured to calculate the nominal value T_{off_nom} of the switch-on timing of the switch by subtracting the constant duration of closure T_{on} of the switch from the magnified constant duration of conductance T_{active} of the diode of the PFC circuitry.

5 Preferably, the control circuitry comprises a sigma-delta modulator.

Preferably, the control circuitry is configured to establish an error T_{off_err} of the switch-on timing in dependence of the actual value T_{off_act} of the switch-on timing and the nominal value T_{off_nom} of the switch-on timing.

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Preferably, the control circuitry is configured to establish the error T_{off_err} of the switch-on timing by subtracting the actual value T_{off_act} of the switch-on timing from the nominal value T_{off_nom} of the switch-on timing.

15 Preferably, the control circuitry is configured to establish a truncated accumulated error $T_{off_acc_err}$ of the switch-on timing in dependence of the error T_{off_err} of the switch-on timing.

Preferably, the control circuitry is configured to establish the truncated accumulated error $T_{off_acc_err}$ of the switch-on timing by integrating the error T_{off_err} of the switch-on timing over consecutive switching cycles and by truncating decimal digits of the integrated error.

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Preferably, the control circuitry is configured to establish an adjusted value T_{off_adj} of the switch-on timing in dependence of the nominal value T_{off_nom} of the switch-on timing and the truncated accumulated error $T_{off_acc_err}$ of the switch-on timing.

25

Preferably, the control circuitry is configured to establish the adjusted value T_{off_adj} of the switch-on timing by summing up the nominal value T_{off_nom} of the switch-on timing and the truncated accumulated error $T_{off_acc_err}$ of the switch-on timing.

30 Preferably, the control circuitry is configured to establish the actual value T_{off_act} of the switch-on timing in dependence of the adjusted value T_{off_adj} of the switch-on timing.

Preferably, the control circuitry is configured to establish the actual value T_{off_act} of the switch-on timing by detecting a valley of the voltage across the switch succeeding the adjusted value T_{off_adj} of the switch-on timing.

- 5 According to a second aspect, a lighting system is provided. The lighting system comprises a converter according to the first aspect or any of its embodiments; and an LED load being configured to be operated by the converter.

Brief Description of the Drawings

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Further aspects, advantages and objects of the invention will become evident for the skilled reader by means of the following detailed description of the embodiments of the invention, when taking into conjunction with the figures of the enclosed drawings.

- 15 Fig. 1 illustrates a converter according to an embodiment of the present disclosure;

Figs. 2-4 illustrate schematic block diagrams of a control circuitry according to an embodiment of the present disclosure in various levels of detail;

- 20 Fig. 5 illustrates a switch-on timing of the switch of the converter of Fig. 1; and

Fig. 6 illustrates a lighting system according to an embodiment of the present disclosure.

Detailed Descriptions of Embodiments

25

The invention will now be described with respect to various embodiments. The features of these embodiments may be combined with each other unless specified otherwise.

- As used herein, the term “power factor correction” may refer to an increasing/maximizing of a power factor of a load, such as an LED load. A power factor of an AC electrical power system may refer to
30 a ratio of a real power absorbed by the load to an apparent power flowing in the circuit. Statutory provisions usually define a minimum value of a power factor that needs to be maintained.

Fig. 1 illustrates a converter 1 according to an embodiment of the present disclosure.

The converter 1 is for operating an LED load connectable to the converter 1 and comprises an actively switched power factor correction, PFC, circuitry 104-112.

5

As may be taken from Fig. 1, the PFC circuitry 104-112 may be framed by smoothing capacitors 103, 111 on both sides, and be preceded by a rectifier stage, such as the depicted diode bridge including diodes 102, for rectifying an electrical power supplied by a mains grid 101.

10 The PFC circuitry 104-112 of Fig. 1 further comprises an inductor 104 which represents an energy storage of the converter 1.

A switch 105 of the PFC circuitry 104-112 preferably comprises a power FET. The switch 105 is configured, in a period of closure of the switch 105, to effect storage of energy supplied by the mains
15 grid 101 in the inductor 104, and in a subsequent period of opening of the switch 105, to effect an onward transfer of the energy stored in the inductor 104 to the LED load.

The switch 105 of Fig. 1 is protected by a flyback diode 106, which is configured to eliminate flyback, i.e., a sudden voltage spike emerging across the inductor 104 on disruption of its current by the switch
20 105, and a resistor cascade 107, 108, 109 is configured to limit a switch current of the switch 105 and to allow for tapping a voltage 112 that provides an indication of an output voltage 113, V_{bus} of the PFC circuitry 104-112.

The converter of Fig. 1 further shows a diode 110 that is configured to allow for a one-way energy
25 transfer from the mains grid 101 via the inductor 104 towards the LED load.

With continuing reference to Fig. 1, the converter 1 further comprises a control circuitry 2 for controlling the switch 105. In particular, the control circuitry 2 is configured to control a switch-on timing of the switch 105 such that the output voltage 113, V_{bus} of the PFC circuitry 104-112 is
30 feedback-controlled in accordance with a nominal value 201 (shown in Fig. 2).

As used herein, the term “switching cycle” refers to an operation cycle of a switch of a converter, wherein the switch is driven according to a PWM scheme. The switching cycle comprises a period in which the switch is closed/conductive (“on” state), and a remaining period of the switching cycle in which the switch is open/non-conductive (“off” state). A ratio of the duration of the period of closure to the total duration of the switching cycle denotes a duty cycle of the switch, which is typically manipulated to regulate a process variable, such as an output voltage, in accordance with a nominal value.

As used herein, the term “switch-on timing” may refer to a time instant denoting a beginning of a subsequent switching cycle, or to a time duration of the remaining period of the switching cycle in which the switch is open/non-conductive.

In a discontinuous conduction mode, DCM, the control circuitry 2 is configured to control an actual value 204, T_{off_act} of the switch-on timing of the switch 105 in one or more switching cycles to be a time of a valley 503 of a voltage across the switch 105 *succeeding* a nominal value 302, T_{off_nom} of the switch-on timing of a control algorithm implemented by the control circuitry 2-4. In other words, if the nominal value 302, T_{off_nom} of the switch-on timing calculated by the control circuitry 2 coincides with a significant non-zero voltage across the switch 105, such as indicated in Fig. 5, the control circuitry 2 is configured to delay the switch-on timing such that the actual value 204, T_{off_act} of the switch-on timing succeeds the nominal value 302, T_{off_nom} and coincides with a zero-crossing voltage across the switch 105 in the valley 503 succeeding the nominal value 302, T_{off_nom} .

As used herein, the term “discontinuous conduction mode” may refer to a mode of operation of a converter wherein switching cycles of a switch of the converter comprise a period in which all stored energy of an inductor of the converter has dissipated and an inductor current that decreased to zero starts floating or ringing due to resonant oscillations until a subsequent switching cycle begins.

As used herein, the term “valley” may refer to a transient depression of an electrical parameter, such as a voltage.

Preferably, the one or more switching cycles comprise consecutive switching cycles.

Likewise, the control circuitry 2 is configured to control the actual value 204, T_{off_act} of the switch-on timing of the switch 105 in one or more subsequent switching cycles that are subsequent to the one or more switching cycles to be a time of a valley 504 of the voltage across the switch 105 preceding the nominal value 302, T_{off_nom} of the switch-on timing. That is to say, the control circuitry 2 is further configured to “frontload” the switch-on timing such that the actual value 204, T_{off_act} of the switch-on timing precedes the nominal value 302, T_{off_nom} and coincides with a zero-crossing voltage across the switch 105 in the valley 504 preceding the nominal value 302, T_{off_nom} .

Preferably, the one or more subsequent switching cycles comprise consecutive subsequent switching cycles.

By performing a high-frequency modulation of the nominal value T_{off_nom} of the switch-on timing in accordance with an error $T_{off_acc_err}$ of the switch-on timing that has accumulated over a number of switching cycles, the converter 1 achieves that the actual value T_{off_act} of the switch-on timing oscillates between valleys of the voltage across the switch that succeed or precede the nominal value T_{off_nom} of the switch-on timing, such that the actual value T_{off_act} of the switch-on timing corresponds, on average, to the nominal value T_{off_nom} of the switch-on timing. As a result, valley switching without visible light flicker is realized.

Details of the delaying and frontloading of the switch-on timing will now be explained in more detail in connection with Figs. 2-5.

Figs. 2-4 illustrate schematic block diagrams of a control circuitry 2-4 according to an embodiment of the present disclosure in various levels of detail. In connection with the following description of Figs. 2-4, also Fig. 5 will be referenced, which illustrates a switch-on timing of the switch 105 of the converter 1 of Fig. 1.

An upper portion of Fig. 5 shows a switching cycle of the switch 105 as represented by a gate voltage 115, V_g of the switch 105.

The switching cycle comprises a period in which the switch 105 is closed/conductive (“on” state) in accordance with a high-level gate voltage 115, V_g for a constant duration of closure denoted as 501, T_{on} . In a remaining period of the switching cycle, the switch 105 is open/non-conductive (“off” state) in accordance with a vanishing gate voltage 115, V_g for a variable duration denoted as actual value
 5 204, T_{off_act} of the switch-on timing.

A lower portion of Fig. 5 shows an inductor current 114, i_L resulting from the switching cycle of the switch 105. As the converter 1 of Fig. 1 is preferably DCM operated, the outer loop controller 3 (see Fig. 3) of control circuitry 2-3 is preferably configured to calculate the nominal value 302, T_{off_nom} of
 10 the switch-on timing of the switch 105 in dependence of the constant duration of closure 501, T_{on} of the switch 105 and a magnified constant duration of conductance 502, T_{active} of the diode 110 of the PFC circuitry 104-112. That is to say, the outer loop controller 3 of the control circuitry 2-4 is preferably configured to calculate the nominal value 302, T_{off_nom} of the switch-on timing of the
 15 switch 105 by subtracting the constant duration of closure 501, T_{on} of the switch 105 from the magnified (by scalar K) constant duration of conductance 502, T_{active} of the diode 110 of the PFC circuitry 104-112, in accordance with the following equation:

$$T_{off_nom} = K \cdot T_{active} - T_{on}, \quad (K > 1 \text{ for DCM})$$

20 With reference to Fig. 5, it will be appreciated that as the duration of closure 501, T_{on} of the switch 105 is held constant in DCM operation, so is the duration of conductance 502, T_{active} of the diode 110 until the conduction of the diode becomes discontinuous. The scalar $K > 1$ in the above formula is used to express that in this mode of operation, each switching cycle of the switch 105 comprises a period in which all stored energy of the inductor 104 of the converter 1 has dissipated and its current
 25 114, i_L is floating or ringing until a subsequent switching cycle commences. To this end, Fig. 5 shows two valleys 503, 504 emerging in the floating or ringing period of the switching cycle.

Fig. 2 shows a block diagram of a relatively slow outer control loop of the output voltage 113, V_{bus} of the PFC circuitry 104-112 of Fig. 1. In other words, the output voltage 113, V_{bus} is feedback-
 30 controlled in accordance with a nominal value 201 as the reference value of the outer control loop.

As such, the control circuitry 2 of Fig. 2 is preferably configured to establish a regulation error 202 of the outer control loop in dependence of the nominal value 201 and the output voltage 113, V_{bus} . In more detail, the control circuitry 2 is preferably configured to establish the regulation error 202 by subtracting the output voltage 113, V_{bus} from the nominal value 201.

5

An outer loop controller 3 is configured to transform the regulation error 202 to the actual value 204, T_{off_act} of the switch-on timing as the manipulated variable of the control loop. Details of this transformation will be explained in connection with Fig. 3 below.

10 Subsequently, the control circuitry 2 is preferably configured to establish the output voltage 113, V_{bus} in dependence of the actual value 204, T_{off_act} of the switch-on timing. More specifically, the switch 105, which is included in process 205, is closed in accordance with the actual value 204, T_{off_act} of the switch-on timing to begin a subsequent switching cycle, which results in the desired output voltage 113, V_{bus} in the long run.

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Fig. 3 shows a more detailed block diagram of the outer loop controller 3 of Fig. 2. As already mentioned, the outer loop controller 3 is configured to transform the regulation error 202 to the actual value 204, T_{off_act} of the switch-on timing.

20 The control algorithm 301 implemented by the control circuitry 2-3 is configured to provide the nominal value 302, T_{off_nom} of the switch-on timing in dependence of the regulation error 202 of the outer control loop. In the example of Fig. 5, this nominal value 302, T_{off_nom} corresponds to a peak of the inductor current 114, i_L , or equivalently, of the voltage across the switch 105, in the interest of better understanding.

25 The nominal value 302, T_{off_nom} of the switch-on timing needs to be turned into the actual value 204, T_{off_act} of the switch-on timing, which defines the actual beginning of the subsequent switching cycle. In the example of Fig. 5, the actual value 204, T_{off_act} of the switch-on timing effects an activation/closure of the switch 105 when the voltage across it experiences a zero crossing.

30 Preferably, the control circuitry 2 comprises a sigma-delta modulator to obtain the actual value 204, T_{off_act} of the switch-on timing, which sigma-delta modulator is explained in the following.

A relatively responsive inner control loop transforms the provided nominal value 302, T_{off_nom} of the switch-on timing to the actual value 204, T_{off_act} of the switch-on timing. In other words, the actual value 204, T_{off_act} of the switch-on timing is feedback-controlled in accordance with the nominal value 302, T_{off_nom} of the switch-on timing as the reference value of the inner control loop.

5

The control circuitry 2-3 is preferably configured to establish an error 303, T_{off_err} of the switch-on timing in dependence of the actual value 204, T_{off_act} of the switch-on timing and the nominal value 302, T_{off_nom} of the switch-on timing. In more detail, the control circuitry 2-3 is preferably configured to establish the error 303, T_{off_err} of the switch-on timing by subtracting the actual value 204, T_{off_act} of the switch-on timing from the nominal value 302, T_{off_nom} of the switch-on timing. In the example of Fig. 5, the error 303, T_{off_err} of the switch-on timing is depicted as the difference of the actual value 204, T_{off_act} of the switch-on timing and the nominal value 302, T_{off_nom} of the switch-on timing.

10

An inner loop controller 4 is configured to transform the error 303, T_{off_err} of the switch-on timing to an adjusted value 305, T_{off_adj} of the switch-on timing as the manipulated variable of the control loop. Details of this transformation will be explained in connection with Fig. 4 below.

15

Subsequently, the control circuitry 2-3 is preferably configured to establish the actual value 204, T_{off_act} of the switch-on timing in dependence of the adjusted value 305, T_{off_adj} of the switch-on timing. More specifically, the control circuitry 2-3 is preferably configured to establish the actual value 204, T_{off_act} of the switch-on timing by detecting one of the valleys 503, 504 (see Fig. 5) of the voltage across the switch 105 succeeding the adjusted value 305, T_{off_adj} of the switch-on timing. Thus, the adjusted value 305, T_{off_adj} of the switch-on timing may denote a beginning of a valley detection. According to the example of Fig. 3, a valley detection block 306 may be used to this end.

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Fig. 4 shows a more detailed block diagram of the inner loop controller 4 of Fig. 3. As already mentioned, the inner loop controller 4 is configured to transform the error 303, T_{off_err} of the switch-on timing to the adjusted value 305, T_{off_adj} of the switch-on timing.

30

The control circuitry 2-4 is preferably configured to establish the adjusted value 305, T_{off_adj} of the switch-on timing in dependence of the nominal value 302, T_{off_nom} of the switch-on timing and a

truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing. More precisely, the control circuitry 2-4 is preferably configured to establish the adjusted value 305, T_{off_adj} of the switch-on timing by summing up the nominal value 302, T_{off_nom} of the switch-on timing and the truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing.

5

In turn, the control circuitry 2-4 is preferably configured to establish the truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing in dependence of the error 303, T_{off_err} of the switch-on timing. That is to say, the control circuitry 2-4 is preferably configured to establish the truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing by integrating the error 303, T_{off_err} of the switch-on timing over consecutive switching cycles and by truncating 403 decimal digits of the integrated error 402.

10

According to the example of Fig. 4, an integration block 401 indicated by a “1/z” label may be used to integrate the error 303, T_{off_err} of the switch-on timing over consecutive switching cycles to yield the integrated error 402, and an integer/truncation block 403 indicated by a stair symbol may be used to truncate the decimal digits of the integrated error 402.

15

The truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing adjusts the nominal value 302, T_{off_nom} of the switch-on timing to yield the adjusted value 305, T_{off_adj} of the switch-on timing, which may denote a beginning of a valley detection. In the example of Fig. 5, a plurality of dots on the graph of the inductor current 114, i_L represents possible positive or negative adjustments of the nominal value 302, T_{off_nom} of the switch-on timing by the truncated accumulated error 404, $T_{off_acc_err}$ of the switch-on timing. Depending on the particular adjustment, i.e., depending on the adjusted value 305, T_{off_adj} of the switch-on timing, a valley detection may begin at a time instant corresponding to the respective dot. For example, beginning the valley detection at one of the dots in the first valley 504 may result in a beginning of the subsequent switching cycle within or at the end of the first valley 504, as is indicated by a suggested rising edge of the gate voltage 115, V_g of the switch 105 in Fig. 5. As another example, beginning the valley detection at one of the dots between the valleys 504, 503 or in the second valley 504 may result in a beginning of the subsequent switching cycle within or at the end of the first valley 504, as is indicated by a rising edge of the gate voltage 115, V_g in Fig. 5.

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Fig. 6 illustrates a lighting system 6 according to an embodiment of the present disclosure.

The lighting system 6 comprises a converter 1 according to the first aspect of the present disclosure or any of its embodiments; and an LED load 601, which is configured to be operated by the converter

5 1.

Claims:

1. A converter (1) for operating an LED load, comprising:
 - an actively switched power factor correction, PFC, circuitry (104-112), having
 - 5 a control circuitry (2-4) for controlling a switch (105) of the PFC circuitry (104-112),
 - wherein the control circuitry (2-4) is configured to control a switch-on timing of the switch (105) such that an output voltage (113) of the PFC circuitry (104-112) is feedback-controlled in accordance with a nominal value (201);
 - 10 wherein in a discontinuous conduction mode, DCM, the control circuitry (2-4) is configured to control an actual value (204, $T_{\text{off_act}}$) of the switch-on timing of the switch (105) in one or more switching cycles to be a time of a valley of a voltage across the switch (105) succeeding a nominal value (302, $T_{\text{off_nom}}$) of the switch-on timing of a control algorithm implemented by the control circuitry (2-4); and
 - 15 wherein the control circuitry (2-4) is configured to control the actual value (204, $T_{\text{off_act}}$) of the switch-on timing of the switch (105) in one or more subsequent switching cycles being subsequent to the one or more switching cycles to be a time of a valley of the voltage across the switch (105) preceding the nominal value (302, $T_{\text{off_nom}}$) of the switch-on timing.
- 20 2. The converter (1) of claim 1,
 - wherein the one or more switching cycles comprise consecutive switching cycles.
3. The converter (1) of claim 1 or claim 2,
 - wherein the one or more subsequent switching cycles comprise consecutive subsequent
 - 25 switching cycles.
4. The converter (1) of any one of the preceding claims,
 - wherein the switch (105) is a power field effect transistor, FET.
- 30 5. The converter (1) of any one of the preceding claims,
 - wherein the control circuitry (2-4) is configured to calculate the nominal value (302, $T_{\text{off_nom}}$) of the switch-on timing of the switch (105) in dependence of a constant duration of closure

(501, T_{on}) of the switch (105) and a magnified constant duration of conductance (502, T_{active}) of a diode (110) of the PFC circuitry (104-112).

6. The converter (1) of claim 5,

5 wherein the control circuitry (2-4) is configured to calculate the nominal value (302, T_{off_nom}) of the switch-on timing of the switch (105) by subtracting the constant duration of closure (501, T_{on}) of the switch (105) from the magnified constant duration of conductance (502, T_{active}) of the diode (110) of the PFC circuitry (104-112).

10 7. The converter (1) of any one of the preceding claims,

 wherein the control circuitry (2-4) comprises a sigma-delta modulator (3-4).

8. The converter (1) of claim 7,

 wherein the control circuitry (2-4) is configured to establish an error (303, T_{off_err}) of the
15 switch-on timing in dependence of the actual value (204, T_{off_act}) of the switch-on timing and the nominal value (302, T_{off_nom}) of the switch-on timing.

9. The converter (1) of claim 8,

 wherein the control circuitry (2-4) is configured to establish the error (303, T_{off_err}) of the
20 switch-on timing by subtracting the actual value (204, T_{off_act}) of the switch-on timing from the nominal value (302, T_{off_nom}) of the switch-on timing.

10. The converter (1) of any one of claims 7 to 9,

 wherein the control circuitry (2-4) is configured to establish a truncated accumulated error
25 (404, $T_{off_acc_err}$) of the switch-on timing in dependence of the error (303, T_{off_err}) of the switch-on timing.

11. The converter (1) of claim 10,

 wherein the control circuitry (2-4) is configured to establish the truncated accumulated error
30 (404, $T_{off_acc_err}$) of the switch-on timing by integrating the error (303, T_{off_err}) of the switch-on

timing over consecutive switching cycles and by truncating decimal digits of the integrated error (402).

12. The converter (1) of any one of claims 7 to 11,

5 wherein the control circuitry (2-4) is configured to establish an adjusted value (305, $T_{\text{off_adj}}$) of the switch-on timing in dependence of the nominal value (302, $T_{\text{off_nom}}$) of the switch-on timing and the truncated accumulated error (404, $T_{\text{off_acc_err}}$) of the switch-on timing.

13. The converter (1) of claim 12,

10 wherein the control circuitry (2-4) is configured to establish the adjusted value (305, $T_{\text{off_adj}}$) of the switch-on timing by summing up the nominal value (302, $T_{\text{off_nom}}$) of the switch-on timing and the truncated accumulated error (404, $T_{\text{off_acc_err}}$) of the switch-on timing.

14. The converter (1) of any one of the preceding claims,

15 wherein the control circuitry (2-4) is configured to establish the actual value (204, $T_{\text{off_act}}$) of the switch-on timing in dependence of the adjusted value (305, $T_{\text{off_adj}}$) of the switch-on timing.

15. The converter (1) of claim 14,

20 wherein the control circuitry (2-4) is configured to establish the actual value (204, $T_{\text{off_act}}$) of the switch-on timing by detecting a valley of the voltage across the switch (105) succeeding the adjusted value (305, $T_{\text{off_adj}}$) of the switch-on timing.

16. A lighting system (6), comprising:

25 a converter (1) of one any of the preceding claims; and
 an LED load (601) being configured to be operated by the converter (1).

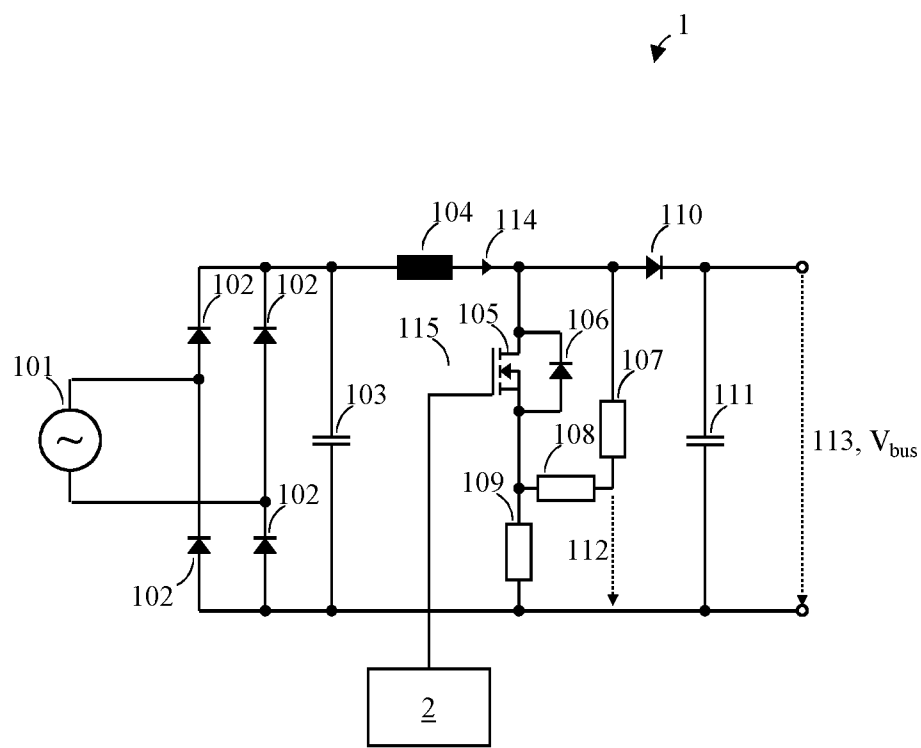


Fig. 1

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2

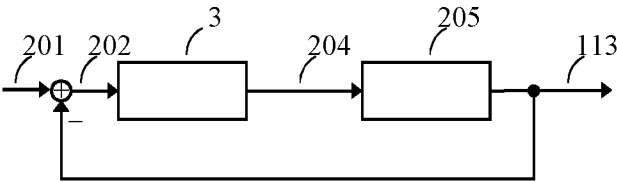


Fig. 2

3

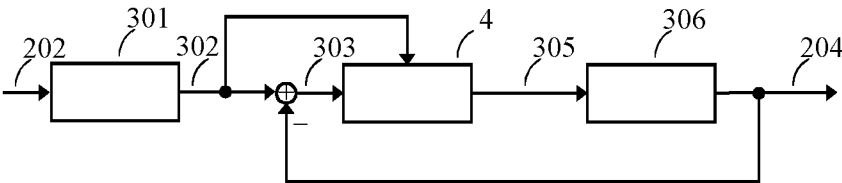


Fig. 3

4

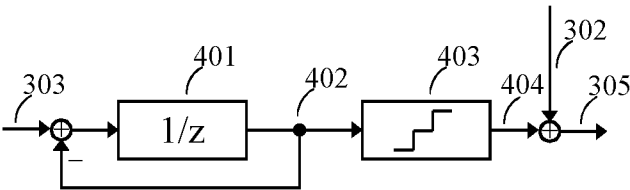


Fig. 4

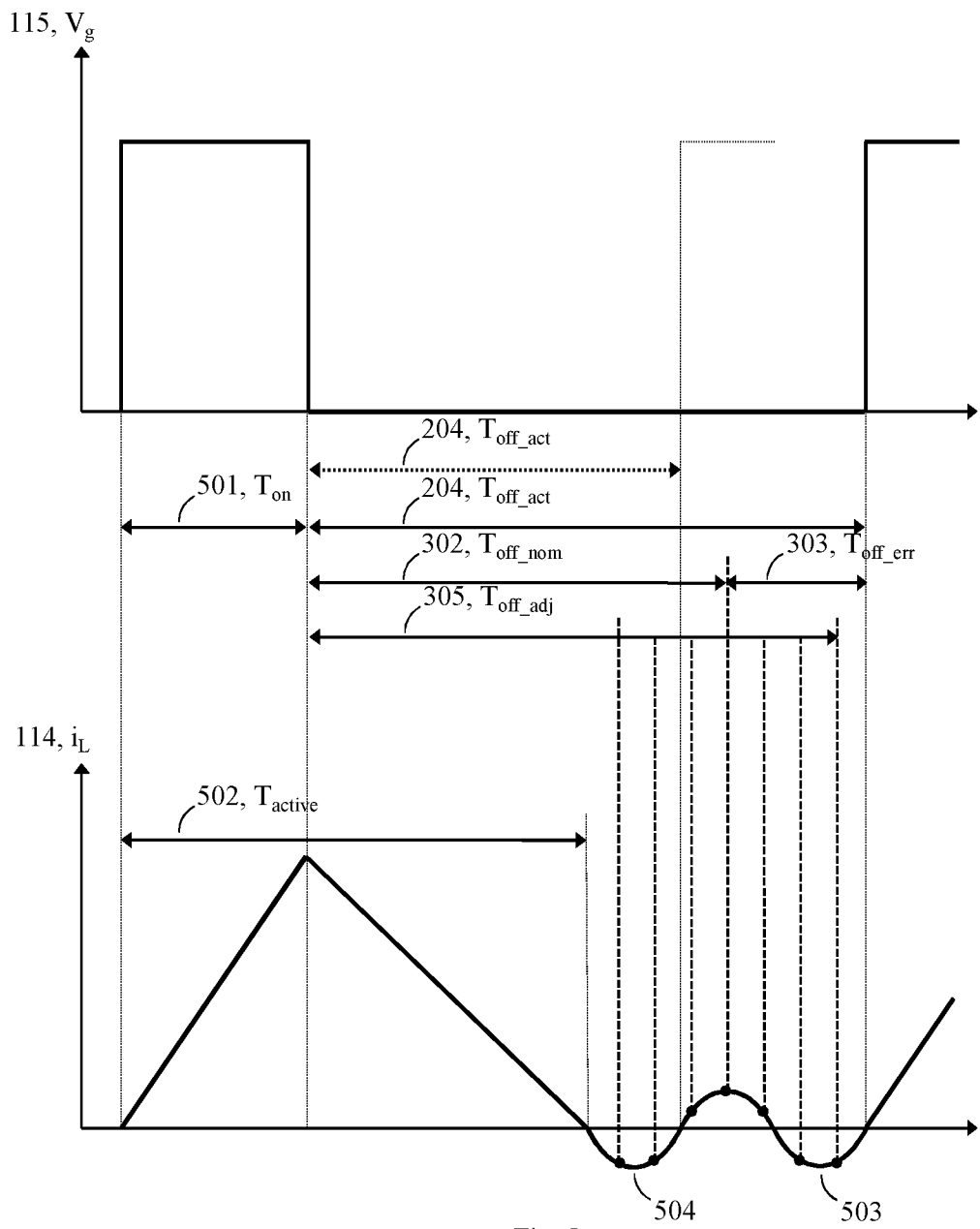


Fig. 5

6

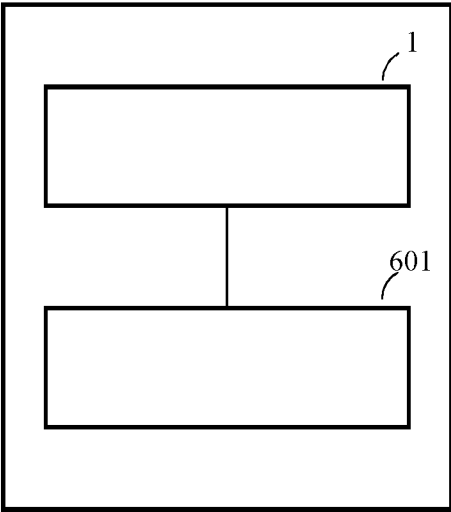


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2021/078253

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/42
ADD. H02M1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 10 090 757 B2 (FAIRCHILD SEMICONDUCTOR [US]) 2 October 2018 (2018-10-02) columns 4-6,12; figures 1, 2A, 2C -----	1-16
A	SANG HEE KANG ET AL: "Efficiency Optimization in Digitally Controlled Flyback DC DC Converters Over Wide Ranges of Operating Conditions", IEEE TRANSACTIONS ON POWER ELECTRONICS, INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, USA, vol. 27, no. 8, 1 August 2012 (2012-08-01), pages 3734-3748, XP011454760, ISSN: 0885-8993, DOI: 10.1109/TPEL.2012.2186590 Section V.A; page 3740 page 3741; figure 8 -----	1-16



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

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Date of mailing of the international search report

11/11/2021

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2021/078253

Patent document cited in search report		Publication date		Patent family member(s)		Publication date
US 10090757	B2	02-10-2018	CN	107769537 A		06-03-2018
			US	2018054113 A1		22-02-2018
			US	2019013729 A1		10-01-2019
