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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) Title: SYSTEMS AND METHODS FOR CONTROLLING A MEMORY PERFORMANCE POINT

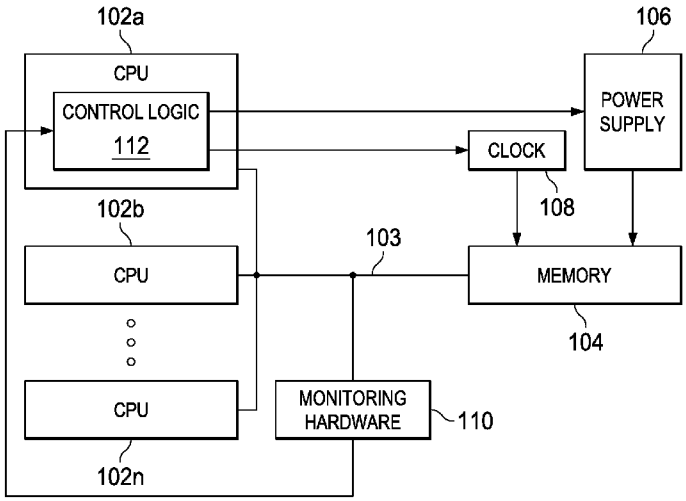


FIG. 1a

(57) Abstract: In described examples, a system includes a processor (102a), memory (104) coupled to the processor (102a) by an interconnect (103), and monitoring hardware (110) coupled to the interconnect (103). The memory (104) operates at least at first and second performance points, where the first performance point has a higher performance than the second performance point. The monitoring hardware (110) monitors transactions on the interconnect (103) to detect a usage level of the interconnect (103) and transmits an indication of the detected usage level to control logic (112). Based on the detected usage level being above a first threshold, the control logic (112) causes the memory (104) to operate at the first performance point. Based on the detected usage level being below a second threshold, the control logic (112) causes the memory (104) to operate at the second performance point. The second threshold is equal to or less than the first threshold.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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— *with international search report (Art. 21(3))*

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SYSTEMS AND METHODS FOR CONTROLLING A MEMORY PERFORMANCE POINT

BACKGROUND

[0001] Modern computers include processors and memory (e.g., random access memory (RAM)) that may operate at different voltage and/or frequency levels, or "performance points." Power consumption of these devices is related to the performance point at which they operate. Accordingly, a processor or memory device operating at a higher performance point consumes more power, while a processor or memory device operating at a lower performance point consumes less power. Thus, power consumption may be reduced by allowing both the processor and memory device to operate at the lowest performance point permitted for a given computing load.

SUMMARY

[0002] In described examples, a system includes a processor, memory coupled to the processor by an interconnect, and monitoring hardware coupled to the interconnect. The memory operates at least at first and second performance points, where the first performance point has a higher performance than the second performance point. The monitoring hardware monitors transactions on the interconnect to detect a usage level of the interconnect and transmits an indication of the detected usage level to control logic. Based on the detected usage level being above a first threshold, the control logic causes the memory to operate at the first performance point. Based on the detected usage level being below a second threshold, the control logic causes the memory to operate at the second performance point. The second threshold is equal to or less than the first threshold.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] FIG. 1a is a block diagram of a computing system in accordance with example embodiments.

[0004] FIG. 1b is a block diagram of an alternate embodiment of a computing system in accordance with example embodiments.

[0005] FIG. 2 is a flow chart of a method in accordance with example embodiments.

[0006] FIG. 3 is a block diagram of a system to control a memory performance point in

accordance with example embodiments.

[0007] FIG. 4 is a block diagram of another example system to control a memory performance point in accordance with example embodiments.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0008] In computing systems, processors such as central processing units (CPUs) are configured to operate at multiple combinations of clock frequency and power supply voltage, or performance points. For example, in a time period where processing requirements on a CPU are high, the CPU may operate at a higher frequency-voltage combination. By comparison, in a time period where processing requirements on the CPU are minimal, the CPU may operate at a lower frequency-voltage combination, which conserves power. In this way, power consumption of the CPU is reduced when processing requirements on that CPU are lessened.

[0009] Similarly, memory such as random access memory (RAM) may be configured to operate at multiple performance points. In some cases, the performance point of the memory is based on the requirements of the CPU. For example, when the CPU is operating at a higher performance point, the memory may also be caused to operate at a correspondingly higher performance point. However, in other cases, the performance point of the memory does not necessarily correspond to the performance point of the CPU. For example, where multiple CPUs are using memory, even where the CPUs are operating at a lower performance point, the memory may be caused to operate at a higher performance point to ensure adequate performance for all CPUs. Thus, in these cases, when the CPU is able to operate at a lower performance point, the memory does not necessarily transition to a lower performance point, and thus consumes more power than is necessary for a given CPU performance point. Further, in certain other cases, the CPU may be at a higher performance point but actually does not require memory to be at a correspondingly high performance point, such as if the CPU is accessing cache rather than memory. In the example embodiments, a system and method allow and cause the memory to operate at a lower performance point when system processing requirements do not necessitate the memory to operate at a higher performance point to provide acceptable system performance, thereby decreasing excess power consumption when not necessary.

[0010] FIG. 1a shows a computing system 100 in accordance with example embodiments. The computing system 100 includes one or more CPUs 102a, 102b, …, 102n coupled to a memory 104 by an interconnect 103. Certain embodiments include only one CPU 102, but more than one CPU

102 may be included for increased processing ability. In the case where multiple CPUs 102 exist, one CPU 102a may be a master while the other CPUs 102b-n are slaves. A power supply 106 supplies the memory 104 with one or more voltages, which may vary depending on the performance point at which the memory 104 operates. Similarly, a clock circuit 108 supplies the memory 104 with a clock signal (e.g., generated using a digital phase-locked loop (DPLL)) having a variable frequency, depending on the performance point at which the memory 104 operates.

[0011] In accordance with example embodiments, monitoring hardware 110 is coupled to the interconnect 103 and detects a usage level of the interconnect 103. In some embodiments, the usage level may be expressed as a utilization percentage. In other embodiments, the usage level may be expressed as a bandwidth (e.g., MB/sec). The monitoring hardware 110 generates and transmits an indication of the detected usage level to control logic 112, which (in FIG. 1a) is software executed by CPU 102a. In the case of multiple CPUs 102, the control logic 112 may be executed by the CPU 102a that is the master. By monitoring the actual usage of the interconnect 103 between the CPUs 102 and the memory 104, a more accurate representation of a required memory performance point for given processing tasks is available.

[0012] The control logic 112 causes the memory 104 to operate at a particular performance level based on the detected usage level or the indication of the detected usage level generated by the monitoring hardware 110. In accordance with example embodiments, if the detected usage level is above a first threshold, then the control logic 112 causes the memory 104 to operate at a higher first performance point. However, if the detected usage level is below a second threshold, then the control logic 112 causes the memory 104 to operate at a lower second performance point.

[0013] The particular values of the first and second threshold may be selected to optimize overall system 100 performance. For example, in some embodiments, the first and second thresholds may be equal (e.g., 50% interconnect 103 utilization), such that: if interconnect 103 utilization is greater than 50%, then the control logic 112 causes the memory 104 to operate at the first performance point; and if interconnect 103 utilization is less than 50%, then the control logic 112 causes the memory 104 to operate at the second performance point. However, in other embodiments, the second threshold may be less than the first threshold (e.g., the first threshold is 70% interconnect 103 utilization, and the second threshold is 30% interconnect 103 utilization), to allow for some hysteresis in the system 100. For example, if the control logic 112 causes the memory 104 to operate at the first performance point, and if the interconnect 103 utilization falls

below 70% but not below 30%, then the control logic 112 continues to cause the memory 104 to operate at the first performance point.

[0014] The frequency of the clock signal generated by clock circuit 108 may be altered by modifying registers internal to the clock circuit 108, which modifies the DPLL or an external divider on the output of the DPLL. The voltage supplied by the power supply 106 may be altered based on communications received through an interface, such as a serial peripheral interface (SPI) or an inter-integrated circuit (I2C) interface. The control logic 112 causes the clock circuit 108 to generate a clock signal for the memory 104 having a frequency value that is based on the detected usage level, such as by modifying registers of the clock circuit 108. Similarly, the control logic 112 also causes the power supply 106 to supply an operating voltage to the memory 104 having a voltage value that is based on the detected usage level, such as through communications via an SPI or I2C interface.

[0015] In some embodiments, the control logic 112 causes the memory 104 to operate at a higher or lower performance point based on the detected usage level being above the first threshold or below the second threshold, respectively, for at least a predetermined time. For example, if the memory 104 is operating at the lower performance point, and if the detected usage level rises above the first threshold but for less than the predetermined threshold amount of time, and if it then falls below the first threshold, then the control logic 112 would not cause the memory 104 to operate at the higher performance point. Conversely, if the memory 104 is operating at the lower performance point, and if the usage level rises above the first threshold and remains there for at least the predetermined threshold amount of time, then the control logic 112 causes the memory 104 to operate at the higher performance point.

[0016] In certain embodiments, the various parameters described above with respect to the control logic 112 may be configurable, either at the time of system 100 design, by a user of the system 100, or both. For example, the various usage level thresholds may be configured, the predetermined threshold amounts of time may be configured, and other such parameters may be similarly configured. Also, although described generally with respect to a higher and lower performance point, the example embodiments may be similarly applied to three or more performance points.

[0017] FIG. 1b shows an alternate embodiment of a system 150 in accordance with example embodiments. In FIG. 1a, the control logic 112 was executed by the CPU 102a, which is the master

in a multiprocessor system 100. As a result, if the master CPU 102a is not active, but one or more of the other CPUs 102b-n necessitate the memory 104 to operate at a higher performance point, then the CPU 102a must be woken up to execute the control logic 112 to cause the memory 104 to operate at the higher performance point. By requiring a dormant master CPU 102a to wake up to perform this task, additional power is consumed, which is disadvantageous. Thus, in FIG. 1b, the control logic 112 is implemented as dedicated hardware, such as a microcontroller or hardware state machine, which consumes less power than a CPU 102. This avoids the need to wake up a CPU 102 to implement the control of the performance point of the memory 104. As a result, the power consumption of 150 is reduced, such as in scenarios where the master CPU 102a is dormant but one or more of the other CPUs 102b-n require the memory 104 to operate at a higher performance point. Aside from this difference, the elements shown in FIG. 1b operate similarly to those explained above with respect to FIG. 1a.

[0018] FIG. 2 shows a method 200 in accordance with example embodiments. The method 200 begins at block 202 with monitoring transactions on an interconnect 103 and detecting a usage level of the interconnect 103 that couples processors 102 to memory 104. As explained above, monitoring hardware 110 may be implemented to detect interconnect 103 usage, such as a percent utilization value or as a bandwidth value. The method 200 continues at block 204 with causing the memory 104 to operate at a higher first performance point based on the detected usage level being above a first threshold. At block 206, the method 200 includes causing the memory 104 to operate at a lower second performance point based on the detected usage level being below a second threshold.

[0019] Control logic 112, which may be software executed by one of the CPUs 102 or hardware logic such as a microcontroller, implements this control of the performance point of the memory 104 by interfacing with a clock circuit 108 to vary the frequency of a clock signal provided to the memory 104 and by interfacing with a power supply 106 to vary the voltage level being supplied to the memory 104. In some cases, the first and second thresholds are equal. In other cases, the second threshold is less than the first threshold to introduce an amount of hysteresis to the performance point control. Also, in certain embodiments, the method 200 includes causing the memory 104 to operate at the first performance point only when the detected usage is above the first threshold for at least a predetermined amount of time. Similarly, the method 200 may include causing the memory 104 to operate at the second performance point only when the detected usage

is below the second threshold for at least a predetermined amount of time.

[0020] FIG. 3 shows a system 300 to control a memory performance point. As shown, the system 300 includes monitoring engine 302 and a control engine 304. The monitoring engine 302 is connected to interconnect 103 and monitors a usage level of the interconnect 103. The control engine 304 is coupled to memory 104 and controls the performance point of the memory 104. The monitoring engine 302 and the control engine 304 are combinations of programming and hardware to execute the programming. Although shown separately, the monitoring engine 302 and the control engine 304 are not required to represent separate pieces of software programming. For example, each engine 302, 304 may share a common processor and memory, although this is not required. Also, the programming that enables the functionality of each engine 302, 304 may be included in the same executable file or library.

[0021] The monitoring engine 302 monitors transactions occurring on the interconnect 103 and, based on these transactions, detects a usage level of the interconnect 103. The monitoring engine transmits an indication of the usage level to the control engine 304. The control engine 304 causes the memory 104 to operate at: (a) a higher first performance point based on the detected usage level being above a first threshold; and (b) a lower second performance point based on the detected usage level being below a second threshold. As explained above, the second threshold is less than or equal to the first threshold.

[0022] FIG. 4 shows another example of a system 400 to control a memory performance point. The system 400 includes a storage resource 402 coupled to a processing resource 404. The processing resource 404 may be a single processor, a group of distributed processors, a single computer, or multiple computers. The storage resource 402 includes one or more local or distributed volatile storage devices (e.g., RAM) and/or non-volatile storage devices (e.g., HDD, flash storage) and includes a monitoring module 406 and a control module 408. Thus, the storage resource 402 and the processing resource 404 are hardware components of the system 400. The system 400 also includes an interconnect and a memory as above, but which are not shown for simplicity.

[0023] Each module 406, 408 represents instructions that, when executed by the processing resource 404, implement an associated engine. For example, when the monitoring module 406 is executed by the processing resource 404, the above-described monitoring engine 302 functionality is implemented. Similarly, when the control module 408 is executed by the processing resource

404, the above-described control engine 304 functionality is implemented. The modules 406, 408 may also be implemented as an installation package or packages stored on the storage resource 402, which may be a CD/DVD or a server from which the installation package may be downloaded.

[0024] Modifications are possible in the described embodiments, and other embodiments are possible, within the scope of the claims.

CLAIMS

What is claimed is:

1. A system, comprising:

a processor;

memory coupled to the processor by an interconnect, the memory configured to operate at least at first and second performance points, the first performance point having a higher performance than the second performance point; and

monitoring hardware coupled to the interconnect, the monitoring hardware configured to: monitor transactions on the interconnect to detect a usage level of the interconnect; and transmit an indication of the detected usage level to control logic;

the control logic configured to: based on the detected usage level being above a first threshold, cause the memory to operate at the first performance point; and based on the detected usage level being below a second threshold, cause the memory to operate at the second performance point; wherein the second threshold is equal to or less than the first threshold.

2. The system of claim 1 further comprising a clock circuit coupled to the memory to supply a clock signal to the memory, wherein the first and second performance points each include a frequency value, and wherein the control logic causes the clock circuit to:

generate a clock signal corresponding to the frequency value of the first performance point based on the detected usage level being above the first threshold; and

generate a clock signal corresponding to the frequency value of the second performance point based on the detected usage level being below the second threshold.

3. The system of claim 1 further comprising a power supply coupled to the memory to supply an operating voltage to the memory, wherein the first and second performance points each include a voltage value, and wherein the control logic causes the power supply to:

supply an operating voltage corresponding to the voltage value of the first performance point based on the detected usage level being above the first threshold; and

supply an operating voltage corresponding to the voltage value of the second performance point based on the detected usage level being below the second threshold.

4. The system of claim 1 wherein the control logic is further configured to:

based on the detected usage level being above the first threshold for at least a predetermined amount of time, cause the memory to operate at the first performance point; and

based on the detected usage level being below the second threshold for at least a predetermined amount of time, cause the memory to operate at the second performance point.

5. The system of claim 1 wherein the second threshold is less than the first threshold, and the control logic is further configured to:

cause the memory to transition from the first performance point to the second performance point based on the detected usage falling below the second threshold; and

cause the memory to transition from the second performance point to the first performance point based on the detected usage rising above the first threshold.

6. The system of claim 1 wherein the control logic includes software executed by the processor.

7. The system of claim 1 wherein the control logic includes one or more hardware logic elements separate from the processor.

8. The system of claim 7 wherein the one or more hardware logic elements include a state machine or a microcontroller.

9. The system of claim 1 wherein the usage level includes a utilization percentage or a bandwidth value.

10. A method, comprising:

monitoring transactions on an interconnect and detecting usage level of the interconnect, wherein the interconnect couples a memory to a processor;

based on the detected usage level being above a first threshold, causing the memory to operate at a first performance point; and

based on the detected usage level being below a second threshold, causing the memory to operate at a second performance point;

wherein the first performance point has a higher performance than the second performance point; and wherein the second threshold is equal to or less than the first threshold.

11. The method of claim 10 wherein the first and second performance points each include a frequency value, and the method further comprises:

generating, by a clock circuit coupled to the memory, a clock signal corresponding to the frequency value of the first performance point based on the detected usage level being above the first threshold; and

generating, by the clock circuit, a clock signal corresponding to the frequency value of

the second performance point based on the detected usage level being below the second threshold.

12. The method of claim 10 wherein the first and second performance points each include a voltage value, and the method further comprises:

supplying, by a power supply coupled to the memory, an operating voltage corresponding to the voltage value of the first performance point based on the detected usage level being above the first threshold; and

supplying, by the power supply, an operating voltage corresponding to the voltage value of the second performance point based on the detected usage level being below the second threshold.

13. The method of claim 10 further comprising:

based on the detected usage level being above the first threshold for at least a predetermined amount of time, causing the memory to operate at the first performance point; and

based on the detected usage level being below the second threshold for at least a predetermined amount of time, causing the memory to operate at the second performance point.

14. The method of claim 10 wherein the second threshold is less than the first threshold, and the method further comprises:

causing the memory to transition from the first performance point to the second performance point based on the detected usage falling below the second threshold; and

causing the memory to transition from the second performance point to the first performance point based on the detected usage rising above the first threshold.

15. A system, comprising:

hardware logic including monitoring logic and control logic, the monitoring logic configured to: monitor transactions on an interconnect between a processor and memory to detect a usage level of the interconnect; and transmit an indication of the detected usage level to the control logic;

the control logic configured to: based on the detected usage level being above a first threshold, cause the memory to operate at the first performance point; and based on the detected usage level being below a second threshold, cause the memory to operate at the second performance point; wherein the second threshold is equal to or less than the first threshold.

16. The system of claim 15 wherein the first and second performance points each include a

frequency value, and wherein the control logic causes a clock circuit coupled to the memory to:

generate a clock signal corresponding to the frequency value of the first performance point based on the detected usage level being above the first threshold; and

generate a clock signal corresponding to the frequency value of the second performance point based on the detected usage level being below the second threshold.

17. The system of claim 15 wherein the first and second performance points each include a voltage value, and wherein the control logic causes a power supply coupled to the memory to:

supply an operating voltage corresponding to the voltage value of the first performance point based on the detected usage level being above the first threshold; and

supply an operating voltage corresponding to the voltage value of the second performance point based on the detected usage level being below the second threshold.

18. The system of claim 15 wherein the control logic is further configured to:

based on the detected usage level being above the first threshold for at least a predetermined amount of time, cause the memory to operate at the first performance point; and

based on the detected usage level being below the second threshold for at least a predetermined amount of time, cause the memory to operate at the second performance point.

19. The system of claim 15 wherein the second threshold is less than the first threshold, and the control logic is further configured to:

cause the memory to transition from the first performance point to the second performance point based on the detected usage falling below the second threshold; and

cause the memory to transition from the second performance point to the first performance point based on the detected usage rising above the first threshold.

20. The system of claim 15 wherein the usage level includes a utilization percentage or a bandwidth value.

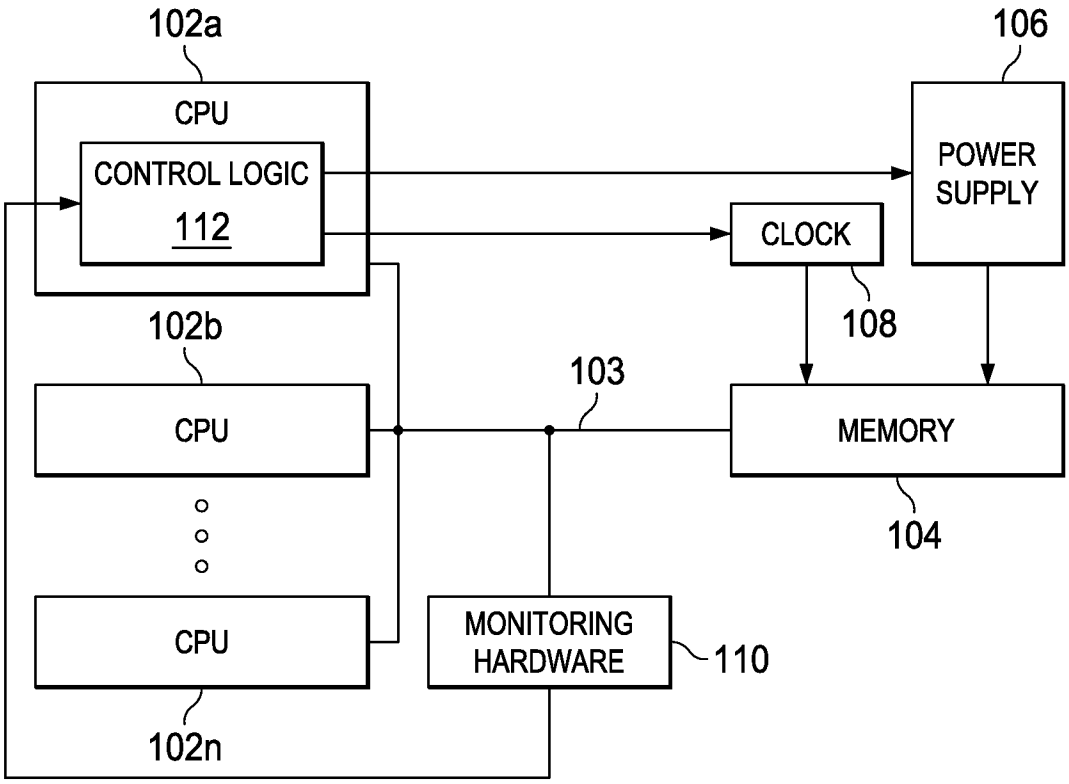

102a
CPU
CONTROL LOGIC
112
106
POWER SUPPLY
CLOCK
108
102b
CPU
103
MEMORY
104
CPU
MONITORING HARDWARE
110
102n

FIG. 1a

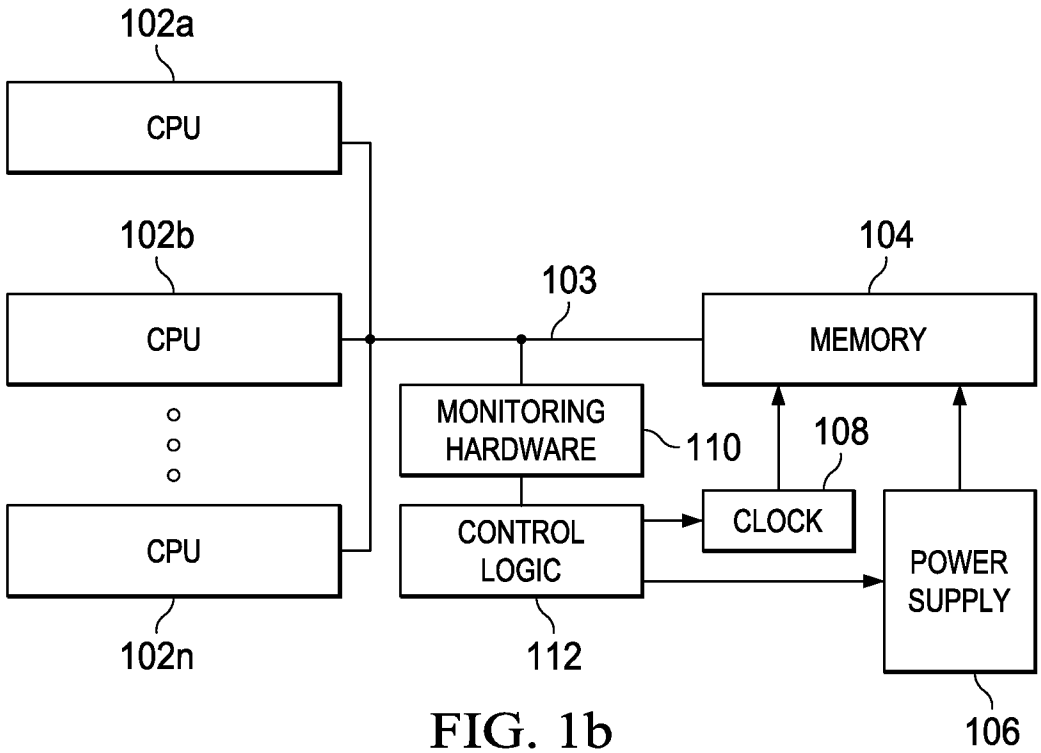

102a
CPU
102b
CPU
103
104
MEMORY
MONITORING HARDWARE
110
108
CLOCK
CPU
CONTROL LOGIC
POWER SUPPLY
102n
112
106

FIG. 1b

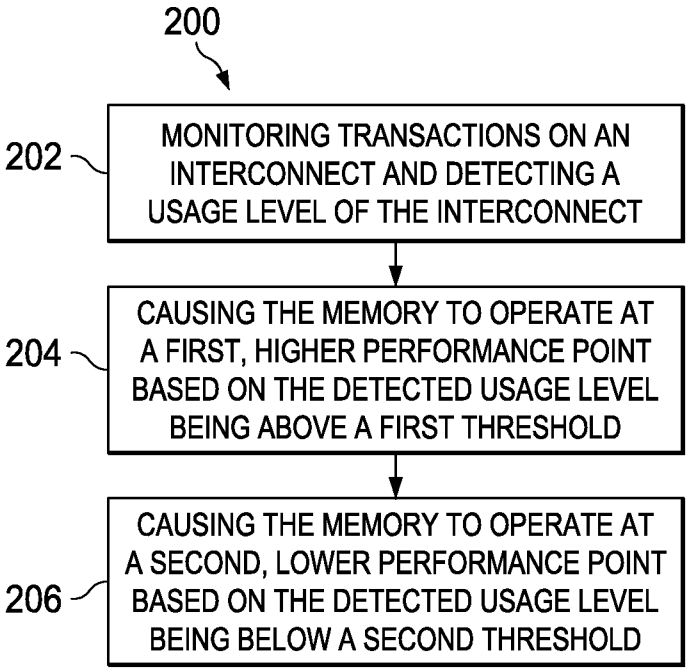


FIG. 2

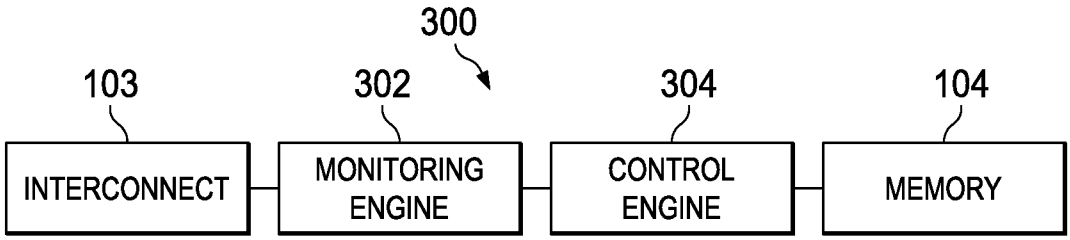


FIG. 3

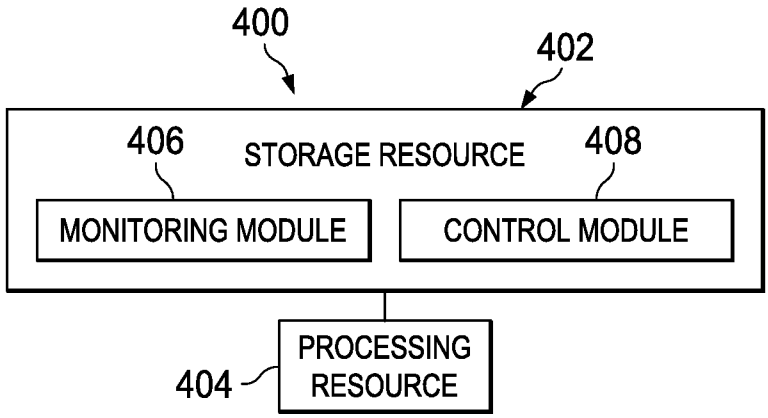


FIG. 4

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference TI-71729WO	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US 2015/028390	International filing date *(day/month/year)* 30 April 2015 (30.04.2015)	(Earliest) Priority Date *(day/month/year)* 30 April 2014 (30.04.2014)
Applicant TEXAS INSTRUMENTS INCORPORATED et al.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title,**

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings,**

   a. the figure of the drawings to be published with the abstract is Figure No. 1a

   ☒ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☐ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 2015/028390

A. CLASSIFICATION OF SUBJECT MATTER

G06F 11/30 *(2006.01)*
G06F 12/00 *(2006.01)*
G06F 13/16 *(2006.01)*

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 11/00, 11/30, 12/00, 13/00, 13/14, 13/16, 1/00, 1/04

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

PatSearch (RUPTO internal), USPTO, PAJ, K-PION, Esp@cenet, Information Retrieval System of FIPS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2009/0070605 A1 (DELL PRODUCTS L.P) 12.03.2009, abstract, paragraphs [0010]-[0014], [0016]-[0018], [0022]-[0027], fig. 1, 2	1, 3-7, 10, 12-15, 17-19
Y		2, 8, 9, 11, 16, 20
Y	US 2004/0139359 A1 (ERIC C. SAMSON et al.) 15.07.2004, paragraphs [0018], [0022]	2, 8, 11, 16
Y	US 2006/0179333 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 10.08.2006, paragraph [0032]	9, 20

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
24 August 2015 (24.08.2015)	03 September 2015 (03.09.2015)

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