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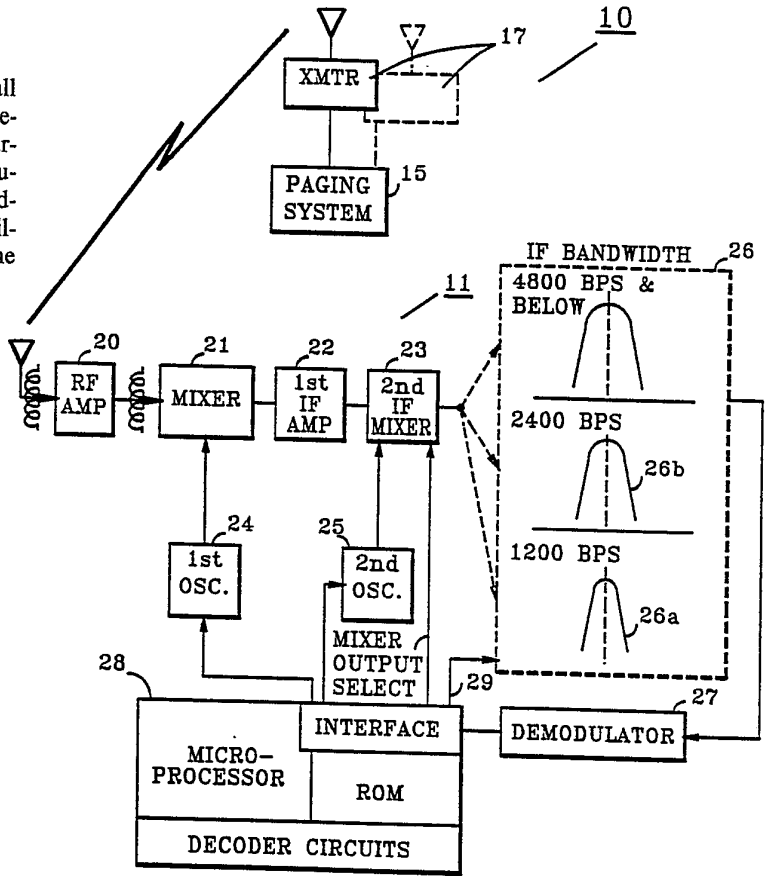
(54) Title: RECEIVER WITH VARIABLE PREDETECTION BANDWIDTH BASED ON EXPECTED DATA RATE

(57) Abstract

This invention relates to selective call receivers (11), such as paging receivers, for receiving modulated data signals having a variable bit rate. A band pass filter (26), particularly an I. F. filter, is provided having an adjustable bandwidth. The bandwidth of the filter is adjusted in accordance with a code in the received signal which indicates the bit rate.



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Receiver With Variable Predetection Bandwidth Based on Expected Data Rate

Background of the Invention

This invention relates to selective call receivers, such as paging receivers, employing variable data rates.

Current paging receivers operate on a variety of signaling code formats that can all be detected using a consistent (fixed) IF bandwidth. Examples of existing code formats and their respective bit rates in bits per second (BPS) are:

Motorola GSC:	300 BPS Address /600 BPS Message
POCSAG:	512 BPS
POCSAG:	1200 BPS
NEC D2, D3:	200 BPS
NEC D4:	512 BPS

It is within the performance capability of today's receivers and transmitters to achieve consistent system sensitivity at these low bit rates.

In order to achieve higher throughput of information, it is advantageous to use higher bit rates, for example 2400, 4800, and conceivably 9600 BPS. However, it would be desirable to provide a pager which could operate on existing paging systems, e.g. at 1200 BPS and could also operate at higher bit rates to give increased capacity for future system expansion. With the higher bit rate system operation there is a need to compensate for the loss in energy per bit by adding additional transmitters. These added transmitters fill in the coverage areas where the received signal is inadequate for acceptable higher bit rate operation. In this way, by adding further transmitters and increasing the bit rate, the capacity of the overall system can be increased substantially. In changing from 1200 to 4800 BPS, only an additional 6db of

signal is required to compensate for this loss whereas the throughput capacity is quadrupled. In addition, it would also be desirable to provide a paging system with the capability of paging different pagers at different bit rates, because greater range is achievable with lower bit rates. In order to achieve optimum range, for each system operation however, it is important to optimize the band width of the IF filter. The narrow bandwidth IF filter required at the lower bit rates would be unsuitable for the higher bit rates.

U. S. Patent 4,642,632 describes a paging system in which an address code is transmitted at a lower transmission rate than the message code. The receiver includes a low pass filter which filters the signal at the post-detection stage, immediately prior to the bit slicer. The low pass filter has a cut-off frequency switchable between the reception rate for the address and the reception rate for the message. This is done to maximize the paging code reception probabilities at both data rates.

Summary of the Invention

According to the invention, there is provided a selective call receiver and system and a method of operation thereof. The receiver comprises means for receiving a modulated data signal having a variable bit rate and including a code indicative of the bit rate; a demodulator; a bandpass filter for filtering the signal prior to demodulation in the demodulator, the bandpass filter having an adjustable bandwidth; and means for adjusting the bandwidth of the bandpass filter in response to the code received.

By this means, the bandwidth of the filter can be selected according to the bit rate of the received signal, as indicated by the code included in the signal. In this way, a signal having a low bit rate can be filtered through a narrow bandwidth filter, thereby giving a good signal-to-

noise ratio, while a higher bit rate requiring a wider bandwidth to prevent intersymbol interference can be filtered through a wider bandwidth filter.

The invention results in improved overall performance.

A preferred embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings.

Brief Description of the Drawings

Figure 1 shows a paging system having a transmitter and a receiver, in accordance with the invention.

Figure 2 shows the format of the signal transmitted by the transmitter of Figure 1.

Figure 3 shows the predetection filter of the receiver of Figure 1.

Detailed Description of the Invention

Referring to Figure 1, there is shown a paging transmitter 10 and a paging receiver 11. The transmitter 10 comprises a paging system controller 15 and one or more transmitters 17. The receiver 11 comprises an RF amplifier 20, a first mixer 21, a first IF amplifier 22 and a second mixer 23. First and second oscillators 24 and 25 provide signals to the first and second mixers 21 and 23 respectively. The first oscillator 24 is crystal controlled. A variable IF bandwidth filter is shown generally at 26, receiving an IF signal from second mixer 23 and passing the filtered signal to a demodulator 27. A microprocessor 28 is shown, with control lines connected to the second mixer 23, the oscillators 24 and 25 and the filter 26.

In operation, the transmitter 10 transmits a signal having the format shown in Figure 2. On this figure, there

is shown line 30 which illustrates on a small scale the structure of a complete frame of page data. The frame comprises a sync portion 31 followed by page data 32. The page data portion 32 may contain addresses and data for paging receivers. Together the blocks 31 and 32 comprise a single frame of page data. At the end of this frame, another frame begins, i.e. the sequence of sync portion and frame portion repeats itself.

At the bottom of Figure 2, sync portion 31 is shown in a larger scale, from which it can be seen that portion of the frame comprises a settling signal A, bit/word sync signal B, and a frame information signal C.

Settling signal A includes at least 24 bits which provides time for receiver stabilization. The 24 bits may consist of an alternating "1" "0" pattern. The bit/word sync signal B, may consist of a 32 bit predetermined pattern which provides for bit synchronization and frame synchronization. The frame information signal C comprises a 32 bit code word which is structured as a 31,21 BCH code word with one additional bit of parity. Thus, the frame information signal C has 21 information bits which may be made up as follows:

6 BITS - FRAME NUMBER (00-63)
3 BITS - FRAME SPEED (600,1200,2400,4800,9600,19.2K, 38.4K,X)
12 BITS - SPARES

It can be seen that the frame information signal includes a signal which indicates the frame speed. This signal is comprised within three bits which are capable of indicating 8 speeds, these being 600, 1200, 2400, 4800, 9600, 19.2K and 38.4K, with capacity for one further speed. In the remainder of the description which follows, the case will be described where only the speeds 1200, 2400 and 4800 BPS are used.

The system operates as follows. The transmitter puts together the sync portion of the frame in controller 15. Depending on the volume of traffic and/or other factors, the controller 15 will determine the three bits within frame information signal which indicate the frame speed. The transmitter 17 transmits the sync portion 31 of the frame at a predetermined speed of 1200 bits per second. Corresponding to the beginning of the first block of portion 32, the transmitter 17 switches to the bit rate of the frame, for example 2400 BPS, and the remainder of the frame 32 is transmitted at the higher bit rate.

The receiver 11 receives this signal, which is amplified in amplifier 20, mixed down to an IF frequency by mixer 21 and oscillator 24, amplified in amplifier 22, further mixed down in the frequency by mixer 23 and oscillator 25, and then filtered by filter 26. The filtered signal from filter 26 is demodulated at 1200 BPS in demodulator 27, and the bit stream derived from the signal is fed to microprocessor 28. On receipt of the frame info code word D or E, microprocessor 28 identifies the bit rate of the forthcoming frame, whereupon it adjusts the bandwidth of IF filter 26 via control line 29. In response to a signal from control line 29, filter 26 changes its bandwidth. In the present case, with the forthcoming frame bit rate determined as 2400 BPS, and the rate of the sync portion being 1200 BPS the filter 26 switches from the narrow bandwidth 26a to the intermediate bandwidth 26b. This is necessary because the narrow bandwidth, while giving better signal-to-noise at 1200 BPS, is too narrow for a 2400 BPS signal. One possible manner in which this change is implemented is illustrated in Figure 3.

Referring to that figure, three ceramic filters are shown 40, 41 and 42. Filter 40 has a typical bandwidth of 5.5 KHz + or - 10%. Filter 41 has a typical bandwidth of

8.25 KHz + or - 10% and filter 42 has a typical bandwidth of 11 KHz + or - 10%. A CMOS analog switch 43 is provided of the type MC14066B. The filter circuits 26 receives inputs from the second mixer 23 and provide the inputs to the filters 40,41 and 42. There is a three-bit control line 29 from the microprocessor 28 to the switch 43. The outputs of the filters 40, 41 and 42 are connected to an IF amplifier 45, which is connected to the demodulator 27.

The filter operates as follows. On receipt of the frame speed code (1200 BPS), the microcomputer 28 provides a signal on control line 29 which operates analog switch 43 to remain connected to IF amp 45 from filter 40 for continued 1200 BPS operation. In this instance filters 41 and 42 are isolated from the IF amp 45.

If the frame speed is to be changed from 1200 BPS to 4800 BPS, the microcomputer 28 receives the appropriate frame speed code, and causes the switch 43 to disconnect filter 40 and connect the IF amp 45 to the filter 42. In this instance, filters 40 and 41 are isolated from the circuit.

The demodulator 27 acts as a frequency discriminator, and the possible choices could be: at the bit rate of 1200, the high and low bit frequencies are at the carrier frequency + or -2.2KHz, at the bit rate of 2400 BPS, the frequencies are carrier + or -3.8 KHz. At 4800 BPS, the frequencies are carrier + or -4.5 KHz.

It should be understood that there may be numerous other ways of implementing the invention, particularly in implementing the variable bandwidth filter 26. It will also be appreciated that the filter 26, may be capable of providing two bandwidths only, or more than three bandwidths, and for example wider bandwidths may be provided for higher bit rates such as 9600 BPS, 19.2 K and 38.4 K. It should be further appreciated that the receiver

of the present invention may alternately be constructed with a single intermediate frequency, thereby eliminating elements 22, 23 and 25 from Figure 1. Alternately, more than two intermediate frequencies may be used.

What is claimed is:

Claims

1. A selective call receiver, comprising:

means for receiving a modulated data signal having a variable bit rate and including a code indicative of the bit rate;

a demodulator;

a bandpass filter for filtering the signal prior to demodulation in the demodulator, said bandpass filter having an adjustable bandwidth; and

means for adjusting the bandwidth of the bandpass filter in response to the code received.

2. The receiver of claim 1, wherein said means for adjusting the filter bandwidth are arranged to change the bandwidth a predetermined first time after receipt of the code.

3. The receiver of claim 2, wherein said means are arranged to increase the bandwidth at said first time from a narrower to a wider bandwidth.

4. The receiver of claim 3 wherein means are provided for switching the receiver from a lower to a higher bit rate receive mode at substantially the same time as said first time.

5. The receiver of claim 4 wherein means are provided for returning the receiver to said lower bit rate receive mode at a predetermined second time after said first time and for restoring the filter bandwidth from said wider to said narrower bandwidth at substantially the same time as said second time.

6. The receiver of claim 1 wherein said filter is arranged to provide a bandwidth selectable to correspond to at least two different bandwidths.

7. The receiver of claim 1, wherein said adjustable bandwidth filter comprises at least two discrete filters and switching means for directing the signal through a selected one thereof.

8. The receiver of claim 8 wherein the discrete filters are ceramic filters.

9. A selective call system, comprising:

a transmitter for transmitting a modulated data signal, said transmitter including means for selecting a bit rate for the signal, and means for including a code in said signal indicating the bit rate determined;

a selective call receiver for receiving the signal including the code, said receiver having a demodulator and a bandpass filter for filtering the signal prior to demodulation in the demodulator, said bandpass filter having an adjustable bandwidth; said receiver also having means for adjusting the bandwidth of the bandpass filter in response to the code received.

10. A method of operation of a selective call system, comprising the steps of:

transmitting a modulated data signal at a bit rate selected from a plurality of bit rates, said signal including a code indicating the bit rate;

receiving the signal at a selective call receiver having a demodulator and a bandpass filter for filtering the signal prior to demodulation in the demodulator, said bandpass filter having an adjustable bandwidth; and

adjusting the bandwidth of the bandpass filter in response to the code received.

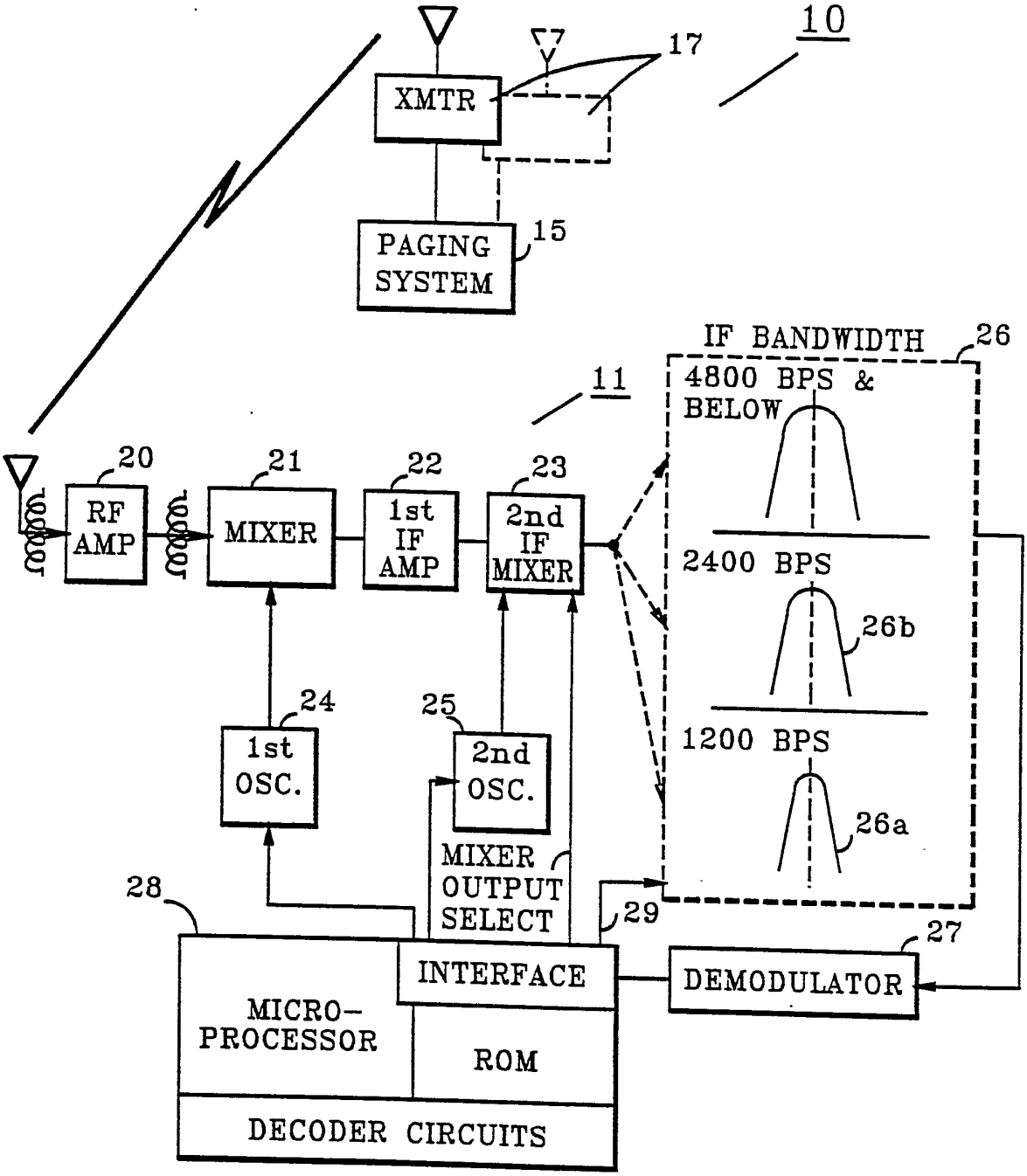
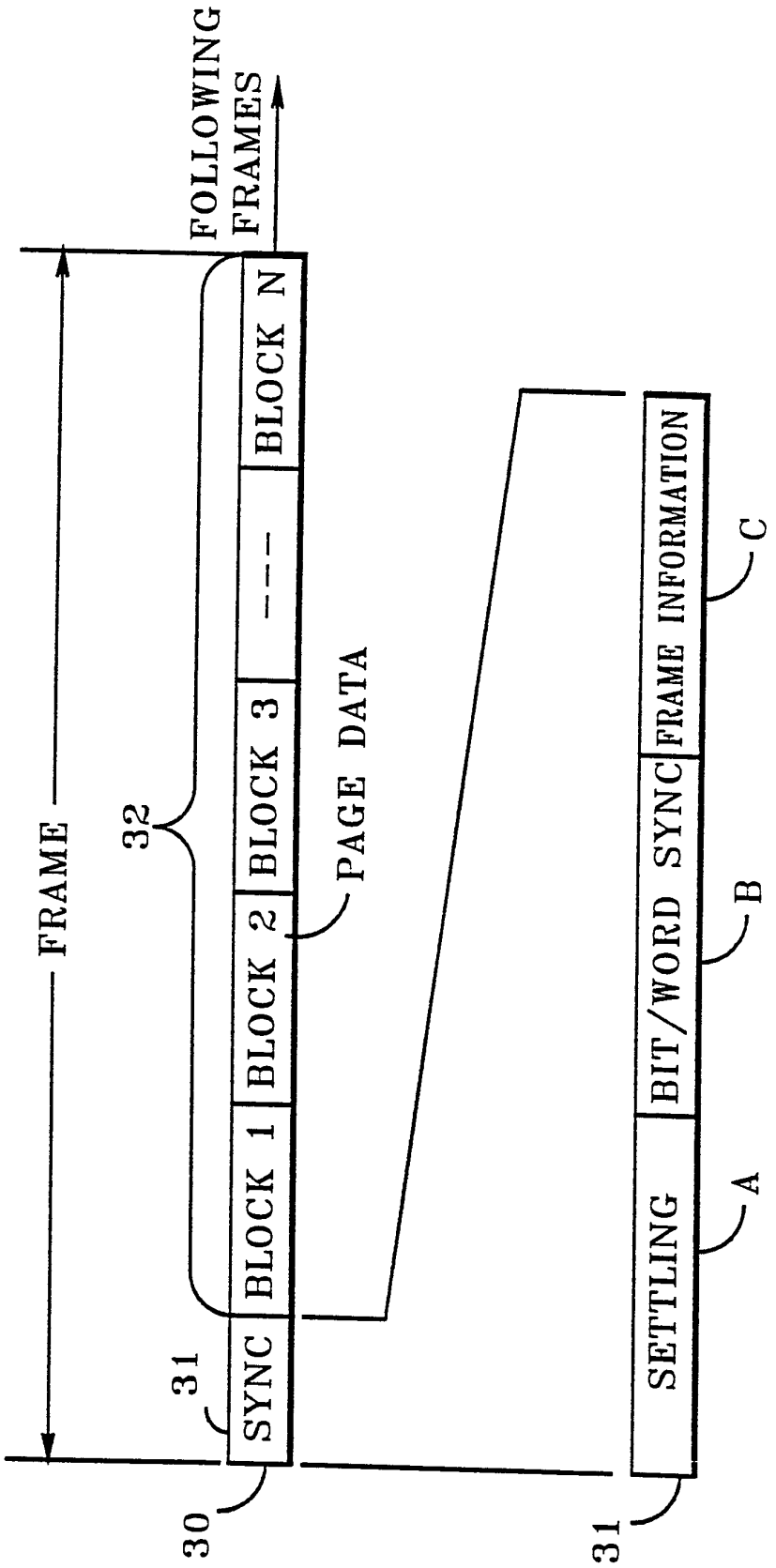

10
17
XMTR
PAGING SYSTEM
15
IF BANDWIDTH
26
11
4800 BPS & BELOW
2400 BPS
26b
1200 BPS
26a
20
RF AMP
21
MIXER
22
1st IF AMP
23
2nd IF MIXER
24
1st OSC.
25
2nd OSC.
MIXER OUTPUT SELECT
28
29
27
INTERFACE
DEMODULATOR
MICRO-PROCESSOR
ROM
DECODER CIRCUITS

FIG. 1


FOLLOWING FRAMES
FRAME
32
SYNC
BLOCK 1
BLOCK 2
BLOCK 3

BLOCK N
PAGE DATA
31
30
SETTLING
BIT/WORD SYNC
FRAME INFORMATION
A
B
C
31

FIG. 2

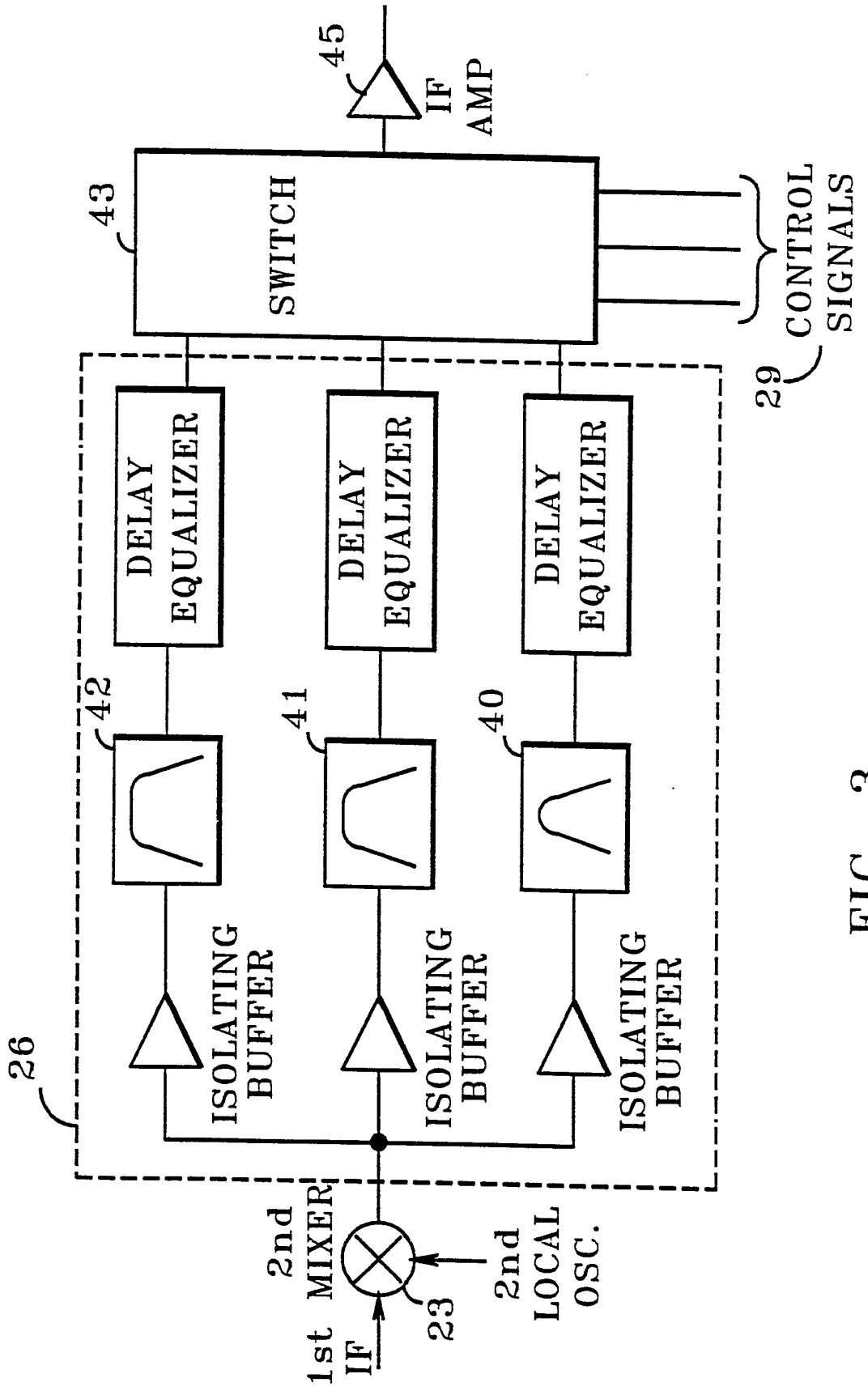

45
IF AMP
43
SWITCH
CONTROL SIGNALS
29
DELAY EQUALIZER
DELAY EQUALIZER
DELAY EQUALIZER
42
41
40
ISOLATING BUFFER
ISOLATING BUFFER
ISOLATING BUFFER
26
2nd MIXER
1st IF
23
2nd LOCAL OSC.

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/02679

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) 3

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): H04B 1/10
U.S.Cl.: 455/266

II. FIELDS SEARCHED

Minimum Documentation Searched 4

Classification System	Classification Symbols
U.S.	455/138,228,266; 370/84; 340/825.44

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched 5

III. DOCUMENTS CONSIDERED TO BE RELEVANT 14

Category *	Citation of Document, 16 with indication, where appropriate, of the relevant passages 17	Relevant to Claim No. 18
Y	U.S., A, 4,816,820 (DAVIS) 28 March 1989 col. 4, lines 52-60; col. 6, lines 18-43	1-10
A	U.S., A, 4,642,632 (OHYAGI et al.) 10 February 1987 See abstract	
A	U.S., A, 4,008,373 (NASH et al.) 15 February 1977 col. 1, lines 24-37	

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IV. CERTIFICATION

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27 July 1990	19 OCT 1990
International Searching Authority 1	**Signature of Authorized Officer 20**
ISA/US	for Edward Urban NGUYEN NGOC-HO INTERNATIONAL DIVISION

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