A lamp control circuit useful as a lamp flasher, dimmer or timer and to obtain stroboscopic or other unusual lighting effects. The circuit includes a switch which alternates between two stable states with the dwell time in each state established by a respective interval timing circuit. Power from an ac source is supplied to the lamp by a controlled rectified gated via one of two diacs. The first diac conducts when the voltage across a first capacitor, charged from the ac source, exceeds a certain level and when the switch is in one state. When the switch is in the other state, a discharge circuit maintains the capacitor charge below the diac threshold level. During this time, however, the second diac can gate on the rectifier when the voltage across an associated capacitor, charged from an adjustable voltage source, is sufficiently great. In a flasher mode the switch continuously alternates between states, the circuit providing separate control of the lamp bright and dim time interval and of the dim light intensity. Unusual lighting effects are obtained when the switch dwell time in each state is less than the ac source period.

10 Claims, 1 Drawing Figure
1 LAMP CONTROL CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a lamp control circuit for intermittently changing the intensity level of an incandescent or fluorescent lamp. The circuit is useful as a lamp flasher, dimmer, timer or stroboscope control, and to provide other unusual lighting effects.

2. Description of the Prior Art

A wide variety of applications exist for lamps exhibiting intermittently changing intensity levels. Such lamps may be used to attract attention, as in a sign or advertising display; for decorative or aesthetic effect, as in twinkling Christmas tree lights; and for functional purposes such as timing in an educational game or a stroboscope. In the past, no lamp control device has been available having the versatility for implementing all of these functions, and it is an object of the present invention to provide such a circuit which is operative with either incandescent or fluorescent lamps.

Most prior art lamp flashers merely switch on and off the power to the lamp. The lamp alternates between conditions of maximum brightness and no light output. The resultant display lacks the unusual, aesthetically pleasing effect achieved when a lamp alternates between two different intensity levels, one mode of operation implemented by the present invention.

Another shortcoming of prior art lamp flashers is a lack of control over the time duration that the lamp is on or off. Thus, many lamp flashers employ a fixed, periodic cycle with identical on and off times. The result is a monotonous blinking of the lights. Other devices utilize thermostatic type switches which open or close for short periods of time when a heater reaches a certain temperature. Random blinking is achieved.

In contradistinction, the present invention facilitates independent control of the time intervals during which the lamp is at each intensity level. Thus, in an advertising display a lamp may be maintained at a bright level for a relatively long period, then switched to a dim level for a very short time interval. In another application, Christmas tree lights can be adjusted to glow dimly, with sudden bright flashes; a twinking effect is produced.

The independent time interval adjustment feature permits the present invention to be used for stroboscopic control of a lamp. In another application, the circuit may be used in conjunction with an educational game. Thus the lamp may illuminate a question for a selected period of time. At the end of this interval, the lamp intensity is reduced so that the question no longer can be seen. The off interval, during which time the question must be answered, can be separately controlled. Thus, e.g., the student may have five seconds to read the question, and one second to provide the answer. At the end of the answer time, the light comes on again to illuminate another, or perhaps the same, question. In an alternative embodiment, a second lamp may be lit during the answer period, telling the student that he must answer the question. The second lamp could illuminate the correct answer.

In still another mode of operation the present invention can be used to provide unusual, "psychedelic" lighting effects. For example, a fluorescent lamp can be made to flash at rates greater than the ac source frequency. The flashing rate may be asynchronous with the line frequency, producing unique optical beat effects.

SUMMARY OF THE INVENTION

The foregoing objectives are achieved by providing a lamp control circuit including a switch which alternates between two stable states with the dwell time in each state established by a respective interval timing circuit. Power from an ac source is supplied to an incandescent or fluorescent lamp via a controlled rectifier which is gated on by one of two diac circuits, depending on the setting of the bistable switch.

The first diac supplies a rectifier gating signal when the voltage across a first capacitor charged from the ac source exceeds a certain level and when the switch is in a first stable state. When the switch is in the second state, a discharge circuit maintains the capacitor charge below the diac threshold level. During this time, however, the second diac can gate on the controlled rectifier when the voltage across a second capacitor is sufficiently great. A potentiometer controls the voltage used to charge the second capacitor. Thus, the potentiometer setting may establish the lamp intensity level when the switch is in the second state.

The bistable switch itself includes a pair of transistors connected so that one conducts when the other is off. Separate interval timing circuits, each including a capacitor charged via a resistor from an adjustable voltage source, are associated with the transistors. These circuits independently establish the dwell times of the switch in the two stable states.

The discharge circuit includes a complementary pair of transistors connected in series. The base of one transistor receives an input only when the switch is in the second stable state. The base of the other transistor is grounded. A pair of diodes connect the first capacitor to the otherwise unconnected, non-control elements of the complementary transistors. The diodes are oriented to accomplish discharge of the capacitor regardless of the charge polarity.

BRIEF DESCRIPTION OF THE DRAWING

A detailed description of the invention will be made with reference to the accompanying drawing.

FIG. 1 is an electrical schematic diagram of a lamp flasher in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The following detailed description is of the best presently contemplated mode of carrying out the invention. This description is not to be taken in a limiting sense, but is made merely for the purpose of illustrating the general principles of the invention, since the scope of the invention best is defined by the appended claims.

Referring now to the drawing, the inventive lamp control circuit 10 is connected to an ac source by a plug 11, and supplies power from this source to a lamp or other load via a socket 12. The power thus supplied alternates between two levels under control of a bistable switch generally designated 13. When the switch 13 is in one stable state, the setting of a potentiometer 14 establishes the level of power supplied to the load. Separate potentiometers 15, 16, independently control the
In an illustrative mode of operation, the switch \( 13 \) dwell time in each state may be longer than the ac source period. With the dwell times so adjusted, the lamp will alternate between maximum intensity when the switch \( 13 \) is in the first (“bright”) state, and a level of lesser intensity, established by the potentiometer \( 14 \), when the switch \( 13 \) is in the second (“dim”) state. The potentiometers \( 15, 16 \) respectively control how long the lamp remains at the bright and dim intensity levels.

One line \( 20 \) from the ac source is connected directly to the terminal \( 12a \) of the socket \( 12 \). The other line \( 21 \) from the ac source is connected via a fuse \( 22 \) and a triac \( 23 \) or like controlled rectifier to the terminal \( 12b \) of the socket \( 12 \). The triac \( 23 \) is controlled by a signal supplied via a line \( 24 \) to the triac gate. When the switch \( 13 \) is in the first state, this signal is provided by a circuit \( 25 \); with the switch \( 13 \) in the second state, the triac \( 23 \) is controlled by a circuit \( 26 \) including the potentiometer \( 14 \).

The potentiometer \( 14 \) is connected in series with a current limiting resistor \( 27 \) across the triac \( 23 \). The potentiometer tap \( 14a \) is connected to the gate of the triac \( 23 \) via a diac \( 28 \) and a current limiting resistor \( 29 \), and to a capacitor \( 30 \). The capacitor \( 30 \) is charged to a voltage level adjusted by the potentiometer \( 14 \). The diac \( 28 \) conducts when the voltage across the capacitor \( 30 \) exceeds a certain threshold level (typically on the order of 5 to 10 volts). Accordingly, a gating signal may be supplied to the line \( 24 \) during a portion of each ac half cycle established by the setting of the potentiometer \( 14 \). The triac \( 23 \) goes into conduction when a gating signal is present on the line \( 24 \), thereby supplying power to the load for the remainder of the ac half cycle.

The circuit \( 25 \) similarly includes a diac \( 33 \) connected to the triac control line \( 24 \) via a current limiting resistor \( 34 \). When the switch \( 13 \) is in the first state, an ac signal from the line \( 20 \) charges a capacitor \( 35 \) via a capacitor \( 36 \) and a line \( 37 \). When the voltage across the capacitor \( 35 \) exceeds the threshold level of the diac \( 33 \), a gating signal is supplied to the triac \( 23 \). When the switch \( 13 \) dwell times are adjusted to be greater than the ac period, this diac \( 33 \) gating signal occurs near the beginning of each ac half cycle, causing the triac \( 23 \) to conduct for most of each ac cycle, thereby supplying the load with maximum power.

When the switch \( 13 \) assumes the second state, a circuit \( 25a \) maintains the capacitor \( 35 \) discharged so that the diac \( 33 \) does not conduct, and no output signal is provided by the circuit \( 25 \). During this interval, conduction of the triac \( 23 \) is controlled by the circuit \( 26 \) as described above.

With the switch \( 13 \) in the second state, a positive signal is provided on a line \( 38 \) to the discharge circuit \( 25a \). During each ac half cycle that the source power on the line \( 20 \) is positive, the switch \( 13 \) output signal is supplied via a resistor \( 39 \) to the base of an NPN transistor \( 40 \), causing that transistor to conduct.

Thus whenever the transistor \( 40 \) conducts during a positive half of the ac cycle, the positive charge on the capacitor \( 35 \) rapidly is discharged to ground via a resistor \( 41 \), a diode \( 42 \), the transistor \( 40 \) and the emitter-to-base path through a grounded base PNP transistor \( 43 \). During the negative half of each ac cycle, the capacitor \( 35 \) is discharged via the resistor \( 41 \), another diode \( 44 \) and the collector-to-base path through the transistor \( 43 \). Thus, the capacitor \( 35 \) remains discharged and no gating signal is supplied via the diac \( 33 \) as long as the switch \( 13 \) is in the second state.

When the switch \( 13 \) assumes the first state, the line \( 38 \) is held near ground, the transistor \( 40 \) remains off, and the capacitor \( 35 \) can charge sufficiently to provide a triac gating signal via the diac \( 33 \) as discussed above.

The bistable switch \( 13 \) itself operates in a manner not unlike a free-running multivibrator. Thus the switch \( 13 \) includes a pair of transistors \( 51, 52 \) which alternate continuously between the first state in which the transistor \( 51 \) is off and the transistor \( 52 \) is on, and the second state in which the transistor \( 51 \) is on and the transistor \( 52 \) is off. The dwell times in the first and second states are controlled by interval timing circuits \( 53 \) and \( 54 \) respectively including the potentiometers \( 15 \) and \( 16 \).

When the switch \( 13 \) assumes the first state, the transistor \( 52 \) goes on. As a result, the line \( 38 \) drops to ground potential, biasing the base of the transistor \( 51 \) to ground via a resistor \( 55 \); the transistor \( 51 \) goes off. The potentiometer \( 15 \) is connected between a positive supply line \( 56 \) and ground, so that a positive voltage is provided at the potentiometer tap \( 15a \). This voltage begins to charge a timing capacitor \( 57 \) via a resistor \( 58 \) connected by a line \( 59 \) to one terminal of the capacitor \( 57 \). The other capacitor \( 57 \) is connected to the line \( 38 \), and thus is held at ground potential.

As the capacitor \( 57 \) charges, the voltage on the line \( 59 \) becomes increasingly positive. This line \( 59 \) also is connected via a diode \( 60 \) and a resistor \( 61 \) to the base of the transistor \( 51 \). Thus as the capacitor \( 57 \) charges, the voltage at the transistor \( 51 \) base goes more positive, eventually reaching a level sufficiently high so as to bias the transistor \( 51 \). When this occurs, the collector voltage of the transistor \( 51 \), on a line \( 62 \), drops from a positive value to ground. Since the line \( 62 \) is connected via a resistor \( 55' \) to the transistor \( 52 \) base, that transistor goes off. The switch \( 13 \) thus slips from the first to the second state.

The setting of the potentiometer \( 15 \) will establish the voltage level supplied via the resistor \( 58 \) to charge the capacitor \( 57 \). Accordingly, the setting of the potentiometer \( 15 \) will control how soon the transistor \( 51 \) is turned on, and thus will establish the interval or dwell time during which the switch \( 13 \) remains in the first state. The second interval timing circuit \( 54 \) functions in a manner exactly analogous to the timing circuit \( 53 \) (and includes components identified by corresponding primed numbers). The setting of the potentiometer \( 16 \) controls the voltage level used to charge the capacitor \( 57' \) and thus establishes the timer interval taken to turn on the transistor \( 52 \).

The transistor \( 51 \) collector voltage is provided by a divider including the resistors \( 64, 65 \) series connected between the line \( 56 \) and ground. Collector voltage to the transistor \( 52 \) is supplied via a resistor \( 66 \). A speed-up capacitor \( 67 \) connected between the collectors of the transistors \( 51, 52 \) completes the switch \( 13 \) circuit.

Power to the switch \( 13 \) is supplied by single diode \( 70 \) connected in series with a current limiting resistor \( 71 \) between the voltage supply line \( 20 \) and the line \( 56 \). A capacitor \( 72 \) provides some filtering for the otherwise
pulsating dc supplied on the line 56 during each ac half cycle that the line 20 is positive.

If the first timing potentiometer 15 is set at a minimum and the second timing potentiometer 16 set at a maximum, the switch 13 essentially will remain set in the second ("dim") state. Under this condition, power supplied via the socket 12 is controlled entirely by the potentiometer 14. The potentiometer 14 thus can be used as a dimmer, to control the constant light level from a lamp connected to the socket 12.

The device 10 can be used with either an incandescent or a fluorescent lamp. When flashing a fluorescent lamp, the potentiometer 14 is adjusted to a level which will maintain ionization when the switch 13 is in the "dim" state. When the switch 13 flips to the "bright" state, the fluorescent lamp will go to full intensity. The lamp will continue to flash at the duty cycle established by the interval timing potentiometers 15 and 16.

The discharge circuit 25ε is extremely fast acting. Thus the circuit 10 will operate effectively when the dwell time in either or both switch 13 stable states is less than the ac source period. With the switch 13 dwell times so adjusted, the triac 23 may be gated into conduction by either of the circuits 25, 26 during each ac half cycle, depending on whether the capacitor 35 or the capacitor 36 first reaches dcic threshold level. As a result, unusual lighting effects are achieved, which may include flashing at a beat frequency related to the difference between the ac source frequency and the switch 13 alternation rate.

As an optional feature, the device 10 also may supply power to a second lamp or other load under timing control of the same switch 13. The circuit shown at the bottom of FIG. 1 facilitates such operation.

The second lamp is connected to a socket 12' having a first terminal 12α' connected to the ac line 20, and a second terminal 12β' connected via a triac 23' to the ac source line 21. The triac 23' is controlled by circuits 25' and 26' identical to the circuits 25, 26 described above.

Note that the input to the circuit 25' is connected to the line 62 of the switch 13. As a result, the triac 23' gating signal will be provided by the circuit 25' when the switch 13 is in the second state. With the switch 13 in the first state, the gating signal on the line 24' will be established by the setting of a potentiometer 14' associated with the circuit 26'. Thus, if two lamps are connected to the respective sockets 12 and 12', the lamps will flash in unison, but one lamp will become bright when the other goes dim, and vice versa.

The inventive lamp control circuit can be employed advantageously in an educational game. Thus a lamp connected to the socket 12 will go on to illuminate brightly a question to be answered. How long the question may be studied is adjusted by the potentiometer 15. At the end of the study period, the question lamp goes off and a second lamp, connected to the socket 12' goes on indicating that the question must be answered. The answer period is controlled by the potentiometer 16. Programmed learning is enhanced.

Intending to claim all novel, useful and unobvious features shown or described, the applicant claims:

1. A lamp control circuit comprising:
   a controlled rectifier connecting an ac power source to said lamp,
   switch means alternating between first and second stable states,

2. A control circuit according to claim 1 wherein said discharge circuit comprises:
   a first gating circuit including a first capacitor charged from said source, a first diac operatively connecting said first capacitor to the control electrode of said rectifier, said first gating circuit gating said rectifier into conduction when the voltage across said first capacitor exceeds a threshold level, and a discharge circuit connected to inhibit charging of said capacitor when said switch means is in said second state, so that said first gating circuit can gate said rectifier into conduction only when said switch means is in said first state, and
   a second gating circuit including a second capacitor, a second diac operatively connecting said second capacitor to the control electrode of said rectifier, and potentiometer means connected to said ac source to provide an adjustable voltage for charging said second capacitor, said second gating circuit gating said rectifier into conduction when the voltage across said second capacitor exceeds said threshold value and when said switch means is in said second state in which said first capacitor is discharged.

3. A control circuit according to claim 1 wherein said switch means comprises:
   first and second transistors connected so that one conducts when the other is off, and
   a separate interval timing circuit associated with each transistor and operative to turn on that associated transistor after the other transistor has been on for a selectable interval of time.

4. A control circuit according to claim 3 wherein the interval timing circuit associated with each transistor comprises:
   a capacitor having one terminal connected to a non-control element of the other transistor,
   means supplying a selectable voltage via a resistor to the other terminal of said capacitor, the values of said capacitor, said resistor, and said selectable voltage establishing said interval of time, unidirectionally conducting means connecting said capacitor other terminal to the control electrode of the associated transistor, and
   a resistor connected between said associated transistor control electrode and said other transistor non-control element.

5. A device according to claim 1 wherein said load comprises an incandescent or a fluorescent lamp.

6. A control circuit according to claim 1 and adapted to supply power to two lamps, further comprising:
   another controlled rectifier connecting said ac source to the second lamp,
   a third gating circuit for gating said other rectifier into conduction when the voltage across a third ca-
7. A lamp control circuit comprising:

a source of ac power connected to said load via a controlled rectifier;

a first gating means for initiating conduction of said rectifier when a signal derived from said source exceeds a certain value, said first gating means including a first capacitor charged from the ac source to provide said derived signal, and a first diac operatively connected between said first capacitor and the control electrode of said rectifier;

a second gating means comprising a potentiometer connected to said source to provide an adjustable voltage, a second capacitor charged by said adjustable voltage, and a second diac operatively connected between said second capacitor and said rectifier control electrode, said second gating means initiating conduction of said rectifier at a phase angle of the ac cycle established by the magnitude of said adjustable voltage, switch means continuously alternating between two stable states and having separate interval timing means to establish the respective dwell time in each of said stable states, and

disable circuit means, comprising a circuit discharging said first capacitor when said switch means is in one of said stable states, for preventing said first gating means from initiating conduction of said rectifier when said switch means is in said one stable state.

8. A control circuit according to claim 7 wherein said controlled rectifier comprises a triac connected in series with one line between said ac source and said load.

9. A control circuit according to claim 8 wherein said switch means comprises first and second transistors operatively connected so that one transistor conducts when the other is off, each interval timing means comprising:

a capacitor charged through a resistor by a voltage of controllable magnitude, said capacitor being connected between the non-control electrode of one transistor and a diode leading to the control electrode of the other transistor, another resistor shunting said diode and said capacitor.

10. A control circuit according to claim 7 wherein said switch means is powered by substantially unfiltered dc voltage supplied during half of each ac source cycle by a single diode.

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