



- (51) International Patent Classification:
H03M 1/00 (2006.01) *H03M 1/74* (2006.01)
- (21) International Application Number:
PCT/US2018/027792
- (22) International Filing Date:
16 April 2018 (16.04.2018)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
15/488,931 17 April 2017 (17.04.2017) US
- (71) Applicant: **CIRRUS LOGIC INTERNATIONAL SEMICONDUCTOR, LTD.** [GB/GB]; 7B Nightingale Way, Quartermile, Edinburgh EH3 9EG (GB).
- (72) Inventor; and
(71) Applicant (for US only): **DAS, Tejasvi** [IN/US]; 14521 Ballimamore Drive, Austin, Texas 78717 (US).
- (72) Inventors: **ZHAO, Xin**; 2600 Golden Gate Park, Austin, Texas 78732 (US). **MELANSON, John L.**; 901 W. 9th Street, #201, Austin, Texas 78703 (US).
- (74) Agent: **PREWITT, Brian K.** et al.; JACKSON WALKER L.L.P., 100 Congress Avenue, Suite 1100, Austin, Texas 78701 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME,

(54) Title: FULLY-DIFFERENTIAL CURRENT DIGITAL-TO-ANALOG CONVERTER

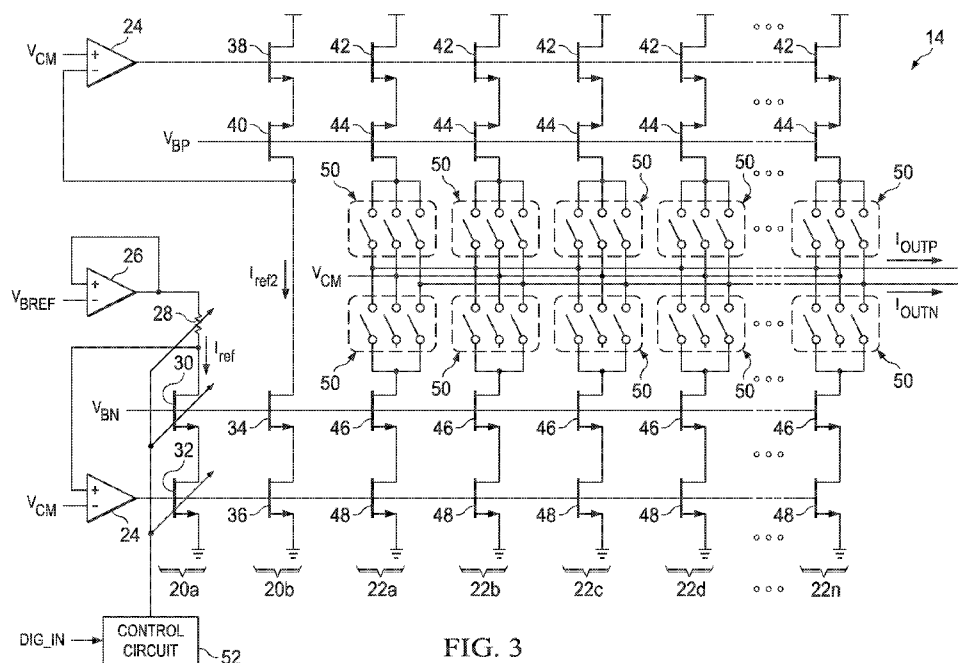


FIG. 3

(57) Abstract: A playback path may include an input configured to receive an input signal, an output configured to drive a differential output signal, a differential current-mode digital-to-analog converter configured to convert the input signal into the differential output signal, and a control circuit. The differential current-mode digital-to-analog converter may include a plurality of current-mode digital-to-analog elements configured to be selectively enabled and disabled based on the input signal and at least one reference element in a current mirror relationship with the plurality of current-mode digital-to-analog elements such that each individual current through each current-mode digital-to-analog element is a scaled version of a reference current of the at least one reference element. The control circuit may be configured to scale current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements based on a characteristic of the input signal.

MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ,
OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA,
SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States** (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
-

FULLY-DIFFERENTIAL CURRENT DIGITAL-TO-ANALOG CONVERTER**FIELD OF DISCLOSURE**

The present disclosure relates in general to circuits for audio devices, including
5 without limitation personal audio devices, such as wireless telephones and media players,
and more specifically, to systems and methods relating to a fully-differential digital-to-
analog converter.

BACKGROUND

10 Personal audio devices, including wireless telephones, such as mobile/cellular
telephones, cordless telephones, mp3 players, and other consumer audio devices, are in
widespread use. Such personal audio devices may include circuitry for driving a pair of
headphones or one or more speakers. Such circuitry often includes a digital-to-analog
converter (DAC) for converting a digital audio signal into a corresponding analog audio
15 signal, which may be amplified and driven to a loudspeaker or other audio transducer.

One example of a DAC is a current DAC, which converts a digital audio signal
into an equivalent current-mode audio signal. A current DAC may be single-ended,
generating a single-ended current audio signal, or may be differential, generating a
differential audio signal. In its simplest form, a differential current DAC may comprise a
20 collection of switched current sources wherein each current source is switched between
one of the differential outputs or a common-mode ground. The current sources may be
fractionally weighted relative to each other (e.g., each current source may be weighted by
a power of two relative to other current sources), and the output current on each of the
differential outputs may be the sum of current flowing into and out of the output. In
25 many implementations, each current source may be embodied as a scaled mirror from a
reference leg current source of the current DAC. As a result, noise in such reference leg
may be a critical parameter of the current DAC performance, as the mirroring ratio of the
reference leg to each of the switched current sources may mirror and multiply such noise.
To avoid the dominance of such noise, very low mirroring ratios may be established
30 between the switched current source and the reference leg current source. However, such
low mirroring ratios may lead to considerable consumption of power of the reference leg

current, such that the reference leg becomes the dominant component of power consumption of the current DAC. Accordingly, systems and methods are desired to overcome this limitation in order to minimize both noise and power consumption in current DACs.

5

SUMMARY

In accordance with the teachings of the present disclosure, one or more disadvantages and problems associated with existing approaches to signal amplification in an audio system may be reduced or eliminated.

10

In accordance with embodiments of the present disclosure, a playback path may include an input configured to receive an input signal, an output configured to drive a differential output signal, a differential current-mode digital-to-analog converter configured to convert the input signal into the differential output signal, and a control circuit. The differential current-mode digital-to-analog converter may include a plurality of current-mode digital-to-analog elements configured to be selectively enabled and disabled based on the input signal and at least one reference element in a current mirror relationship with the plurality of current-mode digital-to-analog elements such that each individual current through each current-mode digital-to-analog element is a scaled version of a reference current of the at least one reference element. The control circuit may be configured to scale current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements based on a characteristic of the input signal.

15

20

25

30

A method may include receiving an input signal and scaling current mirror ratios between at least one reference element and a plurality of current-mode digital-to-analog elements of a differential current-mode digital-to-analog converter based on a characteristic of the input signal, wherein the differential current-mode digital-to-analog converter is configured to convert the input signal into the differential output signal, the plurality of current-mode digital-to-analog elements are configured to be selectively enabled and disabled based on the input signal, and the at least one reference element is in a current mirror relationship with the plurality of current-mode digital-to-analog elements

such that each individual current through each current-mode digital-to-analog element is a scaled version of a reference current of the at least one reference element.

Technical advantages of the present disclosure may be readily apparent to one skilled in the art from the figures, description and claims included herein. The objects
5 and advantages of the embodiments will be realized and achieved at least by the elements, features, and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are examples and explanatory and are not restrictive of the claims set forth in this disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present embodiments and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings, in which like reference numbers indicate like features,
15 and wherein:

FIGURE 1 is an illustration of an example personal audio device, in accordance with embodiments of the present disclosure;

FIGURE 2 is a block diagram of selected components of an example audio integrated circuit of a personal audio device, in accordance with embodiments of the
20 present disclosure; and

FIGURE 3 is a block diagram of selected components of an example current DAC for use in the example audio integrated circuit of FIGURE 2, in accordance with embodiments of the present disclosure.

DETAILED DESCRIPTION

FIGURE 1 is an illustration of an example personal audio device 1, in accordance with embodiments of the present disclosure. FIGURE 1 depicts personal audio device 1 coupled to a headset 3 in the form of a pair of earbud speakers 8A and 8B. Headset 3 depicted in FIGURE 1 is merely an example, and it is understood that personal audio
30 device 1 may be used in connection with a variety of audio transducers, including without limitation, headphones, earbuds, in-ear earphones, and external speakers. A plug 4 may

provide for connection of headset 3 to an electrical terminal of personal audio device 1. Personal audio device 1 may provide a display to a user and receive user input using a touch screen 2, or alternatively, a standard liquid crystal display (LCD) may be combined with various buttons, sliders, and/or dials disposed on the face and/or sides of personal audio device 1. As also shown in FIGURE 1, personal audio device 1 may include an audio integrated circuit (IC) 9 for generating an analog audio signal for transmission to headset 3 and/or another audio transducer.

FIGURE 2 is a block diagram of selected components of an example audio IC 9 of a personal audio device, in accordance with embodiments of the present disclosure. In some embodiments, example audio IC 9 may be used to implement audio IC 9 of FIGURE 1. As shown in FIGURE 2, a microcontroller core 18 may supply a digital audio input signal DIG_IN to a digital-to-analog converter (DAC) 14, which may convert the digital audio input signal to a differential analog current-mode input signal equal to the difference between currents I_{OUTP} and I_{OUTN} . DAC 14 may supply a differential analog current-mode input signal to an amplifier 16 which may amplify or attenuate the differential analog current-mode input signal to provide an audio output signal V_{OUT} , which may operate a speaker, headphone transducer, a line level signal output, and/or other suitable output. Examples of amplifier 16 include a Class-AB amplifier and a Class-D amplifier.

FIGURE 3 is a block diagram of selected components of an example current DAC 14 for use in example audio integrated circuit 9 of FIGURE 2, in accordance with embodiments of the present disclosure. As shown in FIGURE 3, current DAC 14 may include one or more reference elements 20 (e.g., 20a, 20b), a plurality of current-mode DAC elements 22 (e.g., 22a, 22b, 22c, 22d, ..., 22n), biasing operational amplifiers 24 and 26, and a control circuit 52, as coupled as depicted in FIGURE 3. Each DAC element 22 may comprise a differential current mirror comprising p-type field effect transistors 42 and 44, n-type field effect transistors 46 and 48, and a plurality of switches 50, coupled as shown in FIGURE 3. Reference element 20a may comprise n-type field effect transistors 30 and 32 and a reference resistor 28 coupled as shown in FIGURE 3. As shown in FIGURE 3, reference resistor 28 may have a variable resistance controlled by control circuit 52. In addition or alternatively, one or both of n-type field effect

transistors 30 and 32 may have an admittance controlled by control circuit 52. To implement an n-type field effect transistor 30 and/or 32 as a variable-admittance transistor, each such transistor may comprise a plurality of switched transistors that are enabled and/or disabled under the control of control circuit 52 in order to achieve the
5 desired admittance. Reference element 20b may comprise n-type field effect transistors 34 and 36 and p-type field effect transistors 38 and 40, coupled as shown in FIGURE 3.

In operation, a reference bias voltage V_{BREF} may be applied as shown to operational amplifier 26 and a common mode voltage V_{cm} may be applied as shown to operational amplifiers 24 to generate bias voltages for biasing n-type field effect
10 transistors 32, 36, and 48 and p-type field effect transistors 38 and 42. In addition, a p-type bias voltage V_{BP} may be applied to gates of p-type field effect transistors 38 and 40 to bias p-type field effect transistors 38 and 40, and an n-type bias voltage V_{BN} may be applied to gates of n-type field effect transistors 30, 34, and 46 to bias n-type field effect transistors 30, 34, and 46. Accordingly, as so biased, a circuit is formed by which
15 reference elements 20a and 20b generate reference currents I_{ref} and I_{ref2} as shown in FIGURE 3, one of which (e.g., reference current I_{ref2}) may be used as a reference current for the differential current mirrors implemented by each current-mode DAC element 22. Thus, at least one reference element 20 may have a current mirror relationship with each of the plurality of current-mode DAC elements 22 such that each individual current
20 through each current-mode DAC element 22 is a scaled version of a reference current (e.g., reference currents I_{ref} and I_{ref2}) of the at least one reference element 20. Each current-mode DAC element 22 may be sized or otherwise configured such that it generates a current which is a power of 2 greater than or less than another current-mode DAC element 22. For example, current-mode DAC element 22a may generate a current
25 having twice the magnitude of the current generated by current-mode DAC element 22b, current-mode DAC element 22b may generate a current having twice the magnitude of the current generated by current-mode DAC element 22c, and so on. For each current-mode DAC element 22, its respective switches 50 may be selectively enabled and disabled based on digital audio input signal DIG_IN. For example, each current-mode
30 DAC element 22 may correspond to a respective bit of digital audio input signal DIG_IN, and the respective switches 50 of a current-mode DAC element 22 may be selectively

enabled and disabled based on the respective bit. For purposes of clarity and exposition, the coupling of digital audio input signal DIG_IN and its individual bits to individual switches 50 is not shown. Accordingly, each current-mode DAC element 22 comprises a current source switched between one of the differential outputs (e.g., I_{OUTP} or I_{OUTN}) or a common-mode ground (e.g., V_{cm}). Accordingly output currents (e.g., I_{OUTP} or I_{OUTN}) on each of the differential outputs may be the sum of current flowing into and out of the particular output from the individual current-mode DAC elements 22.

Control circuit 52 may include any system, device, or apparatus configured to receive digital audio input signal DIG_IN (or another signal derived therefrom), and based on a characteristic (e.g., magnitude, frequency, etc.) of digital audio input signal DIG_IN, control one or more components of DAC 14 in order to scale current mirror ratios between at least one reference element 20 and the plurality of current-mode DAC elements 22. For example, control circuit 52 may modify current mirror ratios between at least one reference element 20 and the plurality of current-mode DAC elements 22 responsive to the magnitude of digital audio input signal DIG_IN crossing a predetermined threshold magnitude. As a specific example, in response to digital audio input signal DIG_IN crossing from above to below such predetermined threshold magnitude, control circuit 52 may control one or more components of DAC 14 to decrease a reference current (e.g., I_{ref} and/or I_{ref2}) while increasing a scaling ratio of the currents of current-mode DAC elements 22 relative to a current of at least one reference element 20. In these and other embodiments, such predetermined threshold magnitude may be a threshold magnitude for entering or exiting a noise gating mode of the playback path of the audio signal, whereby noise gating involves for low magnitudes of an audio input signal (e.g., digital audio input signal DIG_IN), an output signal (e.g., difference between I_{OUTP} or I_{OUTN}) of an audio system forced to zero, so as to avoid audio output of noise present in the signal path.

In some embodiments, control circuit 52 may be configured to modify current mirror ratios between the at least one reference element 20 and the plurality of current-mode digital-to-analog elements 22 by modifying a resistance (e.g., resistance of variable resistor 28) of the at least one reference element for setting a current of the at least one reference element. In these and other embodiments, control circuit 52 may be configured

to modify current mirror ratios between the at least one reference element 20 and the plurality of current-mode digital-to-analog elements 22 by modifying an effective device size (e.g., admittance) of the at least one reference element 20 (e.g., the effective admittance of one or both of n-type field effect transistors 30 or 32) for setting a current
5 of the at least one reference element 20. Although, for the purposes of descriptive clarity, FIGURE 3 shows n-type field effect transistors 34 and 36 and p-type field effect transistors 38 and 40 as not having variable admittances controllable by control circuit 52, in some embodiments, control circuit 52 may be configured to modify current mirror ratios between the at least one reference element 20 and the plurality of current-mode
10 digital-to-analog elements 22 by modifying an effective device size of one or more of n-type field effect transistors 34 and 36 and p-type field effect transistors 38 and 40 in addition to or in lieu of modifying an effective device size of n-type field effect transistors 30 and/or 32. Because control circuit 52 may perform such scaling of current mirror ratios by modifying components of a reference element 20: (a) such scaling of
15 current mirror ratios may be performed such that an amount of current flowing through the plurality of current-mode digital-to-analog elements 22 is unchanged when the ratios are scaled and such that the current flowing through the reference element 20 is changed; and/or (b) the plurality of current-mode digital-to-analog elements may be unchanged when the ratios are scaled.

20 In these and other embodiments, in order to reduce or eliminate audio artifacts associated with modifying current mirror ratios, control circuit 52 may modify current mirror ratios during one or more blanking windows of the audio playback path of audio IC 9, wherein each of the one or more blanking windows comprises a finite time duration within a sampling period of DAC 14 in which the output of DAC 14 is prevented from
25 being transmitted to a downstream circuit (e.g., amplifier 16) coupled to the output.

As used herein, when two or more elements are referred to as “coupled” to one another, such term indicates that such two or more elements are in electronic communication or mechanical communication, as applicable, whether connected indirectly or directly, with or without intervening elements.

30 This disclosure encompasses all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in

the art would comprehend. Similarly, where appropriate, the appended claims encompass all changes, substitutions, variations, alterations, and modifications to the exemplary embodiments herein that a person having ordinary skill in the art would comprehend. Moreover, reference in the appended claims to an apparatus or system or a component of
5 an apparatus or system being adapted to, arranged to, capable of, configured to, enabled to, operable to, or operative to perform a particular function encompasses that apparatus, system, or component, whether or not it or that particular function is activated, turned on, or unlocked, as long as that apparatus, system, or component is so adapted, arranged, capable, configured, enabled, operable, or operative.

10 All examples and conditional language recited herein are intended for pedagogical objects to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are construed as being without limitation to such specifically recited examples and conditions. Although embodiments of the present inventions have been described in detail, it should be understood that various changes,
15 substitutions, and alterations could be made hereto without departing from the spirit and scope of the disclosure.

WHAT IS CLAIMED IS:

1. A playback path comprising:
an input configured to receive an input signal;
an output configured to drive a differential output signal; and
5 a differential current-mode digital-to-analog converter configured to convert the input signal into the differential output signal, the differential current-mode digital-to-analog converter comprising:
a plurality of current-mode digital-to-analog elements configured to be selectively enabled and disabled based on the input signal; and
10 at least one reference element in a current mirror relationship with the plurality of current-mode digital-to-analog elements such that each individual current through each current-mode digital-to-analog element is a scaled version of a reference current of the at least one reference element; and
a control circuit configured to scale current mirror ratios between the at least one
15 reference element and the plurality of current-mode digital-to-analog elements based on a characteristic of the input signal.
2. The playback path of Claim 1, wherein the characteristic of the input signal is a magnitude of the input signal.
20
3. The playback path of Claim 2, wherein the control circuit is configured to modify current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements responsive to the magnitude of the input signal crossing a predetermined threshold magnitude.
25
4. The playback path of Claim 3, wherein the predetermined threshold magnitude is a threshold magnitude for entering or exiting a noise gating mode of the playback path.

5. The playback path of Claim 1, wherein the characteristic of the input signal is a frequency of the input signal.

6. The playback path of Claim 1, wherein the control circuit scales the
5 current mirror ratios such that an amount of current flowing through the plurality of current-mode digital-to-analog elements is unchanged when the ratios are scaled and such that another amount of current flowing through the at least one reference element is changed.

10 7. The playback path of Claim 1, wherein the control circuit scales the current mirror ratios such that the plurality of current-mode digital-to-analog elements are unchanged when the ratios are scaled.

8. The playback path of Claim 1, wherein the control circuit is configured to
15 modify current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements during one or more blanking windows of the playback path, wherein each of the one or more blanking windows comprises a finite time duration within a sampling period of the differential current-mode digital-to-analog converter in which the output of the differential current-mode digital-to-analog converter
20 is prevented from being transmitted to a downstream circuit coupled to the output.

9. The playback path of Claim 1, wherein the control circuit is configured to modify current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements by modifying a resistance of the at least one
25 reference element for setting a current of the at least one reference element.

10. The playback path of Claim 1, wherein the control circuit is configured to modify current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements by modifying an effective device size of the at
30 least one reference element for setting a current of the at least one reference element.

11. The playback path of Claim 1, further comprising an amplifier configured to amplify the differential output signal to generate an amplified differential output signal.

12. The playback path of Claim 11, wherein the amplifier comprises one of a
5 Class-AB audio amplifier and a Class-D audio amplifier.

13. A method comprising:
receiving an input signal; and
scaling current mirror ratios between at least one reference element and a plurality
10 of current-mode digital-to-analog elements of a differential current-mode digital-to-analog converter based on a characteristic of the input signal, wherein the differential current-mode digital-to-analog converter is configured to convert the input signal into a differential output signal, the plurality of current-mode digital-to-analog elements is configured to be selectively enabled and disabled based on the input signal, and at least
15 one reference element is in a current mirror relationship with the plurality of current-mode digital-to-analog elements such that each individual current through each current-mode digital-to-analog element is a scaled version of a reference current of the at least one reference element.

14. The method of Claim 13, wherein the characteristic of the input signal is a
20 magnitude of the input signal.

15. The method of Claim 14, further comprising modifying current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements responsive to the magnitude of the input signal crossing a
25 predetermined threshold magnitude.

16. The method of Claim 15, wherein the predetermined threshold magnitude is a threshold magnitude for entering or exiting a noise gating mode of a playback path.

17. The method of Claim 13, wherein the characteristic of the input signal is a frequency of the input signal.

18. The method of Claim 13, further comprising scaling the current mirror ratios such that an amount of current flowing through the plurality of current-mode digital-to-analog elements is unchanged when the ratios are scaled and such that another amount of current flowing through the at least one reference element is changed.

19. The method of Claim 13, further comprising scaling the current mirror ratios such that the plurality of current-mode digital-to-analog elements are unchanged when the ratios are scaled.

20. The method of Claim 13, further comprising modifying current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements during one or more blanking windows of a playback path, wherein each of the one or more blanking windows comprises a finite time duration within a sampling period of the differential current-mode digital-to-analog converter in which an output of the differential current-mode digital-to-analog converter is prevented from being transmitted to a downstream circuit coupled to the output.

20

21. The method of Claim 13, further comprising modifying current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements by modifying a resistance of the at least one reference element for setting a current of the at least one reference element.

25

22. The method of Claim 13, further comprising modifying current mirror ratios between the at least one reference element and the plurality of current-mode digital-to-analog elements by modifying an effective device size of the at least one reference element for setting a current of the at least one reference element.

30

23. The method of Claim 13, further comprising an amplifier configured to amplify the differential output signal to generate an amplified differential output signal.

24. The method of Claim 23, wherein the amplifier comprises one of a Class-
5 AB audio amplifier and a Class-D audio amplifier.

1/2

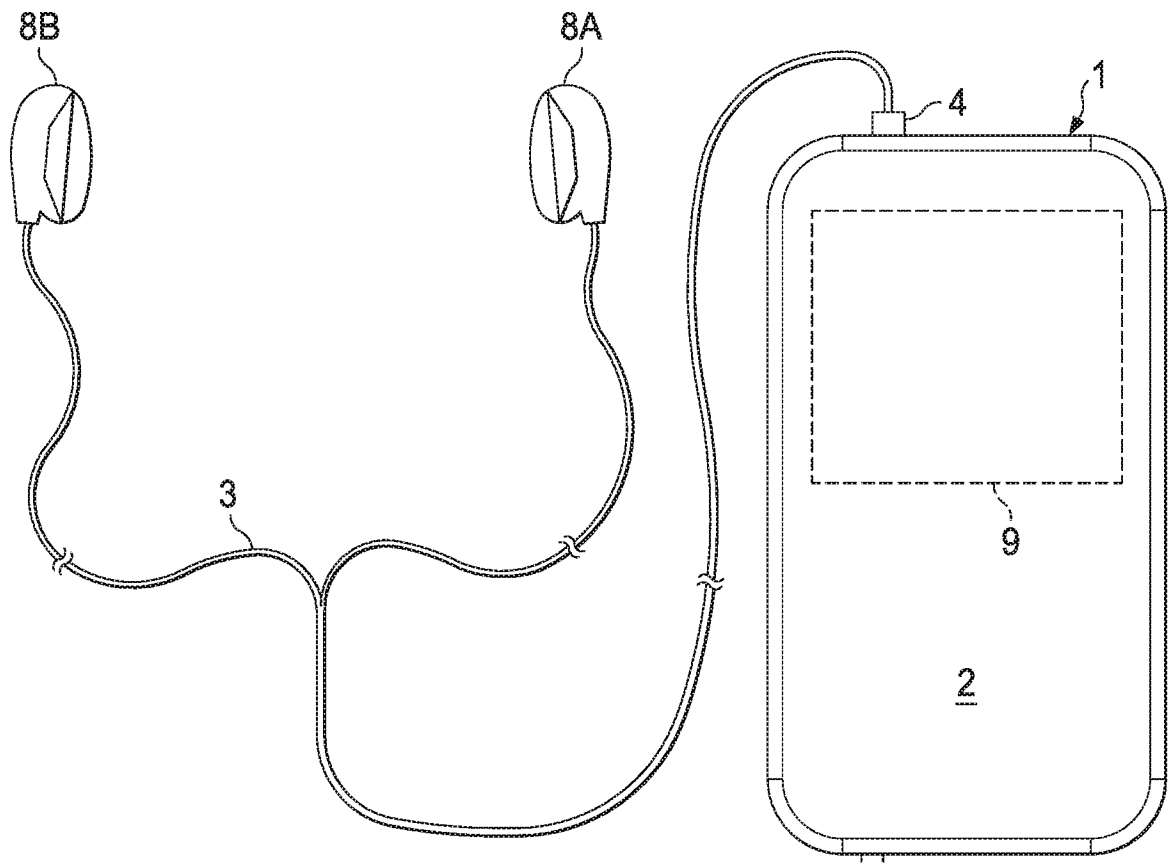


FIG. 1

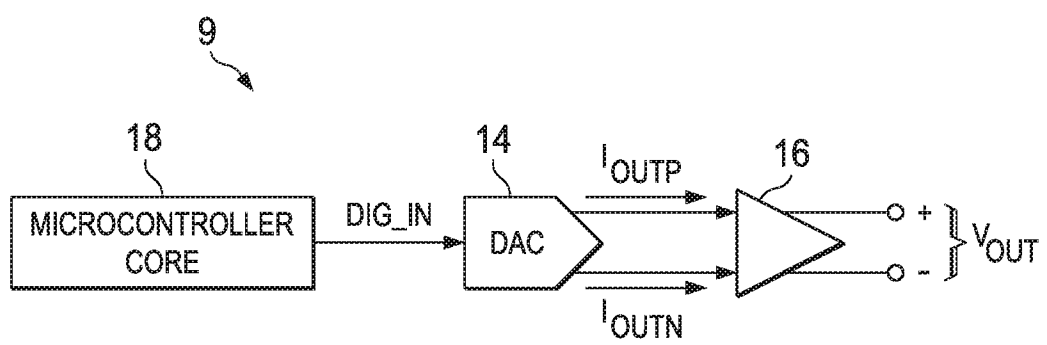
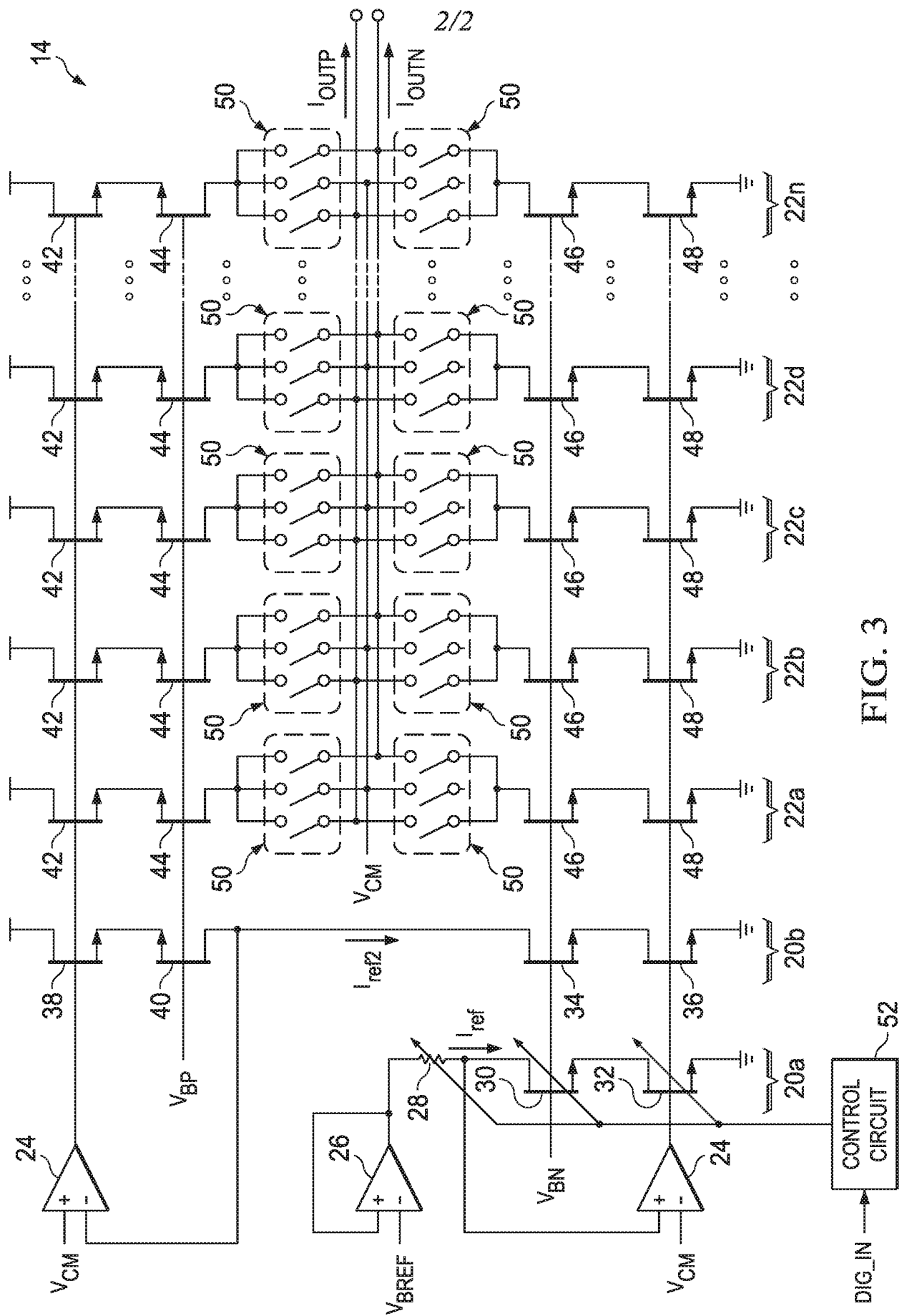


FIG. 2



3
G
H
L

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/027792

A. CLASSIFICATION OF SUBJECT MATTER
INV. H03M1/00 H03M1/74
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013/027235 A1 (RICHES JAMES J [US]) 31 January 2013 (2013-01-31) figure 1 paragraphs [0012] - [0029] ----- -/--	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

18 July 2018

Date of mailing of the international search report

26/07/2018

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Jespers, Michaël

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2018/027792

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
T	Willy Sansen: "Analog Design Essentials", 1 January 2006 (2006-01-01), pages 117-147, XP055492064, Boston DOI: 10.1007/b135984 ISBN: 978-0-387-25746-4 Retrieved from the Internet: URL: https://epo.summon.serialssolutions.com/2.0.0/link/0/eLvHCXMwtV07T8MwED5oWWDiJbW81AFYKiPbSWpnhKqUARZUIdeIsmNHYokYQIh_z91xE1IxwMASJZaSk-sy3139meAc1VkvGqdEV6m1CRCM6JZoonRRvECIRf37PrPs2S5EI-L5H5z4yNYumv7V0tjG9ra7Zz9g7Xbj2ID3qPN8YpWx-taQNw-N1TILg8zMX5JxsRRglDvT1ybQ1FVyLa4HMvn50EqZEh_wvwN9HN1Z5xuSc0B3ie [retrieved on 2018-07-12] slide 0442 -----	1-24

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2018/027792

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2013027235	A1	31-01-2013	NONE
