

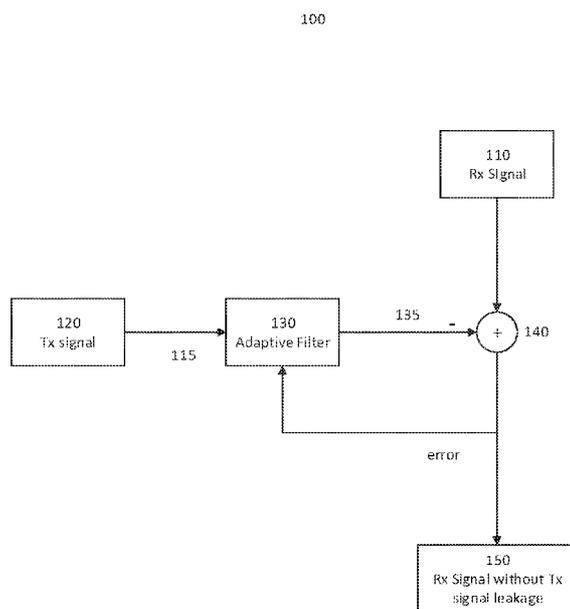


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(54) **Title:** ADAPTIVE FILTER CIRCUITS AND METHODS

FIG. 1



(57) **Abstract:** A method and circuitry for determining an adaptive filter step size for processing a received signal, the circuitry including an adaptive filter circuit configured to receive a first input signal and produce a variable cancellation signal, wherein a step size for each iteration of the variable cancellation signal is the lesser of a first element which monotonically decreases over the number iterations or a second element calculated from a power of the first input signal; and an evaluation circuit configured to subtract the variable cancellation signal from the received signal to generate a second input signal, wherein the adaptive filter circuit adjusts the variable cancellation signal based on the second input signal.

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## ADAPTIVE FILTER CIRCUITS AND METHODS

### Cross-Reference to Related Applications

[0001] This application claims priority to European Patent Application Serial No. 16 191 469.2, which was filed September 29, 2016, and is incorporated herein by reference in its entirety.

### Technical Field

[0002] Various aspects of this disclosure relate generally to a method and a device for adaptive filtering.

### Background

[0003] Adaptive filters are computational devices that attempt to model the relationship between two signals in real time in an iterative manner by modifying variable parameters in each iteration. The least mean square (LMS) algorithm is one of the most used methods for adjusting the variable parameters of an adaptive filter. LMS adaptive filters provide for high levels of accuracy when using small step sizes, but these adaptive filters deliver slow convergence. On the other hand, large step sizes lead to instability. An alternative to the LMS algorithm for adaptive filtering is the normalized LMS (NLMS) algorithm, which normalizes the LMS with the power of the input to the adaptive filter. While improving the convergence and providing stability, the NLMS based filters lack on accuracy. Another method used in adaptive filtering is the recursive least square (RLS) algorithm, which provides both fast convergence and high accuracy. However, these benefits come at the cost of high computational complexity.

[0004] The extended LMS (XLMS) algorithm and mechanisms disclosure herein provide for both fast convergence and high accuracy at low computational complexity, thereby minimizing hardware requirements.

#### **Brief Description of the Drawings**

[0005] In the drawings, like reference characters generally refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the invention are described with reference to the following drawings, in which:

FIG. 1 shows a basic adaptive filter arrangement in an aspect of this disclosure;

FIG. 2 shows a detailed adaptive filter arrangement in an aspect of this disclosure;

FIG. 3 shows a hardware implementation for an adaptive filter circuit in an aspect of this disclosure;

FIG. 4 shows a step size table for an adaptive filter algorithm in an aspect of this disclosure;

FIG. 5 shows a comparison of the results of the methods and devices in this disclosure with known methods;

FIG. 6 is a graph showing a settling performance of the methods and devices of this disclosure;

FIG. 7 is a graph showing a settling performance of the methods and devices of this disclosure;

FIG. 8 shows a configuration of a device which implements the circuitry and methods in an aspect of this disclosure;

FIG. 9 shows a flowchart for an adaptive filter method in an aspect of this disclosure.

#### **Description**

[0006] The following details description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced.

[0007] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration". Any embodiment or design described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0008] The words "plural" and "multiple" in the description and the claims, if any, are used to expressly refer to a quantity greater than one. Accordingly, any phrases explicitly invoking the aforementioned words (e.g. "a plurality of [objects]", "multiple [objects]") referring to a quantity of objects is intended to expressly refer more than one of the said objects. The terms "group", "set", "collection", "series", "sequence", "grouping", "selection", etc., and the like in the description and in the claims, if any, are used to refer to a quantity equal to or greater than one, i.e. one or more. Accordingly, the phrases "a group of [objects]", "a set of [objects]", "a collection of [objects]", "a series of [objects]", "a sequence of [objects]", "a grouping of [objects]", "a selection of [objects]", "[object] group", "[object] set", "[object] collection", "[object] series", "[object] sequence", "[object] grouping", "[object] selection", etc., used herein in relation to a quantity of objects is intended to refer to a quantity of one or more of said objects. It is appreciated that unless directly referred to with an explicitly stated plural quantity (e.g. "two [objects]" "three of the [objects]", "ten or more [objects]", "at least four [objects]", etc.) or express use of the words "plural", "multiple", or similar phrases, references to quantities of objects are intended to refer to one or more of said objects.

[0009] A "circuit" as used herein is understood as any kind of logic-implementing entity, which may include special-purpose hardware or a processor executing software. A circuit may thus be an analog circuit, digital circuit, mixed-signal circuit, logic circuit, processor, microprocessor, Central Processing Unit (CPU), Graphics Processing Unit (GPU), Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), integrated circuit, Application Specific Integrated Circuit (ASIC), etc., or any combination thereof. Any other

kind of implementation of the respective functions which will be described below in further detail may also be understood as a "circuit". It is understood that any two (or more) of the circuits detailed herein may be realized as a single circuit with substantially equivalent functionality, and conversely that any single circuit detailed herein may be realized as two (or more) separate circuits with substantially equivalent functionality. Additionally, references to a "circuit" may refer to two or more circuits that collectively form a single circuit. The term "circuit arrangement" may refer to a single circuit, a collection of circuits, and/or an electronic device composed of one or more circuits.

[0010] A "processing circuit" (or equivalently "processing circuitry" or "processor") as used herein is understood as referring to any circuit that performs an operation(s) on signal(s), such as e.g. any circuit that performs processing on an electrical signal or an optical signal. A processing circuit may thus refer to any analog or digital circuitry that alters a characteristic or property of an electrical or optical signal, which may include analog and/or digital data. A processing circuit may thus refer to an analog circuit (explicitly referred to as "analog processing circuit(ry)"), digital circuit (explicitly referred to as "digital processing circuit(ry)"), logic circuit, processor, microprocessor, Central Processing Unit (CPU), Graphics Processing Unit (GPU), Digital Signal Processor (DSP), Field Programmable Gate Array (FPGA), integrated circuit, Application Specific Integrated Circuit (ASIC), etc., or any combination thereof. Accordingly, a processing circuit may refer to a circuit that performs processing on an electrical or optical signal as hardware or as software, such as software executed on hardware (e.g. a processor or microprocessor). As utilized herein, "digital processing circuit(ry)" may refer to a circuit implemented using digital logic that performs processing on a signal, e.g. an electrical or optical signal, which may include logic circuit(s), processor(s), scalar processor(s), vector processor(s), microprocessor(s), controller(s), microcontroller(s), Central Processing Unit(s) (CPU), Graphics Processing Unit(s) (GPU), Digital Signal Processor(s) (DSP), Field Programmable Gate Array(s) (FPGA), integrated

circuit(s), Application Specific Integrated Circuit(s) (ASIC), or any combination thereof.

Furthermore, it is understood that a single a processing circuit may be equivalently split into two separate processing circuits, and conversely that two separate processing circuits may be combined into a single equivalent processing circuit.

[0011] As used herein, "memory" may be understood as an electrical component in which data or information can be stored for retrieval. References to "memory" included herein may thus be understood as referring to volatile or non-volatile memory, including random access memory (RAM), read-only memory (ROM), flash memory, solid-state storage, magnetic tape, hard disk drive, optical drive, etc., or any combination thereof. Furthermore, it is appreciated that registers, shift registers, processor registers, data buffers, etc., are also embraced herein by the "term" memory. It is appreciated that a single component referred to as "memory" or "a memory" may be composed of more than one different type of memory, and thus may refer to a collective component comprising one or more types of memory. It is readily understood that any single memory "component" may be distributed or/separated multiple substantially equivalent memory components, and vice versa. Furthermore, it is appreciated that while "memory" may be depicted, such as in the drawings, as separate from one or more other components, it is understood that memory may be integrated within another component, such as on a common integrated chip.

[0012] For purposes of this disclosure, radio communication technologies may be classified as one of a Short Range radio communication technology, Metropolitan Area System radio communication technology, or Cellular Wide Area radio communication technology. Short Range radio communication technologies include Bluetooth, WLAN (e.g. according to any IEEE 802. 11 standard), and other similar radio communication technologies. Metropolitan Area System radio communication technologies include Worldwide Interoperability for Microwave Access (WiMax) (e.g. according to an IEEE 802. 16 radio communication standard, e.g. WiMax fixed or WiMax mobile) and other similar radio communication

technologies. Cellular Wide Area radio communication technologies include Global System for Mobile Communications (GSM), Code Division Multiple Access 2000 (CDMA2000), Universal Mobile Telecommunications System (UMTS), Long Term Evolution (LTE), General Packet Radio Service (GPRS), Evolution-Data Optimized (EV-DO), Enhanced Data Rates for GSM Evolution (EDGE), High Speed Packet Access (HSPA), etc., and other similar radio communication technologies. Cellular Wide Area radio communication technologies also include "small cells" of such technologies, such as microcells, femtocells, and picocells. Cellular Wide Area radio communication technologies may be generally referred to herein as "cellular" communication technologies. It is understood that exemplary scenarios detailed herein are demonstrative in nature, and accordingly may be similarly applied to various other mobile communication technologies, both existing and not yet formulated, particularly in cases where such mobile communication technologies share similar features as disclosed regarding the following examples.

**[0013]** The term "network" as utilized herein, e.g. in reference to a communication network such as a mobile communication network, is intended to encompass both an access component of a network (e.g. a radio access network (RAN) component) and a core component of a network (e.g. a core network component).

**[0014]** Unless explicitly specified, the term "transmit" encompasses both direct (point-to-point) and indirect transmission (via one or more intermediary points). Similarly, the term "receive" encompasses both direct and indirect reception. The term "communicate" encompasses one or both of transmitting and receiving, i.e. unidirectional or bidirectional communication in one or both of the incoming and outgoing directions. The term "calculate" encompass both 'direct' calculations via a mathematical expression/formula/relationship and 'indirect' calculations via lookup tables and other array indexing or searching operations.

**[0015]** It is appreciated that any vector and/or matrix notation utilized herein is exemplary in nature and is employed solely for purposes of explanation. Accordingly, it is understood that

the approaches detailed in this disclosure are not limited to being implemented solely using vectors and/or matrices, and that the associated processes and computations may be equivalently performed with respect to sets, sequences, groups, etc., of data, observations, information, signals, samples, symbols, elements, etc. Furthermore, it is appreciated that references to a "vector" may refer to a vector of any size or orientation, e.g. including a  $1 \times 1$  vector (e.g. a scalar), a  $1 \times M$  vector (e.g. a row vector), and an  $M \times 1$  vector (e.g. a column vector). Similarly, it is appreciated that references to a "matrix" may refer to matrix of any size or orientation, e.g. including a  $1 \times 1$  matrix (e.g. a scalar), a  $1 \times M$  matrix (e.g. a row vector), and an  $M \times 1$  matrix (e.g. a column vector).

[0016] The subject matter disclosed herein provides devices and methods for adaptive filtering with fast convergence and high accuracy at low computation complexity. The disclosure herein improves the LMS adaptive filtering algorithm settling time and accuracy close to the performance of the very hardware intensive RLS algorithm, and, in some cases, even improves upon the RLS performance. The adaptive filtering methods and devices herein may be used in many implementations, including, but not limited to: self-interference cancellation (SIC), modulated spur cancellation,  $n$ th harmonic cancellation, IM3 cancellation, digital pre-distortion, and 3G Radio Resource Control (RRC) equalization. For example, the mechanisms and methods herein disclosed may be implemented into a baseband modem of a wireless device for transmission (TX)-reception (RX) crosstalk, repeater, or audio applications. In another example, the disclosed mechanisms and methods may be applied to adaptive equalizers for cellular and connectivity for time domain equalization, e.g. CDMA baseband modems.

[0017] For LMS, the step size of each iteration ( $\mu$ ) must be chosen to be relatively small to avoid stability problems as well as achieving accuracy. However, this small step size increases the settling time (i.e. convergence), and thereby decreasing the stability. NLMS solves the stability issue, but does so at the sacrifice of accuracy, especially in the presence of

an interferer or noise. The solution presented by RLS is hardware intensive (i.e. needs more hardware due to high computation complexity) and has a lower tracking capability in a settled condition. Tracking is an adaptive filters ability to alter its parameter values to follow the changes in its input with that of a received signal.

[0018] The disclosure herein provides two elements from which to select the lower step size in each iteration of the cancellation signal (i.e. adaptive filter output): a step size which decreases with time and a step size dependent on the power of the input signal to the adaptive filter. The step size dependent on power is similar to step size determination in the NLMS method. In another aspect of this disclosure, the step size dependent on time may be scaled to account for interference and noise in order to deliver even better results.

[0019] In the adaptive filtering mechanisms and methods presented in this disclosure, the initial step sizes of the adaptive filter are dominated by the power dependent step size (i.e. similar to NLMS) which provides for fast convergence while maintaining stability, but in the later stages, the step size selection is dominated by the time dependent step size, ensuring high accuracy.

[0020] FIG. 1 shows an adaptive filter diagram 100 in an aspect of this disclosure. It is appreciated that adaptive filter diagram 100 is exemplary in nature and may therefore be simplified for purposes of this explanation. The ensuing explanation focuses on the application of the disclosed adaptive filter mechanism and methods to self-interference cancellation between transmit and receive equipment in a wireless device, but it is appreciated that the ensuing disclosure encompasses other adaptive filter applications, e.g. IM3 cancellation, digital pre-distortion, and 3G Radio Resource Control (RRC) equalization, as well. In these applications different to self-interference cancellation, the terminology for input and output signals would be changes according to use case.

[0021] In diagram 100, the received signal (Rx signal) 110 includes the intended Rx signal (i.e. the signal as received at the device) plus interference produced by unknown signal leakage from the transmission equipment of the device (among other forms of interference).

[0022] However, the transmitted signal 120 cannot simply be subtracted from the Rx signal 110 in order to recover the intended Rx signal because this would not account for the effects of signal leakage from components of the Rx/Tx chain (e.g. mixers, amplifiers, converters, etc.). In order to account for the signal leakage, an adaptive filter 130 is implemented to produce a more accurate representation of the signal leakage interference in the adaptive filter signal, i.e. cancellation signal, 135. This cancellation signal is then subtracted 140 from the Rx signal 110 in order to attempt to retrieve the intended Rx signal, i.e. the Rx signal without the Tx signal leakage, 150. This resulting signal is fed back to the adaptive filter 130 as an error so the adaptive filter 130 may update the cancellation signal 135 in the next iteration.

[0023] In an aspect of this disclosure, adaptive filter 130 is implemented with an adaptive finite impulse response (FIR) filtering algorithm, which may be shown in the general form:

$$W(n + 1) = W(n) + \mu(\eta) * F(e(n), X(n), \Phi(n)) \quad (1)$$

where  $W(n)$  is the parameter or coefficient vector at time (i.e. iteration)  $n$ ,  $\mu(\eta)$  is the step size at time  $n$ , and  $F(\cdot)$  is a function dependent on the error signal  $e(n)$ , the input signal (i.e. Tx signal 120)  $X(n)$ , and a vector of states that stores other pertinent information, e.g. characteristics of the input and error signals, the coefficients at prior times, etc.,  $\Phi(\eta)$ .

[0024] The focal point of the disclosure is the calculation of the step size (i.e. the weight calculation applied in each iteration) of the adaptive filter. The step size ( $\mu$ ) determines the magnitude of the change (i.e. "step") taken by the adaptive filter algorithm in iteratively determining a useful coefficient vector to be used in the next iteration (i.e.  $W(n + 1)$ ) in Equation (1) of cancellation signal 135.

[0025] Current adaptive filter implementations include LMS algorithms which have a constant step size (problem: slow settling), NLMS algorithms which normalize the step sizes

with the power of the Tx signal (problem: lower accuracy), and RLS which uses complex matrix operations for step size calculations (problem: high operational complexity). By implementing the novel step size method of this disclosure, a highly accurate and quickly converging adaptive filter with low computational complexity is achieved.

[0026] The following figure (FIG. 2) provides a more detailed configuration for adaptive filter 130 in this disclosure.

[0027] FIG. 2 shows a more detailed structure 200 for adaptive filter (i.e. for adaptive filter 130). It is appreciated that configuration 200 is exemplary in nature and may therefore be simplified for purposes of this explanation.

[0028] The Tx and Rx signals are composed of both in-phase and quadrature components, shown as  $ITX+jQTX$  202 and  $IRX+jQRX$  204, respectively. In terms of FIG. 1,  $ITX+jQTX$  202 is representative of Tx signal 120 and  $IRX+jQRX$  204 is representative of Rx signal 110.

[0029] The complex FIR sum 214 sums all of the components of adaptive filter structure 200 in order to produce cancellation signal 206. Complex filter taps 210-212 produce delays in adaptive filter structure 200 to determine the components to be summed by Complex FIR sum 214.

[0030] The focal point of structure 200 as associated with this disclosure is in the weight (i.e. step size) determination performed for weight accumulators 220-224. The dashed lines are meant to provide depiction of the different stages of the adaptive filter structure 200.

[0031] A variable step size ( $\mu$ ) is determined in each iteration of Equation 1. The lesser of two elements is chosen as the step size ( $\mu$ ) for that particular iteration. The first element ( $\mu\bar{r}$ ) is inversely proportional to a time ( $t$ ). In other words,  $\mu\bar{r}$  is a monotonically decreasing function as related to time, i.e. the number of iterations. The second element ( $\mu_2$ ) is determined from the power of the Tx signal. In other words,  $\mu_2$  may be determined in similar fashion to the NLMS step size.

[0032] The step size ( $\mu$ ) chosen in each iteration may be demonstrated by the following equation:

$$\mu = \eta \cdot \eta(\mu_1, \mu_2) \quad (2)$$

where  $\mu_1$  is determined by the time of the iteration (i.e. at what point in time the iteration occurs) and  $\mu_2$  is a function of Tx power. The power calculation can be simplified by sum of the absolute values terms. By including a step size option ( $\mu_1$ ) dependent on time, the adaptive filter ensures high accuracy. By including a step size option ( $\mu_2$ ) dependent on the Tx power, the adaptive filter provides fast convergence and high stability.

[0033] A scaling of the time dependent step size ( $\mu_1$ ) may be implemented in order to account for interference and noise of the receive path. This scaling may be shown by the following equation:

$$\mu_1 = m_1 * f(t * t_1) \quad (3)$$

where function  $f$  has lower and upper boundaries for  $t = [0 \dots \text{inf}]$  and typically monotonically decreasing characteristics inside constant boundaries (e.g.,  $f = \frac{0.4}{t * t_1 + 0.01} + 0.0005$ ), and  $t_1$  and  $m_1$  depend on the ratio of the power of the Rx signal to the expected Tx power within the Rx signal. More specifically,  $t_1$  is a time-dependent component of the scaling and  $m_1$  is a signal magnitude-dependent component. The scaling is chosen based on known or estimated Rx wanted level (or noise level or both) on the Rx input side. By implementing the scaling of  $\mu_1$ , as the noise increases, the scaling (i.e. via the values of  $t_1$  and  $m_1$ ) decreases in order to provide optimal results.

[0034] Furthermore, the step size determination for  $\mu$  may be numerically limited to a minimum and maximum step size, where the minimum is determined by the required accuracy and tracking performance in the settled state of the system, and the maximum is determined to be a value slightly larger than the expected maximum step size which would be determined in a strictly NLMS implementation.

[0035] In another aspect of this disclosure, a cold/soft restart of the step size control may be employed, where the maximum step size of the control is dependent on changing signal conditions, e.g. the frequency allocation of the Tx signal. This, for example, may lead to a lower calculation for  $\mu\bar{\tau}$ .

[0036] In another aspect of this disclosure, in order to solve delay problems cause by long combination path to the cancellation point or in the error feedback portion presented by pipelining taps, a blind tap is introduced, for example, in place of Complex FIR tap n 212.

[0037] In multi-kernel usage, where the same error signal is used for filter adaptation of two or more nonlinear terms of the Tx signal, the higher order/less dominating kernels are given a later start in order to improve convergence/settling. In case of discrete tables, only the first step size table entries (for  $\mu\bar{\tau}$ ) in the corresponding kernels would be zero.

[0038] The  $\mu\bar{\tau}$  step size may be realized by a 1/t decay, or more preferably, by a discrete step size table (Table) and its scaling can be controlled by additional parameters, such as interference and/or noise or if boundary conditions are changing (e.g. signal levels or signal types).

[0039] Since the step size determination is a known decay function, multipliers in error feedback can use barrel shifters (e.g. two shift values, one for time iteration  $[0, \dots, t_l]$  and one for time iterations greater than  $t_l$ ) in order to avoid big multiplier word lengths, thereby minimizing hardware requirements.

[0040] FIG. 3 shows a hardware (HW) implementation 300 in an aspect of this disclosure. It is appreciated that HW implementation 300 is exemplary in nature and may therefore be simplified for purposes of this disclosure. It is also realized that alternate forms of HW implementation which achieve analogous results by implementing the step size calculations of this disclosure are encompassed by the explanation herein.

[0041] HW implementation 300 is similar to the configuration disclosed in FIG. 2, and therefore, the same reference numbers refer to similar components.

[0042] The aforementioned barrel shifters 342-344 are implemented in series with the XLMS weight accumulators 222-224 to avoid big multiplier word lengths and minimize hardware.

[0043] The Complex blind FIR tap 312 is employed in lieu of Complex FIR tap n 212 of FIG. 2 to, in addition to realizing the once cycle delay of tap 210, to account for the compensating effect of the pipelined register 335, which is introduced for synchronizing combination logic which may be included in the cancellation signal 206, and therefore, find its way into the error feedback path 330.

[0044] The XLMS step size algorithm is implemented into unit 301, which selects the lesser of the step sizes,  $\mu_1$  and  $\mu_2$ , determined from the  $\mu$ Table (i.e. time-dependent) and the Tx Power (P), respectively. Control 302 may introduce other inputs to the XLMS step size unit 301. These inputs may include a cold/soft restart and/or a signal to interference ratio.

[0045] In another embodiment of this disclosure, a power detector may be implemented at the adaptive filter input (i.e. at 115 in FIG. 1), providing a Tx signal power check and switching the XLMS algorithm unit 301 to hold a coefficient state (i.e. stopping adaptation) if the Tx signal power is below a certain threshold. In other words, if the power of the Tx signal reaches low values or zero, i.e. there is no signal being transmitted, then there is no need to provide the adaption filtering. Or, the lower the Tx signal power, the less suppression and less adaptive filtering is needed in order to produce the intended Rx signal.

[0046] FIG. 4 shows an exemplary  $\mu_1$  step size table (i.e. graph) 400 with corresponding exemplary code 450. It is appreciated that graph 400 is exemplary in nature and may therefore be modified and still be encompassed within disclosure.

[0047] The discrete step size table line (i.e.  $\mu_1$  step size table) is indicated by the step line depicted in graph 400. This line corresponds to the exemplary code 450. It represents a typical cold start (adaptive filter weights starting from zero). Code 450 depicts the manner in which a predetermined step size table may be selected. It is appreciated that a similar step

size table, with a similar descending step-like (i.e. monotonically decreasing) relationship between the step size and the number of iterations may be implemented.

[0048] The line marked by the circles represents  $1/t$  behavior.

[0049] The region outlined by line **410** and line **420** is the region where the NLMS is potentially limiting, and the area below line **420** is the area where the  $1/t$  behavior limits the step size in order to achieve higher accuracy and better adaptation (i.e. better cancellation in case of SIC).

[0050] To achieve minimum tracking performance of this disclosure, the minimum step size of  $\mu\bar{r}$  is limited to line **430**. In this manner, the smaller step sizes can be avoided in order to achieve faster convergence.

[0051] A soft restart table for  $\mu\bar{r}$  would lower line **410** (i.e. the upper step size limit) to the region between line **420** and line **430**, assuming that the current adaptive filter weight state are not zero, but in fact closer to the optimum state.

[0052] FIG. 5 shows a comparison of the settling behavior of an NLMS algorithm **510**, an LMS algorithm **520**, and the XLMS algorithm **530** of this disclosure.

[0053] The NLMS algorithm **510** shows good settling, but lacks the accuracy (i.e. the interference suppression) of the other signals as demonstrated by its spur power out/in ratio of about -11.5 dBs.

[0054] The LMS algorithm **520** (with a constant step size of  $1.0E-4$ ) shows good accuracy demonstrated by its spur power out/in ratio of about -17 dBs, but it also shows slow settling as evident in the slow convergence to its final state.

[0055] On the other hand, the XLMS algorithm **530** shows both good settling and high accuracy when compared to **510** and **520**.

[0056] FIG. 6 is a graph **600** showing the settling performance of the XLMS algorithm of this disclosure for suppressing Tx spur in Rx signal for a low intended Rx signal using a 12-

tap filter for adaption of multiple hundreds duplexer transfer functions, which results in the multiple hundred settling curves shown in graph **600**.

[0057] For the XLMS step size algorithm unit used to achieve the results in graph **600**, the scaling used in  $\mu\bar{r}$  (as shown by Equation 3) was set with values of  $t_1 = 2$  and  $m_1 = \backslash$ . A full allocation of LTE20 was used for the Tx signal and for the Rx signal LTE10. The suppression was calculated by the spur power out/spur power in, where the modulated spur power is equal to the noise power plus the intended Rx signal. One symbol number (along the x-axis) is equal to 0.5 ms (1 slot)/7symbols= 71  $\mu$ s.

[0058] As is shown by graph **600**, none of the XLMS use cases fail to converge, and in the worst case scenario, the suppression ratio result is about -16.5 dB, which is a more than adequate result considering that the duplexer isolation has a strong frequency response with many notch type areas which are close to each other.

[0059] FIG. 7 shows a graph **700** depicting the settling performance of the XLMS algorithm of this disclosure for suppressing Tx spur in Rx signal for a high intended Rx signal. The Rx signal is 30 dB above Tx (LTE20) and the signal to interference ratio (SIR) is 30 dB, thereby implementing the adapted  $\mu\bar{r}$  step size table.

[0060] A 12-tap filter was used and the scaling factors were set to  $t_1 = 1$  and  $m_1 = 0.1$ . The measured data in graph **600** is the receiver signal.

[0061] The spur in/out of the XLMS algorithm of this disclosure after 7 symbols is about -2.2 dBs, signifying a +2.2 dB interference cancellation. After 80 symbols, it is -6.5 dBs, signifying a 6.5 dB interference cancellation.

[0062] Chart **750** shows a comparison of the novel XLMS methods and mechanisms of this disclosure (in the second column) when compared to the highly computational complex RLS (in the first column) method in a high interference (30 dBs) scenario. Higher positive numbers indicate better results, with negative value indicating an increase in distortion, i.e. the cancellation circuit is counterproductive. As is clearly evident from chart **750**, the XLMS

method and mechanism of this disclosure achieves better results than the RLS algorithm at a lower computational complexity.

[0063] FIG. 8 shows an internal configuration of user equipment (UE) 800, which may be configured to perform the adaptive filtering procedure of this disclosure. As shown in FIG. 8, UE 800 may include antenna system 802, radio frequency (RF) transceiver 804, baseband modem 806 (including physical layer processing circuit 808 and controller 810), data source 812, memory 814, and data sink 816. Although not explicitly shown in FIG. 8, UE 800 may include one or more additional hardware, software, and/or firmware components (such as processors/microprocessors, controllers/microcontrollers, other specialty or generic hardware/processors/circuits, etc.), peripheral device(s), memory, power supply, external device interface(s), subscriber identify module(s) (SIMs), user input/output devices (display(s), keypad(s), touchscreen(s), speaker(s), external button(s), camera(s), microphone(s), etc.), etc.

[0064] In an abridged operational overview, UE 800 may transmit and receive radio signals on one or more RANs. Baseband modem 806 may direct such communication functionality of UE 800 according to the communication protocols associated with each RAN, and may execute control over antenna system 802 and RF transceiver 804 in order to transmit and receive radio signals according to the formatting and scheduling parameters defined by each communication protocol.

[0065] UE 800 may transmit and receive radio signals with antenna system 802, which may be a single antenna or an antenna array composed of multiple antennas and may additionally include analog antenna combination and/or beamforming circuitry. The receive path (RX) of RF transceiver 804 may receive analog radio frequency signals from antenna system 802 and perform analog and digital RF front-end processing on the analog radio frequency signals to produce digital baseband samples (e.g. In-Phase/Quadrature (IQ) samples) to provide to baseband modem 806. RF transceiver 804 may accordingly include analog and digital

reception circuitry including amplifiers (e.g. a Low Noise Amplifier (LNA), filters, RF demodulators (e.g. an RF IQ demodulator)), and analog-to-digital converters (ADCs) to convert the received radio frequency signals to digital baseband samples. In the transmit path (TX), RF transceiver **804** may receive digital baseband samples from baseband modem **806** and perform analog and digital RF front-end processing on the digital baseband samples to produce analog radio frequency signals to provide to antenna system **802** for wireless transmission. RF transceiver **804** may thus include analog and digital transmission circuitry including amplifiers (e.g. a Power Amplifier (PA), filters, RF modulators (e.g. an RF IQ modulator), and digital-to-analog converters (DACs) to mix the digital baseband samples received from baseband modem **806** to produce the analog radio frequency signals for wireless transmission by antenna system **802**. Baseband modem **806** may control the RF transmission and reception of RF transceiver **804**, including specifying transmit and receive radio frequencies for operation of RF transceiver **804**.

[0066] As shown in FIG. 8, baseband modem **806** may include physical layer processing circuit **808**, which may perform physical layer (Layer 1) transmission and reception processing to prepare outgoing transmit data provided by controller **810** for transmission via RF transceiver **804** and prepare incoming received data provided by RF transceiver **804** for processing by controller **810**. Physical layer processing circuit **810** may accordingly perform one or more of adaptive filtering, error detection, forward error correction encoding/decoding, channel coding and interleaving, physical channel modulation/demodulation, physical channel mapping, radio measurement and search, frequency and time synchronization, antenna diversity processing, power control and weighting, rate matching, retransmission processing, etc. Physical layer processing circuit **808** may be structurally realized as hardware logic, e.g. as an integrated circuit or FPGA, as software logic, e.g. as program code defining arithmetic, control, and I/O instructions stored in a non-transitory computer-readable storage medium and executed on a processor, or as a combination of hardware and software logic. Although not

explicitly shown in FIG. 8, physical layer processing circuit 808 may include a control circuit such as a processor configured to control the various hardware and software processing components of physical layer processing circuit 808 in accordance with physical layer control logic defined by the communications protocol for the relevant radio access technologies (RATs). Furthermore, while physical layer processing circuit 808 is depicted as a single component in FIG. 8, physical layer processing circuit 808 may be collectively composed separate sections of physical layer processing circuitry where each respective section is dedicated to the physical layer processing of a particular RAT.

[0067] Physical layer processing circuit 808 may include hardware and/or software to implement the adaptive filtering methods of this disclosure, e.g. as described in the other figures.

[0068] UE 800 may be configured to operate according to one or more RATs, which may be directed by controller 810. Controller 810 may thus be responsible for controlling the radio communication components of UE 800 (antenna system 802, RF transceiver 804, and physical layer processing circuit 808) in accordance with the communication protocols of each supported RAT, and accordingly may represent the Access Stratum (AS) and Non-Access Stratum (NAS) (also encompassing Layer 2 and Layer 3) of each supported RAT. Controller 810 may be structurally embodied as a protocol processor configured to execute protocol software (retrieved from controller memory MEM as shown in FIG. 4) and subsequently control the radio communication components of UE 800 in order to transmit and receive communication signals in accordance with the corresponding protocol control logic defined in the protocol software.

[0069] Controller 810 may therefore be configured to manage the radio communication functionality of UE 800 in order to communicate with the various radio and core network components of a radio communication network, and accordingly may be configured according to the communication protocols for both the LTE network and the GSM/UMTS legacy

network. Controller 810 may either be a unified controller that is collectively responsible for all supported RATs (e.g. LTE and GSM/UMTS) or may be composed of multiple separate controllers where each controller is a dedicated controller for a particular RAT, such as e.g. a dedicated LTE controller and a dedicated legacy controller (or alternatively a dedicated LTE controller, dedicated GSM controller, and a dedicated UMTS controller). Regardless, controller 810 may be responsible for directing radio communication activity of UE 800 according to the communication protocols of the LTE and legacy networks. As previously noted regarding physical layer processing circuit 808, one or both of antenna system 802 and RF transceiver 804 may similarly be partitioned into multiple dedicated components that each respectively correspond to one or more of the supported RATs. Depending on the specifics of each such configuration and the number of supported RATs, controller 810 may be configured to control the radio communication operations of UE 800 in accordance with a master/slave RAT hierarchical or multi-SIM scheme.

[0070] UE 800 may further comprise data source 812, memory 814, and data sink 816, where data source 812 may include sources of communication data above controller 810 (i.e. above the NAS/Layer 3) and data sink 816 may include destinations of communication data above controller 810 (i.e. above the NAS/Layer 3). Such may include, for example, an application processor of UE 800, which may be configured to execute various applications and/or programs of UE 800 at an application layer of UE 800, such as e.g. an Operating System (OS), a User Interface (UI) for supporting user interaction with UE 800, and/or various user applications. The application processor may interface with baseband modem 806 (as data source 812/data sink 816) as an application layer to transmit and receive user data such as voice data, audio/video/image data, messaging data, application data, basic Internet/web access data, etc., over a the radio network connection(s) provided by baseband modem 806. Data source 812 and data sink 816 may additionally represent various user input/output devices of UE 800, such as display(s), keypad(s), touchscreen(s), speaker(s),

external button(s), camera(s), microphone(s), etc., which may allow a user of **UE 800** to control various communication functions of **UE 800** associated with user data.

[0071] Memory **814** may embody a memory component of **UE 800**, such as e.g. a hard drive or another such permanent memory device. Although not explicitly depicted in FIG. **8**, the various other components of **UE 800** shown in FIG. **8** may additionally each include integrated permanent and non-permanent memory components, such as for storing software program code, buffering data, etc.

[0072] FIG. **9** shows a flowchart **900** detailing an adaptive filter method in an aspect of this disclosure. It is appreciated that flowchart **900** is exemplary in nature and may therefore be simplified for purposes of this explanation.

[0073] The adaptive filtering method described in flowchart **900** may be implemented by the physical processing layer circuit **808** of **UE 800** in FIG. **8** in order to determine a step size (i.e. weight) for each iteration of an adaptive filtering process.

[0074] A first element is determined which monotonically decreases over the number of iterations **902**. For example, as the number of the iterations increases (i.e. as time increases), the first element will either decrease or stay the same (i.e. is monotonic in nature).

[0075] A second element is determined (i.e. calculated) from a power of the first input signal to the adaptive filter **904**. The first input signal may be, for example, the transmitted signal from the communication device which is interfering with the received signal. In this case, the adaptive filtering process disclosed herein is implemented in order to mimic the leakage of the transmitted signal into the received signal (in the transceiver and the physical processing layer circuit) in order to remove said leakage.

[0076] It is appreciated that the order of **902** and **904** may be switched or they may be performed simultaneously.

[0077] After determining the first and the second elements, the lesser of the two is chosen as the step size for that particular iteration of the adaptive filtering process **906**.

[0078] In Example 1, a circuitry for determining an adaptive filter step size for processing a received signal, the circuitry including an adaptive filter circuit configured to receive a first input signal and produce a variable cancellation signal, wherein a step size for each iteration of the variable cancellation signal is the lesser of a first element which monotonically decreases over the number of iterations; or a second element calculated from a power of the first input signal; and an evaluation circuit configured to subtract the variable cancellation signal from the received signal to generate a second input signal, wherein the adaptive filter circuit adjusts the variable cancellation signal based on the second input signal.

[0079] In Example 2, the subject matter of Example 1 may include wherein the first element is determined by a function which is inversely proportional to the number of iterations.

[0080] In Example 3, the subject matter of Example 1 may include wherein the first element is determined by a predetermined step size table.

[0081] In Example 4, the subject matter of Examples 1-3 may include wherein the second element is limited by a normalized least mean squares step size.

[0082] In Example 5, the subject matter of Examples 1-4 may include wherein the power of the first input signal is determined by the sum of the absolute value of its terms.

[0083] In Example 6, the subject matter of Examples 1-5 may include wherein a scalar is applied to the first element.

[0084] In Example 7, the subject matter of Example 6 may include wherein the scalar is dependent on an interference and/or a noise of the received signal.

[0085] In Example 8, the subject matter of Examples 6-7 may include wherein the scalar is represented by the formula:

$$\mu_i = m_1 * f(t * t_1)$$

wherein function  $f$  has lower and upper boundaries and has substantially decreasing characteristics inside of the lower and upper boundaries, where  $\mu_1$  is the first element,  $m_1$  is a magnitude factor,  $t_1$  is a time factor, and  $t$  is the time of the iteration.

[0086] In Example 9, the subject matter of Examples 1-8 may include wherein the step size is further limited by a minimum and maximum step size.

[0087] In Example 10, the subject matter of Example 9 may include wherein the minimum step size is determined by a predetermined required accuracy and tracking performance of the circuit in a settled state.

[0088] In Example 11, the subject matter of Examples 9-10 may include wherein the maximum step size is determined by an expected maximum of the second element.

[0089] In Example 12, the subject matter of Example 11 may include wherein a maximum of the first element is larger than the expected maximum of the second element.

[0090] In Example 13, the subject matter of Examples 1-12 may include the adaptive filter comprising barrel shifters, wherein each barrel shifter comprises a shift value.

[0091] In Example 14, the subject matter of Example 13 may include the barrel shifters configured to provide multipliers in the second input signal feedback with shift values.

[0092] In Example 15, the subject matter of Examples 13-14 may include wherein a first barrel shifter comprises a shift value for time iterations between 0 and  $t_b$ , inclusive of  $t_b$ .

[0093] In Example 16, the subject matter of Examples 13-15 may include wherein a second barrel shifter comprises a second shift value for time iterations greater than  $t_b$ .

[0094] In Example 17, the subject matter of Examples 1-16 may include the adaptive filter comprising a complex FIR unit configured to receive as input a plurality of outputs from registers from within the adaptive filter and output the variable cancellation signal.

[0095] In Example 18, the subject matter of Examples 1-17 may include the adaptive filter comprising one or more complex FIR taps configured to implement a one cycle delay.

[0096] In Example 19, the subject matter of Examples 1-18 may include the adaptive filter comprising at least one complex FIR blind tap configured to implement a compensating effect of a pipelined register in the circuitry.

[0097] In Example 20, the subject matter of Examples 1-19 may include a power detector configured to detect the power of the first input signal.

[0098] In Example 21, the subject matter of Example 20 may include wherein the power detector is further configured to stop the adaptive filter from producing the variable cancellation signal if the first input signal falls below a certain threshold.

[0099] In Example 22, the subject matter of Examples 1-21 may include wherein the circuitry is in a signal processing component of a communication device.

[0100] In Example 23, the subject matter of Examples 1-22 may include an input circuit configured to provide the first input signal to the adaptive filter unit.

[0101] In Example 24, the subject matter of Examples 1-23 may include wherein the first input signal is a transmission signal of a communication device.

[0102] In Example 25, the subject matter of Examples 1-24 may include wherein the circuitry is implemented as a self-interference cancellation (SIC) circuit in a communication device with duplex mode capabilities.

[0103] In Example 26, the subject matter of Examples 1-25 may include wherein the circuitry performs a time domain equalization in a communication device.

[0104] In Example 27, a communication device including a transceiver configured to receive a signal from a network; and a baseband processing component, including an adaptive filter circuit, configured to: receive a first input signal and produce a variable cancellation signal, wherein a step size for each iteration of the variable cancellation signal is the lesser of: a first element which monotonically decreases over the number of iterations; or a second element calculated from a power of the first input signal; and subtract the variable cancellation signal from the signal received from the network to generate a second input signal; and control the adaptive filter circuit to adjust the variable cancellation signal based on the second input signal.

[0105] In Example 28, the subject matter of Example 27 may include wherein the first element is determined by a function which is inversely proportional to the number of the iteration.

[0106] In Example 29, the subject matter of Example 27 may include wherein the first element is determined by a predetermined step size table.

[0107] In Example 30, the subject matter of Examples 27-29 may include wherein the second element is limited by a normalized least mean squares step size.

[0108] In Example 31, the subject matter of Examples 27-30 may include wherein the power of the first input signal is determined by the sum of the absolute value of its terms.

[0109] In Example 32, the subject matter of Examples 27-31 may include wherein a scalar is applied to the first element.

[0110] In Example 33, the subject matter of Example 32 may include wherein the scalar is dependent on an interference and/or a noise of the signal received from the network.

[0111] In Example 34, the subject matter of Examples 32-33 may include wherein the scalar is represented by the formula:

$$\mu_i = m_1 * f(t * t_1)$$

wherein function  $f$  has lower and upper boundaries and has substantially decreasing characteristics inside of the lower and upper boundaries, where  $\mu_1$  is the first element,  $m_1$  is a magnitude factor,  $t_1$  is a time factor, and  $t$  is the time of the iteration.

[0112] In Example 35, the subject matter of Examples 27-34 may include wherein the step size is further limited by a minimum and maximum step size.

[0113] In Example 36, the subject matter of Example 35 may include wherein the minimum step size is determined by a predetermined required accuracy and tracking performance of the circuit in a settled state.

[0114] In Example 37, the subject matter of Examples 35-36 may include wherein the maximum step size is determined by an expected maximum of the second element.

[0115] In Example 38, the subject matter of Example 37 may include wherein a maximum of the first element is larger than the expected maximum of the second element.

[0116] In Example 39, the subject matter of Examples 27-38 may include the adaptive filter comprising barrel shifters, wherein each barrel shifter comprises a shift value.

[0117] In Example 40, the subject matter of Example 39 may include the barrel shifters configured to provide multipliers in the second input signal feedback with shift values.

[0118] In Example 41, the subject matter of Examples 39-40 may include wherein a first barrel shifter comprises a shift value for time iterations between 0 and  $t_b$ , inclusive of  $t_b$ .

[0119] In Example 42, the subject matter of Examples 39-41 may include wherein a second barrel shifter comprises a second shift value for time iterations greater than  $t_b$ .

[0120] In Example 43, the subject matter of Examples 27-42 may include the adaptive filter comprising a complex FIR unit configured to receive as input a plurality of outputs from registers from within the adaptive filter and output the variable cancellation signal.

[0121] In Example 44, the subject matter of Examples 27-43 may include the adaptive filter comprising one or more complex FIR taps configured to implement a one cycle delay.

[0122] In Example 45, the subject matter of Examples 27-44 may include the adaptive filter comprising at least one complex FIR blind tap configured to implement a compensating effect of a pipelined register in the circuitry.

[0123] In Example 46, the subject matter of Examples 27-45 may include further comprising a power detector configured to detect the power of the first input signal.

[0124] In Example 47, the subject matter of Example 46 may include wherein the power detector is further configured to stop the adaptive filter from producing the variable cancellation signal if the first input signal falls below a certain threshold.

[0125] In Example 48, the subject matter of Examples 27-47 may include wherein the circuitry is in a signal processing component of a communication device.

[0126] In Example 49, the subject matter of Examples 27-48 may include an input circuit configured to provide the first input signal to the adaptive filter unit.

[0127] In Example 50, the subject matter of Examples 27-49 may include wherein the first input signal is a transmission signal of a communication device.

[0128] In Example 51, the subject matter of Examples 27-50 may include wherein the circuitry is implemented as a self-interference cancellation (SIC) circuit in a communication device with duplex mode capabilities.

[0129] In Example 52, the subject matter of Examples 27-51 may include wherein the baseband processing component performs a time domain equalization in a communication device.

[0130] In Example 53, the subject matter of Example 52 may include wherein a CDMA component of the baseband processing component performs the time domain equalization.

[0131] In Example 54, a method for determining a step size for each iteration of a variable cancellation signal of produced by an adaptive filter in a processing circuitry of a communication device, the method including: determining a first element which monotonically decreases over the number of iterations; determining a second element based on a power of a first input signal to the adaptive filter; and choosing the lesser of the first element and the second element as the step size for the iteration.

[0132] In Example 55, the subject matter of Example 54 may include determining the first element by a function which is inversely proportional to the number of the iteration.

[0133] In Example 56, the subject matter of Example 54 may include determining the first element with a predetermined step size table.

[0134] In Example 57, the subject matter of Examples 54-56 may include limiting the second element by a normalized least mean squares step size.

[0135] In Example 58, the subject matter of Examples 54-57 may include determining the power of the first input signal by the sum of the absolute value of its terms.

[0136] In Example 59, the subject matter of Examples 54-58 may include applying a scalar to the first element.

[0137] In Example 60, the subject matter of Example 59 may include wherein the scalar is dependent on an interference and/or a noise of a signal received at the communication device.

[0138] In Example 61, the subject matter of Examples 59-60 may include wherein the scalar is represented by the formula:

$$\mu_i = m_1 * f(t * t_1)$$

wherein function  $f$  has lower and upper boundaries and has substantially decreasing characteristics inside of the lower and upper boundaries, where  $\mu_1$  is the first element,  $m_1$  is a magnitude factor,  $t_1$  is a time factor, and  $t$  is the time of the iteration.

[0139] In Example 62, the subject matter of Examples 54-61 may include limiting the step size by a minimum and maximum step size.

[0140] In Example 63, the subject matter of Example 62 may include determining the minimum step size by a predetermined required accuracy and tracking performance of the circuit in a settled state.

[0141] In Example 64, the subject matter of Examples 62-63 may include determining the maximum step size by an expected maximum of the second element.

[0142] In Example 65, the subject matter of Example 64 may include wherein a maximum step size of the first element is larger than the expected maximum of the second element.

[0143] In Example 66, the subject matter of Examples 64-65 may include providing barrel shifters to provide multipliers of the second input signal feedback of the adaptive filter with shift values.

[0144] In Example 67, the subject matter of Example 66 may include wherein a first barrel shifter comprises a shift value for time iterations between 0 and  $t_b$ , inclusive of  $t_b$ .

[0145] In Example 68, the subject matter of Examples 66-67 may include wherein a second barrel shifter comprises a second shift value for time iterations greater than  $t_b$ .

[0146] In Example 69, the subject matter of Examples 54-68 may include providing a power detector configured to detect the power of the first input signal.

[0147] In Example 70, the subject matter of Example 69 may include configuring the power detector to stop the adaptive filter from producing the variable cancellation signal if the first input signal falls below a certain threshold.

[0148] In Example 71, a computer readable medium with program instructions when executed cause a processor of a device to implement a method or realize an apparatus as claimed in any preceding Example.

[0149] While the above descriptions and connected figures may depict electronic device components as separate elements, skilled persons will appreciate the various possibilities to combine or integrate discrete elements into a single element. Such may include combining two or more circuits for form a single circuit, mounting two or more circuits onto a common chip or chassis to form an integrated element, executing discrete software components on a common processor core, etc. Conversely, skilled persons will recognize the possibility to separate a single element into two or more discrete elements, such as splitting a single circuit into two or more separate circuits, separating a chip or chassis into discrete elements originally provided thereon, separating a software component into two or more sections and executing each on a separate processor core, etc.

[0150] It is appreciated that implementations of methods detailed herein are demonstrative in nature, and are thus understood as capable of being implemented in a corresponding device. Likewise, it is appreciated that implementations of devices detailed herein are understood as capable of being implemented as a corresponding method. It is thus understood that a device corresponding to a method detailed herein may include one or more components configured to perform each aspect of the related method.

[0151] All acronyms defined in the above description additionally hold in all claims included herein.

[0152] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

What is claimed is:

1. A circuitry for determining an adaptive filter step size for processing a received signal, the circuitry comprising:

an adaptive filter circuit configured to receive a first input signal and produce a variable cancellation signal, wherein a step size for each iteration of the variable cancellation signal is the lesser of:

a first element which monotonically decreases over the number of iterations; or

a second element calculated from a power of the first input signal; and

an evaluation circuit configured to subtract the variable cancellation signal from the received signal to generate a second input signal, wherein the adaptive filter circuit adjusts the variable cancellation signal based on the second input signal.

2. The circuitry of claim 1, wherein the first element is determined by a function which is inversely proportional to the number of iterations.
3. The circuitry of claim 1, wherein the first element is determined by a predetermined step size table.
4. The circuitry of any one of claims 1-3, wherein the second element is limited by a normalized least mean squares step size.
5. The circuitry of any one of claims 1-3, wherein a scalar is applied to the first element.
6. The circuitry of claim 5, wherein the scalar is dependent on an interference and/or a noise of the received signal.
7. The circuitry of claim 5, wherein the scalar is represented by the formula:

$$\mu_i = m_1 * f(t * t_i)$$

wherein function  $f$  has lower and upper boundaries and has substantially decreasing characteristics inside of the lower and upper boundaries, where  $\mu_1$  is the first element,  $m_1$  is a magnitude factor,  $t_1$  is a time factor, and  $t$  is the time of the iteration.

8. The circuitry of claim 1, wherein the step size is further limited by a minimum and maximum step size.
9. The circuitry of claim 1, the adaptive filter comprising barrel shifters, wherein each barrel shifter comprises a shift value.
10. The circuitry of claim 9, the barrel shifters configured to provide multipliers in the second input signal feedback with shift values.
11. The circuitry of claim 9 or 10, wherein a first barrel shifter comprises a shift value for time iterations between 0 and  $t_b$ , inclusive of  $t_b$ , wherein  $t_b$  is a predetermined time.
12. The circuitry of claim 9 or 10, wherein a second barrel shifter comprises a second shift value for time iterations greater than  $t_b$ , wherein  $t_b$  is a predetermined time.
13. The circuitry of claim 1, further comprising a power detector configured to detect the power of the first input signal.
14. The circuitry of claim 13, wherein the power detector is further configured to stop the adaptive filter from producing the variable cancellation signal if the first input signal falls below a certain threshold.
15. A communication device comprising:
  - a transceiver configured to receive a signal from a network; and
  - a baseband processing component, comprising an adaptive filter circuit, configured to:
    - receive a first input signal and produce a variable cancellation signal, wherein a step size for each iteration of the variable cancellation signal is the lesser of:
      - a first element which monotonically decreases over the number of iterations; or
      - a second element calculated from a power of the first input signal; and
    - subtract the variable cancellation signal from the signal received from the network to generate a second input signal; and
    - control the adaptive filter circuit to adjust the variable cancellation signal based on the second input signal.

16. A method for determining a step size for each iteration of a variable cancellation signal produced by an adaptive filter in a processing circuitry of a communication device, the method comprising:
- determining a first element which monotonically decreases over the number of iterations;
  - determining a second element from a power of a first input signal to the adaptive filter;
  - and
  - choosing the lesser of the first element and the second element as the step size for the iteration.
17. The method of claim 16, further comprising determining the first element by a function which is inversely proportional to the number of the iteration.
18. The method of claim 16, further comprising determining the first element with a predetermined step size table.
19. The method of claim 16, further comprising limiting the second element by a normalized least mean squares step size.
20. The method of any one of claims 16-19, further comprising applying a scalar to the first element.
21. The method of claim 20, wherein the scalar is dependent on an interference and/or a noise of a signal received at the communication device.
22. The method of claim 20, wherein the scalar is represented by the formula:
- $$\mu_i = m_1 * f(t * t_1)$$
- wherein function  $f$  has lower and upper boundaries and has substantially decreasing characteristics inside of the lower and upper boundaries, where  $\mu_1$  is the first element,  $m_1$  is a magnitude factor,  $t_1$  is a time factor, and  $t$  is the time of the iteration.
23. The method of claim 16, further comprising providing a power detector configured to detect the power of the first input signal.

24. The method of claim 23, further comprising configuring the power detector to stop the adaptive filter from producing the variable cancellation signal if the first input signal falls below a certain threshold.
25. Machine-readable storage including machine-readable instructions, when executed, to implement a method or realize a circuitry as claimed in any preceding claim.

FIG. 1

100

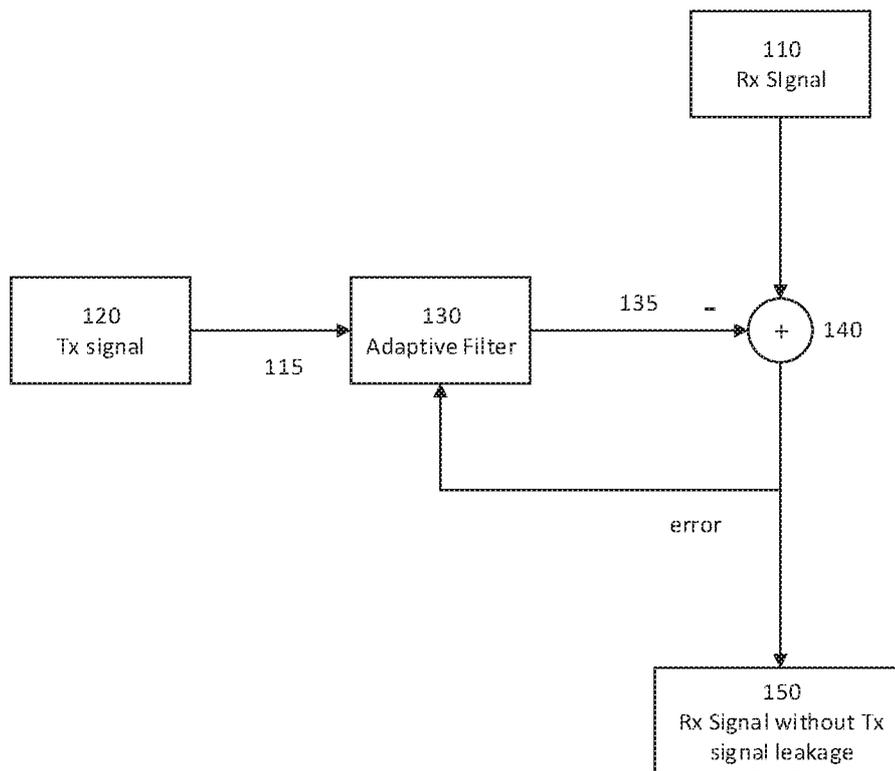


FIG. 2

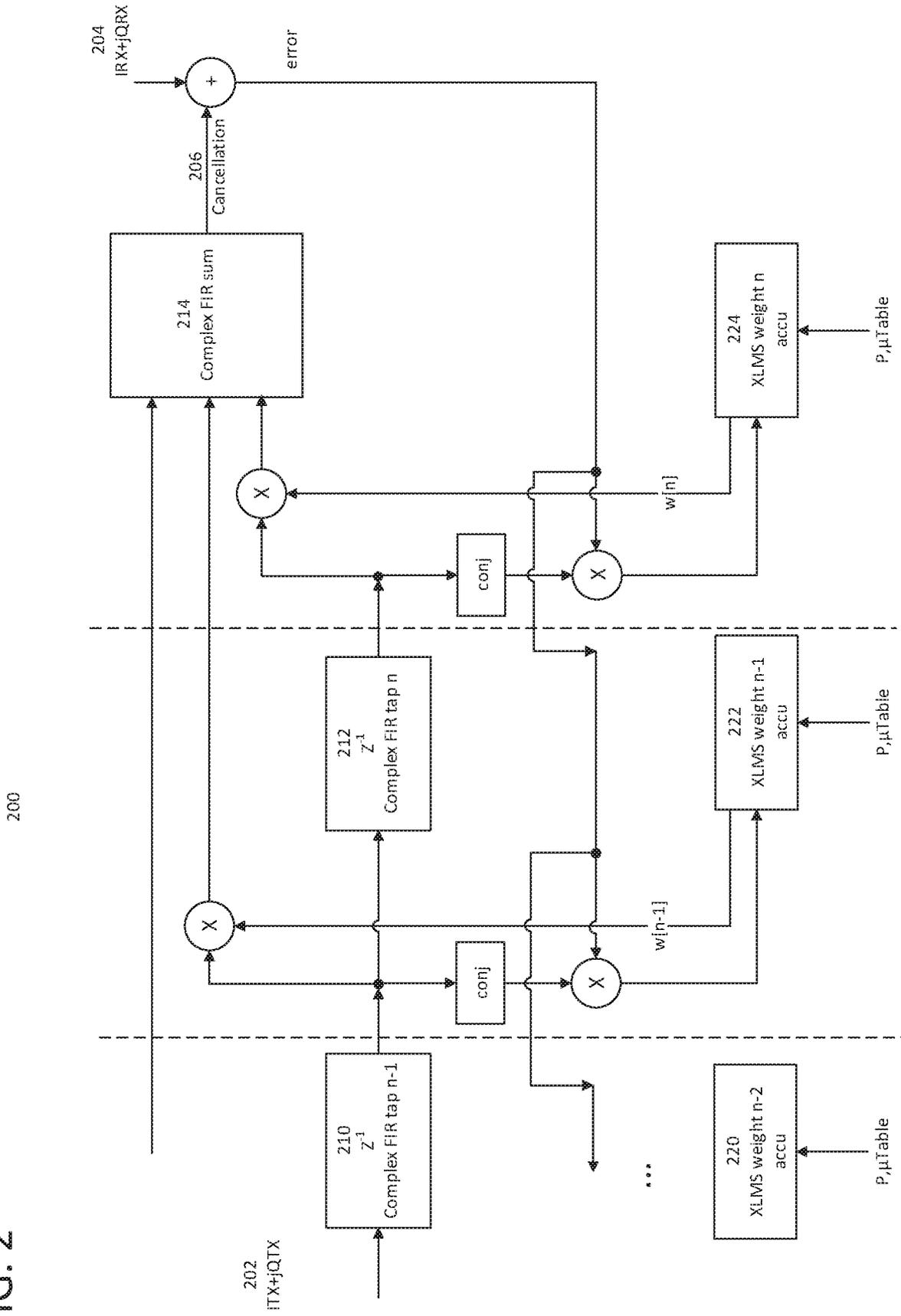


FIG. 3

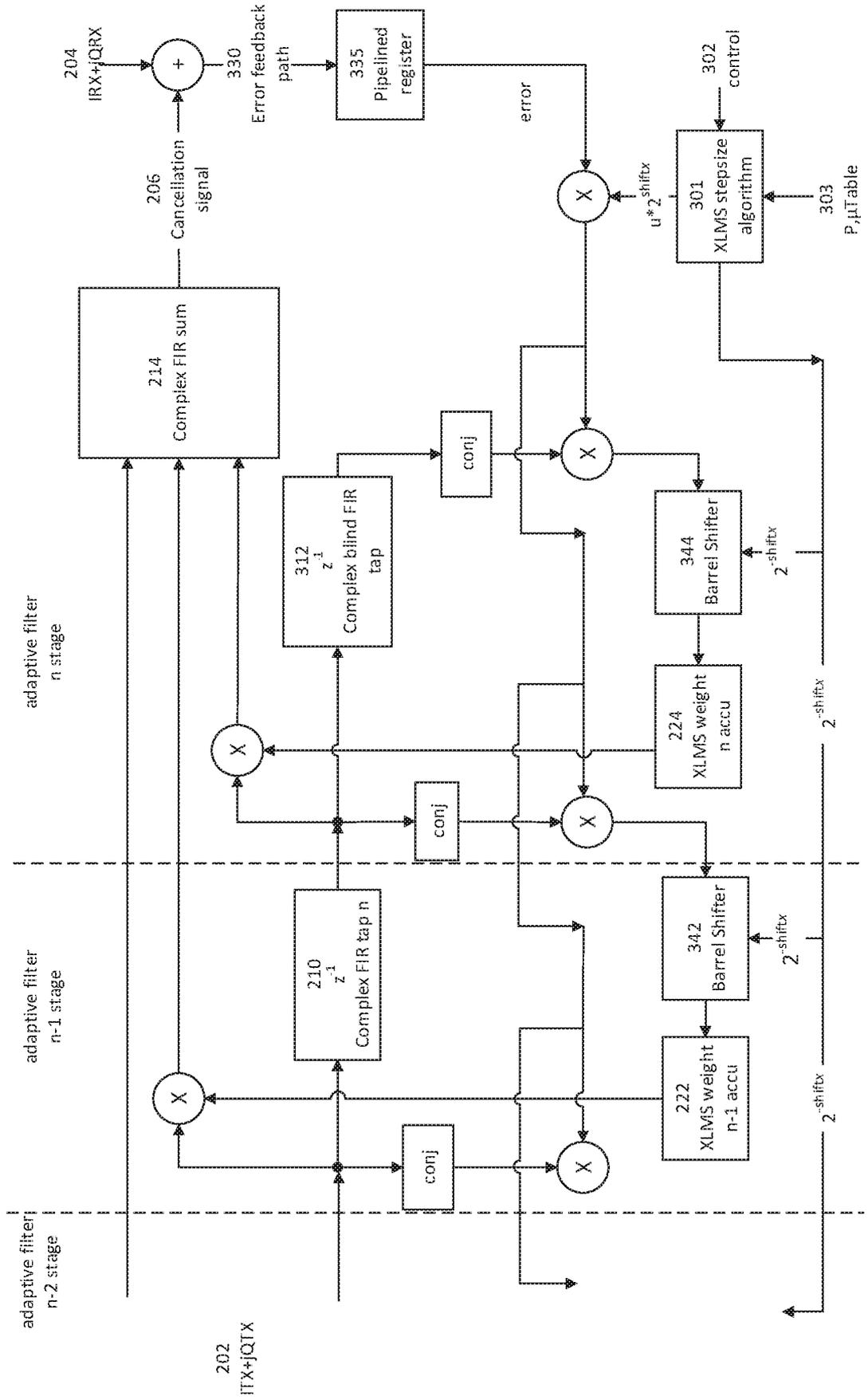
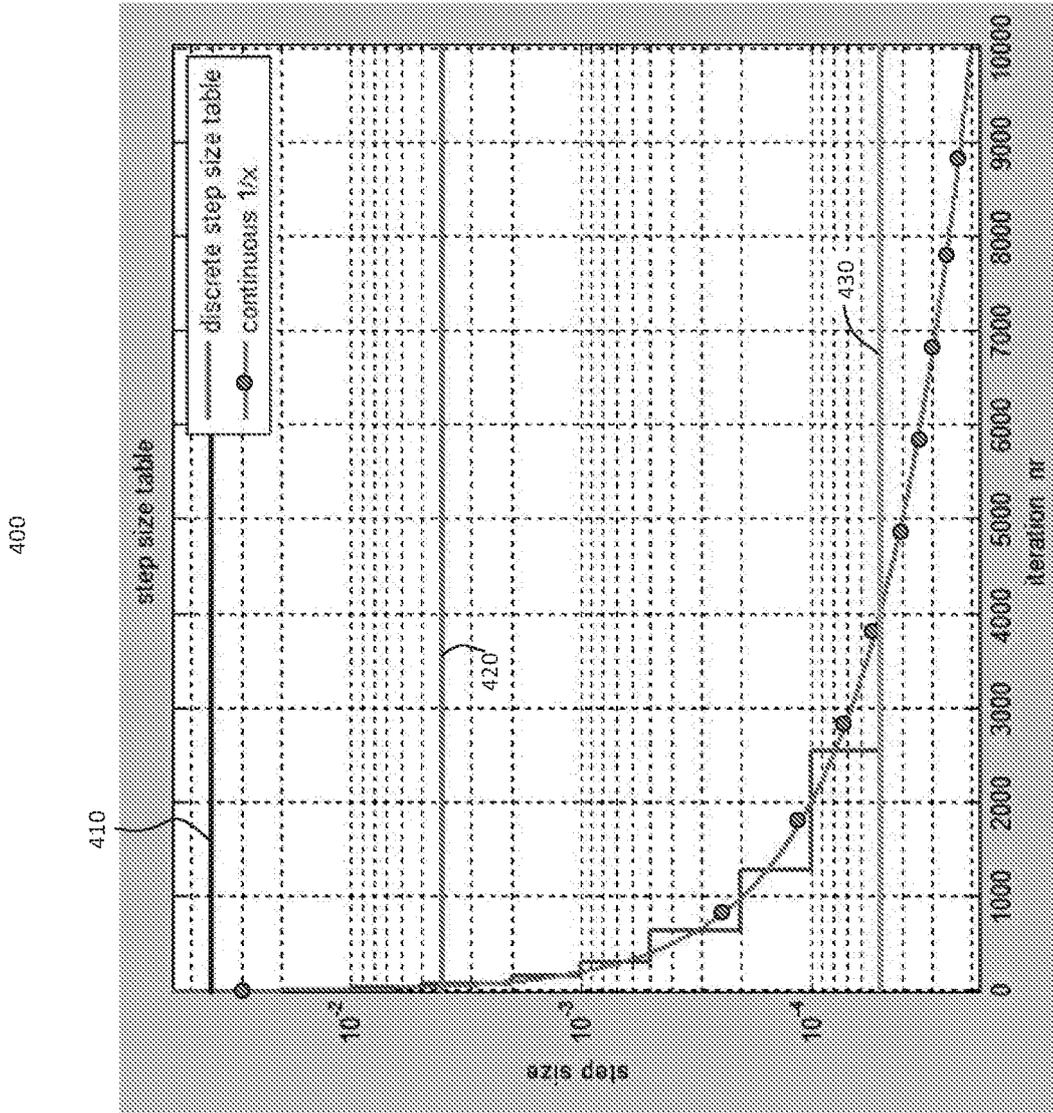


FIG. 4



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450
    if(i1<10*t1)
        u1=0.04*m1;
    elseif(i1<20*t1)
        u1=0.02*m1;
    elseif(i1<40*t1)
        u1=0.01*m1;
    elseif(i1<80*t1)
        u1=0.005*m1;
    elseif(i1<160*t1)
        u1=0.002*m1;
    elseif(i1<320*t1)
        u1=0.001*m1;
    elseif(i1<640*t1)
        u1=0.0005*m1;
    elseif(i1<1280*t1)
        u1=0.0002*m1;
    elseif(i1<2560*t1)
        u1=0.0001*m1;
    else
        u1=0.00005*m1;
    end
    mu=min(u1,1/(1+1/LMSTAPS*
    (sum(abs(real(TX (i1:i1+LMSTAPS-1))))+
    abs(imag(TX (i1:i1+LMSTAPS-1))))^2));
  
```

FIG. 5

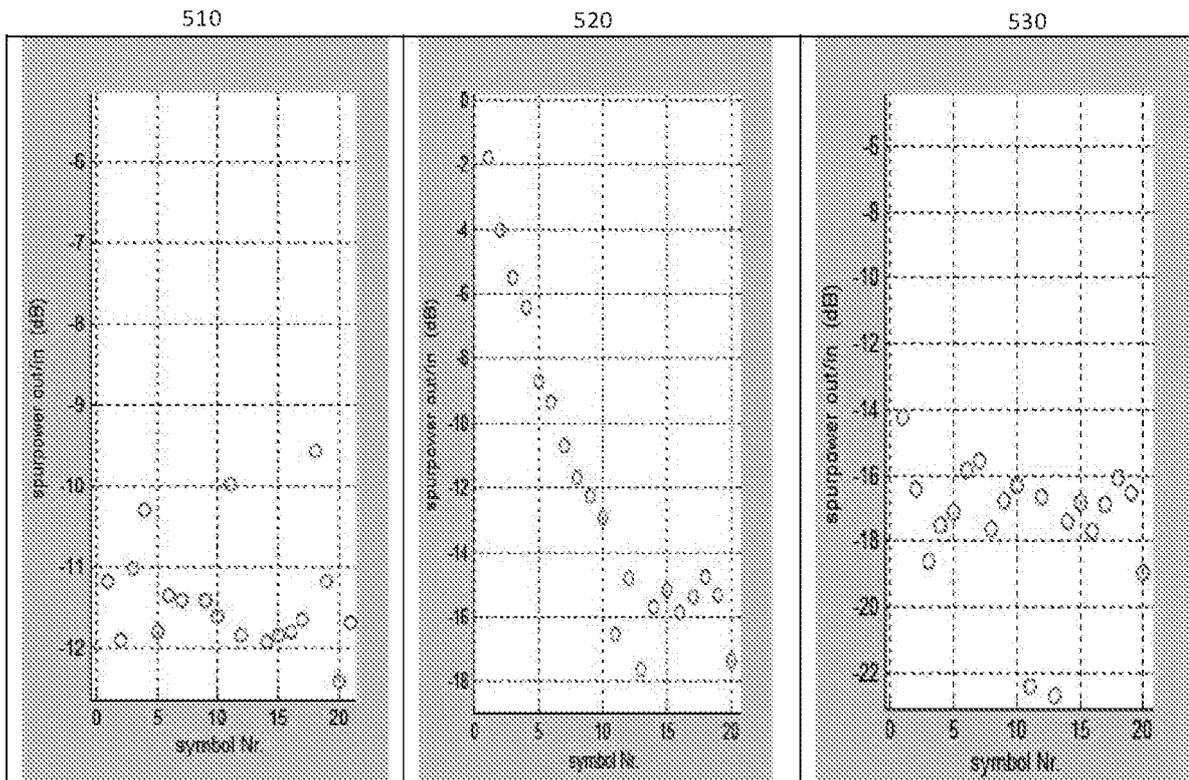


FIG. 6

600

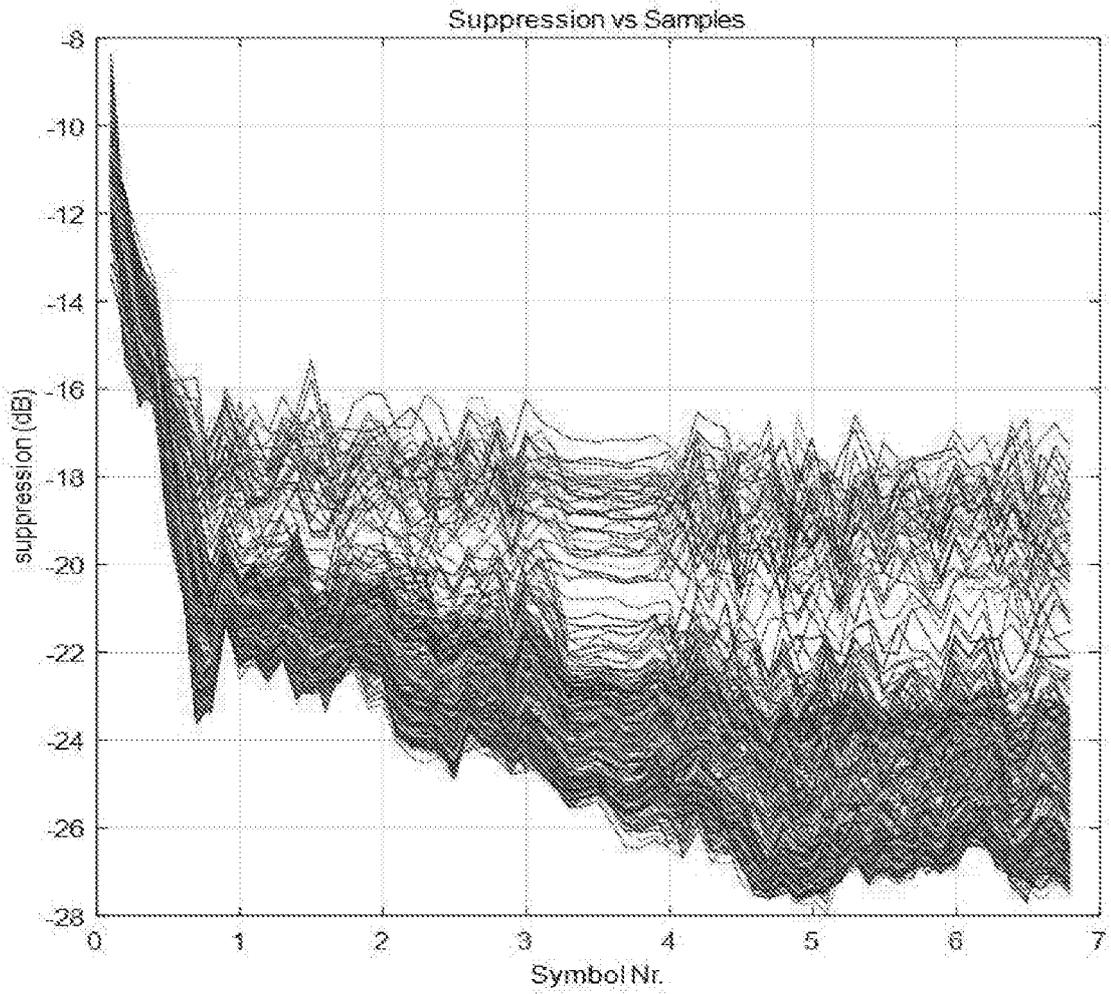
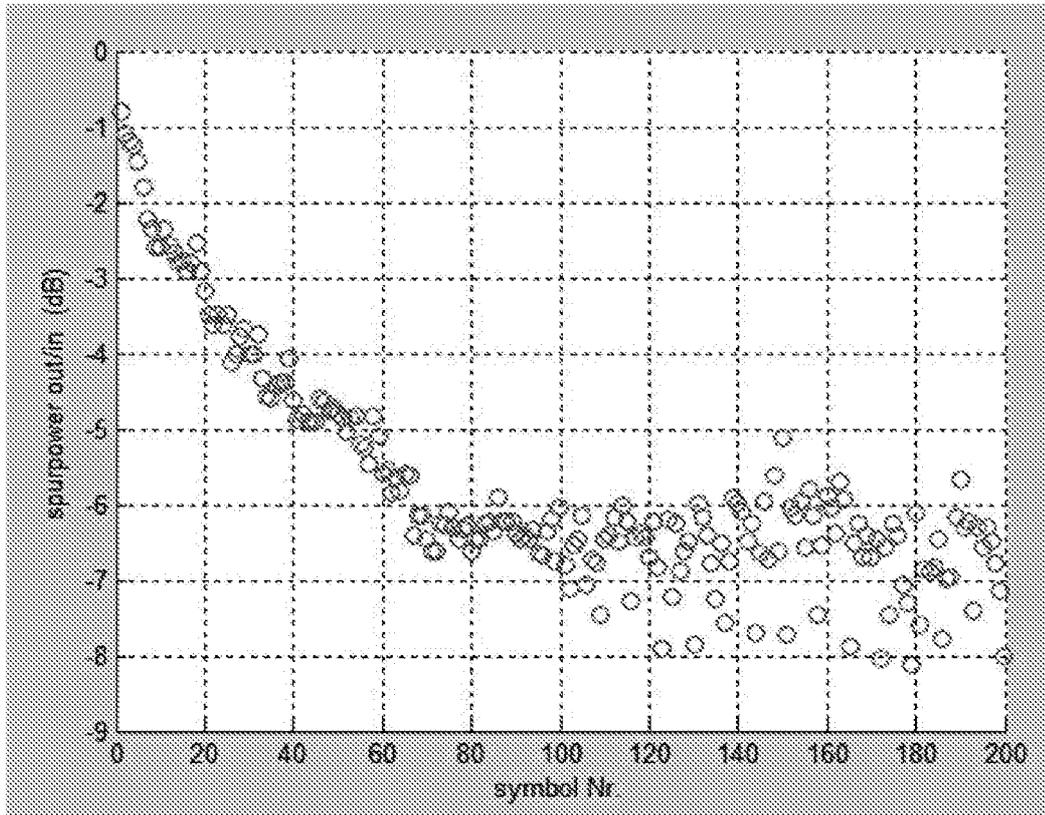


FIG. 7

700



750

Time: after n LTE symbols	RLS (SIR 30dB) Cancellation (higher is better)	novel XLMS (SIR 30dB) Cancellation (higher is better)
1 Symbol	-9.1dB	+0.8dB
7 Symbols	-1.9dB	+2.2dB
80 Symbols	+3.0dB	+6.5dB

FIG. 8

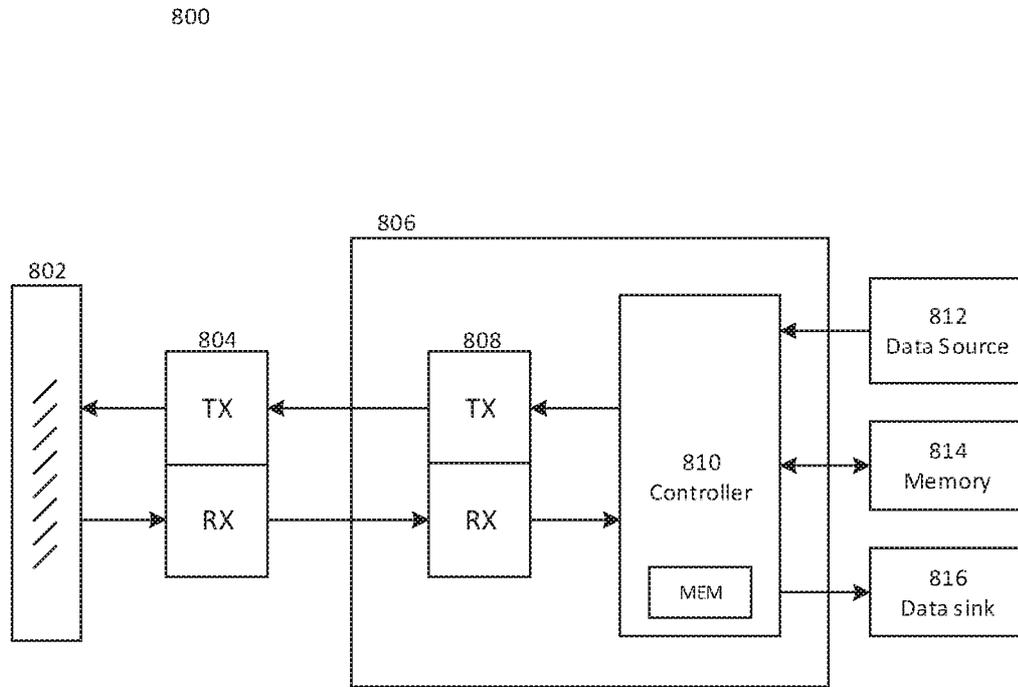
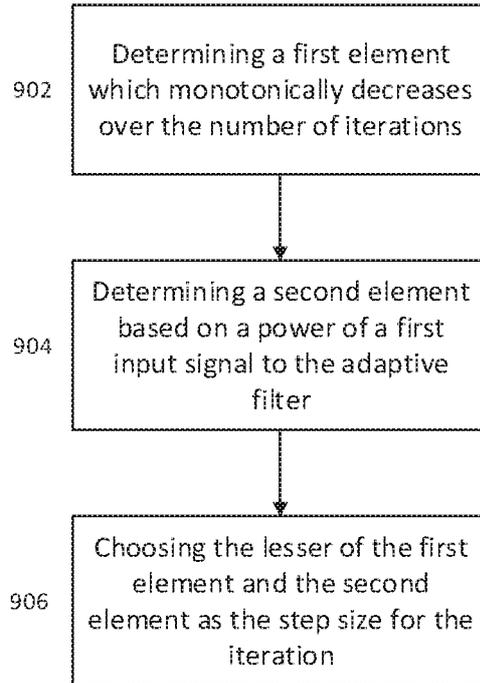


FIG. 9

900



**A. CLASSIFICATION OF SUBJECT MATTER****H04L 25/03(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H04L 25/03; G06F 15/00; H04L 27/01; H03H 7/40; H04L 25/02; H04B 1/02; H04B 1/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: adaptive filter, input, signal, step size, iteration, power

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category <sup>1</sup>	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2008-0175308 AI (MARK FIMOFF et al.) 24 July 2008 See paragraphs [0017] , [0028] , [0052H0056] , [0063] , [0067] ; and figure 9C.	1-6 ,8-21 ,23-25 7, 22
Y	US 2006-0041403 AI (MARWAN JABER) 23 February 2006 See paragraphs [0047] , [0061] , [0066] , [0118] , [0133] , [0136] , [0189] ; and figure 13 .	1-6 ,8-21 ,23-25
Y	US 2010-0266006 AI (CARL W. WERNER et al.) 21 October 2010 See paragraphs [0124] , [0175] ; and figure 8 .	9-12
A	KR 10-2016-0106665 A (QUALCOMM INCORPORATED) 12 September 2016 See paragraphs [0019H0020] , [0025]- [0028] ; and figures 3a-3b .	1-25
A	KR 10-1500922 BI (POSTECH ACADEMY-INDUSTRY FOUNDATION) 18 March 2015 See paragraphs [0022] , [0081H0082] ; and figure 4 .	1-25

**I** Further documents are listed in the continuation of Box C. See patent family annex.

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"&amp;" document member of the same patent family

Date of the actual completion of the international search

10 November 2017 (10.11.2017)

Date of mailing of the international search report

**10 November 2017 (10.11.2017)**

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

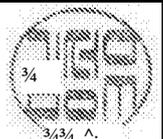
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## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

**PCT/US2017/046401**

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2008-0175308 AI	24/07/2008	US 2008-0175309 AI	24/07/2008
		US 7616685 B2	10/11/2009
		<b>us</b> 8385397 B2	26/02/2013
		<b>wo</b> 2008-089379 A2	24/07/2008
		<b>wo</b> 2008-089379 A3	12/09/2008
		<b>wo</b> 2009-009536 AI	15/01/2009
US 2006-0041403 AI	23/02/2006	<b>us</b> 7533140 B2	12/05/2009
US 2010-0266006 AI	21/10/2010	EP 1618597 A2	25/01/2006
		EP 1618597 B1	25/03/2009
		EP 1626547 A2	15/02/2006
		EP 1626547 A3	28/03/2007
		EP 1626547 B1	28/10/2009
		EP 1665612 A2	07/06/2006
		EP 1698131 AI	06/09/2006
		EP 2063593 A2	27/05/2009
		EP 2063593 B1	10/06/2015
		EP 2107746 A2	07/10/2009
		EP 2107746 A3	30/12/2009
		EP 2107746 B1	28/09/2016
		EP 2259519 A2	08/12/2010
		EP 2259519 A3	04/04/2012
		EP 2259519 B1	03/06/2015
		EP 2945335 AI	18/11/2015
		EP 2945335 B1	07/06/2017
		EP 3190758 AI	12/07/2017
		JP 2007-515130 A	07/06/2007
		JP 2007-525061 A	30/08/2007
		JP 4718451 B2	06/07/2011
		JP 4776548 B2	21/09/2011
		US 2004-0203559 AI	14/10/2004
		<b>us</b> 2005-0058234 AI	17/03/2005
		<b>us</b> 2005-0111585 AI	26/05/2005
		<b>us</b> 2005-0134305 AI	23/06/2005
		<b>us</b> 2005-0134306 AI	23/06/2005
		<b>us</b> 2005-0134307 AI	23/06/2005
		<b>us</b> 2005-0157780 AI	21/07/2005
		<b>us</b> 2005-0157781 AI	21/07/2005
		<b>us</b> 2006-0158225 AI	20/07/2006
		<b>us</b> 2006-0233291 AI	19/10/2006
		<b>us</b> 2006-0280272 AI	14/12/2006
		<b>us</b> 2007-0080718 AI	12/04/2007
		<b>us</b> 2009-0002030 AI	01/01/2009
		<b>us</b> 2009-0175326 AI	09/07/2009
		<b>us</b> 2009-0285272 AI	19/11/2009
		<b>us</b> 2010-0117706 AI	13/05/2010
		<b>us</b> 2010-0142610 AI	10/06/2010
		<b>us</b> 2012-0213267 AI	23/08/2012

## INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2017/046401

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		US 2012-0224621 AI	06/09/2012
		US 2012-0288027 AI	15/11/2012
		US 2013-0272359 AI	17/10/2013
		US 2013-0272446 AI	17/10/2013
		US 2015-0222303 AI	06/08/2015
		US 2015-0319016 AI	05/11/2015
		US 2016-0218895 AI	28/07/2016
		US 2016-0308693 AI	20/10/2016
		US 7030657 B2	18/04/2006
		US 7092472 B2	15/08/2006
		US 7126378 B2	24/10/2006
		US 7176721 B2	13/02/2007
		US 7199615 B2	03/04/2007
		US 7233164 B2	19/06/2007
		US 7397848 B2	08/07/2008
		US 7412016 B2	12/08/2008
		US 7423454 B2	09/09/2008
		US 7433397 B2	07/10/2008
		US 7656981 B2	02/02/2010
		US 7706480 B2	27/04/2010
		US 7715471 B2	11/05/2010
		US 7715501 B2	11/05/2010
		US 7715509 B2	11/05/2010
		US 8170163 B2	01/05/2012
		US 8183887 B2	22/05/2012
		US 8275030 B2	25/09/2012
		US 8428196 B2	23/04/2013
		US 8564328 B2	22/10/2013
		US 8994398 B2	31/03/2015
		US 9000803 B2	07/04/2015
		US 9025678 B2	05/05/2015
		US 9287909 B2	15/03/2016
		US 9407473 B2	02/08/2016
		US 9705710 B2	11/07/2017
		WO 2004-093144 A2	28/10/2004
		WO 2004-093144 A3	12/10/2006
		WO 2005-029743 A2	31/03/2005
		WO 2005-029743 A3	06/07/2006
		WO 2005-060193 A2	30/06/2005
κR 10-2016-0106665 A	12/09/2016	CN 105900341 A	24/08/2016
		EP 3092720 A2	16/11/2016
		JP 2017-502614 A	19/01/2017
		US 2015-0200721 AI	16/07/2015
		US 9306654 B2	05/04/2016
		WO 2015-105810 A2	16/07/2015
		WO 2015-105810 A3	03/09/2015
κR 10-1500922 BI	18/03/2015	None	