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(54) **Title**: CARBON CONTAINING LOW-K DIELECTRIC CONSTANT RECOVERY USING UV TREATMENT

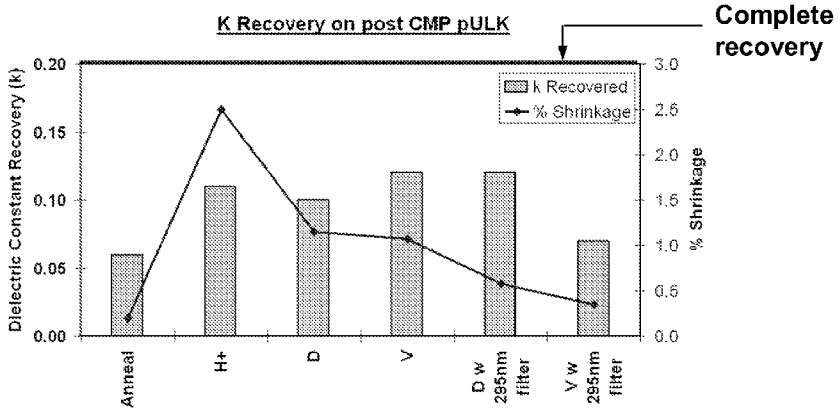

FIG. 5

(57) **Abstract**: A method for the ultraviolet (UV) treatment of carbon-containing low-k dielectric and associated apparatus enables process induced damage repair. The methods of the invention are particularly applicable in the context of damascene processing to recover lost low-k property of a dielectric damaged during processing, either pre-metallization, post-planarization, or both. UV treatments can include an exposure of the subject low-k dielectric to a constrained UV spectral profile and/or chemical silylating agent, or both.

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CARBON CONTAINING LOW-K DIELECTRIC CONSTANT RECOVERY USING UV TREATMENT

BACKGROUND OF THE INVENTION

[0001] The invention relates to low dielectric constant layers in semiconductor processing for use in various applications. More specifically, the invention relates to the treatment for repair of process-induced damage of low dielectric constant dielectric materials in, for example, damascene processing.

[0002] The invention relates to semiconductor processing, in particular to repair of process-induced damage of low dielectric constant dielectric materials in, for example, damascene processing.

[0003] Low dielectric constant (low-k) insulating materials have been integrated into semiconductor devices in order to address reduced feature sizes and high performance requirements. These low-k dielectrics are mechanically weaker than previous generation dielectric materials. The inherently weak nature of the low-k dielectric material can pose significant challenges for downstream electronic-packaging processes and material compatibility.

[0004] Low-k materials are, by definition, those semiconductor-grade insulating materials that have a dielectric constant ("k") lower than that of SiO_2, i.e., 3.9. Various types of low-k materials can have dielectric constants ranging from about 3.8-3.6 (e.g., fluorosilicate glass (FSG)), to less than about 3.2 (e.g., (carbon doped oxide (CDO)), to as low as 2.2 (e.g., spin-on glass (SOG)) or even lower, and encompass low-k dielectrics referred to as “ultra low-k” (ULK) and “extreme ultra low-k” (ELK). In many CDO low-k implementations, such as are described herein as one aspect of the invention, suitable carbon-containing low-k materials have a dielectric constant of about 2.7 or lower. To further reduce the size of devices on integrated circuits, it has become necessary to use conductive materials having low resistivity and insulators having low dielectric constants to reduce the capacitive coupling between adjacent metal lines. Low-k materials are being integrated into the devices to improve device performance and allow for device scaling.

[0005] Low-k materials are less dense than standard insulating materials such as SiO_2. This low density introduces a host of process integration and material compatibility difficulties. Achieving a balance between maintaining a low-k film's

integrity, integrating it properly, and performing the necessary stripping, cleaning, and conditioning is challenging. Patterning processes (etching, stripping, deposition, and cleaning) can also have a drastic impact on the integrity of carbon-containing low-k materials, in particular SiOC-based low-k materials.

[0006] The properties that give carbon-containing low-k dielectric materials their desirable low dielectric constants are the very same properties that are leading to significant integration challenges. Carbon-containing low-k materials achieve lower dielectric constants through the incorporation of non-polar covalent bonds (e.g., from the addition of carbon) and the introduction of porosity to decrease film density. Introducing porosity or the incorporation of terminal bonds, such as $Si\text{-}CH_3$, breaks the continuity of the rigid Si-O-Si lattice of traditional oxides, yielding a lower dielectric constant film that is both mechanically and chemically weaker. Because of the mechanical weakness, carbon-containing low-k films are susceptible to kinetic plasma damage that can undesirably densify the film and thus increase the film's effective k value.

[0007] Furthermore, chemical plasmas used in semiconductor processing operations to which dielectrics are exposed can modify carbon-containing low-k films where bonds such as $Si\text{-}CH_3$ are readily broken. The susceptibility of carbon-containing low-k materials to plasma modification poses a serious integration challenge since plasma processes are routinely used to etch, clean, and deposit films in the manufacturing of a semiconductor device. In a typical Damascene process flow, prior to metal barrier deposition, process induced carbon-containing low-k dielectric damage can be incurred by a patterned low-k dielectric from (plasma) etch, dry resist strip, wet cleaning and dry cleaning. Carbon-containing low-k materials are also susceptible to the intercalation of plasma species, residues, solvents, moisture, and precursor molecules that can either adsorb into, outgas from, or chemically modify the film. Thereafter, a conductive material, typically a metal, for example copper, is deposited onto the patterned dielectric layer to fill vias and trenches formed in the dielectric layer. Then, excess metal is removed via chemical mechanical polishing (CMP), thereby forming a planar surface comprising regions of exposed copper and low-k dielectric onto which other layers, such as a dielectric barrier, are deposited. The CMP process typically damages the low-k dielectric, resulting in

carbon loss and water absorption. This causes the k of the low-k dielectric to increase, thereby lowering the RC improvement that the low-k material can potentially provide.

[0008] Also, exposed metal, particularly copper, regions are subject to oxidation prior to the formation of a dielectric barrier or subsequent layers on the wafer surface. And, organic residues of anti-corrosion components of CMP slurry, for example benzotriazole (BTA), may remain on a wafer surface after a CMP process. The presence of copper oxide and organic residue causes problems with the adhesion of the dielectric barrier on the wafer surface. Therefore, various cleaning processes may be used to remove such oxide and residue (another form of process-induced damage). In one specific example, such a wafer may be exposed to a direct plasma in a plasma-enhanced chemical vapor deposition (PECVD) processing chamber for a period of time prior to introducing chemical vapors to the processing chamber. The use of a reducing plasma, such as an ammonia or hydrogen plasma, may reduce copper oxide and hydrocarbons on the surface, thereby cleaning the surface. However, depending upon processing conditions, such direct plasmas also may affect a low-k dielectric surrounding the copper because the low-k material is locally densified at the surface either by ion bombardment or because of bound carbon removal through chemical activity. Some of the k damage induced by operations such as CMP to the low-k material may be recovered by doing a short anneal prior to the above described pre-treatment and etch stop deposition, but the recovery is only marginal.

SUMMARY OF THE INVENTION

[0009] The present invention provides a method for treatment of carbon-containing low-k dielectric with ultraviolet (UV) radiation and/or a chemical silylating agent, for the repair of process-induced dielectric damage. The carbon-containing low-k dielectric may be, but is not limited to, carbon-doped oxide (CDO) having a dielectric constant of 2.7 or lower, including ultra low-k dielectrics having pre-processing dielectric constants as low as 2.6, 2.5, 2.4 or lower, and possibly including a metal feature. The methods of the invention are particularly applicable in the context of damascene processing to help recover lost low-k (offset increased dielectric constant) of a dielectric damaged during processing, either pre-metallization, post-planarization, or both. In various embodiments of the invention, the treatment is conducted in such

a way that shrinkage of the dielectric is reduced or minimized and/or the extent of k-recovery is greatly enhanced relative to conventional annealing techniques.

[00010] In various embodiments, the incident UV radiation has a wavelength profile selected or configured to achieve k-recovery with relatively little dielectric shrinkage, in particular UV radiation that has a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm, for example UV radiation that has a spectral profile characterized by greater than 50% of the UV radiation power in a wavelength range of about 300 to 450 nm, or less than 10% of the UV radiation power in a wavelength range below 300nm.

[00011] In other embodiments, the treatment combines UV radiation exposure with exposure to a chemical silylating agent. In various embodiments, the incident UV radiation may or may not be as characterized above.

[00012] The carbon containing low-k dielectric that is the subject of the treatment may be at any stage of semiconductor processing, and the treatment is generally applied following a processing operation in which it has been subjected to conditions that have caused its dielectric constant to be increased. Examples are following an etching operation to form trenches in the dielectric, such as pre-metallization in damascene processing. Or, after chemical mechanical polishing (CMP) of a dielectric surface, such as post-metallization and pre-barrier layer deposition in a damascene process. The invention may also be more generally applicable in any semiconductor processing context to decrease the dielectric constant of a susceptible carbon containing dielectric. For example, receiving in a processing chamber a semiconductor device substrate comprising a carbon containing dielectric, and exposing the semiconductor device substrate to UV radiation and, in some embodiments, a chemical silylating agent, as described herein, such that the dielectric constant of the carbon containing dielectric is increased.

[00013] This process is amenable to inclusion on a properly designed load lock or as a module for a PECVD semiconductor wafer processing system, such as a Vector Extreme configured PECVD system, available from Novellus Systems, Inc., San Jose, CA, for example.

[00014] In one aspect, therefore, the invention relates to a method of forming a semiconductor device. The method involves receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric having a first dielectric constant. The carbon containing low-k dielectric is exposed to a UV treatment, the treatment including at least one of:

(a) exposure to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm; and

(b) exposure UV radiation and a chemical silylating agent.

The dielectric constant of the carbon-containing low-k dielectric is decreased to a second dielectric constant.

[00015] In other aspects, the invention may be implemented in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels and the like. The invention may also be implemented as an apparatus configured to accomplish the methods described herein. A suitable apparatus includes hardware for accomplishing the process operations and a system controller having instructions for controlling process operations in accordance with the present invention. Machine-readable media containing instructions for controlling process operations in accordance with the present invention may be coupled to the system controller.

BRIEF DESCRIPTION OF THE DRAWINGS

[00016] Figure 1 is a process flow chart depicting a method of UV treatment and a process context in accordance with an embodiment of the invention.

[00017] Figures 2A-2D are cross-sectional diagrams illustrating the formation of a semiconductor device by a dual damascene process in accordance with an embodiment of the invention.

[00018] Figure 3 is a schematic diagram of an example process chamber suitable for implementing the present invention.

[00019] Figure 4 depicts emission spectra showing the radiated power profiles for H+, D and V bulbs in Fig. 4 (a), (b) and (c), respectively.

[00020] Figures 5 and 6 depict data plots illustrating the benefits of UV treatments in accordance with the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[00021] Embodiments of the present invention are described herein primarily in the context of a treatment for carbon-containing low-k dielectric repair in damascene processing. However, the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to those of ordinary skill in the art having the benefit of this disclosure. Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings.

Introduction

[00022] The term "semiconductor device" as used herein refers to any device formed on a semiconductor substrate or any device possessing a semiconductor material. In many cases, a semiconductor device participates in electronic logic or memory, or in energy conversion. The term "semiconductor device" subsumes partially fabricated devices (such as partially fabricated integrated circuits) as well as completed devices available for sale or installed in particular apparatus. In short, a semiconductor device may exist at any state of manufacture that employs a method of this invention or possesses a structure of this invention.

[00023] The present invention provides a method of semiconductor device fabrication that involves exposure of a carbon containing low-k dielectric to UV radiation having certain wavelength profiles and/or in combination with chemical silylating agents, or both, to reduce the dielectric constant of the subject carbon containing low-k dielectric. Treatments in accordance with the invention are effective for the repair of process-induced damage to the dielectric, for example, broken Si-CH_3 bonds in carbon-containing low-k dielectric (e.g., ULK CDO) resulting from plasma trench etching or CMP. Applicable carbon containing low-k dielectrics typically have SiO-based backbones doped with carbon, in particular CDO (for example, those formed from octamethyl cyclotetrasiloxane (OMCTS), tetramethylcyclotetrasiloxane (TMCTS), dimethyldimethoxysilane (DMDMOS), and diethoxymethylsilane (DEMS) and other known CDO precursors), but may also include hybrid polymers incorporating both C, Si and O in the backbone. The

inventive methods are particularly, though not exclusively, applicable in the context of damascene processing. The invention also related to apparatus configured to implement the described methods.

[00024] In one aspect, therefore, the invention relates to a method of forming a semiconductor device. The method involves receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric layer having a first dielectric constant. The substrate is exposed to UV radiation in accordance with techniques described herein, such that the dielectric constant of the carbon-containing low-k dielectric layer is decreased to a second dielectric constant. While the invention is not limited to any particular theory of operation, it is believed that treatment repairs process induced low-k dielectric damage (e.g., dangling bonds or highly strained bonds, e.g., Si-O-Si or Si-CH_2-Si, caused by removal of organic (generally –CH_3) groups) caused by plasma etch, dry resist strip, wet cleaning and dry cleaning, for example, involved in a feature (e.g., trench) formation process, or other processing operation (e.g., post-metallization planarization. The repaired feature can then be coated with a material such as a barrier layer material, to protect against dielectric constant degradation. For example, where the feature is a trench for forming a line or via, a conductive material, particularly a metal diffusion barrier, followed by copper (or other suitable interconnect metal) may be applied in a metallization operation. In subsequent processing operations of some embodiments, another treatment in accordance with the present invention may be applied to the planarized top surface of a metallized semiconductor device to repair dielectric damage caused by planarization, generally by chemical mechanical polishing (CMP).

[00025] It should be understood that in such multi-step processes, a treatment in accordance with the present invention may be applied at one or more stages; for example, for pre-metallization repair of plasma etch-induced damage and/or post-planarization repair of planarization-induced dielectric damage. Also, UV treatments in accordance with the present invention may be combined with other UV or non-UV dielectric treatments.

Process variations

[00026] As noted above, the present invention provides a method of semiconductor device fabrication that involves exposure of a carbon containing low-k

dielectric to UV radiation having certain wavelength profiles and/or in combination with chemical silylating agents, or both, to reduce the dielectric constant of the subject carbon containing low-k dielectric. The subject carbon containing low-k dielectric is generally one that has been damaged by a prior processing or handling operation such that its dielectric constant has increased from its native value. A UV treatment in accordance with the present invention may have a variety of aspects with characteristics and/or constituents configured to decrease the dielectric constant of the treated carbon containing low-k dielectric.

[00027] According to a first aspect, in various embodiments the substrate is exposed to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm; or where greater than 50% of the UV radiation power is in a wavelength range of about 300 to 450 nm; or where greater than 50% of the UV radiation power is in a wavelength range of about 300 to 400 nm. A suitable spectral profile according to this aspect of the present invention may also be characterized as having less than 10% of the UV radiation power in a wavelength range below 300nm; or having less than 5% of the UV radiation power in a wavelength range below 300nm; or having less than 1% of the UV radiation power in a wavelength range below 300 nm. A suitable spectral profile according to this aspect of the present invention may also be characterized as having a proportion of UV radiation power in a wavelength range of 200 to 240nm to UV radiation power in a wavelength range of 300 to 400nm in the UV radiation to which the carbon containing low-k dielectric is exposed being no more than 10%.

[00028] A suitable source of UV radiation in accordance with some embodiments of this aspect of the present invention is a Fe-filled ("D") bulb. In some embodiments, a high pass filter is used with the D bulb to filter out the UV radiation having a wavelength below 300nm prior to exposure of the carbon containing low-k dielectric. The filter may be a 295nm high pass filter.

[00029] Another suitable source of UV radiation in accordance with some embodiments of this aspect of the present invention is a Ga-filled ("V") bulb. In some embodiments, a high pass filter is used with the V bulb to filter out the UV radiation having a wavelength below 300nm prior to exposure of the carbon containing low-k dielectric. The filter may be a 295nm high pass filter.

[00030] As described further below, changes in material properties correlated with performance advantages have been observed as a result of UV treatments in accordance with the present invention. An important benefit the treatment with radiation having the spectral profile described above is that k-recovery is obtained while dielectric shrinkage associated with other dielectric repair treatments is reduced or minimized. Shrinkage generates stress, particularly post-metallization, potentially leading to stress migration failures. Also, variability in pattern density and consequent variability in shrinkage can cause the dielectric to lose its planarity. While the invention is not limited to any particular theory of operation, this is believed to be achieved by reducing the sub-300nm component of the UV radiation spectral profile where ULK CDO films have significant absorption.

[00031] Treatments of a post-CMP carbon containing low-k dielectric have resulted in a dielectric constant that is at least 0.1 less than the pre-treatment dielectric constant and the dielectric shrinks by less than 2% as a result of the UV radiation exposure; or at least 0.1 less than the pre-treatment dielectric constant and the dielectric shrinks by less than 1% as a result of the UV radiation exposure; or at least 0.06 less than the pre-treatment dielectric constant and the dielectric shrinks by less than 0.5% as a result of the UV radiation exposure.

[00032] According to a second aspect of the invention, the UV treatment may comprise a UV radiation exposure in combination with chemical silylating agent exposure. Silylation involves the replacement of an acidic hydrogen on a compound with an alkylsilyl group. According to this aspect, the UV radiation may be as described above in relation to the first aspect of the invention so that UV radiation incident on the carbon containing low-k dielectric has a spectral profile constrained to achieve reduced shrinkage with k-recovery. Alternatively, the incident UV radiation in conjunction with this aspect of the invention may not be so constrained, and may be, for example, sourced from a convention H or H+ (mercury) bulb, a D bulb, a V bulb or any other suitable source. The UV source can be a single wavelength excimer lamp or broad spectrum source with arc or microwave excitations.

[00033] In general, the selection of UV wavelength(s), total exposure time and intensity, etc., depends on a number of factors, including the thickness of the dielectric film and the composition of the dielectric film. Suitable UV treatment parameters for the constrained spectrum UV radiation exposure of the first aspect of

the invention described above may be in the power intensity range of about 1 mw-20W/cm^2, for example about 500mW-5W/cm^2; at a wavelength of about 300-450nm, for example about 300-400nm. Suitable UV treatment parameters for an unconstrained spectrum UV radiation exposure suitable for use in conjunction with a chemical silylating agent exposure in accordance with the second aspect of the invention described above may be in the power intensity range of about 1 mw-20W/cm^2, for example about 500mW-5W/cm^2; at a wavelength of about 150-500nm, for example about 200-400nm. Exposures for up to about 1 minute, for example about 15, 30 or 45 seconds; at a wafer temperature of between room temperature up to about 450°C, preferably about 200-400°C, for example 400°C, are suitable in either instance. A typical UV exposure in accordance with this aspect of the invention has a power density of about 1-3 W/cm^2 at a wafer temperature of about 400°C for about 45 seconds. The process pressure can range from about 1mTorr to 760 Torr, preferably from about 5 Torr to 700 Torr.

[00034] The apparatus employed to implement the invention can have one or more UV sources. In some embodiments described herein, the apparatus will have a single UV source. In one particular implementation on a SOLA UV thermal processing system, available from Novellus Systems, Inc., UV intensity can be anywhere between 10-100%. Lower intensity generally requires longer exposure times. Temperature is set below target thermal budget (e.g., 350-400°C). Pressure can be as noted above. The UV wavelength sources can be as described above. Suitable apparatus are described in more detail below with reference to Figure 3.

[00035] Further in accordance with the second aspect of the invention, the chemical silylating agent is generally an alkyl silane, substituted or un-substituted. Suitable classes and examples of alkyl silane silylating agents in accordance with this aspect of the invention include:

Methyl silanes

[00036] These could contain either 3, 2 or 1 hydrolyzeable (functional) groups including chloro, methoxy, ethoxy, propoxy, methoxyalkoxy, dimethylamine, dielthyl amine other amines, silazanes (NH), or combinations thereof. Suitable bi-functional examples are dimethyldichlorosilane, dimethyldimethoxysilane,

dimethyldiethoxysilane, dimethylaminao trimethyl silane, bis(dimethylamino)dimethylsilane and bis(diethylamino)dimethylsilane.

Linear alkyl silanes

[00037] As above, but with one or more of the methyl group replaced by other linear alkyl groups (e.g., ethyl, propyl, butyl, etc). A suitable example is ethylmethyldichlorosilane.

Branched and cyclic alkyl silanes

[00038] As the methyl silanes, but with one or more of the methyl groups replaced by branched or cyclic alkyls (e.g., isopropyl, isobutyl, etc).

Dialkyl silanes

[00039] As the methyl silanes, but with all methyl groups replaced by pairs of larger alkyl groups (e.g., diethyldichlorosilane, diethyldiethoxysilane).

[00040] Suitable silylating agent partial pressures are between about 1 and 700 Torr, for example 10-300 Torr. A typical silylating agent flow rate is about 3 to 15 ml/min. Exposure times of about 1 to 10 minutes, for example about 5 minutes, are generally suitable. At very lower partial pressures, longer exposure times will generally be required.

[00041] In still other embodiments, a non-silicon containing chemical reagent that can donate methyl groups or other carbons, or could be UV active such that they can be activated by UV to enable a dielectric repair reaction to proceed may be used in place of the chemical silylating agent. Suitable examples include acetone, dimethyl carbonate.

[00042] The invention may be implemented in a single process module having one or more stations, or across multiple modules each having one or more stations. Often, but not always, the invention is implemented in one or more multi-station modules where the substrate (work piece) can be moved from station to station without necessarily breaking vacuum. The process parameters for the UV treatment, including intensity, wavelength, temperature, pressure, time and reagent flow, including chemical silylating agent, may be independently controlled and varied, and any or all of the process conditions may be varied from station to station. In particular, there may be independent control of temperature, silylating agent and UV

irradiation. For example, the wafer may be brought to a temperature T for a time t, exposed to a silylating agent for a time t1, exposed to UV radiation and a silylating agent for time t2, exposed to UV radiation only for a time t3, and then moved to another station in a multi-station processing apparatus where any of the conditions including temperature, UV radiation intensity, pressure, wavelength, flow, and time may be independently changed within the described parameters.

[00043] A carbon containing low-k dielectric may be subjected to a UV treatment in accordance with the present invention in a variety of different ways according to various embodiments of the invention. The UV treatment may be with UV radiation exposure of a constrained spectral profile, as described herein, alone; and/or with UV radiation of a constrained spectral profile may be combined in various ways with a chemical silylating agent exposure; and/or with UV radiation of an unconstrained spectral profile, as described herein, in the presence of the silylating agent.

[00044] In some specific embodiments, the UV treatment may include the following operations: UV radiation exposure (constrained or unconstrained) in an inert (e.g., He, Ar, etc.) atmosphere; followed by exposure to a chemical silylating agent; followed by UV radiation exposure (constrained or unconstrained) in an inert (e.g., He, Ar, etc.) atmosphere again. The treatment may or may not have an air break between operations, or may have just one air break, either prior to or after the silylating agent exposure. The operations of the treatment could be performed at the same or different temperatures. For example, UV radiation exposure at about 400°C; and silylating agent exposure at the same or a lower temperature in the range of about 50 to 400°C, for example about 90°C in a treatment where UV radiation operations precede and follow the silylating agent exposure.

[00045] Alternatively, the initial UV radiation exposure operation may be replaced with a thermal anneal operation (e.g., 400°C for about 1 to 30 minutes, for example 5 minutes in an inert atmosphere), or not performed at all. Again, the treatment may or may not have an air break between operations. And again, the operations of the treatment could be performed at the same or different temperatures. For example, anneal and/or UV radiation exposure at about 400°C; and silylating agent exposure at the same or a lower temperature in the range of about 50 to 400°C,

for example about 150˚C in a treatment where an anneal operation precedes the silylating agent exposure, which is followed by a UV radiation exposure operation.

[00046] In other embodiments, the subject carbon containing low-k dielectric may be exposed to the UV radiation during exposure to the chemical silylating agent. For example, the treatment may be a single operation including exposure to UV radiation in the presence of the silylating agent. Or, exposure to UV radiation in the presence of the silylating agent can be followed by a further exposure to UV radiation without the silylating agent, for example in an inert gas (e.g., He); or the reverse operations (i.e., exposure to UV radiation without the silylating agent, for example in an inert gas (e.g., He) followed by a further exposure to UV radiation in the presence of the silylating agent.

[00047] Treatments of pre-metallization plasma damaged carbon containing low-k dielectrics with UV treatments including a chemical silylation agent exposure in accordance with the present invention can achieve k reductions of as much as 0.5 or more and to a k value of as low as 2.4 or lower.

[00048] Following the treatment, a barrier layer may be deposited on the low-k dielectric, prior to subsequent processing of the semiconductor device.

Semiconductor Processing Contexts

[00049] Figure 1A is a process flow chart depicting operations that may be performed in various methods in accordance with embodiments of the present invention. The invention is advantageously applied in a damascene processing context, although its application is not so limited. It should be understood that, in some aspects, the present invention requires only a UV treatment as described herein of an applicable semiconductor device substrate having a carbon containing low-k dielectric (e.g., ULK CDO), such as described in operations 104 and/or 110 of the embodiment illustrated in Figure 1A. Other aspects of the invention may include additional processing operations, such as damascene processing operations described herein. But the invention is not limited to the performance of these additional processing operations in all its aspects. A generalized version of a dual damascene technique is described below with reference to Figures 2A through 2D, which depict a partially formed semiconductor device during various stages of this process. The

invention may also be used in conjunction with other semiconductor processing techniques.

[00050] Referring now to Figure 1A, in operations that are not necessarily part of the present invention, but place an embodiment of the invention in context in an advantageous application, a carbon containing low-k dielectric is deposited on a substrate at 100. Patterns of conductive features are formed in the dielectric layer, generally by plasma etching of trenches, at 102. Plasma etching generally results in damage to the pattern edges, generally trench sidewalls and bottoms. Other process operations, such as dry resist strip, wet cleaning and dry cleaning, can also cause or contribute to low-k dielectric damage. The conductive features are typically, though not necessarily, metal lines and vias. In one example, they are the interconnects of a metallization layer that is subsequently formed from copper. As is known to those of skill in the art, various techniques may be employed to form such features.

[00051] The formed features (e.g., etched trenches) are then exposed to an ultraviolet (UV) treatment in accordance with the present invention at 104. Process variations for specific embodiments of a UV treatment in accordance with the present invention are described above and may include a constrained UV spectral profile and/or a chemical silylating agent. While the invention is not limited to any particular theory of operation, it is believed that the UV exposure of the damaged dielectric surface cross-links SiOH groups, to bring about silanol reduction, resulting in the formation of Si-O-Si bonds.

[00052] Following this UV treatment, a barrier layer may be deposited on the low-k dielectric layer prior to subsequent processing of the semiconductor device. For example, in operations that are not necessarily part of the present invention but are provided for context for one embodiment as noted above, the trenches may then be filled at 106 with a conductive material, typically and conductive barrier layer and then copper (Cu), although other metals may also be used. When filling the features, excess material will have to be removed from the top (exposed surface) of the dielectric. The excess material may be removed by a planarization process to form an exposed pattern of conductive features in the dielectric at 108. As discussed above, one widely-used planarization process is chemical mechanical polishing (CMP), however slurry from CMP can chemically remove carbon groups from a carbon containing low-k dielectric.

[00053] According to a further aspect of the invention, to repair the CMP-induced dielectric damage, the planarized surface can be exposed to a further UV treatment in accordance with the present invention, at 110. The UV treatment may be conducted under the same conditions as described above with reference to the post-trench etch treatment, or other conditions as described herein.

[00054] Following the damascene processing repair in accordance with this embodiment of the present invention, a diffusion barrier film, such as a copper diffusion barrier film, may be deposited on the planarized surface of the partially-formed semiconductor device. This layer may serve other purposes aside from that of a diffusion barrier. For example, the diffusion barrier film may also act as an etch stop layer.

[00055] According to various implementations of the present invention, a UV treatment as described herein may be conducted at any stage of a semiconductor processing operation where a carbon containing low-k dielectric has been damaged by a prior processing operation, and/or could otherwise benefit from a treatment to recover or enhance its low-k property. For example, in a semiconductor processing operation that involves damascene processing, a treatment may be applied at either or both the pre-metallization (e.g., trench fill) and post-planarization stages of the damascene processing. Where a plurality of UV radiation treatments in accordance with the present invention are applied, the treatments may be the same or different, within the parameters described herein. Alternatively, a UV radiation treatment in accordance with the present invention may be combined with other processing techniques at one stage or the other of a multi-step process. For example, a UV exposure with a reducing agent exposure, as described in co-pending Application No. 12/646,830, filed December 23, 2009, incorporated by reference herein, may be used at one stage or the other, particularly post-planarization in a damascene processing, while a UV radiation exposure in accordance with the present invention is used in another stage, for example for trench repair pre-metallization.

[00056] Referring now to Figures 2A-2D, a typical dual damascene process incorporating processing-induced damage repair processes of the present invention is illustrated. As noted above, it should be understood that an embodiment of the invention in context in an advantageous application is depicted. In at least some aspects, the present invention requires only a UV treatment of the semiconductor

device substrate, as described above. Other aspects of the invention may include additional processing operations, such as damascene processing operations described herein, including lithographic operations. But the invention is not limited to the performance of these additional processing operations in all its aspects.

[00057] Referring to Figure 2A, first 203 and second 205 layers of dielectric are deposited in succession, possibly separated by deposition of an etch stop layer, such as a silicon nitride layer. As is well known in the art, according to alternative damascene processing techniques a single thicker dielectric layer can be used instead of discrete first and second layers.

[00058] After deposition of the second dielectric layer 205, a via mask 211 is formed having openings where vias will be subsequently etched. Next, the vias are partially etched down through the level of the second dielectric 205. Then via mask 211 is stripped off and replaced with a line mask 213 as depicted in Figure 2B. A second etch operation is performed to remove sufficient amounts of dielectric to define line paths 215 in second dielectric layer 205. The etch operation also extends via holes 217 through first dielectric layer 203, down to contact an etch stop layer 210 above a metal layer 211 on the underlying substrate 209.

[00059] It should be noted that the foregoing description is just an example of one via-first dual damascene process with which the present invention may be implemented. In other embodiments, a via-first process may involve complete etching of the vias prior to etching of the line trenches. Or, a trench-first process, in which the etching of the line trenches precedes the via etching, may be used. These various damascene processing techniques, and other variations thereon, are well known in the art and represent alternative implementation contexts for embodiments of the present invention. The invention is also applicable is single damascene processing, more conventional metal deposition and etch, and essentially any semiconductor processing context where carbon-containing low-k dielectrics are used.

[00060] Further in this regard, the term "trench" in the context of damascene processing is commonly understood to describe a feature formed in dielectric and subsequently filled to form a conductive line in a dielectric layer. In a more general semiconductor processing context, the term is also understood to describe a feature formed in dielectric and subsequently filled to form an element of a semiconductor

device (e.g., via, line, STI, etc.), and may include a damascene trench or a combined damascene structure. Unless it is otherwise clear from the context, when used herein, the term should be understood to have its broader meaning.

[00061] After trench etching, the photoresist is removed in another plasma process, followed by a wet or dry clean and then damage on the low-k dielectric surface is repaired by a UV treatment, as discussed above.

[00062] Thereafter a thin layer of conductive barrier layer material 219 is formed on the exposed surfaces (including sidewalls) of dielectric layers 203 and 205. Conductive barrier layer material 219 may be formed, for example, of tantalum or tantalum nitride. A CVD or PVD operation is typically employed to deposit conductive barrier layer material 219. Prior to the deposition of the barrier material, a plasma process is typically used to clean the bottoms of the trenches to remove oxidation and contaminants from the exposed copper surface on the underlying layer. As is known to those skilled in the art, this barrier "preclean" plasma process can be simply an inert plasma or a reactive plasma of a gas such as hydrogen. The preclean plasma process can also damage a low-k dielectric film. A UV treatment as described above to repair the damaged low-k film may employed prior to the PVD operation for Ta or TaN.

[00063] On top of the barrier layer, a conductive metal (typically copper) is deposited in the trench and line paths 217 and 215. Conventionally this deposition is performed in two steps: an initial deposition of a conductive seed layer followed by bulk deposition of copper by electroplating. The seed layer may be deposited by physical vapor deposition, chemical vapor deposition, electroless plating, etc. Note that the bulk deposition of copper not only fills line paths 215 but, to ensure complete filling, also covers all the exposed regions on top of second dielectric layer 205.

[00064] Thus, it becomes necessary to planarize the structure and remove the excess copper from the device. Planarization removes material down to the level of the top of dielectric layer 205. This results in an exposed pattern of conductive lines 221 in dielectric layer 205 and vias in dielectric layer 203. (See the cross-sectional view of Figure 2C and the simplified top view of Figure 2D.)

[00065] Planarization may be accomplished by various techniques. Typically, the process involves some amount of CMP. It may also involve a combination of

electropolishing, to remove most of the excess bulk copper, followed by CMP to remove the remaining copper down to the level of the top surface of dielectric layer 205. As discussed above, slurry from CMP can chemically remove carbon groups, and the in-situ plasma based processes typically used to remove the oxides from the conductive lines after the planarization process can also remove carbon groups leaving silicon dangling bonds on the surface of low-k dielectric films. Each of these types of damage also results in significant water absorption, resulting in an increase in dielectric k.

[00066] As described previously, another aspect of the invention relates to post-planarization (e.g., CMP) damage repair arising in damascene processing. According to this aspect, following planarization by CMP, Si-OH (silanol) bonds (formed by removal of organic (generally $-CH_3$) groups by CMP slurry and processing and reaction of water in the slurry with resulting dangling Si- bonds), or other carbon-containing low-k dielectric film damage (e.g., highly strained bonds), are repaired by exposing the surface to a UV treatment, as described above.

Apparatus

[00067] The present invention can be implemented in many different types of apparatus. In some embodiments, the apparatus will include one or more chambers (sometimes referred to as process modules) that house one or more wafers and are suitable for wafer processing. At least one chamber will include a UV source. A single chamber may have one or more stations and may be employed for one, some or all operations of the invention. Each chamber may house one or more wafers (substrates) for processing. The one or more chambers maintain the wafer in a defined position or positions (with or without motion within that position, *e.g.,* rotation, vibration, or other agitation) during procedures of the invention. For certain operations in which the wafer temperature is to be controlled, the apparatus may include a controlled temperature wafer support, which may be heated, cooled, or both. The wafer support may also be controllable to provide the defined wafer positions within a process module. The wafer support may rotate, vibrate, or otherwise agitate the wafer relative to the UV source.

[00068] Figure 3 depicts the arrangement of a UV light source suitable for implementation of the present invention. In this embodiment, a cold mirror reflector

seeks to diminish the incidence of IR radiation on the wafer, while permitting UV radiation to be available for processing. For clarity, this figure depicts only one of the possible multiple processing stations available in an apparatus of this invention. Also, this figure omits depiction of the wafer for purposes of clarity, and shows a flood-type reflector. It will be apparent to those skilled in this art that the principles depicted in Figure 3 may also be applied to a focused reflector.

[00069] Referring to Figure 3, pedestal 303 is embedded into one station of a processing chamber 301. Window 305 is located appropriately above pedestal 303 to permit radiation of the wafer (not shown here) with UV output of the desired wavelengths from UV lamps 309 and 319. Suitable lamps for the UV light source may include, but are not limited to, mercury vapor, D or V bulb lamps, with or without filters, as described above. In this embodiment, both lamps 309 and 319 are equipped with reflectors 307 and 317 which render their output into flood illumination. Reflectors 307 and 317 may themselves be made from "cold mirror" materials, i.e., they may also be designed to transmit IR and reflect UV radiation.

[00070] Radiation emanating directly from lamps 309 and 319 as well as that reflected from reflectors 307 and 317 is further incident upon a set of reflectors 311. These reflectors are also cold mirrors designed to reflect only those UV wavelengths that are desired for the purposes of curing the film on the wafer. All other radiation including visible and most particularly the IR is transmitted by this set of cold mirrors. Therefore the UV wavelengths are preferentially transmitted to the film. It will be apparent to those skilled in this art that the specific angle, distance, and orientation of the cold mirror reflectors 311 with respect to the lamps 309 and 319 may be optimized to maximize the UV intensity incident on the wafer and to optimize the uniformity of its illumination.

[00071] The chamber 301 is capable of holding a vacuum and/or containing gases at pressures above atmospheric pressure. For simplicity, only one station of one chamber 301 is shown. It is noted that in some embodiments, chamber 301 is one chamber in a multi-chambered apparatus, although chamber 301 could alternatively be part of a stand-alone single chambered apparatus. In either case, the chamber(s) may have one or more than one station. In some embodiments of the present invention, the UV process modules have one station. Suitable apparatus for implementation of the invention may include configurations as described herein of

INOVA, Sequel, Vector and SOLA systems from Novellus Systems, Inc. of San Jose, CA, and Endura, Centura, Producer and Nanocure systems from Applied Materials of Santa Clara, CA. In a particular example, the invention may be implemented on a Vector Extreme tool from Novellus Systems, Inc. of San Jose, CA.

[00072] Note that the UV light source configuration of Figure 3 is only an example of a suitable configuration. In general, it is preferable that the lamps are arranged to provide uniform UV radiation to the wafer. For example, other suitable lamp arrangements can include arrays of circular lamps concentrically or otherwise arranged, or lamps of smaller length arranged at 90 degree and 180 degree angles with respect to each other may be used. The light source(s) can be fixed or movable so as to provide light in appropriate locations on the wafer. Alternatively, an optical system, including for example a series of movable lenses, filters, and/or mirrors, can be controlled to direct light from different sources to the substrate at different times.

[00073] The UV light intensity can be directly controlled by the type of light source and by the power applied to the light source or array of light sources. Factors influencing the intensity of applied power include, for example, the number or light sources (e.g., in an array of light sources) and the light source types (e.g., lamp type or laser type). Other methods of controlling the UV light intensity on the wafer sample include using filters that can block portions of light from reaching the wafer sample. As with the direction of light, the intensity of light at the wafer can be modulated using various optical components such as mirrors, lenses, diffusers and filters. The spectral distribution of individual sources can be controlled by the choice of sources (e.g., mercury vapor lamp (H or H+ bulb), xenon lamp, deuterium lamp, iron filled ("D") bulb, gallium filled ("V") bulb, excimer laser etc.) as well as the use of filters that tailor the spectral distribution.

[00074] The apparatus also includes a source of a chemical silylating agent 320, such as an alkyl silane as described above.

[00075] In certain embodiments, a system controller 325 is employed to control process conditions during the UV treatment processes in accordance with the present invention. The controller will typically include one or more memory devices and one or more processors. The processor may include a CPU or computer, analog and/or digital input/output connections, stepper motor controller boards, etc.

[00076] In certain embodiments, the controller controls all of the activities of the apparatus. The system controller executes system control software including sets of instructions for controlling the timing, supply of reagents (e.g., silylating agent), chamber pressure, chamber temperature, wafer temperature, UV wavelength, intensity and exposure time, and other parameters of a particular process. Other computer programs stored on memory devices associated with the controller may be employed in some embodiments.

[00077] Typically there will be a user interface associated with controller 325. The user interface may include a display screen, graphical software displays of the apparatus and/or process conditions, and user input devices such as pointing devices, keyboards, touch screens, microphones, etc.

[00078] The computer program code for controlling the processes can be written in any conventional computer readable programming language: for example, assembly language, C, C++, Pascal, Fortran or others. Compiled object code or script is executed by the processor to perform the tasks identified in the program.

[00079] Signals for monitoring the process may be provided by analog and/or digital input connections of the system controller. The signals for controlling the process are output on the analog and digital output connections of the deposition apparatus.

[00080] The system software may be designed or configured in many different ways. For example, various chamber component subroutines or control objects may be written to control operation of the chamber components necessary to carry out the inventive processes. Examples of programs or sections of programs for this purpose include substrate positioning code, silylating agent control code, pressure control code, heater control code, and UV radiation control code. In one embodiment, the controller includes instructions for performing processes of the invention according to methods described above.

[00081] It should be understood that the apparatus depicted in Figure 3 is only an example of a suitable UV process module and that other designs may be used. The semiconductor device should be transferred from the UV module to the barrier layer deposition module without an air break. This may be accomplished on multiple of single tools.

Examples

[00082] The following provides examples of specific implementations of the present invention and performance data in order to give a better understanding of the operation and benefits of the invention. The invention is, however, in no way limited to these specific implementations.

Post-CMP k recovery using UV treatment

[00083] As part of the solution to lower RC delay, materials with significantly lower k ($k<2.60$) are being used as ILD materials. The typical way to reduce the k is through incorporation of porogen in these materials, which is eventually driven out and the film is cross-linked to increase its hardness (typically using UV).

[00084] After electroplating of copper, it is planarized using CMP. These porous ULK materials are susceptible to CMP damage. Some amount of C removal occurs from the surface of these films, with consequent moisture intake resulting in an increase in its dielectric constant.

[00085] The next step in the process is deposition of a dielectric barrier / etch stop layer (typically SiC or SiN using PECVD). Typically, a long soak step (10 – 30s) in an inert atmosphere at 400°C is used to remove the moisture from the film prior to the DB/ESL deposition. At this point, the film is capped off, so no further moisture in-take is possible.

[00086] In experiments performed (on a pULK k2.3x film) to evaluate processes in accordance with the present invention, the k loss brought about by CMP process induced damage was about 0.2. Using just a thermal anneal at 400°C the k recovery was about 0.05-0.06. Time was immaterial; no difference being observed between 1 and 30min.

[00087] When exposed to a broadband UV source, such as that from a H+ bulb having emissions all the way down to 200nm, in an inert atmosphere, the k recovery was about 0.11-0.12, about twice that of a standard anneal. Exposure times of 45s and 60s were evaluated as part of these tests. No difference was observed for longer times.

[00088] The same degree of k recovery as H+ bulbs is seen even with D or V bulbs. These bulbs have different dopants in them such that their emission spectra is

altered. Emission spectra showing the radiated power profile for H+, D and V bulbs are shown in Fig. 4 (a), (b) and (c), respectively, for reference. The main impact of these dopants is that there is very little to no emission in the shorter wavelengths (200-240nm). This is the region where a ULK CDO film has significant absorption. Therefore, not having these wavelengths prevents the ULK films from further curing / shrinkage, while moisture removal still occurs. The 300-40nm region dominates the D bulb emission spectral profile, while V bulbs have their peak emission above 380nm.

[00089] The main drawback of using H+ bulbs for a UV treatment for k recovery is the resulting shrinkage of the treated carbon containing low-k dielectric. As can be seen from Figure 5, UV exposure using an H+ bulb UV source causes the film to further shrink by 2.5%. In comparison, a thermal anneal results in only about 0.2% shrinkage. Since metal lines are already embedded into the ULK, any shrinkage generates stress, potentially leading to stress migration failures. Also, variability in pattern density and consequent variability in shrinkage will cause the ULK to lose its planarity. As Figure 5 indicates, both D and V bulbs result in about the same k recovery, while shrinkage is reduced more than half (to about 1%). Adding a 295nm high pass filter, with D bulbs, results in the same k recovery of about 0.12, but shrinkage now being only 0.5%. This suggests that wavelengths greater than 300nm are sufficient for moisture removal. But the same 295nm filter with a V bulb, while bringing about even lower shrinkage, does not bring about the same level of k recovery. This suggests that significant intensity between 300 and 400nm is helpful for k recovery.

[00090] These findings suggest that a exposure to UV radiation with a constrained spectral profile above 300nm can bring about more k recovery than an anneal, while also avoiding significant shrinkage. This can be achieved with a suitable broad-band source (e.g., D or V bulbs), with or without filters. It can also potentially be done with single wavelength excimer sources between 300 and 400nm or even UV LEDs (395nm or 365nm).

Pre-metallization k recovery using UV treatment

[00091] Treatments of pre-metallization plasma damaged carbon containing low-k dielectrics with UV treatments including a chemical silylation agent exposure

in accordance with the present invention have been found to achieve k reductions of as much as 0.5 or more and to a k value of as low as 2.4 or lower. Fig. 6 depicts data from experiments in which a ULK CDO dielectric was damaged with an oxidizing plasma and then subjected to a UV treatment in accordance with the present invention. The UV treatment involved exposure to a first methyl silane silylating agent (SA1) followed by UV radiation exposure, and separately exposure to a second methyl silane silylating agent (SA2) followed by UV radiation exposure. The UV treatment in each case resulted in a dramatic reduction in the dielectric constant (k recovery) of the treated dielectric from greater than 3 to about 2.6 to 2.7. Similarly beneficial results were obtained with UV treatments involving UV radiation exposures before and after exposure to a silylating agent.

Alternative Embodiments

Patterning Method/Apparatus

[00092] The apparatus/process described hereinabove may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of semiconductor devices, displays, LEDs, photovoltaic panels and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically comprises some or all of the following steps, each step enabled with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

System Controller

[00093] Another aspect of the invention is an apparatus configured to accomplish the methods described herein. A suitable apparatus includes hardware for accomplishing the process operations and a system controller having instructions for controlling process operations in accordance with the present invention, such as

described with reference to Figure 3, above. The system controller will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with the present invention. Machine-readable media containing instructions for controlling process operations in accordance with the present invention may be coupled to the system controller.

Conclusion

[00094] Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should be noted that there are many alternative ways of implementing both the process and compositions of the present invention. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein.

CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, comprising:

receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric having a first dielectric constant;

exposing the carbon containing low-k dielectric to a UV treatment, the treatment comprising at least one of:

(a) exposure to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm; and

(b) exposure to UV radiation and a chemical silylating agent;

such that the dielectric constant of the carbon-containing low-k dielectric is decreased to a second dielectric constant.

2. The method of claim 1, wherein greater than 50% of the (a) and/or (b) UV radiation power is in a wavelength range of about 300 to 450 nm.

3. The method of claim 1, wherein greater than 50% of the (a) and/or (b) UV radiation power is in a wavelength range of about 300 to 400 nm.

4. The method of claim 1, wherein less than 10% of the (a) and/or (b) UV radiation power is in a wavelength range below 300nm.

5. The method of claim 1, wherein less than 5% of the (a) and/or (b) UV radiation power is in a wavelength range below 300nm.

6. The method of claim 1, wherein less than 1% of the (a) and/or (b) UV radiation power is in a wavelength range below 300 nm.

7. The method of claim 1, wherein the proportion of (a) and/or (b) UV radiation power in a wavelength range of 200 to 240nm to UV radiation power in a wavelength

range of 300 to 400nm in the UV radiation to which the carbon containing low-k dielectric is exposed is no more than 10%.

8. The method of claim 1, wherein a Fe-filled ("D") bulb is used a source for the (a) and/or (b) UV radiation.

9. The method of claim 7, wherein a high pass filter is used with the D bulb to filter out the UV radiation having a wavelength below 300nm prior to exposure of the carbon containing low-k dielectric.

10. The method of claim 9, wherein the filter is a 295nm high pass filter.

11. The method of claim 1, wherein a Ga-filled ("V") bulb is used a source for the (a) and/or (b) UV radiation.

12. The method of claim 11, wherein a high pass filter is used with the V bulb to filter out the UV radiation having a wavelength below 300nm prior to exposure of the carbon containing low-k dielectric.

13. The method of claim 12, wherein the filter is a 295nm high pass filter.

14. The method of claim 1, wherein the second dielectric constant is at least 0.1 less than the first dielectric constant and the dielectric shrinks by less than 2% as a result of the UV treatment.

15. The method of claim 1, wherein the second dielectric constant is at least 0.1 less than the first dielectric constant and the dielectric shrinks by less than 1% as a result of the UV treatment.

16. The method of claim 1, wherein the second dielectric constant is at least 0.06 less than the first dielectric constant and the dielectric shrinks by less than 0.5% as a result of the UV treatment.

17. The method of claim 1, wherein the dielectric is selected from the group consisting of carbon doped oxides formed from octamethyl cyclotetrasiloxane

(OMCTS), tetramethylcyclotetrasiloxane (TMCTS), dimethyldimethoxysilane (DMDMOS), and diethoxymethylsilane (DEMS).

18. The method of claim 1, wherein the second dielectric constant is less than 2.7

19. The method of claim 1, wherein the UV exposure is conducted at a temperature of about 400°C.

20. The method of claim 1, wherein the silylating agent comprises an alkyl silane.

21. The method of claim 20, wherein the alkyl silane is substituted with an amino or halo group.

22. The method of claim 20, wherein the alkyl silane is selected from the group consisting of methyl silanes, linear alkyl silanes, branched and cyclic alkyl silanes, dialkyl silanes and combinations thereof.

23. The method of claim 20, wherein the alkyl silane is selected from the group consisting of dimethyldichlorosilane, dimethyldimethoxysilane, dimethyldiethoxysilane, bis(dimethylamino)dimethylsilane, dimethylaminao trimethyl silane, bis(diethylamino)dimethylsilane, ethylmethyldichlorosilane and diethyldichlorosilane, diethyldiethoxysilane.

24. The method of claim 23, wherein the silylating agent is bis(dimethylamino)dimethylsilane.

25. The method of claim 23, wherein the silylating agent is dimethyldichlorosilane.

26. The method of claim 1, wherein the treatment comprises exposure to the chemical silylating agent prior to the UV radiation exposure.

27. The method of claim 26, wherein a second UV radiation exposure precedes the exposing the carbon containing low-k dielectric to the chemical silylating agent.

28. The method of claim 27, wherein there is no air-break between exposures.

29. The method of claim 27, wherein there is an air-break between one or more exposures.

30. The method of claim 26, wherein a thermal anneal exposure precedes the exposing the carbon containing low-k dielectric to the chemical silylating agent.

31. The method of claim 1, wherein the carbon containing low-k dielectric is comprised in an etched pre-metallization substrate.

32. The method of claim 1, wherein the carbon containing low-k dielectric is comprised in a planarized surface having a metal feature formed by damascene processing.

33. The method of claim 1, further comprising depositing a barrier layer on the treated low-k dielectric layer.

34. The method of claim 1, wherein the second dielectric constant is at least 0.5 lower than the first dielectric constant.

35. The method of claim 1, wherein a non-silicon containing chemical reagent that can donate methyl groups or other carbons is used in place of the chemical silylating agent.

36. The method of claim 1 further comprising the steps of:

applying photoresist to the substrate;

exposing the photoresist to light;

patterning the resist and transferring the pattern to the substrate;

and selectively removing the photoresist from the substrate.

37. An apparatus for repairing process-induced damage on a semiconductor device substrate, comprising:

(i) a process chamber having a UV radiation source configured to provide at least one of:

(a) exposure to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm; and

(b) exposure to UV radiation and a chemical silylating agent; and

(ii) a stepper.

38. An apparatus for repairing process-induced damage on a semiconductor device substrate, comprising:

(i) a processing chamber having a UV radiation source configured to provide at least one of:

(a) exposure to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm; and

(b) exposure UV radiation and a chemical silylating agent; and

(ii) a controller comprising program instructions for conducting a process comprising receiving in the processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric having a first dielectric constant and performing at least one of (a) and (b).

39. A non-transitory computer machine-readable medium comprising program instructions for control of an apparatus for repairing process-induced damage on a semiconductor device substrate, the program instructions comprising:

code for receiving in a processing chamber a semiconductor device substrate comprising a carbon-containing low-k dielectric having a first dielectric constant; and

code for exposing the carbon containing low-k dielectric to a UV treatment, the treatment comprising at least one of:

(a) exposure to UV radiation having a spectral profile characterized by greater than 50% of the UV radiation power having a wavelength of greater than 300 nm, and

(b) exposure UV radiation and a chemical silylating agent;

such that the dielectric constant of the carbon-containing low-k dielectric is decreased to a second dielectric constant.

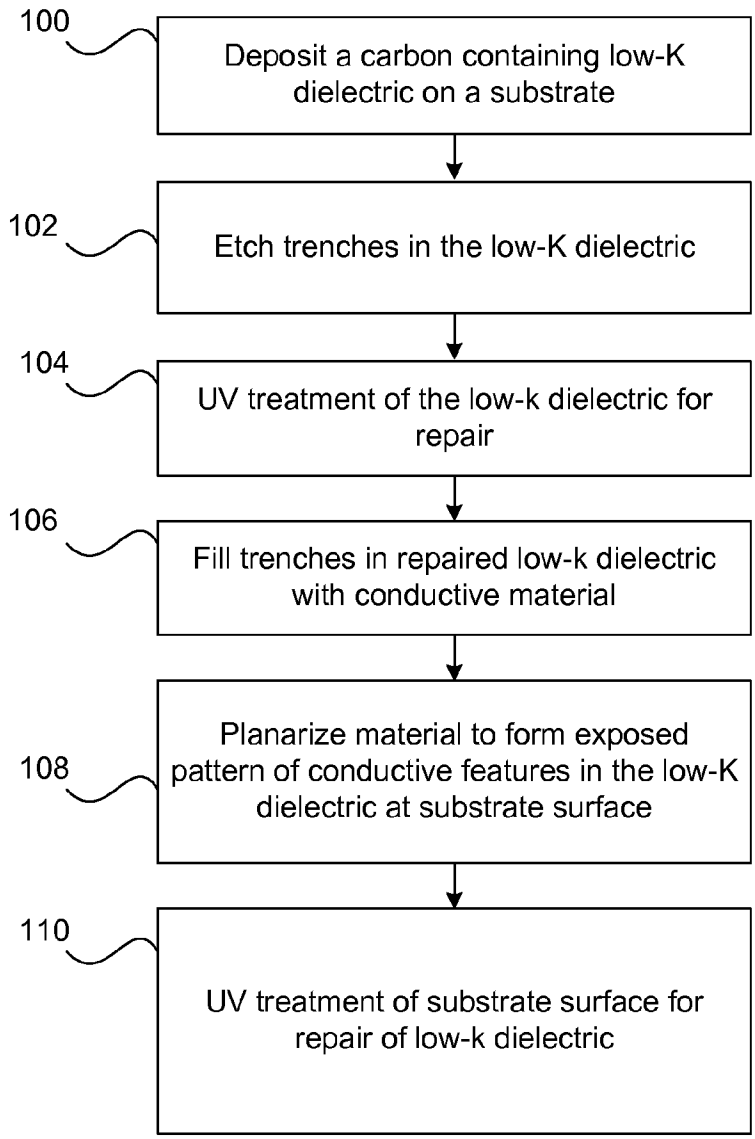
100
Deposit a carbon containing low-K dielectric on a substrate
102
Etch trenches in the low-K dielectric
104
UV treatment of the low-k dielectric for repair
106
Fill trenches in repaired low-k dielectric with conductive material
108
Planarize material to form exposed pattern of conductive features in the low-K dielectric at substrate surface
110
UV treatment of substrate surface for repair of low-k dielectric

Figure 1

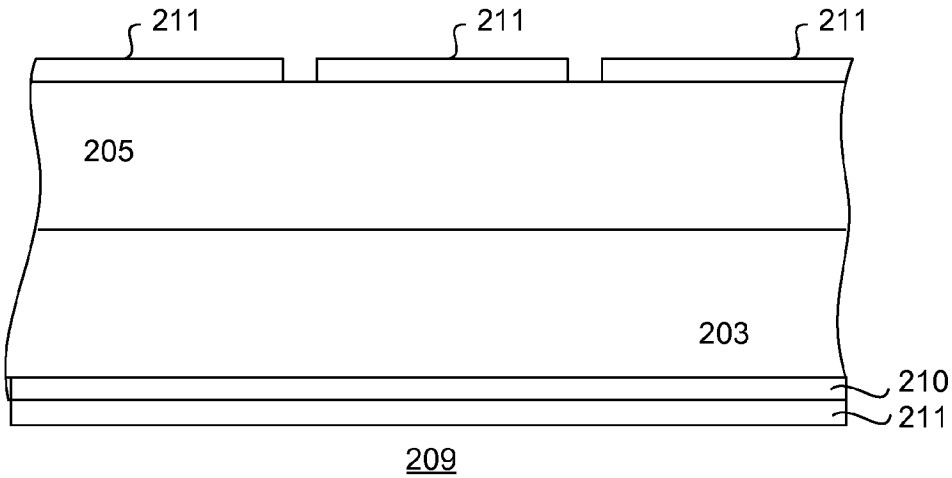

Figure 2A

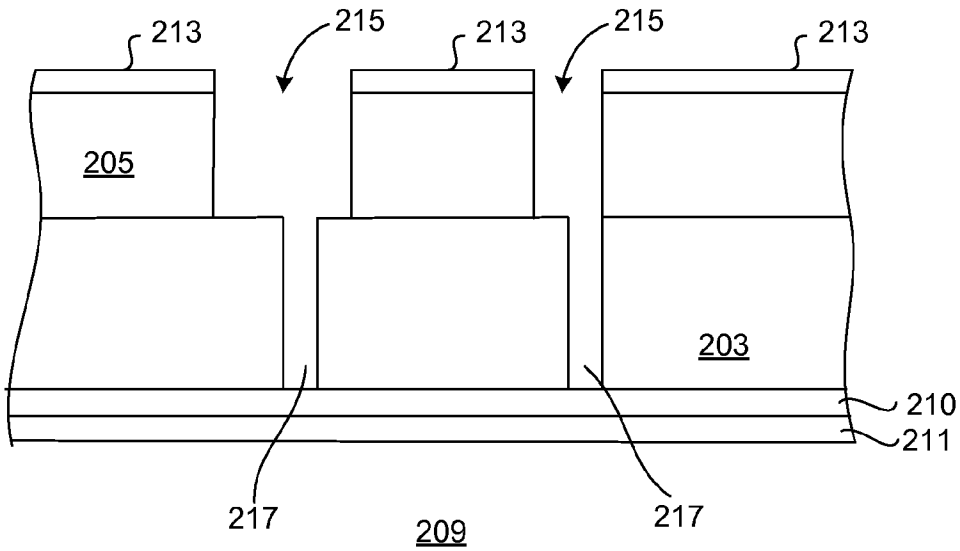

Figure 2B

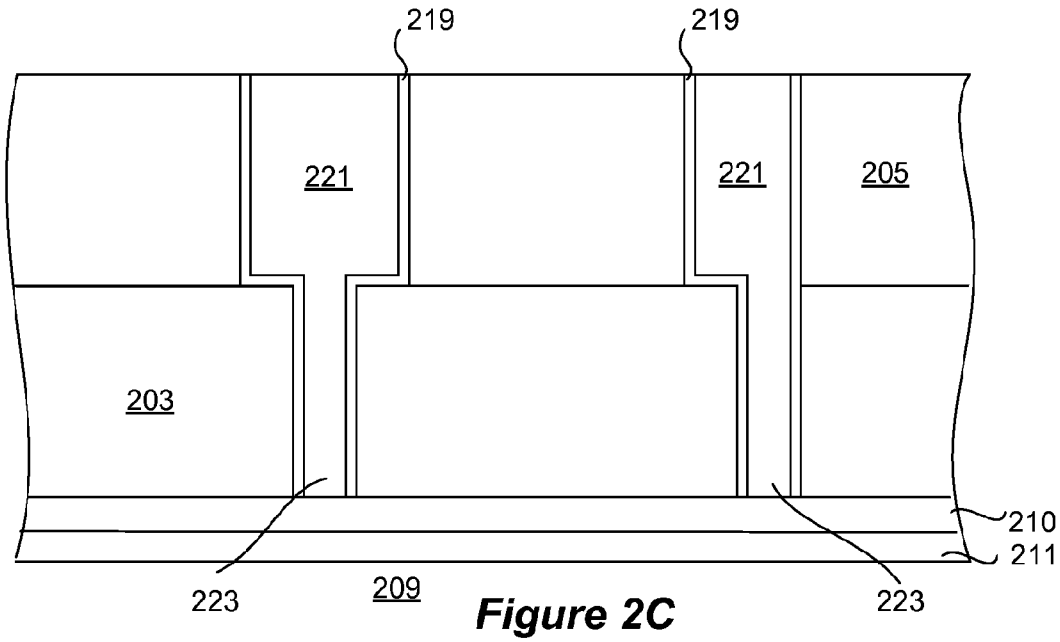

Figure 2C

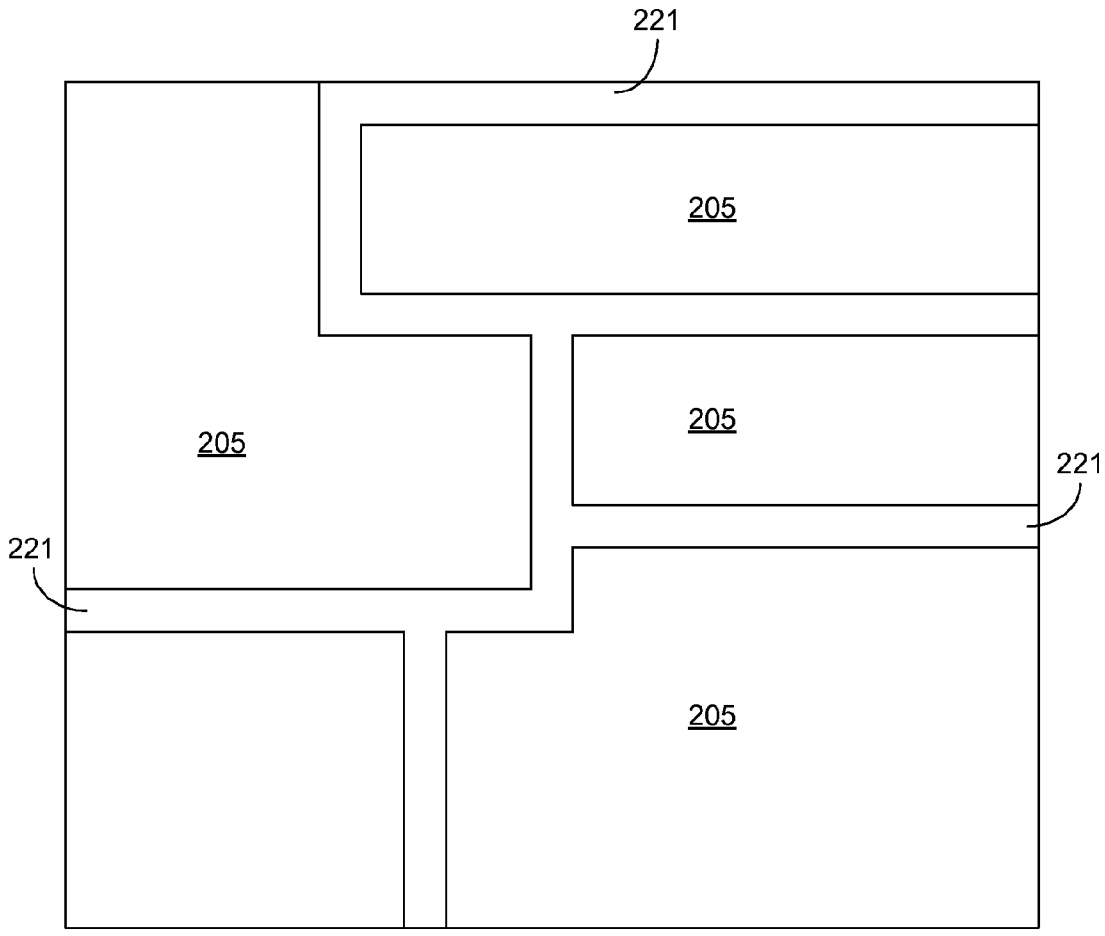

Figure 2D

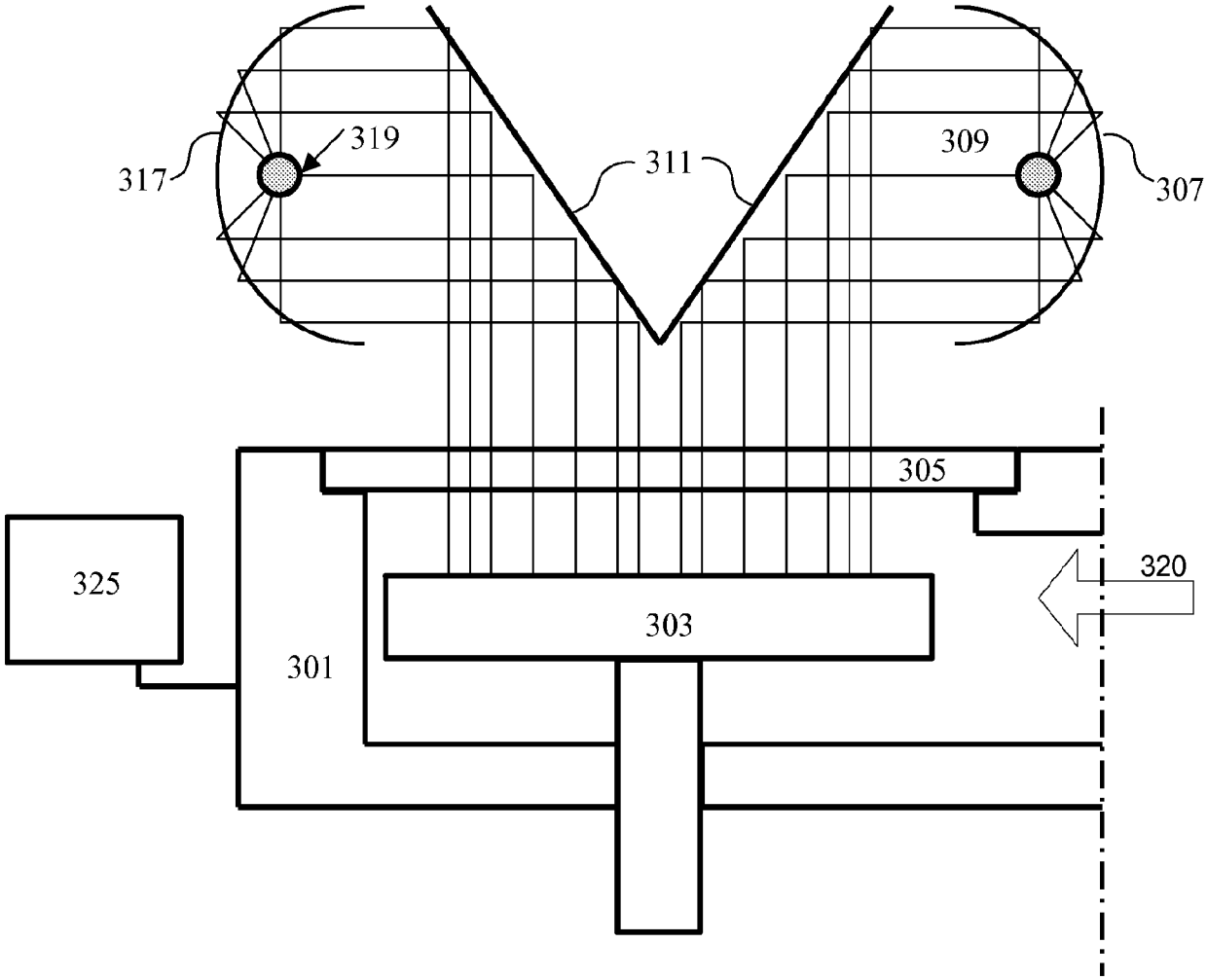

FIG. 3

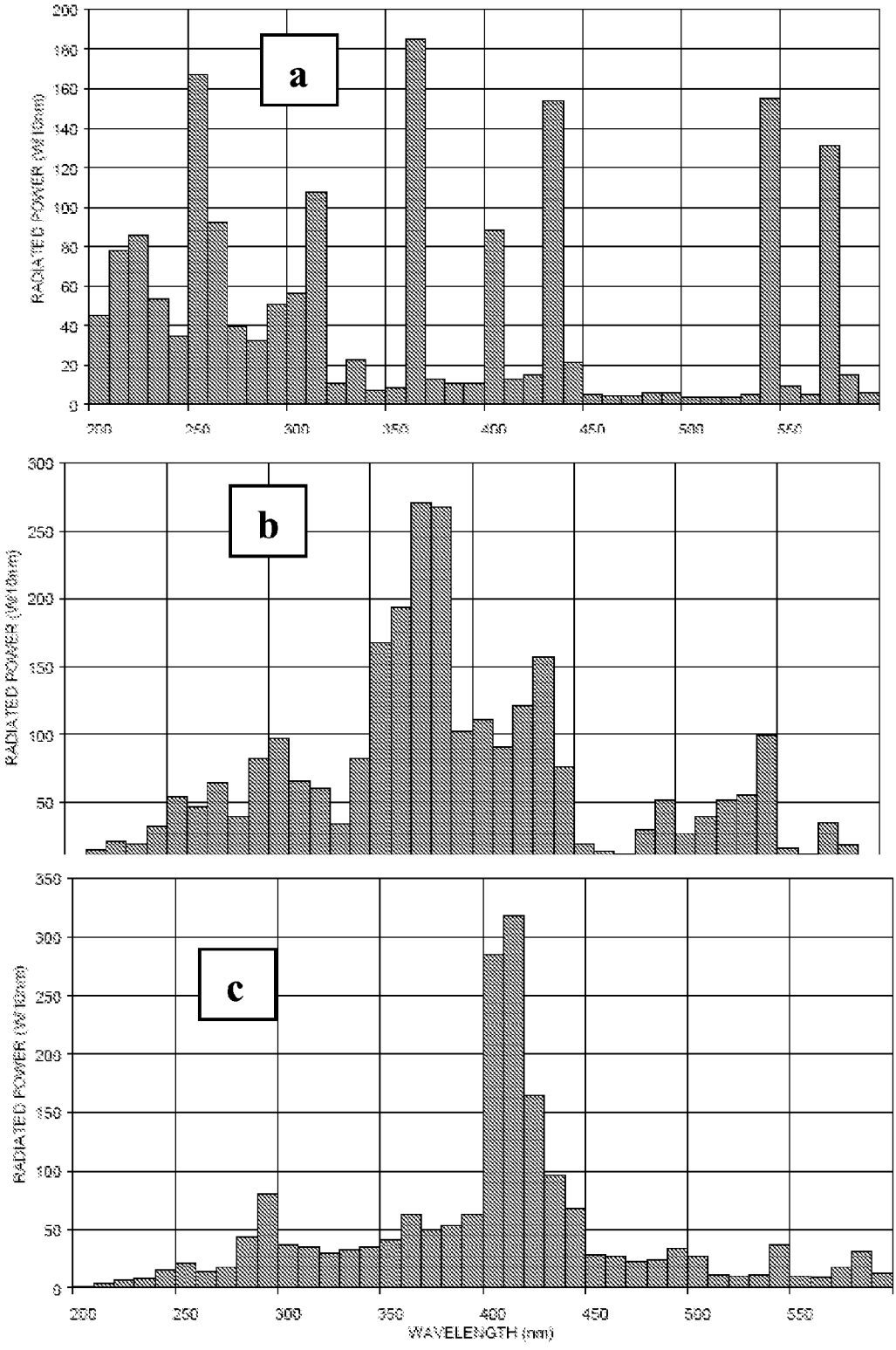

FIG. 4

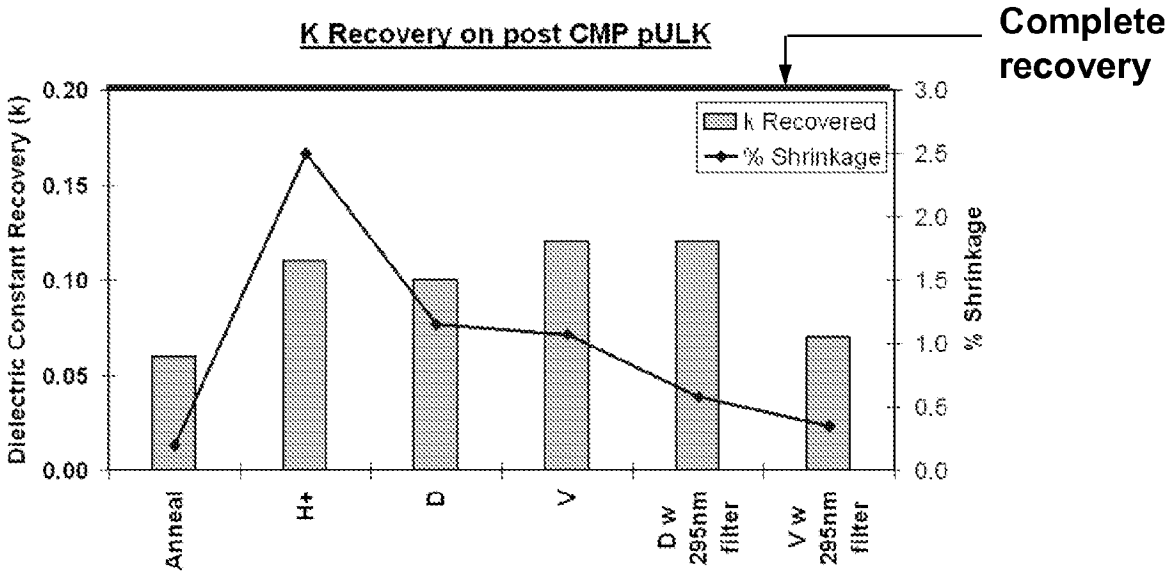
K Recovery on post CMP pULK
Complete recovery
Dielectric Constant Recovery (k)
0.20
0.15
0.10
0.05
0.00
3.0
2.5
2.0
1.5
1.0
0.5
0.0
% Shrinkage
k Recovered
% Shrinkage
Anneal
H+
D
V
D w 295nm filter
V w 295nm filter

FIG. 5

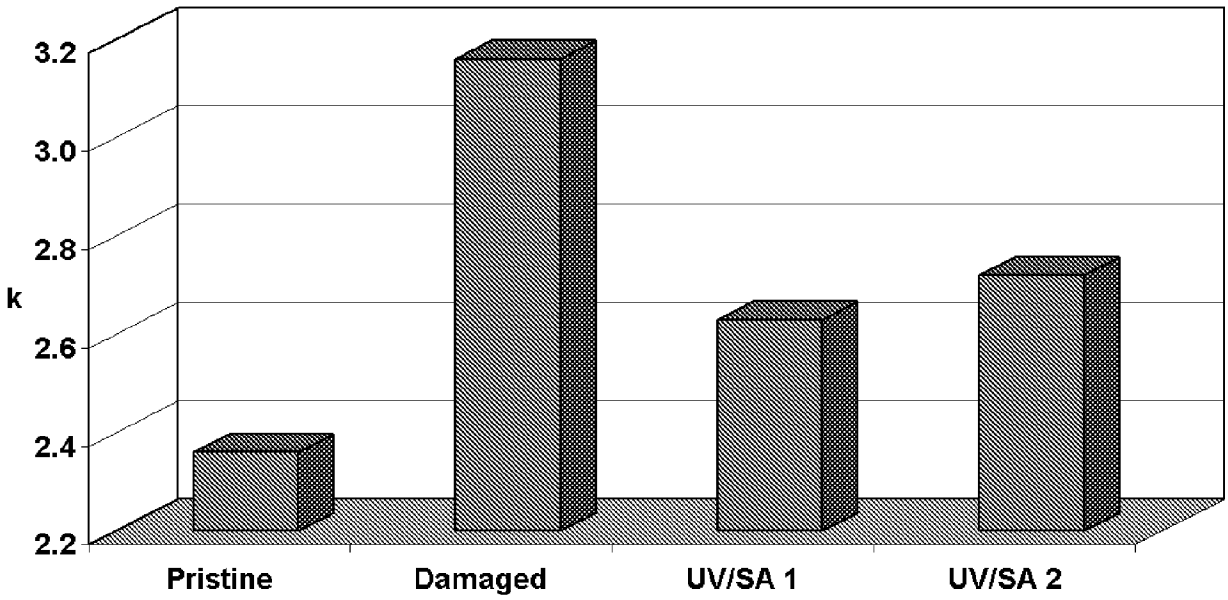

FIG. 6