US007782042B2

(12) **United States Patent**
Fukuzawa

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(45) **Date of Patent: *Aug. 24, 2010**

(54) **REFERENCE VOLTAGE SUPPLY CIRCUIT, ANALOG CIRCUIT, AND ELECTRONIC INSTRUMENT**

(75) Inventor: **Akihiro Fukuzawa**, Hino (JP)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 101 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **11/979,764**

(22) Filed: **Nov. 8, 2007**

(65) **Prior Publication Data**

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(30) **Foreign Application Priority Data**

Nov. 10, 2006 (JP) 2006-305154

(51) **Int. Cl.**
G05F 3/16 (2006.01)

(52) **U.S. Cl.** **323/314**; 330/253

(58) **Field of Classification Search** 323/304, 323/311, 312, 313, 314, 315, 316; 330/253, 330/255; 455/249.1

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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7,619,474 B2 * 11/2009 Fukukaza 330/253

FOREIGN PATENT DOCUMENTS

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OTHER PUBLICATIONS

U.S. Appl. No. 11/803,167, filed May 11, 2007.
U.S. Appl. No. 11/979,820 filed Nov. 8, 2007, which issued as U.S. Appl. No. 7,619,474, on Nov. 17, 2009.
U.S. Appl. No. 11/979,814 filed Nov. 8, 2007.
U.S. Appl. No. 11/979,824 filed Nov. 8, 2007.

* cited by examiner

Primary Examiner—Gary L Laxton
(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC

(57) **ABSTRACT**

A reference voltage supply circuit includes a first supply circuit that includes a reference-voltage first-type operational amplifier and supplies an analog reference voltage to a first analog reference voltage line, and a second supply circuit that includes a reference-voltage second-type operational amplifier and supplies the analog reference voltage to a second analog reference voltage line. When a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage first-type operational amplifier are respectively referred to as W1*a* and L1*a*, a bias current flowing through the differential section is referred to as Ia, a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage second-type operational amplifier are respectively referred to as W1*b* and L1*b*, and a bias current flowing through the differential section is referred to as Ib, W1*b*×L1*b*>W1*a*×L1*a* and Ia>Ib are satisfied.

17 Claims, 23 Drawing Sheets

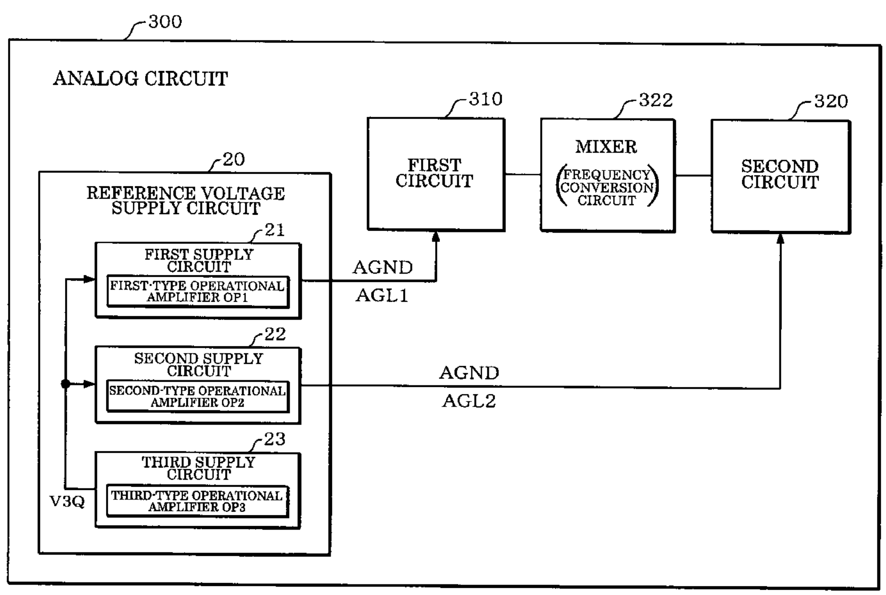
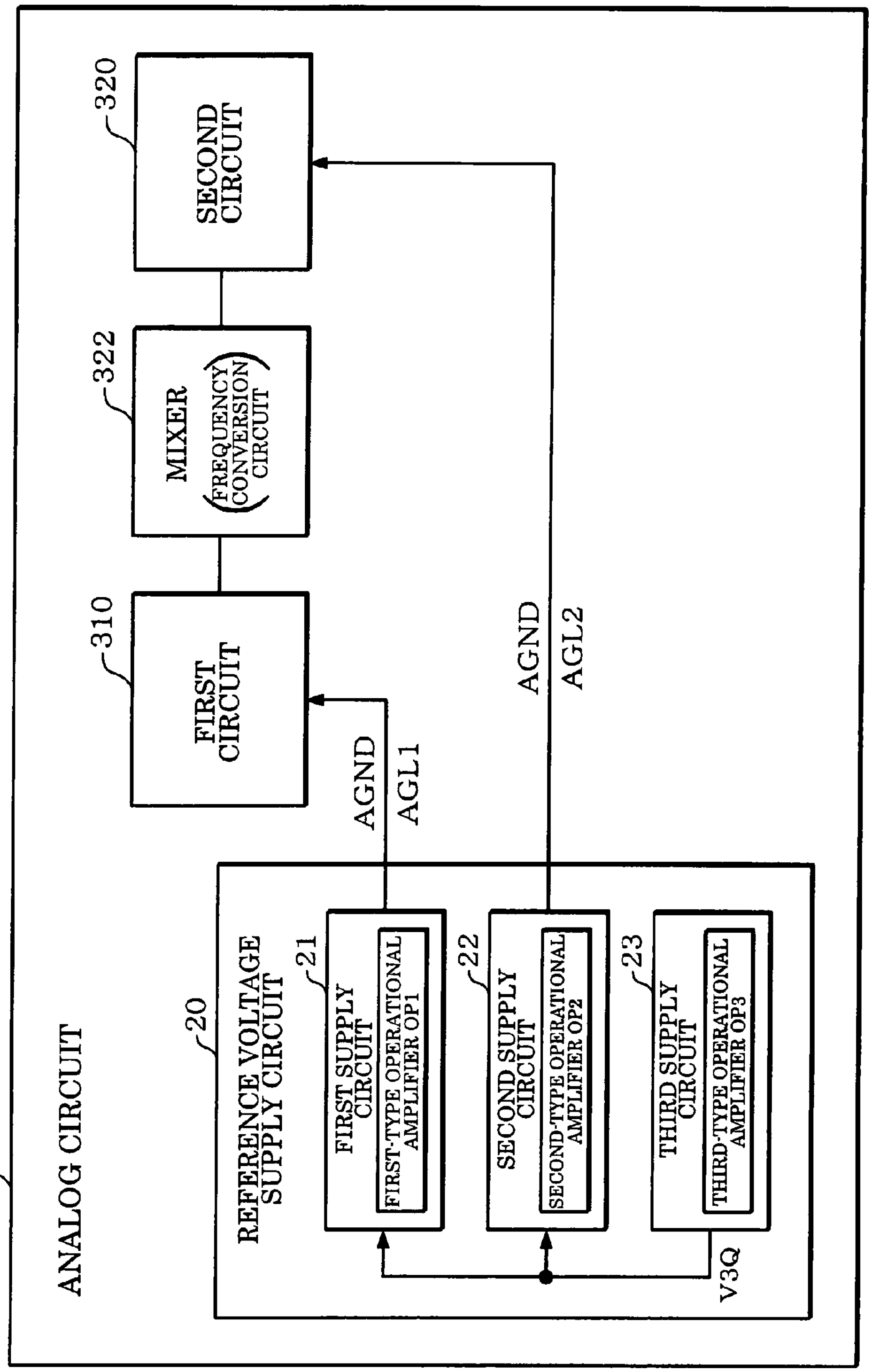


FIG. 1



300
ANALOG CIRCUIT
20
REFERENCE VOLTAGE SUPPLY CIRCUIT
21
FIRST SUPPLY CIRCUIT
FIRST-TYPE OPERATIONAL AMPLIFIER OP1
22
SECOND SUPPLY CIRCUIT
SECOND-TYPE OPERATIONAL AMPLIFIER OP2
23
THIRD SUPPLY CIRCUIT
THIRD-TYPE OPERATIONAL AMPLIFIER OP3
V3Q
AGND
AGL1
AGND
AGL2
310
FIRST CIRCUIT
322
MIXER
(FREQUENCY CONVERSION CIRCUIT)
320
SECOND CIRCUIT

FIG. 2

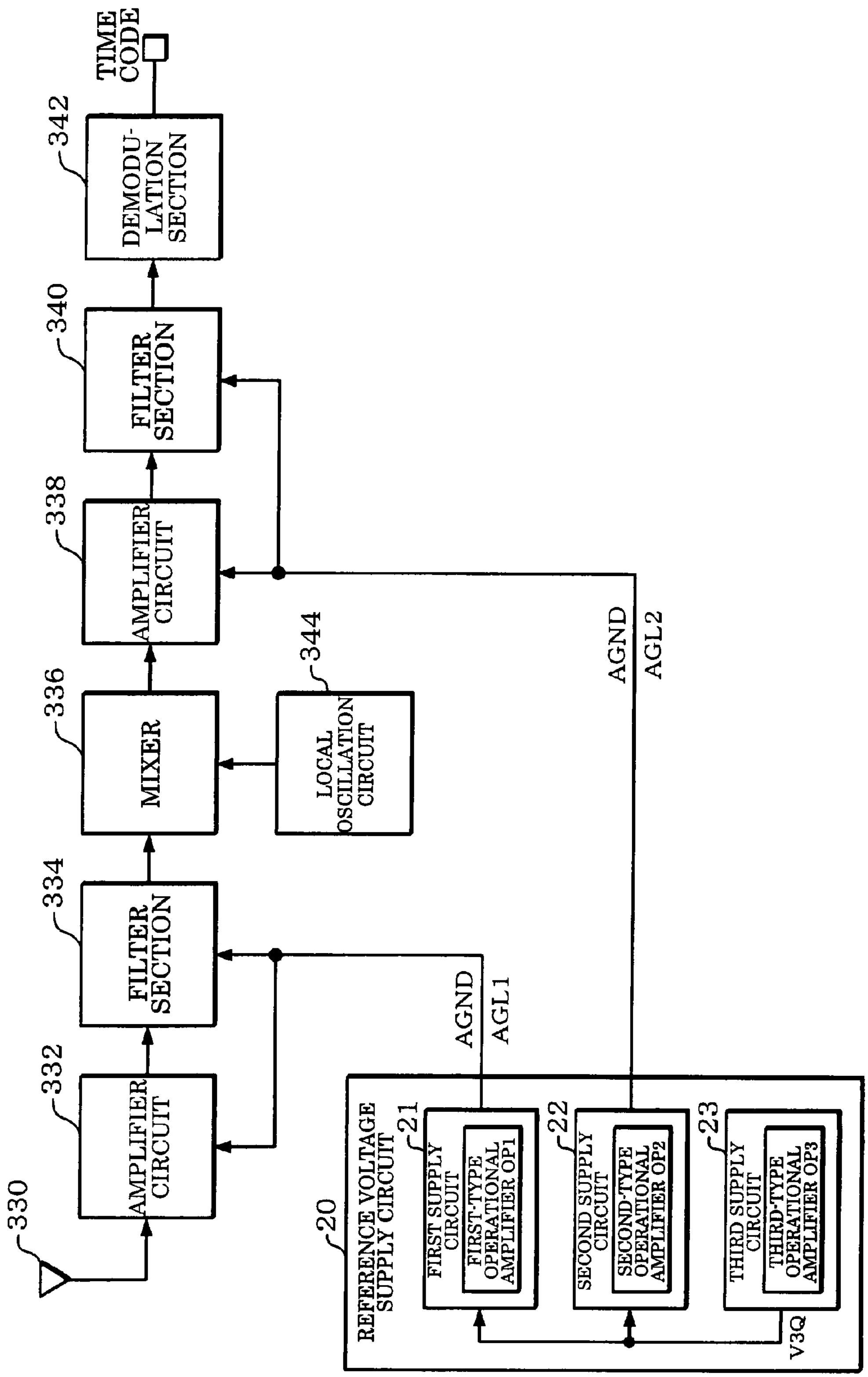
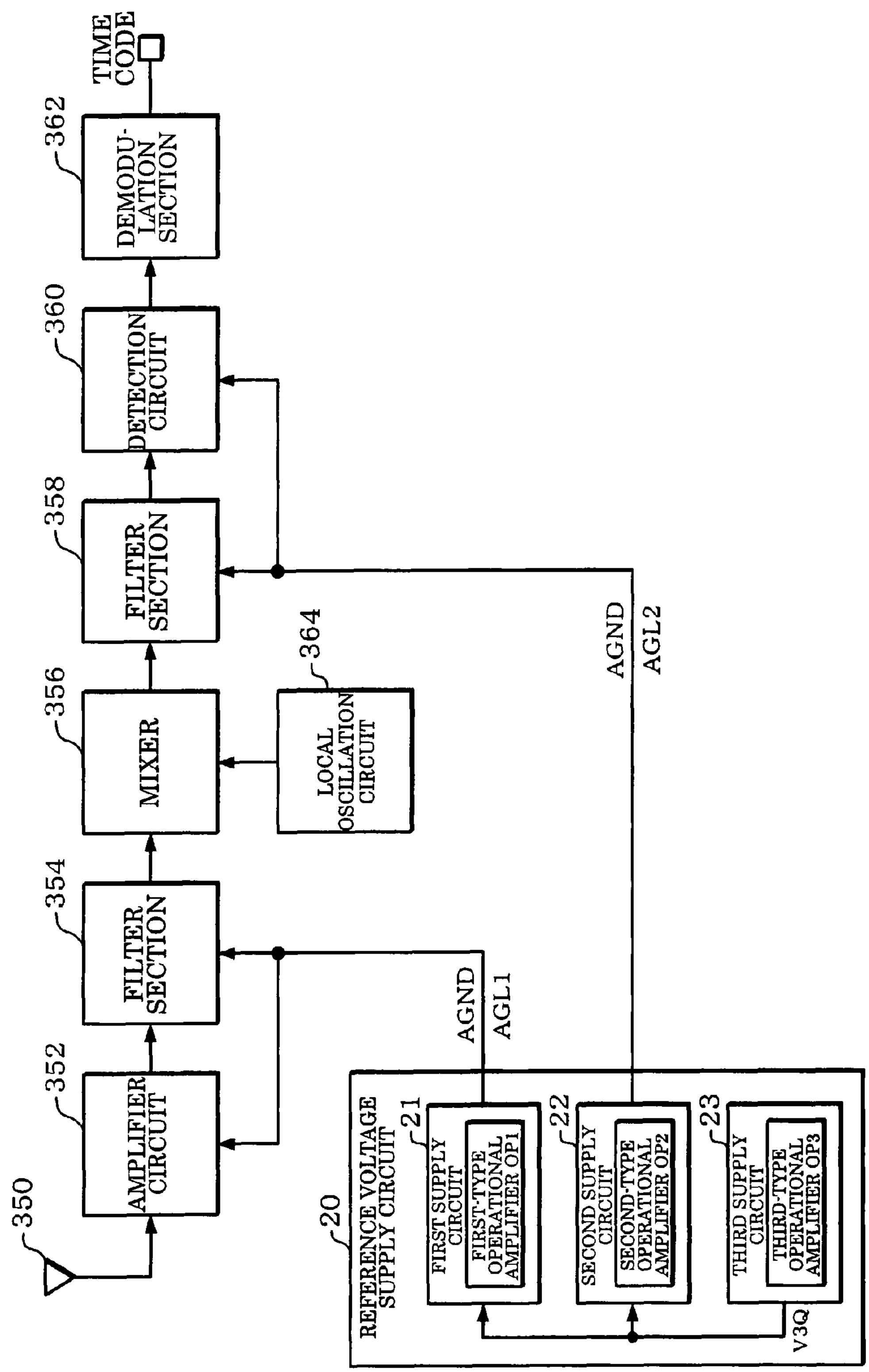
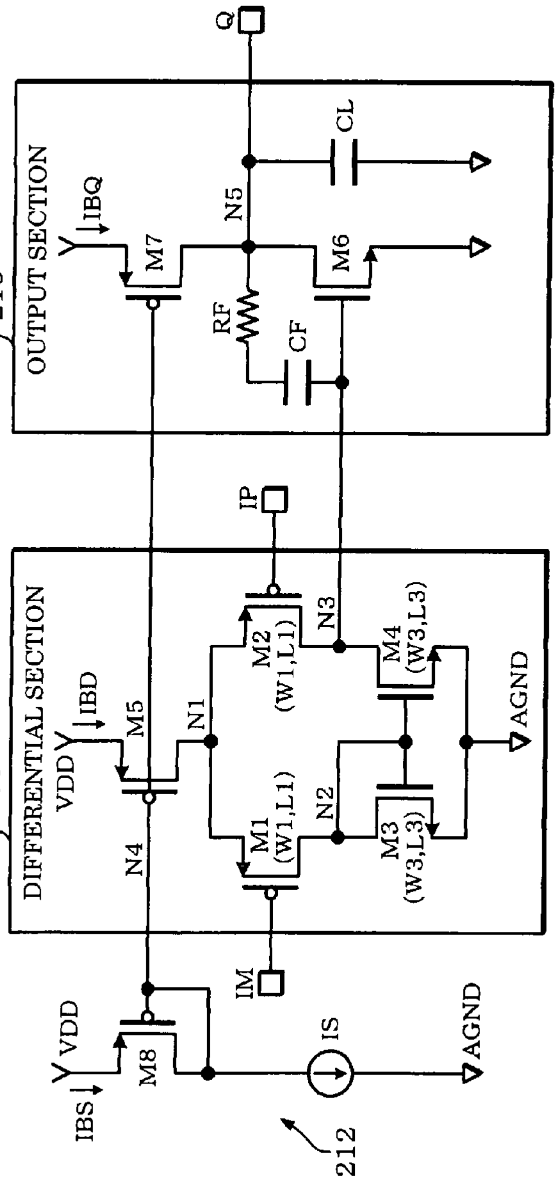

330
332
AMPLIFIER CIRCUIT
334
FILTER SECTION
336
MIXER
344
LOCAL OSCILLATION CIRCUIT
338
AMPLIFIER CIRCUIT
340
FILTER SECTION
342
DEMODU-LATION SECTION
TIME CODE
AGND
AGL1
AGND
AGL2
20
REFERENCE VOLTAGE SUPPLY CIRCUIT
21
FIRST SUPPLY CIRCUIT
FIRST-TYPE OPERATIONAL AMPLIFIER OP1
22
SECOND SUPPLY CIRCUIT
SECOND-TYPE OPERATIONAL AMPLIFIER OP2
23
THIRD SUPPLY CIRCUIT
THIRD-TYPE OPERATIONAL AMPLIFIER OP3
V3Q

FIG. 3

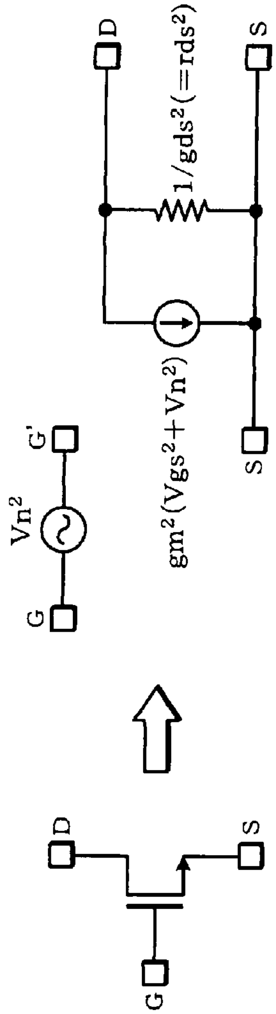


350
352
AMPLIFIER CIRCUIT
354
FILTER SECTION
356
MIXER
358
FILTER SECTION
360
DETECTION CIRCUIT
362
DEMODULATION SECTION
TIME CODE
364
LOCAL OSCILLATION CIRCUIT
AGND
AGL1
AGND
AGL2
20
REFERENCE VOLTAGE SUPPLY CIRCUIT
21
FIRST SUPPLY CIRCUIT
FIRST-TYPE OPERATIONAL AMPLIFIER OP1
22
SECOND SUPPLY CIRCUIT
SECOND-TYPE OPERATIONAL AMPLIFIER OP2
23
THIRD SUPPLY CIRCUIT
THIRD-TYPE OPERATIONAL AMPLIFIER OP3
V3Q



Q
210
OUTPUT SECTION
IBQ
M7
N5
CL
RF
CF
M6
IP
200
DIFFERENTIAL SECTION
VDD
IBD
M5
N1
N3
M2
(W1,L1)
M4
(W3,L3)
AGND
N4
M1
(W1,L1)
N2
M3
(W3,L3)
IM
VDD
IBS
M8
IS
AGND
212

FIG. 4A



D
S
G
G
G'
Vn^2
$gm^2(Vgs^2+Vn^2)$
$1/gds^2(=rds^2)$
D
S
S

FIG. 4B

FIG. 5A

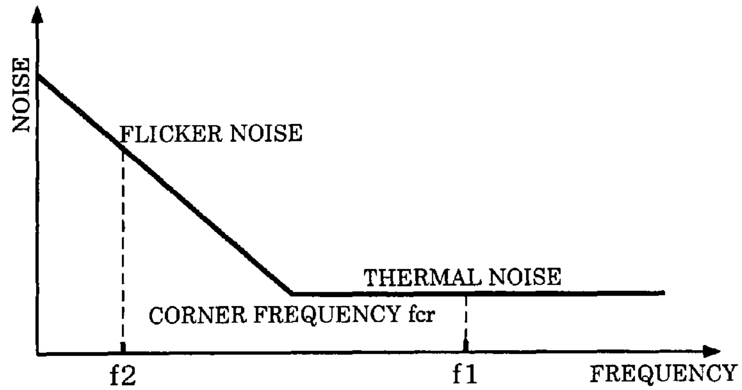


FIG. 5B

FIRST-TYPE OPERATIONAL AMPLIFIER OP1	SECOND-TYPE OPERATIONAL AMPLIFIER OP2	THIRD-TYPE OPERATIONAL AMPLIFIER OP3
W1×L1=W1a×L1a	W1×L1=W1b×L1b	W1×L1=W1c×L1c
IBD=Ia	IBD=Ib	IBD=Ic
fop=f1	fop=f2	
RT1=RT1a=W1a/L1a	L1/L3=L1b/L3b	
RT3=RT3a=W3a/L3a		

FIG. 5C

	OP1 (THERMAL NOISE REDUCTION)	OP2 (FLICKER NOISE REDUCTION)	OP3
W1×L1	SMALL (W1a×L1a)	LARGE (W1b×L1b)	LARGE (W1c×L1c)
IBD	LARGE (Ia)	SMALL (Ib)	LARGE (Ic)
fop	HIGH (f1)	LOW (f2)	
L1/L3		SMALL (L1b<L3b)	
RT1/RT3	LARGE (RT1a>RT3a)		

W1b×L1b>W1a×L1a
Ia>Ib

W1c×L1c>W1a×L1a
Ic>Ib

FIG. 6A

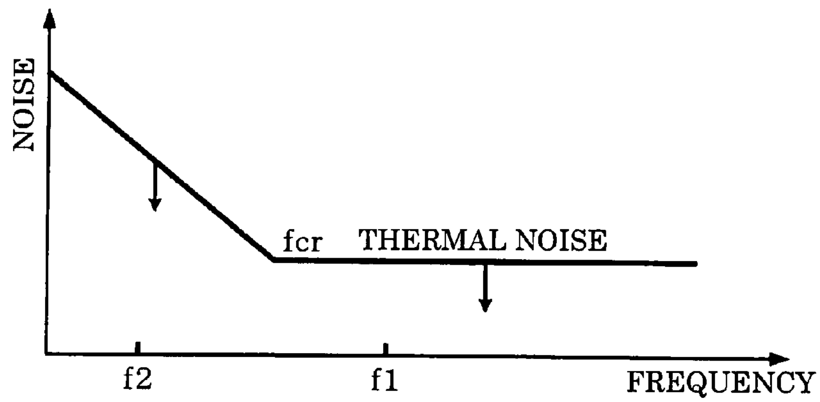


FIG. 6B FIRST-TYPE OPERATIONAL AMPLIFIER OP1

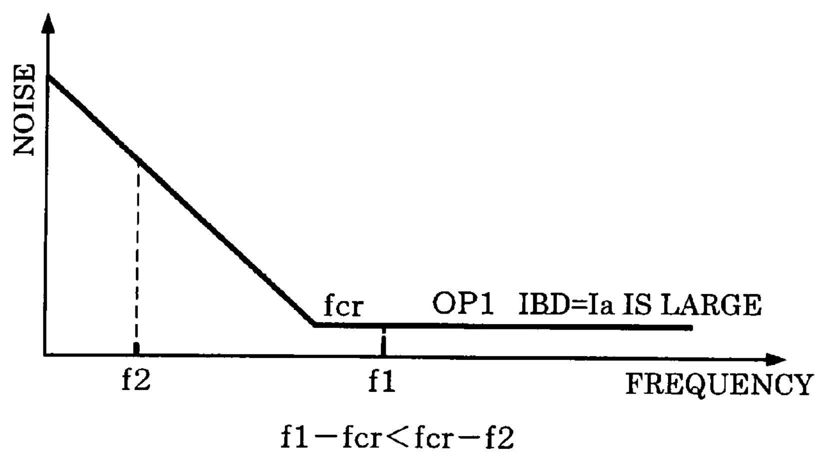


FIG. 6C SECOND-TYPE OPERATIONAL AMPLIFIER OP2

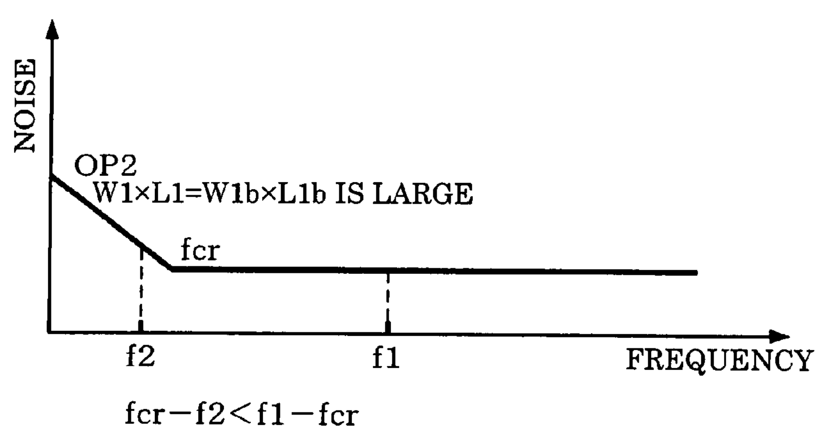


FIG. 7A FIRST-TYPE OPERATIONAL AMPLIFIER OP1

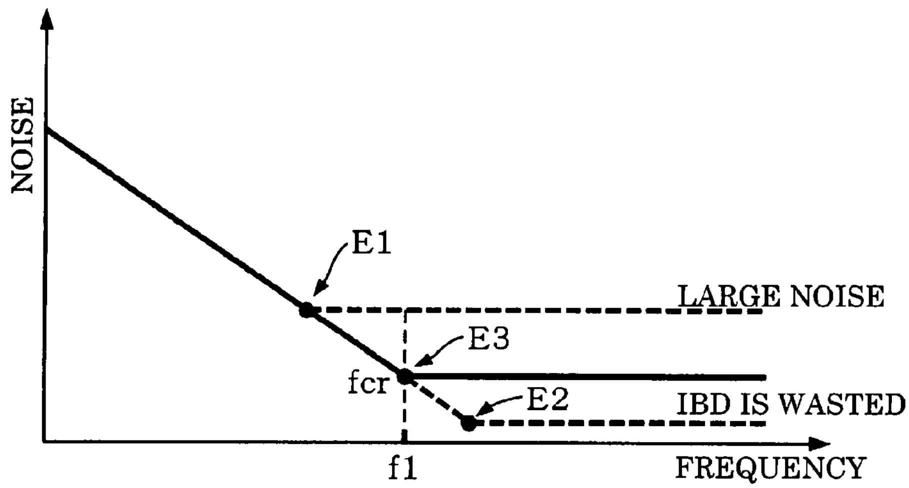


FIG. 7B SECOND-TYPE OPERATIONAL AMPLIFIER OP2

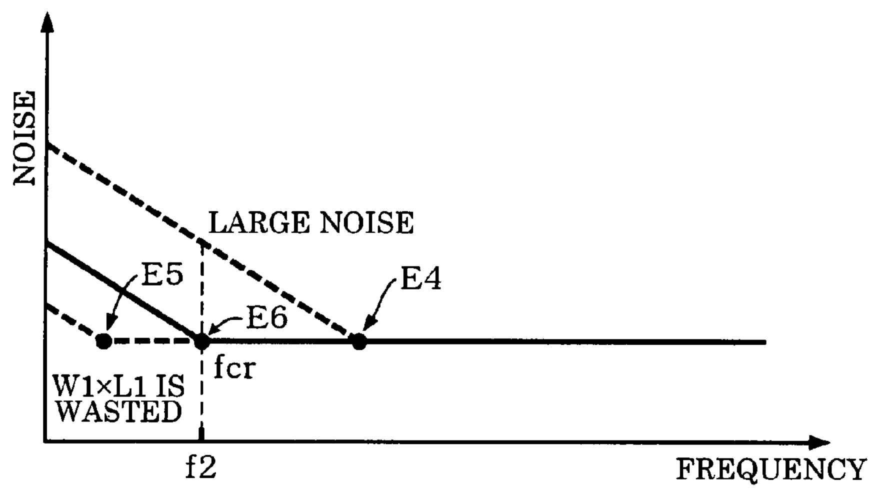


FIG. 8A

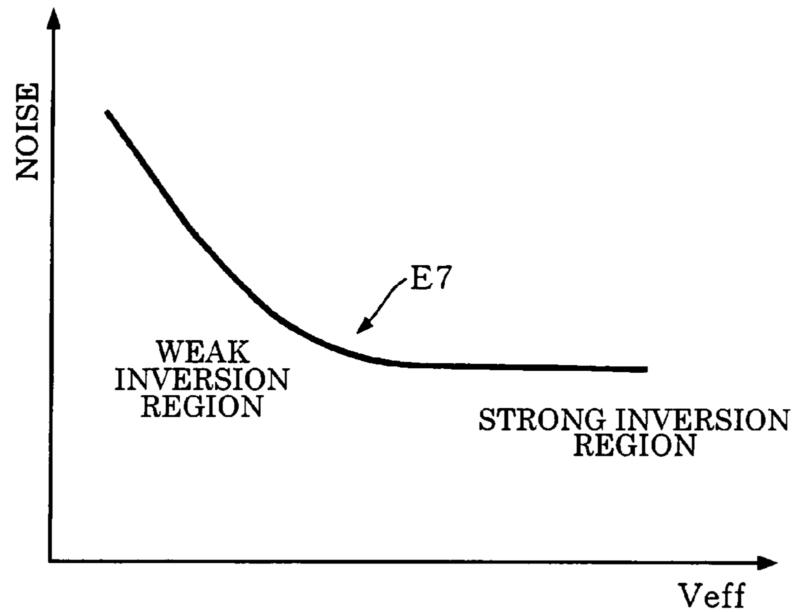

NOISE
E7
WEAK
INVERSION
REGION
STRONG INVERSION
REGION
Veff

FIG. 8B

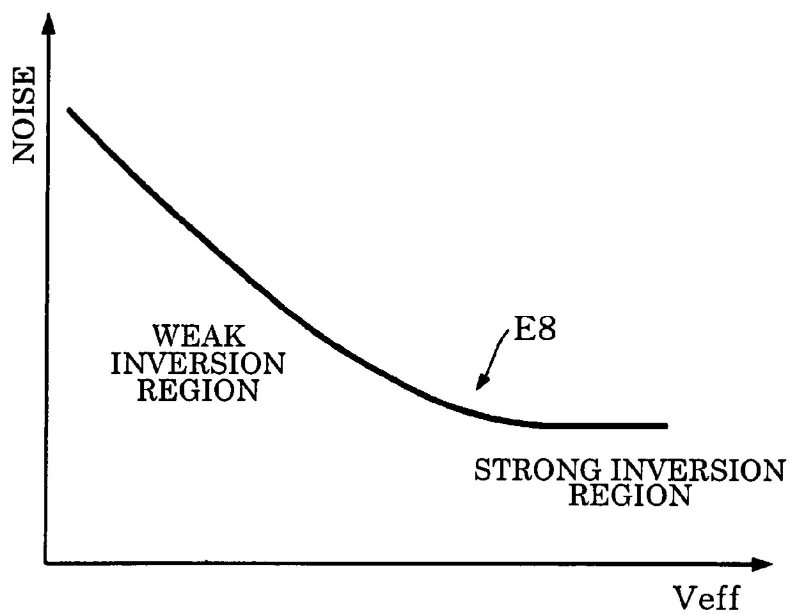

NOISE
E8
WEAK
INVERSION
REGION
STRONG INVERSION
REGION
Veff

FIG. 9A

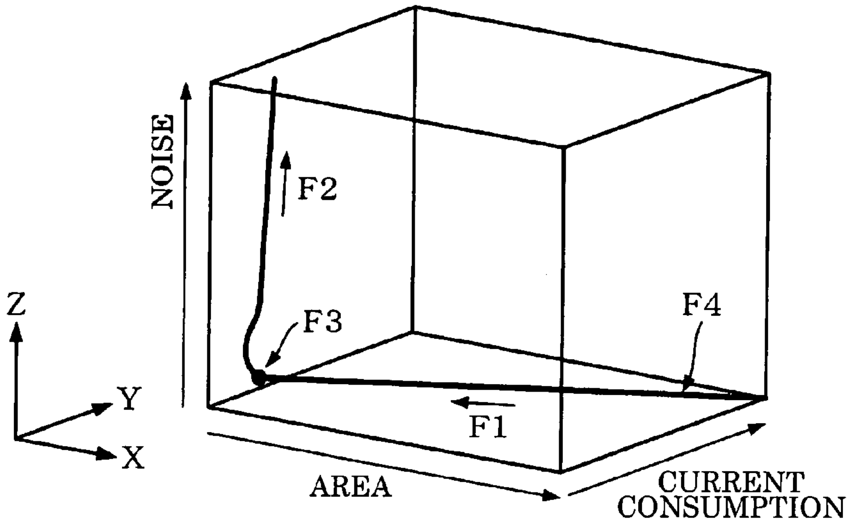

NOISE
F2
Z
F3
F4
Y
X
F1
AREA
CURRENT CONSUMPTION

FIG. 9B

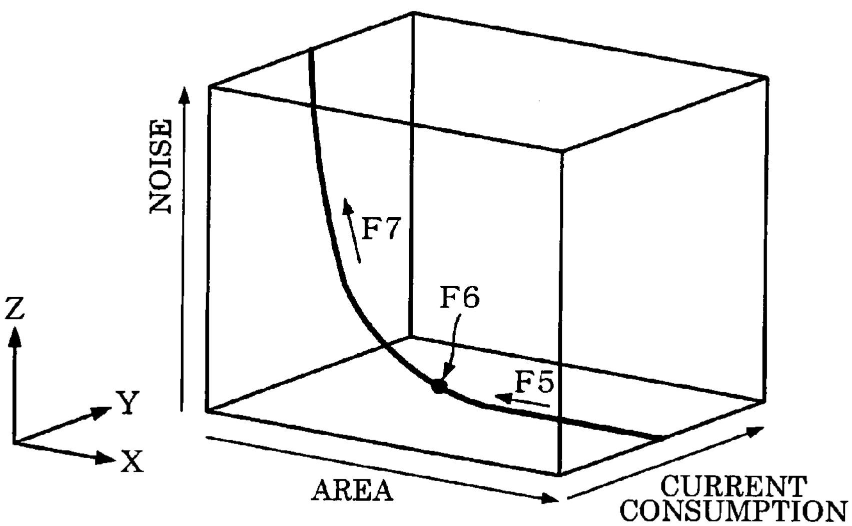

NOISE
F7
Z
F6
F5
Y
X
AREA
CURRENT CONSUMPTION

FIG. 10

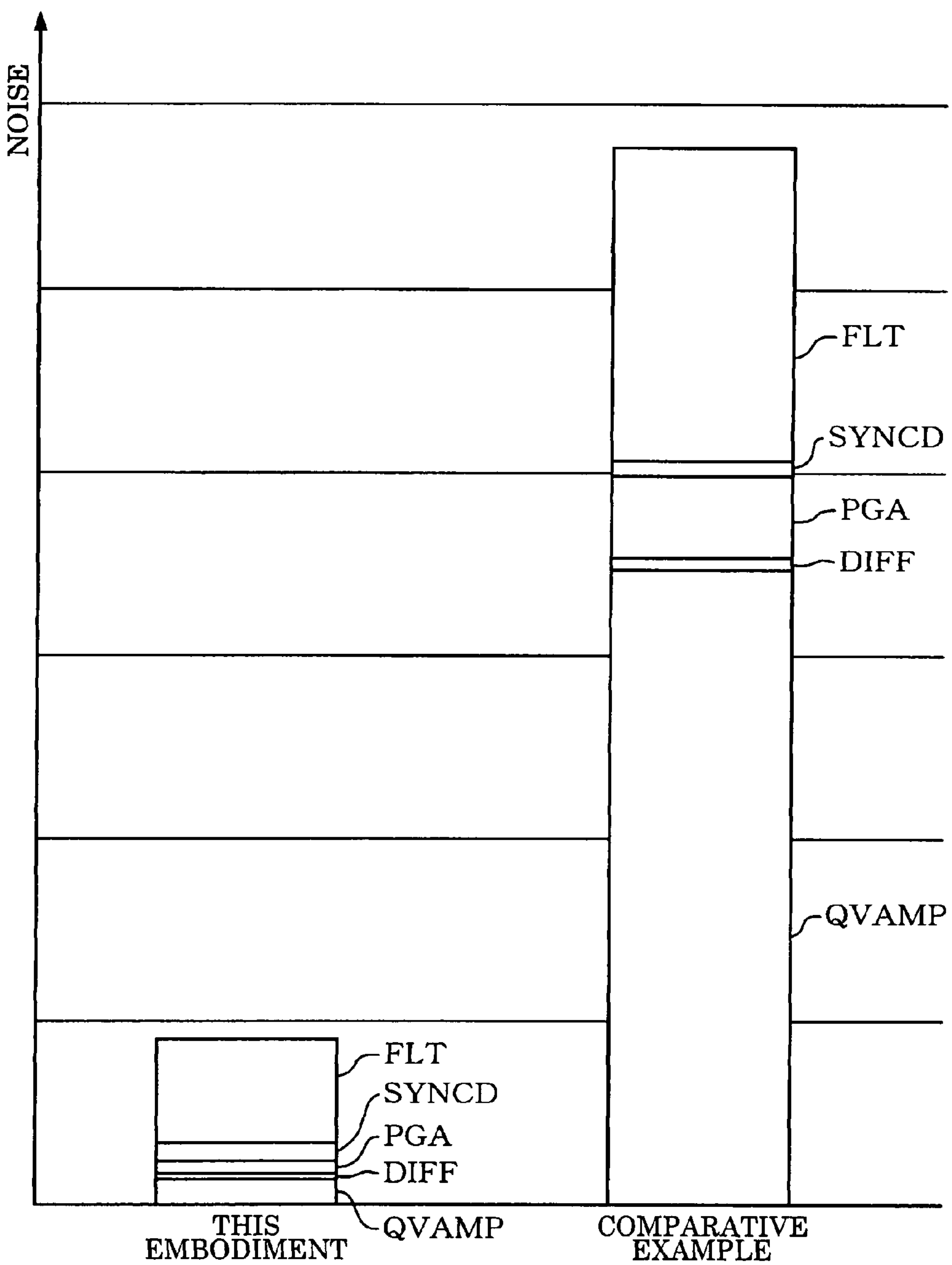

NOISE
FLT
SYNCD
PGA
DIFF
QVAMP
FLT
SYNCD
PGA
DIFF
QVAMP
THIS EMBODIMENT
COMPARATIVE EXAMPLE

FIG. 11A

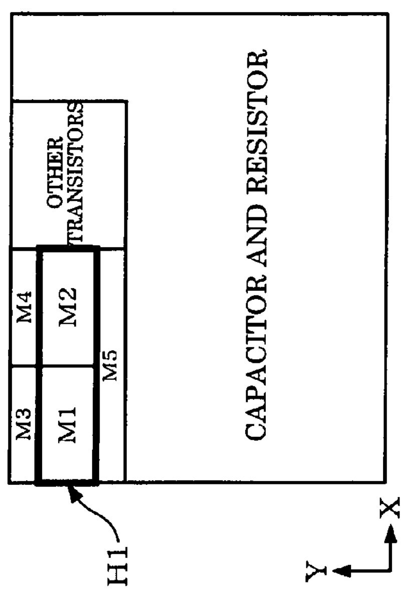


FIG. 11B

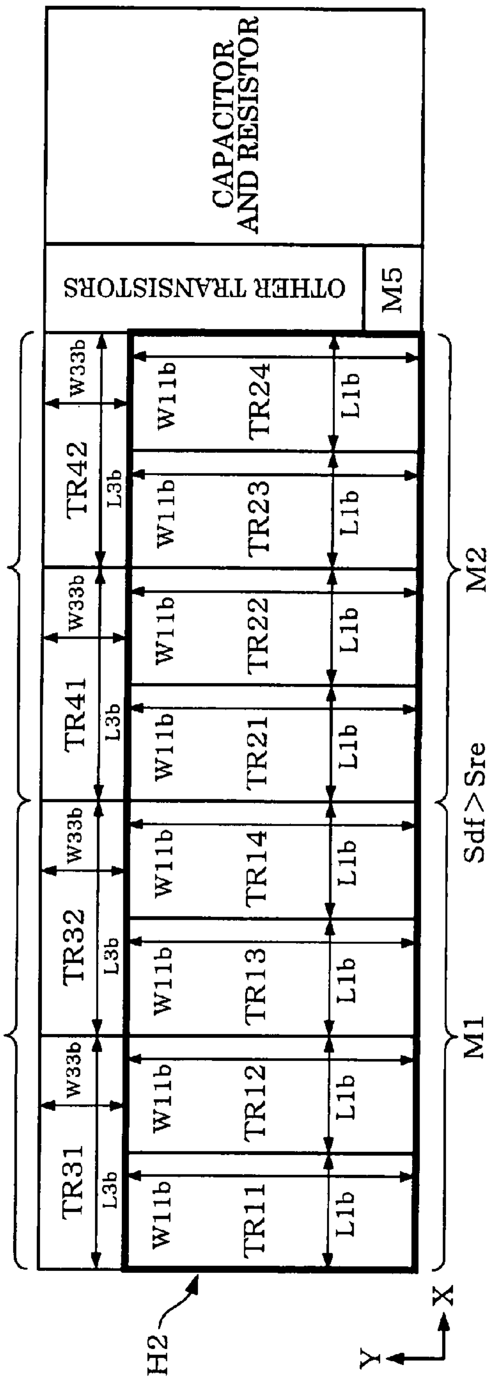


FIG. 12

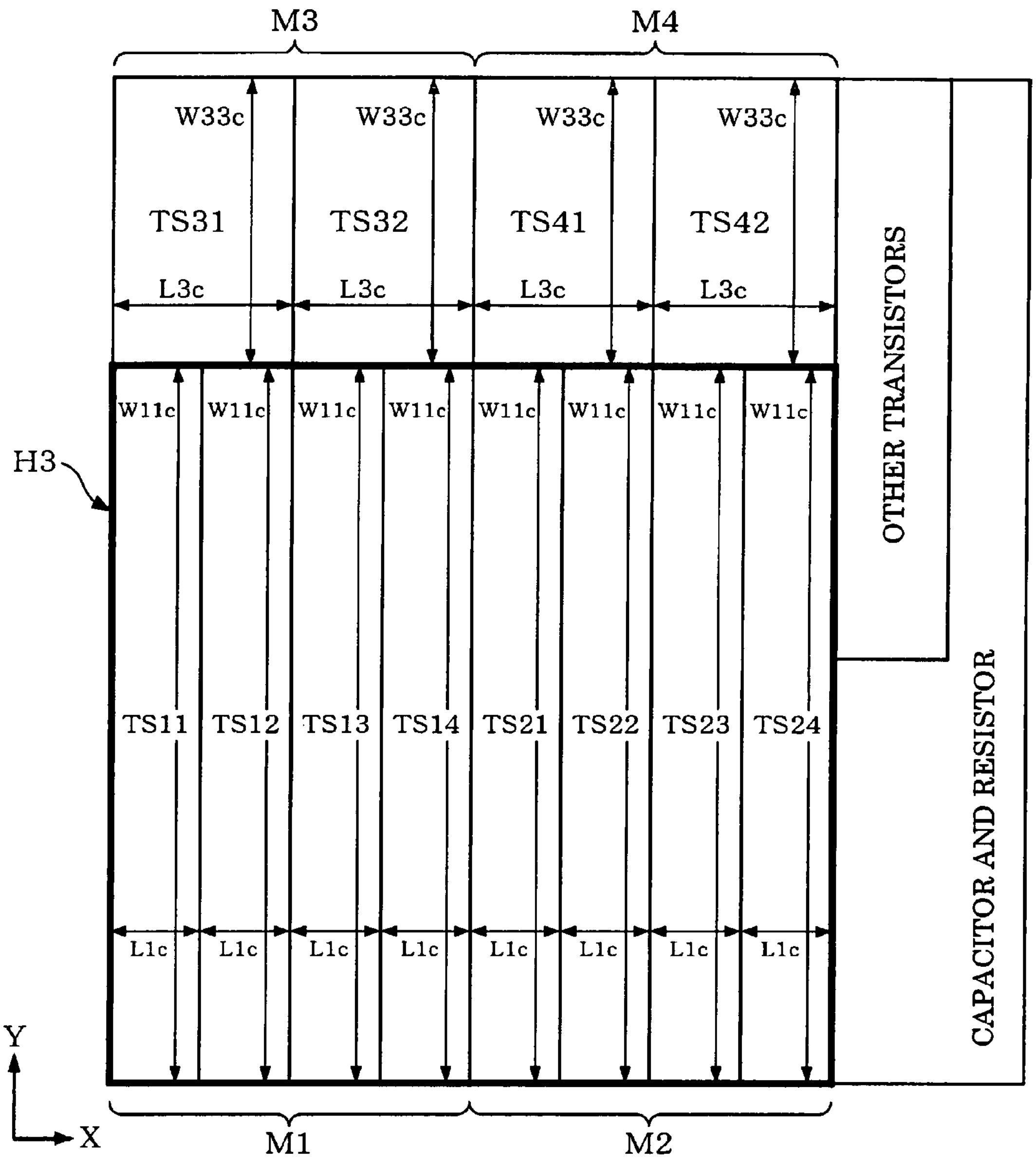

M3
M4
W33c
W33c
W33c
W33c
TS31
TS32
TS41
TS42
L3c
L3c
L3c
L3c
OTHER TRANSISTORS
W11c
W11c
W11c
W11c
W11c
W11c
W11c
W11c
H3
TS11
TS12
TS13
TS14
TS21
TS22
TS23
TS24
CAPACITOR AND RESISTOR
L1c
L1c
L1c
L1c
L1c
L1c
L1c
L1c
Y
X
M1
M2

FIG. 13

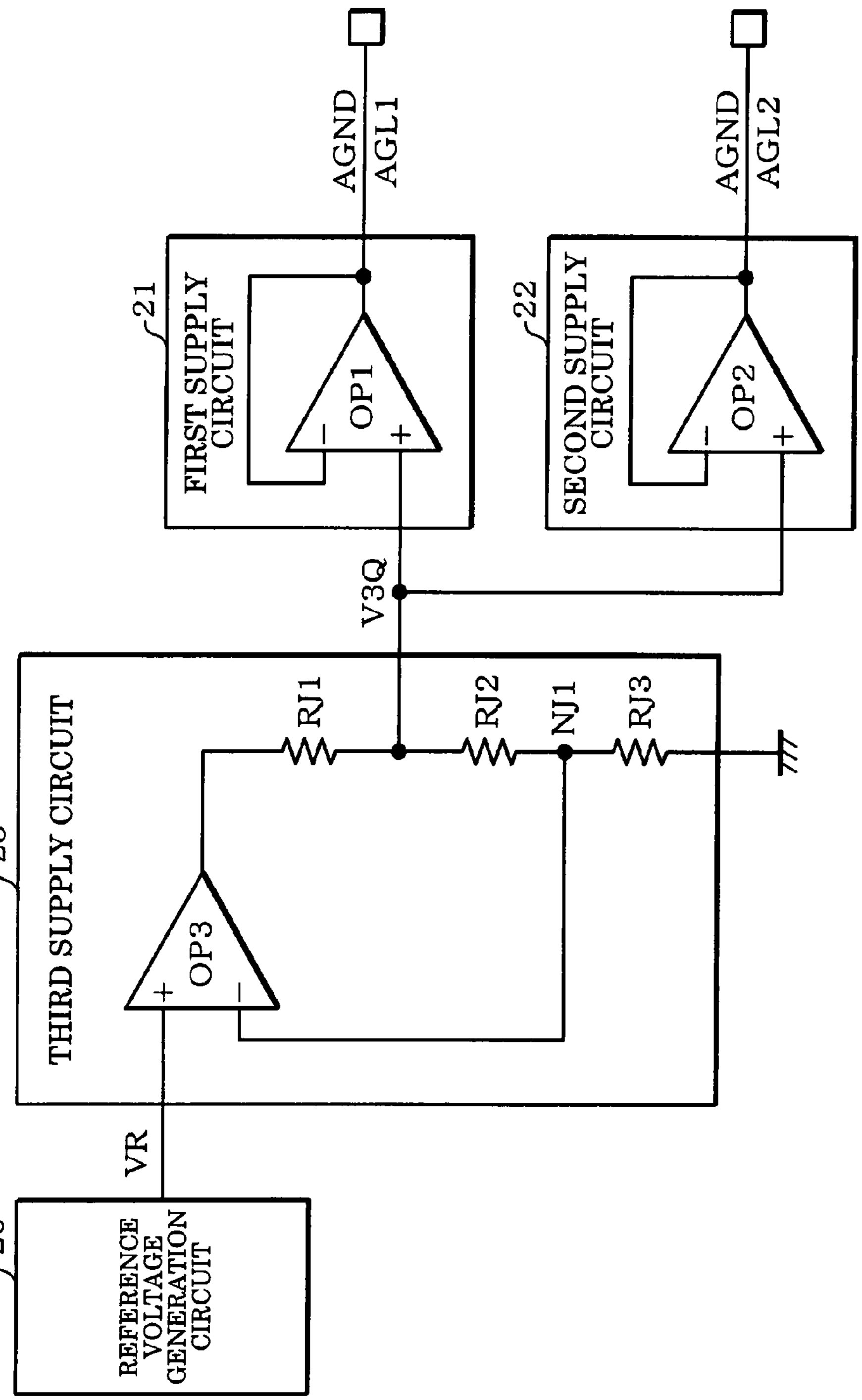

AGND
AGL1
AGND
AGL2
21
FIRST SUPPLY CIRCUIT
OP1
22
SECOND SUPPLY CIRCUIT
OP2
V3Q
23
THIRD SUPPLY CIRCUIT
OP3
RJ1
RJ2
NJ1
RJ3
VR
26
REFERENCE VOLTAGE GENERATION CIRCUIT

FIG. 14

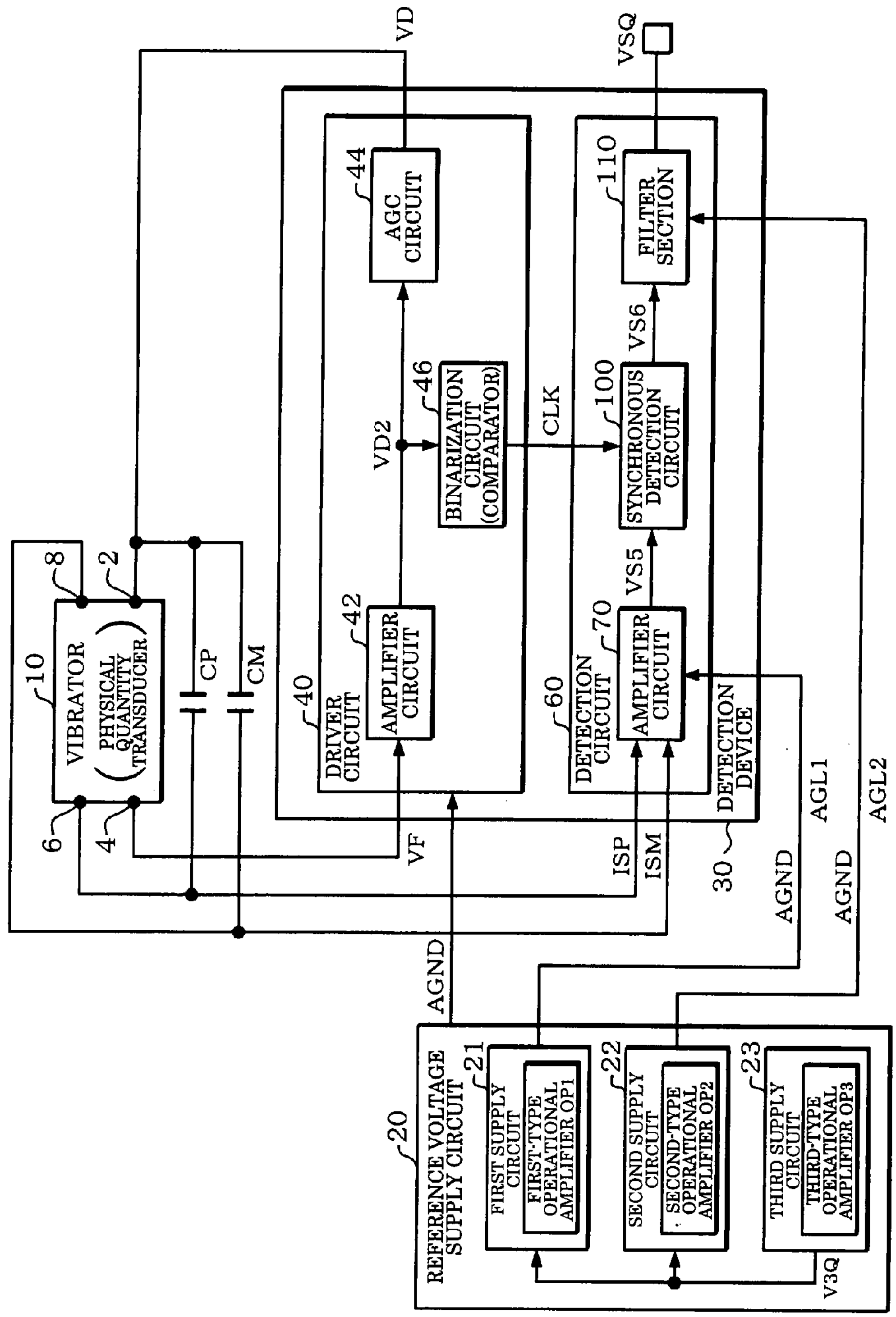

VIBRATOR
PHYSICAL QUANTITY TRANSDUCER
10
8
2
6
4
CP
CM
VD
VSQ
DRIVER CIRCUIT
40
AMPLIFIER CIRCUIT
42
VD2
BINARIZATION CIRCUIT (COMPARATOR)
46
AGC CIRCUIT
44
CLK
DETECTION CIRCUIT
60
AMPLIFIER CIRCUIT
70
VS5
SYNCHRONOUS DETECTION CIRCUIT
100
VS6
FILTER SECTION
110
DETECTION DEVICE
30
VF
ISP
ISM
AGND
AGL1
AGL2
REFERENCE VOLTAGE SUPPLY CIRCUIT
20
FIRST SUPPLY CIRCUIT
21
FIRST-TYPE OPERATIONAL AMPLIFIER OP1
SECOND SUPPLY CIRCUIT
22
SECOND-TYPE OPERATIONAL AMPLIFIER OP2
THIRD SUPPLY CIRCUIT
23
THIRD-TYPE OPERATIONAL AMPLIFIER OP3
V3Q

FIG. 15A

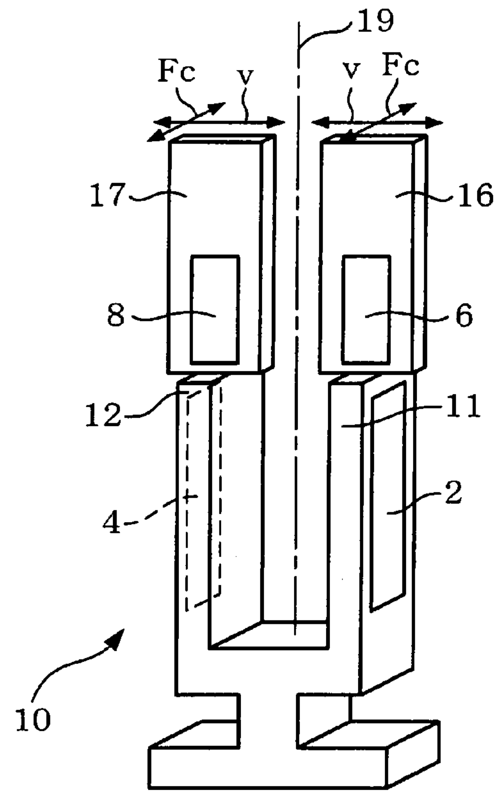


FIG. 15B

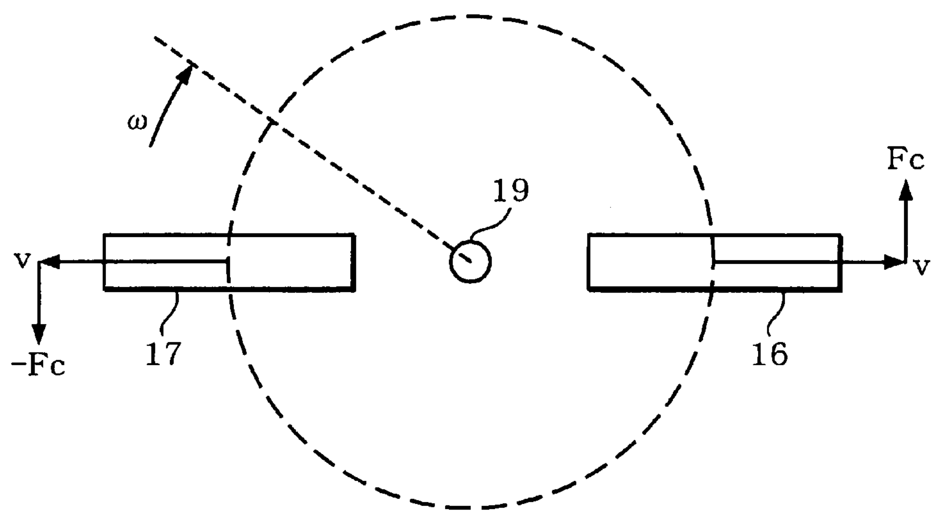


FIG. 16A BEFORE SYNCHRONOUS DETECTION

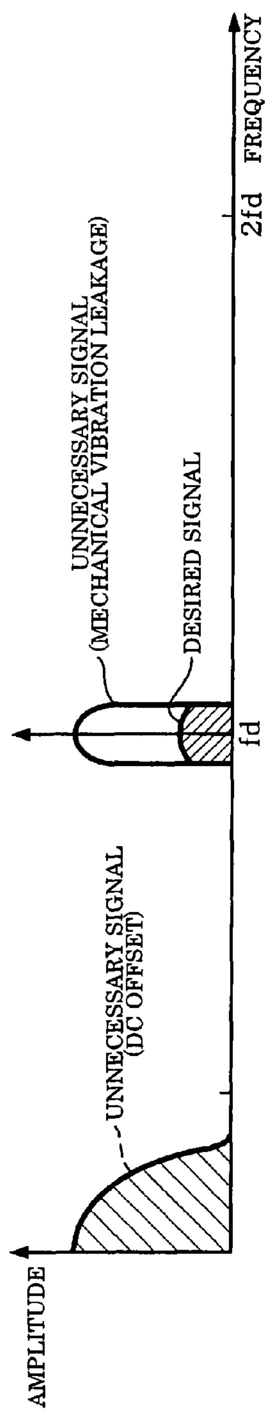


FIG. 16B AFTER SYNCHRONOUS DETECTION

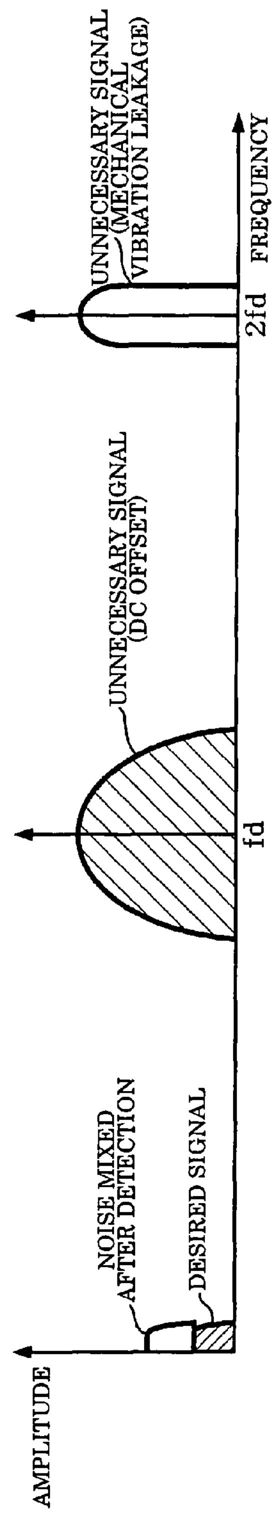


FIG. 16C AFTER FILTERING PROCESS

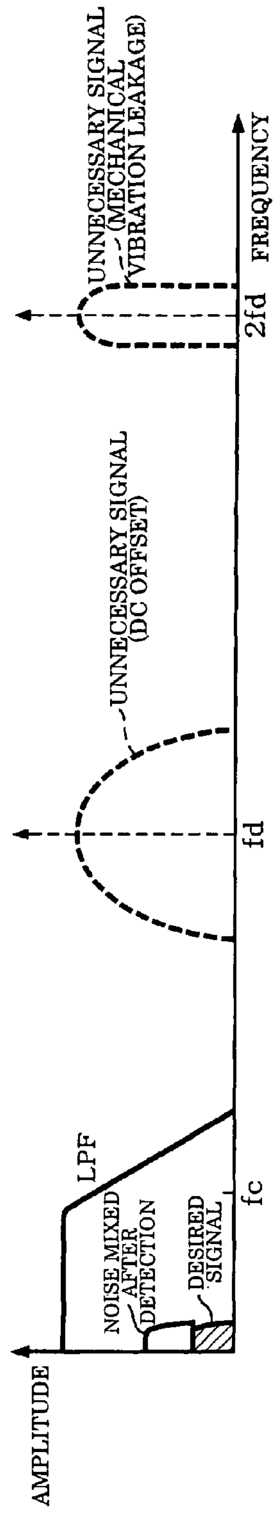
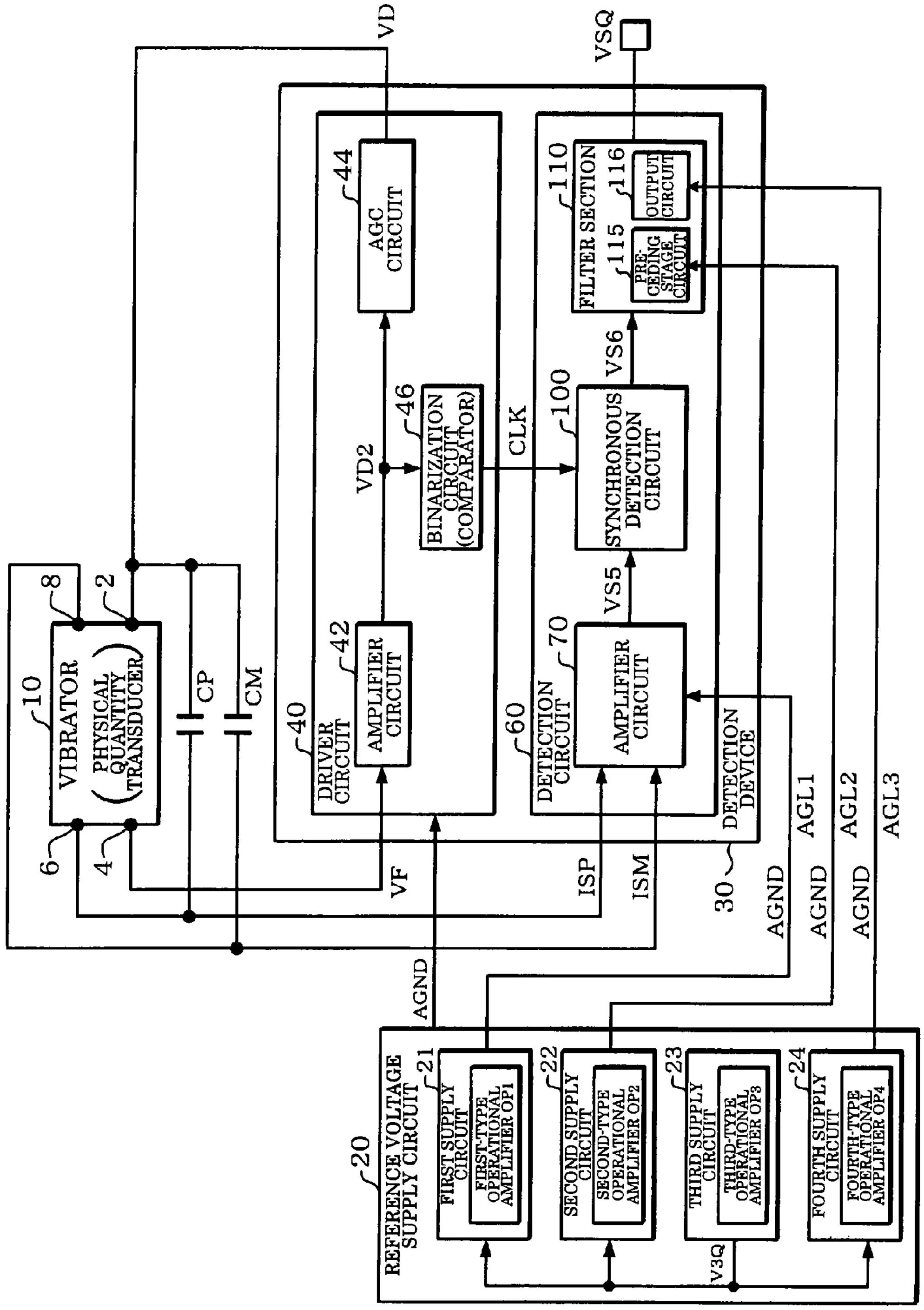


FIG. 17



VIBRATOR
(PHYSICAL QUANTITY TRANSDUCER)
10
8
2
6
4
CP
CM
VD
VSQ
DRIVER CIRCUIT
40
AMPLIFIER CIRCUIT
42
VD2
BINARIZATION CIRCUIT (COMPARATOR)
46
AGC CIRCUIT
44
CLK
DETECTION CIRCUIT
60
AMPLIFIER CIRCUIT
70
VS5
SYNCHRONOUS DETECTION CIRCUIT
100
VS6
FILTER SECTION
110
115
PRE-CEDING STAGE CIRCUIT
116
OUTPUT CIRCUIT
DETECTION DEVICE
30
VF
ISP
ISM
AGND
AGND
AGND
AGND
AGL1
AGL2
AGL3
REFERENCE VOLTAGE SUPPLY CIRCUIT
20
FIRST SUPPLY CIRCUIT
21
FIRST-TYPE OPERATIONAL AMPLIFIER OP1
SECOND SUPPLY CIRCUIT
22
SECOND-TYPE OPERATIONAL AMPLIFIER OP2
THIRD SUPPLY CIRCUIT
23
THIRD-TYPE OPERATIONAL AMPLIFIER OP3
FOURTH SUPPLY CIRCUIT
24
FOURTH-TYPE OPERATIONAL AMPLIFIER OP4
V3Q

FIG. 18

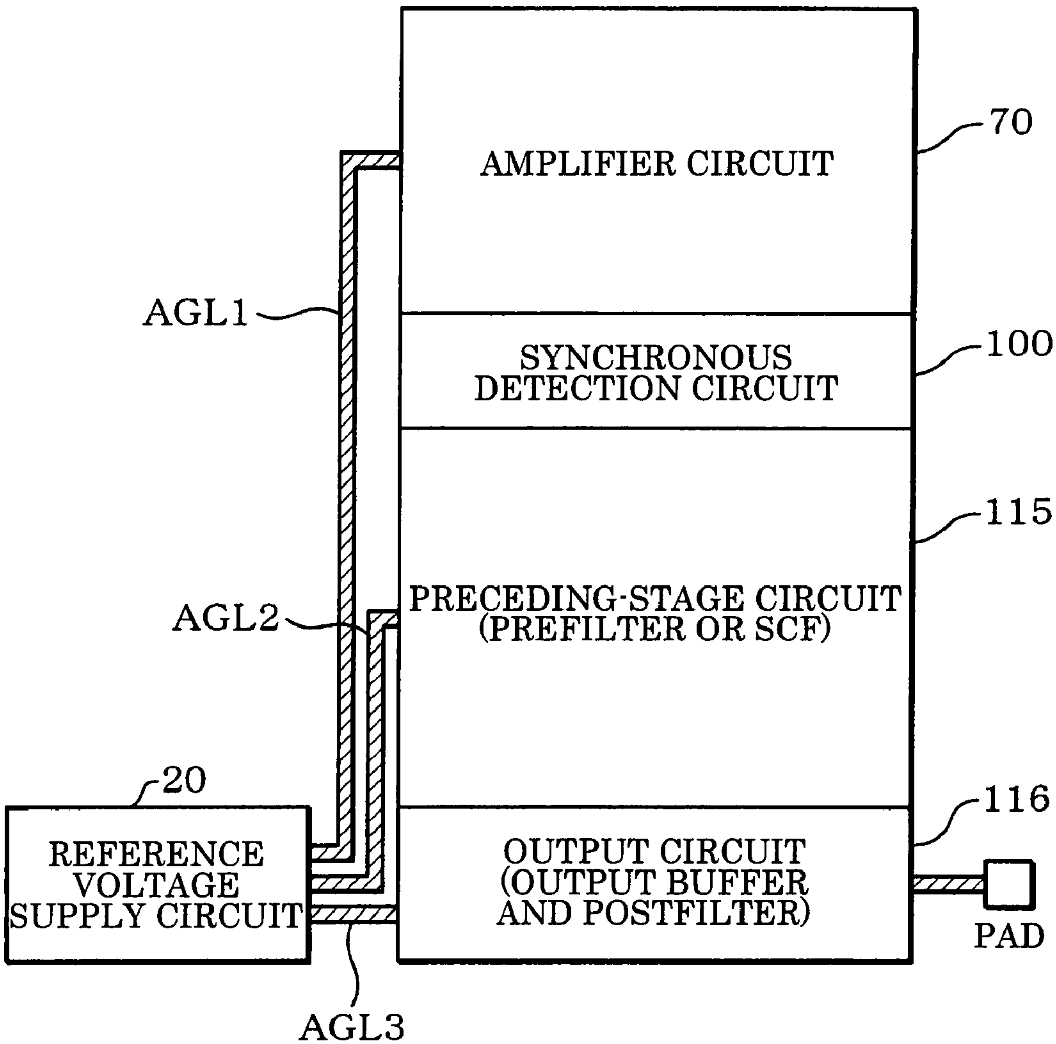

AMPLIFIER CIRCUIT
70
AGL1
SYNCHRONOUS DETECTION CIRCUIT
100
115
AGL2
PRECEDING-STAGE CIRCUIT (PREFILTER OR SCF)
20
116
REFERENCE VOLTAGE SUPPLY CIRCUIT
OUTPUT CIRCUIT (OUTPUT BUFFER AND POSTFILTER)
PAD
AGL3

FIG. 19

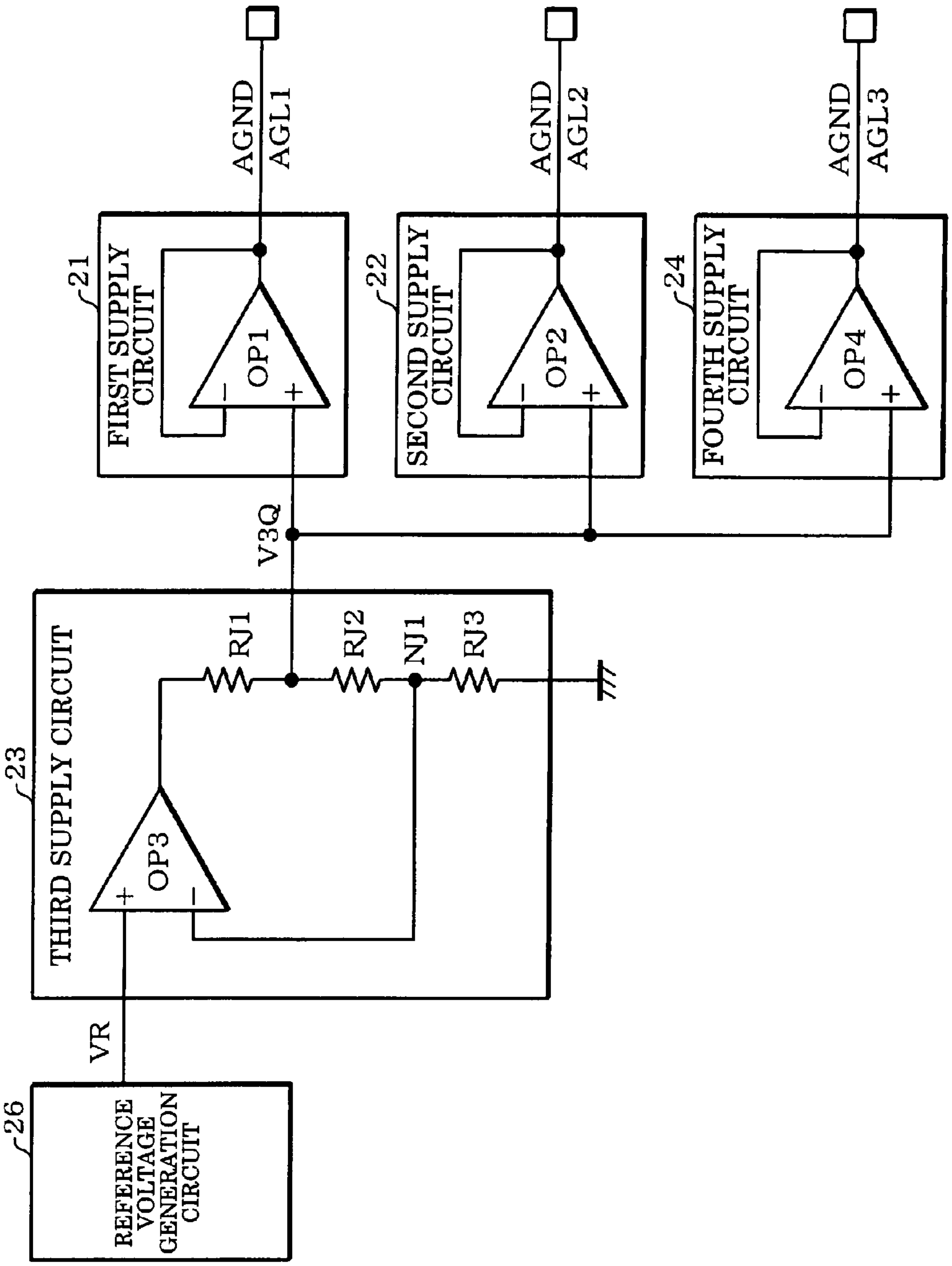

21
FIRST SUPPLY CIRCUIT
OP1
AGND AGL1
22
SECOND SUPPLY CIRCUIT
OP2
AGND AGL2
24
FOURTH SUPPLY CIRCUIT
OP4
AGND AGL3
V3Q
23
THIRD SUPPLY CIRCUIT
OP3
RJ1
RJ2
NJ1
RJ3
VR
26
REFERENCE VOLTAGE GENERATION CIRCUIT

FIG. 20

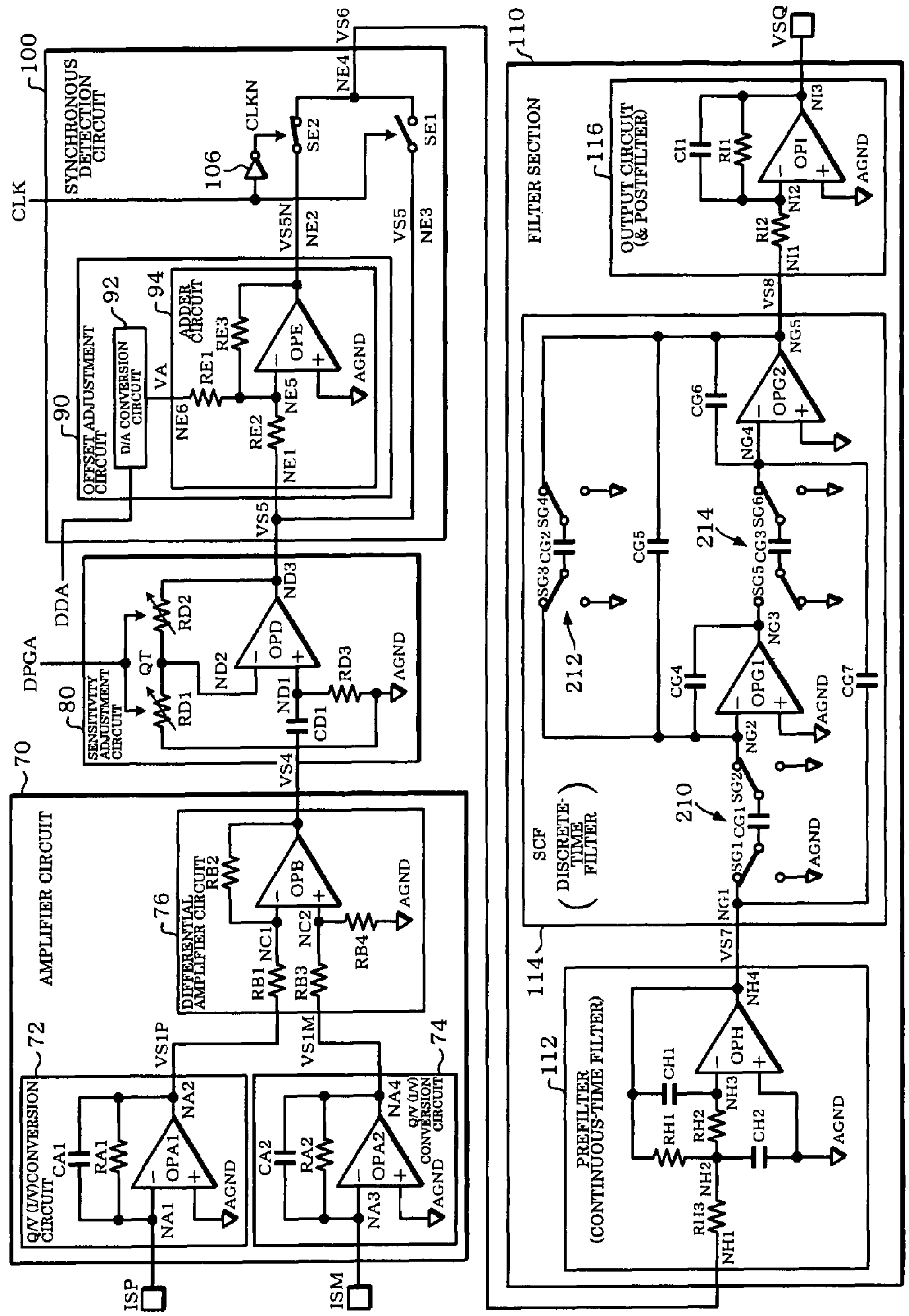

AMPLIFIER CIRCUIT
70
72
74
76
Q/V (I/V) CONVERSION CIRCUIT
DIFFERENTIAL AMPLIFIER CIRCUIT
ISP
ISM
VS1P
VS1M
VS4
80
SENSITIVITY ADJUSTMENT CIRCUIT
DPGA
DDA
VS5
90
OFFSET ADJUSTMENT CIRCUIT
92
D/A CONVERSION CIRCUIT
94
ADDER CIRCUIT
100
SYNCHRONOUS DETECTION CIRCUIT
CLK
CLKN
106
SE1
SE2
VS5N
VS6
110
FILTER SECTION
112
PREFILTER (CONTINUOUS-TIME FILTER)
114
SCF (DISCRETE-TIME FILTER)
210
212
214
116
OUTPUT CIRCUIT (& POSTFILTER)
VS7
VS8
VSQ
AGND

FIG. 21

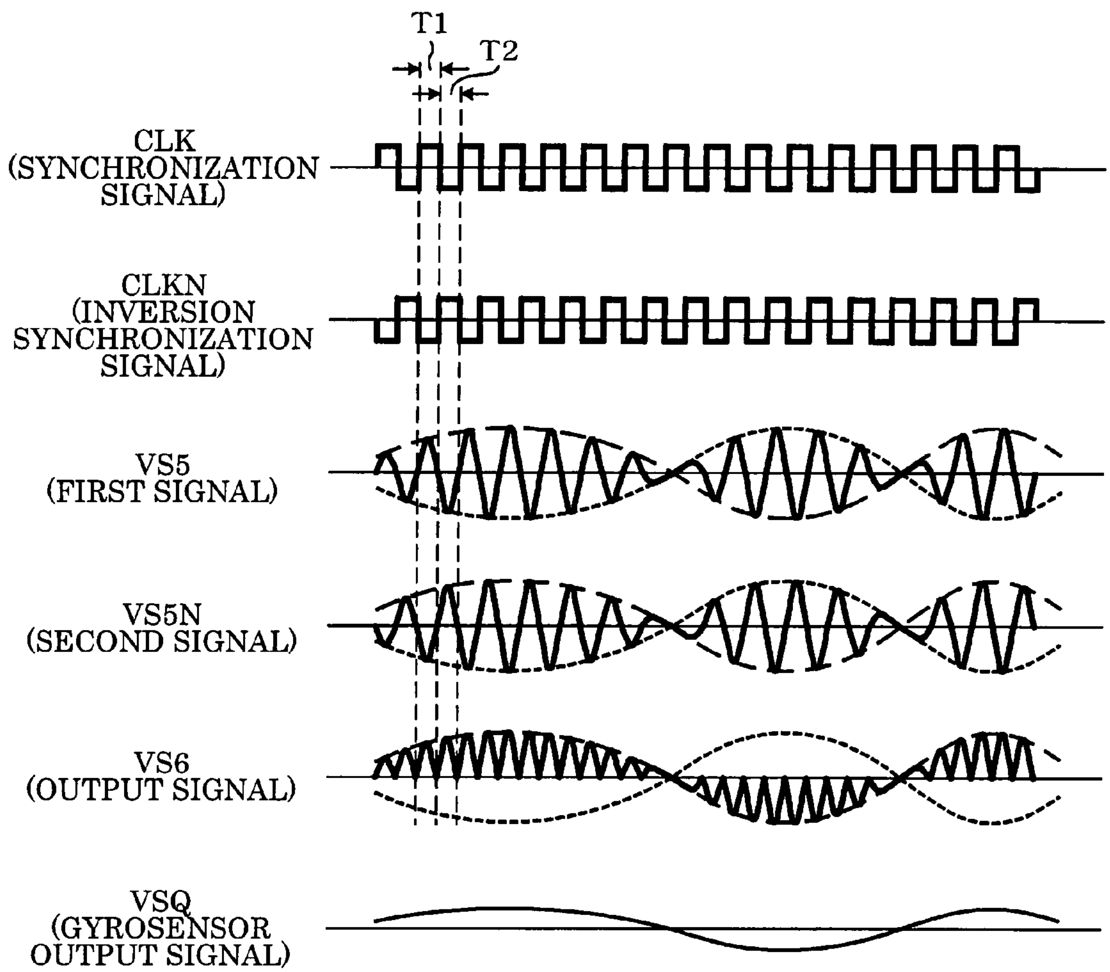

T1
T2
CLK
(SYNCHRONIZATION
SIGNAL)
CLKN
(INVERSION
SYNCHRONIZATION
SIGNAL)
VS5
(FIRST SIGNAL)
VS5N
(SECOND SIGNAL)
VS6
(OUTPUT SIGNAL)
VSQ
(GYROSENSOR
OUTPUT SIGNAL)

FIG. 22

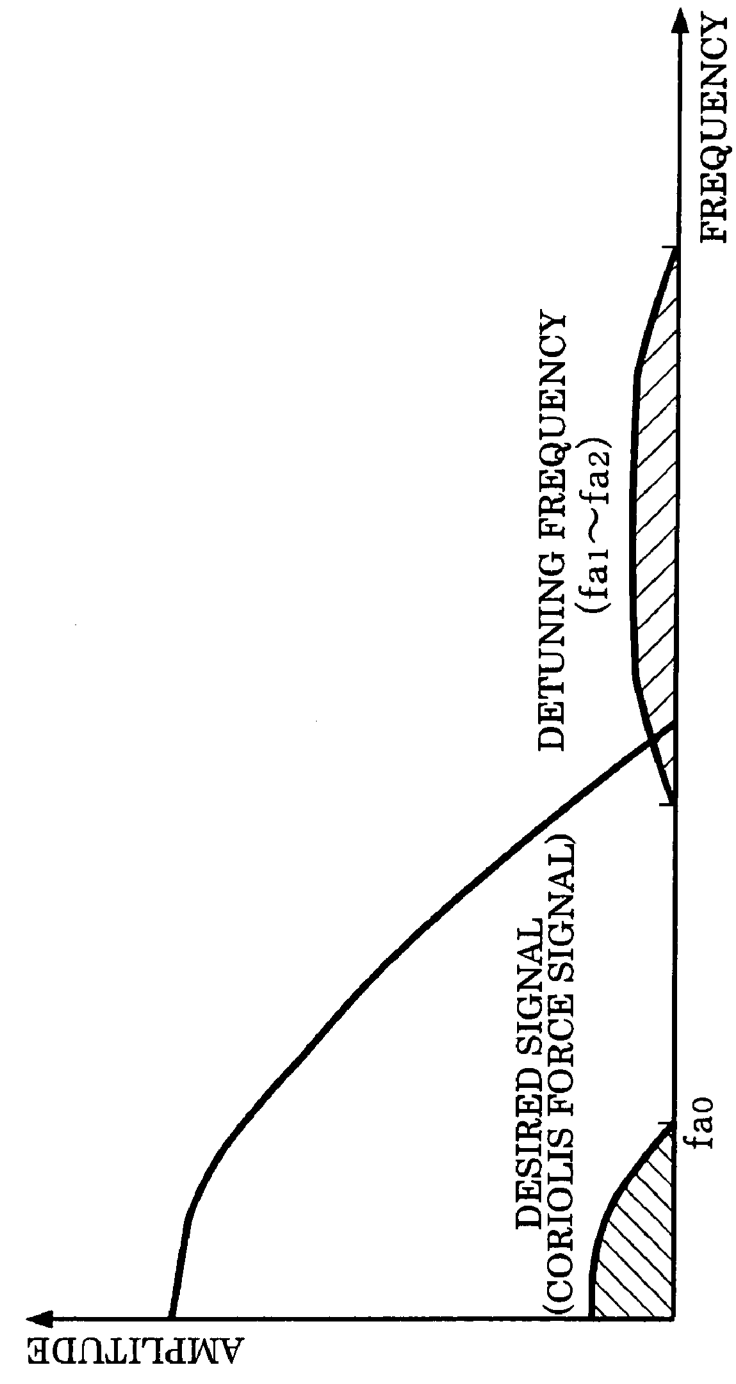
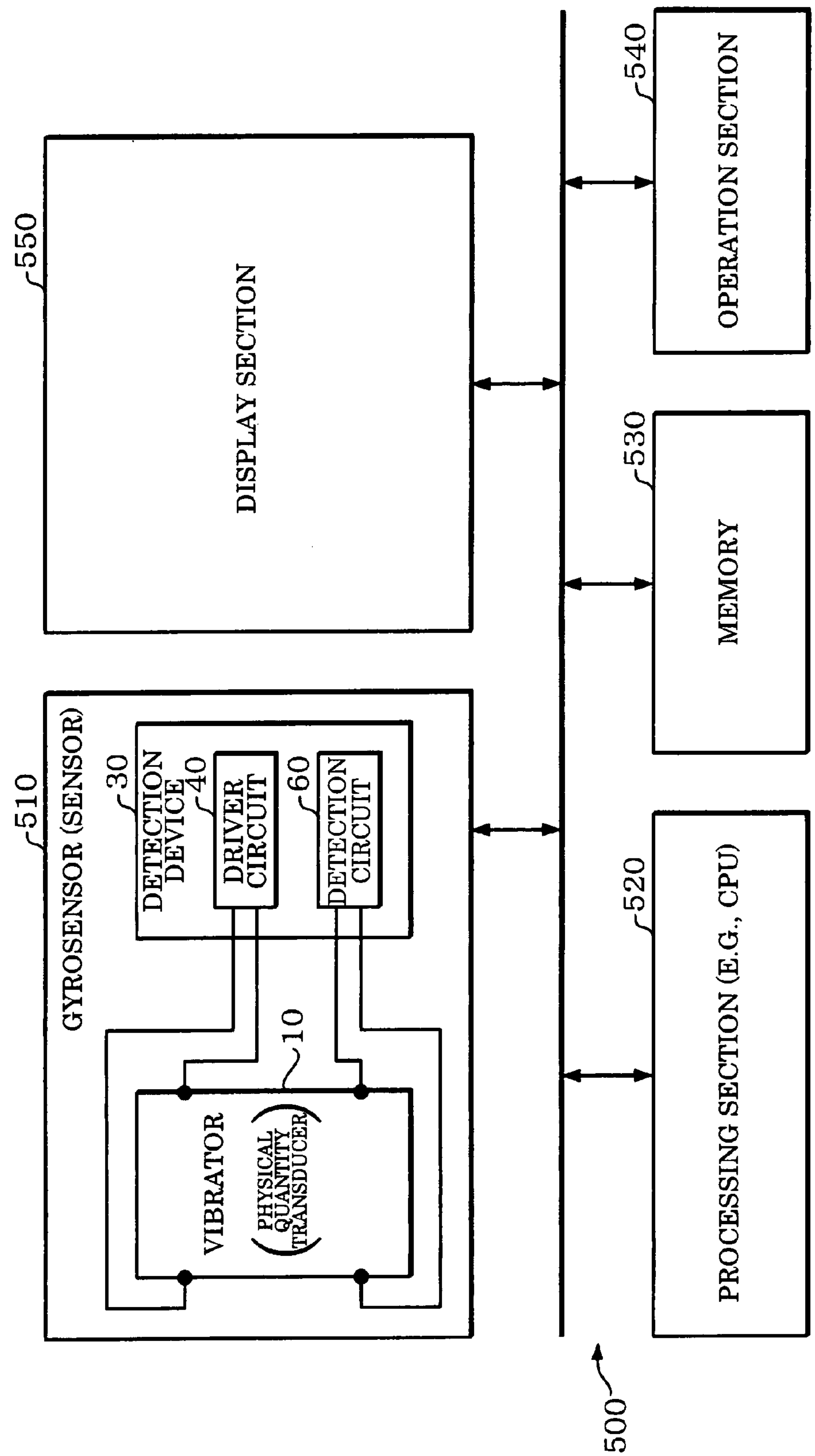

AMPLITUDE
FREQUENCY
DESIRED SIGNAL
(CORIOLIS FORCE SIGNAL)
f_{a0}
DETUNING FREQUENCY
(f_{a1}~f_{a2})

FIG. 23


550
DISPLAY SECTION
540
OPERATION SECTION
530
MEMORY
510
GYROSENSOR (SENSOR)
30
DETECTION DEVICE
40
DRIVER CIRCUIT
60
DETECTION CIRCUIT
10
VIBRATOR
(PHYSICAL QUANTITY TRANSDUCER)
520
PROCESSING SECTION (E.G., CPU)
500

REFERENCE VOLTAGE SUPPLY CIRCUIT, ANALOG CIRCUIT, AND ELECTRONIC INSTRUMENT

Japanese Patent Application No. 2006-305154 filed on Nov. 10, 2006, is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

The present invention relates to a reference voltage supply circuit, an analog circuit, and an electronic instrument.

The noise of a transistor forming an analog circuit is classified as thermal noise and flicker noise. Thermal noise predominantly occurs in a high frequency band and is proportional to the absolute temperature. Flicker noise predominantly occurs in a low frequency band. The noise level of flicker noise increases as the signal frequency decreases.

In analog circuits such as a radio-controlled clock receiver device and a gyrosensor detection device, a frequency is converted using a mixer or the like (e.g., JP-A-3-226620). Specifically, the frequency of a carrier signal is converted into the frequency of a desired signal, for example. Therefore, a high signal frequency and a low signal frequency exist in a mixed state as the small-amplitude amplification target of an operational amplifier forming an analog circuit.

In known a reference voltage supply circuit which supplies an analog reference voltage to analog circuits such as a radio-controlled clock receiver device and a gyrosensor detection device, an operational amplifier has not been optimally sized taking such a difference in signal frequency into consideration. Moreover, a reduction in noise and power consumption in combination has not been taken into consideration.

SUMMARY

According to one aspect of the invention, there is provided a reference voltage supply circuit comprising:

a first supply circuit that includes a reference-voltage first-type operational amplifier and supplies an analog reference voltage to a first analog reference voltage line; and

a second supply circuit that includes a reference-voltage second-type operational amplifier and supplies the analog reference voltage to a second analog reference voltage line;

when a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage first-type operational amplifier are respectively referred to as W**1***a* and L**1***a*, a bias current flowing through the differential section of the reference-voltage first-type operational amplifier is referred to as Ia, a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage second-type operational amplifier are respectively referred to as W**1***b* and L**1***b*, and a bias current flowing through the differential section of the reference-voltage second-type operational amplifier is referred to as Ib, W**1***b*×L**1***b*>W**1***a*×L**1***a* and Ia>Ib being satisfied.

According to another aspect of the invention, there is provided an analog circuit comprising:

the above reference voltage supply circuit,

a first circuit to which the analog reference voltage is supplied from the first supply circuit of the reference voltage supply circuit through the first analog reference voltage line; and

a second circuit to which the analog reference voltage is supplied from the second supply circuit of the reference voltage supply circuit through the second analog reference voltage line.

According to a further aspect of the invention, there is provided an electronic instrument comprising:

the above analog circuit; and

a processing section that performs processes based on detection information of the analog circuit.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. **1** shows a configuration example of a reference voltage supply circuit according to one embodiment of the invention and an analog circuit including the same.

FIG. **2** shows a configuration example of a radio-controlled clock receiver device.

FIG. **3** shows another configuration example of a radio-controlled clock receiver device.

FIGS. **4**A and **4**B are views illustrative of a noise analysis of an operational amplifier.

FIG. **5**A to **5**C are views illustrative of a noise reduction method according to one embodiment of the invention.

FIGS. **6**A to **6**C are views illustrative of the relationship among frequencies f**1** and f**2** and a corner frequency fcr.

FIGS. **7**A and **7**B are views illustrative of a method of setting a corner frequency fcr in first-type and second-type operational amplifiers.

FIGS. **8**A and **8**B are views illustrative of the relationship between an effective gate voltage and noise.

FIGS. **9**A and **9**B are views illustrative of simulation results according to one embodiment of the invention.

FIG. **10** is a bar graph for comparing one embodiment of the invention and a comparative example in terms of the noise level.

FIGS. **11**A and **11**B show layout examples of first-type and second-type operational amplifiers.

FIG. **12** shows a layout example of a third-type operational amplifier.

FIG. **13** shows a detailed configuration example of a reference voltage supply circuit.

FIG. **14** shows a configuration example of a detection device.

FIGS. **15**A and **15**B are views illustrative of a vibrator.

FIGS. **16**A to **16**C are views illustrative of a frequency spectrum.

FIG. **17** shows a first modification of a detection device.

FIG. **18** shows a layout example of a detection circuit.

FIG. **19** show another configuration example of a reference voltage supply circuit.

FIG. **20** shows a second modification of a detection device.

FIG. **21** shows a signal waveform example illustrative of synchronous detection.

FIG. **22** is a view illustrative of a detuning frequency.

FIG. **23** shows a configuration example of an electronic instrument and a gyrosensor.

DETAILED DESCRIPTION OF THE EMBODIMENT

Aspects of the invention may provide a reference voltage supply circuit, an analog circuit, and an electronic instrument capable of reducing noise and power consumption.

According to one embodiment of the invention, there is provided a reference voltage supply circuit comprising:

a first supply circuit that includes a reference-voltage first-type operational amplifier and supplies an analog reference voltage to a first analog reference voltage line; and

a second supply circuit that includes a reference-voltage second-type operational amplifier and supplies the analog reference voltage to a second analog reference voltage line;

when a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage first-type operational amplifier are respectively referred to as $W1a$ and $L1a$, a bias current flowing through the differential section of the reference-voltage first-type operational amplifier is referred to as Ia, a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage second-type operational amplifier are respectively referred to as $W1b$ and $L1b$, and a bias current flowing through the differential section of the reference-voltage second-type operational amplifier is referred to as Ib, $W1b \times L1b > W1a \times L1a$ and $Ia > Ib$ being satisfied.

According to this embodiment, the first supply circuit of the reference voltage supply circuit supplies the analog reference voltage to the first analog reference voltage line using the first-type operational amplifier. The second supply circuit supplies the analog reference voltage to the second analog reference voltage line using the second-type operational amplifier.

The WL product $W1a \times L1a$ of the differential-stage transistor of the first-type operational amplifier and the WL product $W1b \times L1b$ of the differential-stage transistor of the second-type operational amplifier satisfy the relationship $W1b \times L1b > W1a \times L1a$. Therefore, since the WL product $W1b \times L1b$ of the second-type operational amplifier can be increased, flicker noise of the second-type operational amplifier can be reduced. This minimizes flicker noise superimposed on the analog reference voltage supplied from the second supply circuit. On the other hand, since the WL product $W1a \times L1a$ of the first-type operational amplifier can be reduced, a situation can be prevented in which the circuit area of the first-type operational amplifier is unnecessarily increased.

The bias current Ia of the differential section of the first-type operational amplifier and the bias current Ib of the differential section of the second-type operational amplifier satisfy the relationship $Ia > Ib$. Therefore, since the bias current Ia of the first-type operational amplifier can be increased, thermal noise of the first-type operational amplifier can be reduced. This minimizes thermal noise superimposed on the analog reference voltage supplied from the first supply circuit. On the other hand, since the bias current Ib of the second-type operational amplifier can be reduced, a situation in which the current consumption of the second-type operational amplifier is unnecessarily increased can be prevented.

In the reference voltage supply circuit according to this embodiment,

when a frequency of an amplification target signal of a first circuit to which the analog reference voltage is supplied from the first supply circuit is referred to as $f1$, a frequency of an amplification target signal of a second circuit to which the analog reference voltage is supplied from the second supply circuit is referred to as $f2$, and a corner frequency of flicker noise and thermal noise in frequency-noise characteristics is referred to as fcr, the reference-voltage first-type operational amplifier may satisfy $f1-fcr<fcr-f2$, and the reference-voltage second-type operational amplifier may satisfy $fcr-f2<f1-fcr$.

If the relationship $f1-fcr<fcr-f2$ is satisfied, the corner frequency fcr can be brought close to the frequency $f1$, whereby the noise and the power consumption of the operational amplifier can be reduced. If the relationship $fcr-f2<f1-fcr$ is satisfied, the corner frequency fcr can be brought close to the frequency $f2$, whereby the noise and the area of the operational amplifier can be reduced.

In the reference voltage supply circuit according to this embodiment,

when a channel length of an active-load-stage transistor of the differential section of the reference-voltage second-type operational amplifier is referred to as $L3b$, $L1b<L3b$ may be satisfied.

This further reduces the flicker noise of the second-type operational amplifier.

In the reference voltage supply circuit according to this embodiment,

when a WL ratio of the differential-stage transistor of the reference-voltage first-type operational amplifier is referred to as $RT1a$ and a WL ratio of an active-load-stage transistor of the reference-voltage first-type operational amplifier is referred to as $RT3a$, $RT1a>RT3a$ may be satisfied.

This further reduces the thermal noise of the first amplifier circuit.

In the reference voltage supply circuit according to this embodiment,

when an effective gate voltage of the differential-stage transistor of the reference-voltage second-type operational amplifier is referred to as Veff, a drain-source current is referred to as Ids, a mobility is referred to as μ, a gate capacitance per unit area is referred to as Cox, a WL ratio is referred to as $RT1b$, a Boltzmann constant is referred to as k, an absolute temperature is referred to as T, an amount of electronic charge is referred to as q, and a process variation parameter is referred to as P ($P>1$), the WL ratio $RT1b$ may be set at a value satisfying the relationship

$$P\times(k\times T/q)>Veff\{2\times Ids/(\mu\times Cox\times RT1b)\}^{1/2}>k\times T/q.$$

According to this configuration, since the differential-stage transistor of the second-type operational amplifier can be prevented from operating in the weak inversion region or at the boundary between the weak inversion region and the strong inversion region, an increase in flicker noise due to an excessive increase in the WL ratio $RT1b$ can be minimized.

In the reference voltage supply circuit according to this embodiment,

when the area of an arrangement region of the differential-stage transistor among elements forming the reference-voltage second-type operational amplifier is referred to as Sdf and the area of an arrangement region of the elements forming the reference-voltage second-type operational amplifier other than the differential-stage transistor is referred to as Sre, $Sdf>Sre$ may be satisfied.

This enables the differential-stage transistor with a large WL product to be disposed in the arrangement region with an area of Sdf, whereby flicker noise can be reduced.

In the reference voltage supply circuit according to this embodiment,

the differential-stage transistor of the reference-voltage second-type operational amplifier may include J ($J>2$) transistors connected in parallel; and

the J transistors connected in parallel may be disposed in the arrangement region of the differential-stage transistor.

This enables the WL ratio to be increased while increasing the WL product of the differential-stage transistor, whereby flicker noise can be efficiently reduced.

In the reference voltage supply circuit according to this embodiment,

the active-load-stage transistor of the reference-voltage second-type operational amplifier may include I ($J>I>2$) transistors connected in parallel; and

the J transistors forming the differential-stage transistor may be arranged along a direction X, and the I transistors forming the active-load-stage transistor may be arranged along the direction X on a direction Y side of the J transistors.

This enables the J transistors forming the differential-stage transistor and the J transistors forming the active-load-stage transistor to be efficiently disposed symmetrically, whereby the layout efficiency can be increased.

In the reference voltage supply circuit according to this embodiment,

the first supply circuit may be a circuit which performs voltage impedance conversion using the reference-voltage first-type operational amplifier; and

the second supply circuit may be a circuit which performs voltage impedance conversion using the reference-voltage second-type operational amplifier.

This ensures that the analog reference voltage at a stable potential can be supplied.

The reference voltage supply circuit according to this embodiment may further comprise:

a third supply circuit that is provided in a preceding stage of the first and second supply circuits, includes a reference-voltage third-type operational amplifier, and supplies a voltage to the first and second supply circuits;

when a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage third-type operational amplifier are respectively referred to as $W1c$ and $L1c$ and a bias current which flows through the differential section of the reference-voltage third-type operational amplifier is referred to as Ic, $W1c \times L1c > W1a \times L1a$ and Ic>Ib may be satisfied.

This minimizes thermal noise and flicker noise of the output voltage of the third supply circuit. This minimizes a situation in which the thermal noise of the output voltage is transmitted to the first analog reference voltage line through the first supply circuit, or the flicker noise of the output voltage is transmitted to the second analog reference voltage line through the second supply circuit.

In the reference voltage supply circuit according to this embodiment, $W1c \times L1c > W1b \times L1b$ and Ic>Ia may be satisfied.

According to another embodiment of the invention, there is provided an analog circuit comprising:

one of the above reference voltage supply circuits,

a first circuit to which the analog reference voltage is supplied from the first supply circuit of the reference voltage supply circuit through the first analog reference voltage line; and

a second circuit to which the analog reference voltage is supplied from the second supply circuit of the reference voltage supply circuit through the second analog reference voltage line.

According to this embodiment, the thermal noise of the analog reference voltage supplied to the first circuit from the first supply circuit can be reduced, and the flicker noise of the analog reference voltage supplied to the second circuit from the second supply circuit can be reduced. Therefore, the thermal noise and the flicker noise of the first and second circuits can be reduced, whereby the signal-to-noise ratio (SNR) of the analog circuit can be increased.

The analog circuit according to this embodiment may further comprise:

a mixer that mixes a signal with a specific frequency into a signal including a desired signal;

the first circuit may be a circuit provided on a preceding stage of the mixer; and

the second circuit may be a circuit provided on a subsequent stage of the mixer.

When providing such a mixer, the signal frequency in the first circuit in the preceding stage of the mixer differs from the signal frequency in the second circuit in the subsequent stage of the mixer. According to this embodiment, noise and power consumption can be reduced by selectively using the first-type operational amplifier and the second-type operational amplifier in the reference voltage supply circuit which supplies the analog reference voltage to the first and second circuits.

In the analog circuit according to this embodiment,

the first circuit may be a first amplifier circuit which amplifies an input signal; and

the reference voltage supply circuit may supply the analog reference voltage to the first amplifier circuit through the first analog reference voltage line.

This enables the thermal noise of the first amplifier circuit to be reduced, whereby the noise of the analog circuit can be reduced.

In the analog circuit according to this embodiment,

the second circuit may be a second amplifier circuit that amplifies the mixed signal from the mixer or a filter section that filters the mixed signal from the mixer; and

the reference voltage supply circuit may supply the analog reference voltage to the second amplifier circuit or the filter section through the second analog reference voltage line.

This enables the flicker noise of the second amplifier circuit or the filter section to be reduced, whereby the noise of the analog circuit can be reduced.

According to a further embodiment of the invention, there is provided an electronic instrument comprising:

one of the above analog circuits; and

a processing section that performs processes based on detection information of the analog circuit.

Preferred embodiments of the invention are described below in detail. Note that the embodiments described below do not in any way limit the scope of the invention defined by the claims laid out herein. Note that all elements of the embodiments described below should not necessarily be taken as essential requirements for the invention. For example, the following description is given taking a radio-controlled clock receiver device or a gyrosensor detection device as a reference voltage supply circuit to which the invention is applied. Note that the invention is not limited thereto.

1. Configuration of Reference Voltage Supply Circuit and Analog Circuit

FIG. **1** shows a configuration example of a reference voltage supply circuit **20** according to this embodiment and an analog circuit (analog front-end circuit) **300** including the reference voltage supply circuit **20**. The analog circuit **300** includes a first circuit **310** and a second circuit **320**.

The first circuit **310** includes a circuit of which the frequency of the amplification target signal (small-signal amplification target signal of operational amplifier) is a first frequency. The second circuit **320** is a circuit of which the frequency of the amplification target signal is a second frequency lower than the first frequency.

For example, an input signal (reception signal or sensor signal) with the first frequency from an antenna, a sensor, or the like is input to the first circuit **310**. The first circuit **310** includes an amplifier circuit, for example. The amplifier circuit amplifies the input signal. In this case, the input signal (carrier signal) as the amplification target signal is a signal with the high first frequency.

A mixer (frequency conversion circuit) **322** may be provided between the first circuit **310** and the second circuit **320**.

Specifically, the first circuit **310** may be a circuit provided in the preceding stage of the mixer **322**, and the second circuit **320** may be a circuit provided in the subsequent stage of the mixer **322**. The mixer **322** mixes a signal with a given frequency (e.g., station frequency signal or synchronization signal) into a signal including a desired signal.

A signal of which the frequency has been converted into the second frequency due to mixing (frequency conversion) of the mixer **322** is input to the second circuit **320**. An amplifier circuit, a filter section, or an output circuit of the second circuit **320** subjects the signal with the second frequency (amplification target signal) to small-amplitude amplification.

The reference voltage supply circuit **20** supplies a voltage AGND (analog reference voltage in a broad sense) to the first circuit **310** and the second circuit **320**. The reference voltage supply circuit **20** includes a first supply circuit **21** and a second supply circuit **22**. The first supply circuit **21** supplies the voltage AGND (analog ground) to the first circuit **310**. The second supply circuit **22** supplies the voltage AGND to the second circuit **320**. The first supply circuit **21** includes a reference-voltage first-type operational amplifier OP**1**, and the second supply circuit **22** includes a reference-voltage second-type operational amplifier OP**2**.

The reference-voltage first-type operational amplifier OP**1** is an operational amplifier of which the thermal noise at the first frequency (e.g., carrier frequency, modulation frequency, or resonance frequency) is lower than that of the second-type operational amplifier OP**2**, for example. The reference-voltage second-type operational amplifier OP**2** is an operational amplifier of which the flicker noise at the second frequency (e.g., frequency of a desired signal carried by a carrier signal or maximum frequency in a frequency band of a desired signal) is lower than that of the first-type operational amplifier OP**1**.

Specifically, the frequency (e.g., several tens of kilohertz to several hundreds of kilohertz) of the amplification target signal of the first circuit **310** (amplification target signal of the operational amplifier included in the first circuit **310**) is referred to as f**1**, the frequency (e.g., several hertz to several hundreds of hertz) of the amplification target signal of the second circuit **320** (amplification target signal of the operational amplifier included in the first circuit **320**) is referred to as f**2**, and the corner frequency of flicker noise and thermal noise is referred to as fcr. In this case, the first-type operational amplifier OP**1** satisfies the relationship $f1-fcr<fcr-f2$, for example. Specifically, the first-type operational amplifier OP**1** is sized so that the first frequency f**1** is set to be close to the corner frequency fcr. The second-type operational amplifier OP**2** satisfies the relationship $fcr-f2<f1-fcr$, for example. Specifically, the second-type operational amplifier OP**2** is sized so that the second frequency f**2** is set to be close to the corner frequency fcr.

The channel width and the channel length of the differential-stage transistor of the differential section of the first-type operational amplifier OP**1** are respectively referred to as W**1***a* and L**1***a*, and the bias current (current value) flowing through the differential section is referred to as Ia. The channel width and the channel length of the differential-stage transistor of the differential section of the second-type operational amplifier OP**2** are respectively referred to as W**1***b* and L**1***b*, and the bias current flowing through the differential section is referred to as Ib. In this case, the relationship $W1b\times L1b>W1a\times L1a$ and Ia>Ib is satisfied, for example.

As shown in FIG. **1**, the reference voltage supply circuit **20** may include a third supply circuit **23**. The third supply circuit **23** is provided in the preceding stage of the first and second supply circuits **21** and **22**, and supplies an output voltage V3Q to the first and second supply circuits **21** and **22**. The first and second supply circuits **21** and **22** subject the output voltage V3Q from the third supply circuit **23** to impedance conversion and outputs the voltage AGND.

The third supply circuit **23** includes a reference-voltage third-type operational amplifier OP**3**. The reference-voltage third-type operational amplifier OP**3** is an operational amplifier of which the thermal noise at the frequency of the carrier signal is lower than that of the second-type operational amplifier OP**2** (or the first-type operational amplifier OP**1**) and the flicker noise at the frequency of the desired signal is lower than that of the first-type operational amplifier OP**1** (or the second-type operational amplifier OP**2**). For example, when the channel width and the channel length of the differential-stage transistor of the differential section of the third-type operational amplifier OP**3** are respectively referred to as W**1***c* and L**1***c*, and the bias current flowing through the differential section is referred to as Ic, the relationship $W1c\times L1c>W1a\times L1a$ and Ic>Ib is satisfied. Alternatively, the relationship $W1c\times L1c>W1b\times L1b$ and Ic>Ia may be satisfied.

FIGS. **2** and **3** show configuration examples of a radio-controlled clock receiver device as an example of the analog circuit **300**. The receiver device is not limited to the configurations shown in FIGS. **2** and **3**. Various modification may be made such as omitting some elements or adding another element.

The receiver device shown in FIG. **2** is an example of a direct-conversion receiver device. At present, a long-frequency standard radio wave containing a time code (time data) is transmitted in each country (e.g., Japan, Germany, and the United Kingdom). In Japan, a long-frequency standard radio wave (40 KHz and 60 KHz) amplitude-modulated by the time code is transmitted from two stations. Specifically, the time data is transmitted as binary data in cycles of 60 seconds. The radio-controlled clock receives such time code radio waves and corrects the time data of a clock circuit. Therefore, the receiver device of the radio-controlled clock extracts a signal at a desired frequency by detecting and demodulating the received radio waves to obtain the time code.

In FIG. **2**, an antenna **330** formed using a bar antenna or the like receives the long-frequency standard radio wave, and the received radio wave is converted into an electric signal and output. An amplifier circuit (RF amplifier circuit) **332** amplifies and outputs the signal from the antenna **330**. A filter section **334** has high-pass filter frequency characteristics, for example. The filter section **334** filters the signal from the amplifier circuit **332**.

A mixer (frequency conversion circuit) **336** mixes a signal with a local oscillation frequency from a local oscillation circuit **344** into the signal from the filter section **334** to directly convert the signal into a baseband signal (several hertz) (direct conversion).

The amplifier circuit **338** amplifies the signal from the mixer **336**. A filter section **340** has low-pass filter frequency characteristics, for example. The filter section **340** filters the signal from the amplifier circuit **338**. A demodulation section **342** demodulates the signal from the filter section **340**, and outputs the time code obtained by demodulation. The radio-controlled clock corrects the time data using the time code.

The receiver device shown in FIG. **3** is an example of a superheterodyne receiver device. An amplifier circuit **352** amplifies a signal from an antenna **350**. A filter section **354** has band-pass filter frequency characteristics, for example. The filter section **354** filters the signal from the amplifier circuit **352**.

A mixer **356** mixes a signal with a local oscillation frequency from a local oscillation circuit **364** into the signal from the filter section **354** to generate a signal with an intermediate frequency (several hundreds of hertz) (superheterodyne conversion).

A filter section **358** has band-pass filter frequency characteristics, for example. The filter section **358** filters the signal from the mixer **356** so that a frequency component within a specific frequency range around the intermediate frequency passes through and a frequency component outside the specific frequency range is blocked. A detection circuit **360** detects (e.g., envelope detection) the signal from the filter section **358**. A demodulation section **362** demodulates the detection signal from the detection circuit **360**, and outputs the time code obtained by demodulation.

In FIG. **2**, the amplifier circuit **332** (first amplifier circuit) and the filter section **334** correspond to the first circuit **310** shown in FIG. **1**, for example. The first supply circuit **21** supplies the voltage AGND (analog reference voltage) to the amplifier circuit **332** and the filter section **334** through an AGND line (analog reference voltage line) AGL**1**.

In FIG. **2**, the amplifier circuit **338** (second amplifier circuit) and the filter section **340** correspond to the second circuit **320** shown in FIG. **1**, for example. The second supply circuit **22** supplies the voltage AGND to the amplifier circuit **338** and the filter section **340** through an AGND line AGL**2**.

In FIG. **3**, the amplifier circuit **352** and the filter section **354** correspond to the first circuit **310** shown in FIG. **1**, for example. The first supply circuit **21** supplies the voltage AGND to the amplifier circuit **352** and the filter section **354** through the AGND line AGL**1**.

In FIG. **3**, the filter section **358** and the detection circuit **360** correspond to the second circuit **320** shown in FIG. **1**, for example. The second supply circuit **22** supplies the voltage AGND to the filter section **358** and the detection circuit **360** through the AGND line AGL**2**.

The analog circuit **300** to which the voltage AGND (analog reference voltage) is supplied from the reference voltage supply circuit **20** according to this embodiment is not limited to the radio-controlled clock receiver devices shown in FIGS. **2** and **3**. For example, the analog circuit **300** may be applied to an infrared remote control receiver device, or may be applied to detection devices of various sensors such as a gyrosensor described later.

The first circuit **310** shown in FIG. **1** may include the first-type operational amplifier OP**1**, and the second circuit **320** may include the second-type operational amplifier OP**2**. Likewise, the amplifier circuit **332** and the filter section **334** shown in FIG. **2** and the amplifier circuit **352** and the filter section **354** shown in FIG. **3** may include the first-type operational amplifier OP**1**. The amplifier circuit **338** and the filter section **340** shown in FIG. **2** and the filter section **358** and the detection circuit **360** shown in FIG. **3** may include the second-type operational amplifier OP**2**. This reduces the thermal noise and flicker noise of these circuits, whereby the SNR can be further increased.

2. Noise Reduction Method

2.1 Noise Analysis

FIG. **4**A shows a configuration example of an operational amplifier used in this embodiment. The operational amplifier includes a differential section **200** and an output section **210**.

The differential section **200** includes differential-stage transistors M**1** and M**2** and active-load-stage transistors M**3** and M**4**. The differential section **200** also includes a bias-stage transistor M**5**. The differential-stage transistors M**1** and M**2** are provided between a node N**1** and nodes N**2** and N**3**, respectively. Differential input signals IM and IP are input to the gates of the differential-stage transistors M**1** and M**2**. The active-load-stage transistors M**3** and M**4** are provided between the nodes N**2** and N**3** and a power supply AGND (first power supply), respectively. The node N**2** is connected with the gates of the active-load-stage transistors M**3** and M**4**. The bias-stage transistor M**5** is provided between a power supply VDD (second power supply) and the node N**1**. A bias node N**4** of a bias circuit **212** formed of a transistor M**8** and a current source IS is connected with the gate of the bias-stage transistor M**5**. This allows a bias current IBD corresponding to a bias current IBS of the bias circuit **212** to flow through the differential section **200**.

The output section **210** includes a drive-stage transistor M**6** and a bias-stage transistor M**7** provided between the power supply VDD and the power supply AGND. The output node N**3** of the differential section **200** is connected with the gate of the drive-stage transistor M**6**, and the bias node N**4** is connected with the gate of the bias-stage transistor M**7**. A phase-compensation capacitor CF and a resistor RF are provided between the nodes N**3** and N**5**.

The configuration of the operational amplifier according to this embodiment is not limited to the configuration shown in FIG. **4**A. FIG. **4**A shows an example in which the differential-stage transistors M**1** and M**2** and the bias-stage transistor M**5** are P-type transistors and the active-load-stage transistors M**3** and M**4** are N-type transistors. Note that the transistors M**1**, M**2**, and M**5** may be N-type transistors and the transistors M**3** and M**4** may be P-type transistors. Modifications may also be made such as omitting some of the elements (transistor and capacitor) shown in FIG. **4**A or adding another element.

Noise analysis on the operational amplifier shown in FIG. **4**A is described below. FIG. **4**B shows an small-signal equivalent circuit of the transistor. Since noise is expressed in units of V^2 (V^2/Hz), the equivalent circuit shown in FIG. **4**B is also expressed in units of V^2. In the equivalent circuit shown in FIG. **4**B, in order to calculate the input-referred noise (gate-referred noise) of the transistor, a voltage source with a noise of $Svg=Vn^2$ is provided at the gate of the transistor. A current source of gm^2 (Vgs^2+Vn^2) and a resistor of $1/gds^2$ are provided between the drain and the source.

As shown in FIG. **5**A, noise is classified as flicker noise (1/f noise) and thermal noise. Flicker noise occurs when electrons are trapped by or released from dangling bonds at the interface between a gate oxide film and a silicon substrate. Flicker noise increases as the frequency decreases. On the other hand, thermal noise occurs due to random movement of electrons when the channel region of the transistor is considered to be a resistor. Thermal noise is proportional to the absolute temperature.

In the input-referred noise equivalent circuit shown in FIG. **4**B, flicker noise and thermal noise are respectively calculated by the following equations (1) and (2).

$$Vn^2 = \frac{K}{Cox \times W \times L \times f} \tag{1}$$

$$Vn^2 = \frac{8}{3} \times \frac{k \times T}{g_m} \tag{2}$$

In the equation (1), Cox represents the gate capacitance of the transistor per unit area, W represents the channel width, L represents the channel length, f represents the frequency, and K represents the flicker noise constant depending on the manufacturing process. In the equation (2), gm represents the transconductance, k represents the Boltzmann constant, and T represents the absolute temperature.

In this embodiment, the transfer function is calculated by replacing the operational amplifier circuit shown in FIG. **4**A with the equivalent circuit shown in FIG. **4**B. In this case, only the higher-order terms accounting for 99% of the whole are derived by numerical analysis on the assumption that the size (W and L), the noise level, and the drain-source current of all the transistors of the operational amplifier are the same. The noise Svg (noise spectrum) of the operational amplifier is calculated by the following equation (3).

$$Svg = V_{n1}^2 + V_{n2}^2 + \frac{g_{m3}^2 \times V_{n3}^2}{g_{m1}^2} + \frac{g_{m3}^2 \times V_{n4}^2}{g_{m1}^2} \tag{3}$$

In the equation (3), Vn**1**, Vn**2**, Vn**3**, and Vn**4** represent the gate-noise voltages of the transistors M**1**, M**2**, M**3**, and M**4** shown in FIG. **4**A, and gm**1**, gm**2**, gm**3**, and gm**4** represent the transconductances of the transistors M**1**, M**2**, M**3**, and M**4**.

As is clearly from the numerical analysis result of the equation (3), most of the noise Svg of the operational amplifier is caused by noise of the differential-stage transistors M**1** and M**2** and the active-load-stage transistors M**3** and M**4** of the differential section **200** shown in FIG. **4**A. Therefore, the channel widths W and the channel lengths L of the transistors M**1**, M**2**, M**3**, and M**4** may be optimized when sizing the operational amplifier.

Flicker noise is analyzed as follows. The gate-noise voltages Vn**1**, Vn**2**, Vn**3**, and Vn**4** with regard to flicker noise are calculated by the following equations (4), (5), (6), and (7) from the equation (1).

$$V_{n1} = \left(\frac{K_p}{C_{OX} \times W1 \times L1 \times f}\right)^{\frac{1}{2}} \tag{4}$$

$$V_{n2} = \left(\frac{K_p}{C_{OX} \times W1 \times L1 \times f}\right)^{\frac{1}{2}} \tag{5}$$

$$V_{n3} = \left(\frac{K_n}{C_{OX} \times W3 \times L3 \times f}\right)^{\frac{1}{2}} \tag{6}$$

$$V_{n4} = \left(\frac{K_n}{C_{OX} \times W3 \times L3 \times f}\right)^{\frac{1}{2}} \tag{7}$$

In the equations (4) to (7), W**1** and L**1** respectively represent the channel width and the channel length of the differential-stage transistors M**1** and M**2**, and W**3** and L**3** respectively represent the channel width and the channel length of the active-load-stage transistors M**3** and M**4**. Note that the equations (4) to (7) are given on the assumption that the channel width W**2** and the channel length L**2** of the transistor M**2** are the same as the channel width W**1** and the channel length L**1** of the transistor M**1**, and the channel width W**4** and the channel length L**4** of the transistor M**4** are the same as the channel width W**3** and the channel length L**3** of the transistor M**3**. Kp and Kn respectively represent the process-dependent constants of the P-type transistor and the N-type transistor.

The transconductance gm**1** (=gm**2**) of the differential-stage transistors M**1** and M**2** and the transconductance gm**3** (=gm**4**) of the active-load-stage transistors M**3** and M**4** are calculated by the following equations (8) and (9).

$$g_{m1} = \left(\frac{2\mu_p \times C_{OX} \times W1}{L1} \times Ids\right)^{\frac{1}{2}} \tag{8}$$

$$g_{m3} = \left(\frac{2\mu_n \times C_{OX} \times W3}{L3} \times Ids\right)^{\frac{1}{2}} \tag{9}$$

In the equations (8) and (9), μp and μn respectively represent the mobilities of the P-type transistor and the N-type transistor, and Ids represents the drain-source current of the transistor, provided that the transistors M**1** to M**4** have the same drain-source current Ids.

Flicker noise SvgFlc of the operational amplifier is calculated by the following equation (10) by substituting the equations (4) to (9) into the equation (3).

$$SvgFlc = \frac{2K_p}{C_{OX} \times W1 \times L1 \times f} + \frac{2L1 \times \mu_n \times K_n}{\mu_p \times W1 \times L3^2 \times C_{OX} \times f} \tag{10}$$

Thermal noise is analyzed as follows. The gate-noise voltages Vn**1**, Vn**2**, Vn**3**, and Vn**4** with regard to thermal noise are calculated by the following equations (11), (12), (13), and (14) from the equation (2).

$$V_{n1} = \left(\frac{8}{3} \times \frac{k \times T}{g_{m1}}\right)^{\frac{1}{2}} \tag{11}$$

$$V_{n2} = \left(\frac{8}{3} \times \frac{k \times T}{g_{m1}}\right)^{\frac{1}{2}} \tag{12}$$

$$V_{n3} = \left(\frac{8}{3} \times \frac{k \times T}{g_{m3}}\right)^{\frac{1}{2}} \tag{13}$$

$$V_{n4} = \left(\frac{8}{3} \times \frac{k \times T}{g_{m3}}\right)^{\frac{1}{2}} \tag{14}$$

Thermal noise SvgThm of the operational amplifier is calculated by the following equation (15) by substituting the equations (11) to (14) into the equation (3).

$$SvgThm = \frac{16}{3} \times \frac{k \times T}{g_{m1}} + \frac{16}{3} \times \frac{g_{m3} \times k \times T}{g_{m1}^2} \tag{15}$$

The thermal noise SvgThm of the operational amplifier is calculated by the following equation (16) by substituting the equations (8) and (9) into the equation (15).

$$SvgThm = \frac{8}{3} \times \frac{k \times T \times \sqrt{2} \times \sqrt{L1}}{\sqrt{Ids} \times \sqrt{\mu_p \times C_{OX}} \times \sqrt{W1}} + \frac{8}{3} \times \frac{k \times T \times \sqrt{2} \times L1 \times \sqrt{\mu_n \times C_{OX}} \times \sqrt{W3}}{\sqrt{Ids} \times \sqrt{L3} \times \mu_p \times C_{OX} \times W1} \tag{16}$$

When excluding the constant determined by the natural world and the constant which depends only on the process from the equation (10) relating to the flicker noise SvgFlc and the equation (16) relating to the thermal noise SvgThm, W**1**, W**3**, L**1**, L**3**, and Ids are variables which can be managed in the design stage. Therefore, the flicker noise SvgFlc is reduced by satisfying the following items in view of the equation (10).

(P1) Increase the WL product W1×L1 (gate area) of the differential-stage transistors M1 and M2 as much as possible. This reduces the first term of the equation (10), whereby the flicker noise SvgFlc is reduced.

(P2) Reduce the ratio L1/L3 as much as possible. Specifically, the channel lengths L1 and L3 are set so that L1<L3, for example. This reduces the second term of the equation (10), whereby the flicker noise SvgFlc is reduced. As a result, the WL product W3×L3 of the active-load-stage transistors M3 and M4 increases.

(P3) The flicker noise SvgFlc is independent of the drain-source current Ids. Therefore, when taking only the flicker noise into consideration, power consumption can be reduced by reducing the drain-source current Ids.

As is clear from the above description, the flicker noise SvgFlc and power consumption can be reduced by increasing the WL product W1×L1 of the differential-stage transistor and reducing the bias current IBD (Ids) flowing through the differential section.

The thermal noise SvgThm is reduced by satisfying the following items in view of the equation (16).

(Q1) Increase the current Ids (IBD) as much as possible. This reduces the first and second terms of the equation (16), whereby the thermal noise SvgThm is reduced.

(Q2) Increase the WL ratio RT1=W1/L1 of the differential-stage transistors M1 and M2 as much as possible, and reduce the WL ratio RT3=W3/L3 of the active-load-stage transistors M3 and M4 as much as possible. Specifically, the ratios RT1 and RT3 are set so that RT1>RT3, for example.

(Q3) The thermal noise SvgThm is independent of the WL products W1×L1 and W3×L3. Therefore, when taking only the thermal noise into consideration, the area of the operational amplifier can be reduced by reducing the WL products W1×L1 and W3×L3.

As is clear from the above description, the thermal noise SvgThm and the area of the operational amplifier can be reduced by increasing the bias current IBD flowing through the differential section and reducing the WL products W1×L1 and W3×L3 to provide a small operational amplifier.

2.2 Selective Use of Operational Amplifiers

As is clear from the items (P1) and (Q1), the noise of the operational amplifier can be reduced by increasing the WL product W1×L1 of the differential-stage transistor to reduce flicker noise and increasing the bias current IBD of the differential section to reduce thermal noise.

However, the layout area of the operational amplifier is increased by increasing the WL product W1×L1, whereby the circuit scale is increased. On the other hand, the current consumption of the operational amplifier is increased by increasing the bias current IBD, thereby hindering a reduction in power consumption.

In this embodiment, in order to achieve a reduction in noise, circuit area, and power consumption in combination, the first-type and second-type operational amplifiers OP1 and OP2 are provided and are used selectively.

As transistor noise, flicker noise predominantly occurs in a low frequency region, and thermal noise predominantly occurs in a high frequency region, as shown in FIG. 5A.

As shown in FIG. 5A, the frequency f1 (first frequency) of the amplification target signal (small-signal amplification target signal of the operational amplifier) of the first circuit 310 (amplifier circuits 332 and 352 and filter sections 334 and 354) shown in FIG. 1 is high, and the frequency f2 (second frequency) of the amplification target signal of the second circuit 320 (amplifier circuit 338, filter sections 340 and 358, and detection circuit 360) is low.

Specifically, the frequency f1 corresponds to the frequency of the carrier signal. For example, the frequency f1 is a frequency in a band of several tens of kilohertz to several hundreds of kilohertz (AC band).

On the other hand, the frequency f2 corresponds to the frequency of the desired signal carried by the carrier signal (maximum frequency in the frequency band of the desired signal). For example, the frequency f2 is a frequency in a band of several hertz to several hundreds of hertz (DC band).

In this embodiment, the first-type operational amplifier OP1 which reduces thermal noise as compared with the second-type operational amplifier OP2 is used in the first supply circuit 21 supplies the voltage AGND to the first circuit 310 in the preceding stage of the mixer 322 (336 and 356) which extracts the desired signal from the carrier signal. Specifically, an operational amplifier is used of which the thermal noise at the frequency f1 of the carrier signal is lower than that of the second-type operational amplifier OP2.

On the other hand, the second-type operational amplifier OP2 which reduces flicker noise as compared with the first-type operational amplifier OP1 is used in the second supply circuit 22 which supplies the voltage AGND to the second circuit 320 in the subsequent stage of the mixer 322. Specifically, an operational amplifier is used of which the flicker noise at the frequency f2 of the desired signal is lower than that of the first-type operational amplifier OP1.

The third-type operational amplifier OP3 of which the thermal noise at the frequency of the carrier signal is lower than that of the second-type operational amplifier OP2 and the flicker noise at the frequency of the desired signal is lower than that of the first-type operational amplifier OP1 is used in the third supply circuit 23 which supplies the voltage V3Q to the first and second supply circuits 21 and 22. As the third-type operational amplifier OP3, it is more desirable to use an operational amplifier of which the thermal noise at the frequency of the carrier signal is lower than that of the first-type operational amplifier OP1 and the flicker noise at the frequency of the desired signal is lower than that of the second-type operational amplifier OP2.

In FIG. 5B, the WL product of the differential-stage transistor of the first-type operational amplifier OP1 is indicated by W1×L1=W1a×L1a, and the bias current flowing through the differential section is indicated by IBD=Ia, for example. The frequency (operating frequency) of the amplification target signal of the first circuit 310 (first-type operational amplifier OP1) is indicated by fop=f1. The WL ratio of the differential-stage transistor is indicated by RT1=RT1a=W1a/L1a, and the WL ratio of the active-load-stage transistor is indicated by RT3=RT3a=W3a/L3a.

The WL product of the differential-stage transistor of the second-type operational amplifier OP2 is indicated by W1×L1=W1b×L1b, and the bias current flowing through the differential section is indicated by IBD=Ib. The frequency of the amplification target signal of the second circuit 320 (second-type operational amplifier OP2) is indicated by fop=f2. The channel length ratio of the differential-stage transistor and the active-load-stage transistor is indicated by L1/L3=L1b/L3b. The WL product of the third-type operational amplifier OP3 is indicated by W1×L1=W1c×L1c, and the bias current flowing through the differential section is indicated by IBD=Ic.

In this embodiment, the relationship W1b×L1b>W1a×L1a, Ia>Ib, and f1>f2 is satisfied between the first-type and second-type operational amplifiers OP1 and OP2, as shown in

FIG. 5C. The relationship $RT1a>RT3a$ is satisfied for the first-type operational amplifier OP1, and the relationship $L1b<L3b$ is satisfied for the second-type operational amplifier OP2. The relationship $W1c \times L1c > W1a \times L1a$ and $Ic>Ib$ is satisfied for the third-type operational amplifier OP3. Note that the relationship $W1c \times L1c > W1b \times L1b$ and $Ic>Ia$ may be satisfied.

For example, flicker noise can be reduced by increasing the WL product $W1 \times L1$ of the differential-stage transistor, as shown in FIG. 6A and described in the item (P1), thermal noise can be reduced by increasing the bias current IBD of the differential section, as shown in FIG. 6A and described in the item (Q1). The first-type operational amplifier OP1 has the high signal frequency f1, and the second-type operational amplifier OP2 has the low signal frequency f2.

In this embodiment, as shown in FIG. 6B, thermal noise which predominantly occurs at the high frequency f1 is effectively reduced by increasing the bias current $IBD=Ia$ of the first-type operational amplifier OP1 having the high signal frequency f1, thereby reducing the noise of the entire system. Specifically, the bias current Ia of the first-type operational amplifier OP1 is set to be about twice to ten times, and preferably about four to seven times the bias current Ib of the second-type operational amplifier OP2, for example. On the other hand, since the effect of flicker noise is small at the high frequency f1, the layout area of the operational amplifier is unnecessarily increased when increasing the WL product $W1 \times L1 = W1a \times L1a$ of the first-type operational amplifier OP1. This does not contribute to a reduction in the noise of the entire system. In this embodiment, since the WL product $W1a \times L1a$ is set to be smaller than the WL product $W1b \times L1b$, a situation in which the layout area is unnecessarily increased can be prevented.

In this embodiment, as shown in FIG. 6C, flicker noise which predominantly occurs at the low frequency f2 is effectively reduced by increasing the WL product $W1 \times L1 = W1b \times L1b$ of the second-type operational amplifier OP2 having the low signal frequency f2, thereby reducing the noise of the entire system. Specifically, the WL product $W1b \times L1b$ of the second-type operational amplifier OP2 is set to be about 10 to 100 times, and preferably about 30 to 60 times the WL product $W1a \times L1a$ of the first-type operational amplifier OP1, for example. On the other hand, since the effect of thermal noise is small at the low frequency f2, the current consumption of the operational amplifier is unnecessarily increased when increasing the bias current $IBD=Ib$. This contributes to a reduction in power consumption of the entire system to only a small extent. In this embodiment, since the bias current Ib is set to be lower than the bias current Ia, a situation in which the current consumption is unnecessarily increased can be prevented.

In the first-type operational amplifier OP1 mainly aiming at reducing thermal noise, thermal noise can be reduced by increasing the WL ratio $RT1a=W1a/L1a$ as much as possible and reducing the WL ratio $RT3a=W3a/L3a$ as much as possible, as is clear from the equation (16) and the item (Q2). Therefore, the transistors of the first-type operational amplifier OP1 are sized so that the relationship $RT1a>RT3a$ is satisfied. Specifically, the WL ratio RT1a is set to be about twice to eight times, and preferably about three to six times the WL ratio RT3a, for example. This further reduces the noise of the entire system.

In the second-type operational amplifier OP2 mainly aiming at reducing flicker noise, flicker noise can be reduced by reducing the ratio $L1b/L3b$ as much as possible, as is clear from the equation (10) and the item (P2).

Therefore, the transistors of the second-type operational amplifier OP2 are sized so that the relationship $L1b<L3b$ is satisfied. Specifically, the channel length L1b is set to be about 0.4 to 0.8 times the channel length L3b, for example. This further reduces the noise of the entire system.

2.3 Corner Frequency

In this embodiment, the transistors of the first-type and second-type operational amplifiers OP1 and IP2 are sized so that frequencies f1 and f2 and the corner frequency fcr have the relationship shown in FIGS. 6B and 6C, for example.

Specifically, the first-type operational amplifier OP1 is designed so that the relationship $f1-fcr<fcr-f2$ is satisfied, as shown in FIG. 6B. The second-type operational amplifier OP2 is designed so that the relationship $fcr-f2<f1-fcr$ is satisfied, as shown in FIG. 6C.

The corner frequency fcr is the frequency corresponding to the intersection of the flicker noise characteristic line and the thermal noise characteristic line in the frequency-noise characteristics shown in FIGS. 6A to 6C.

For example, when the corner frequency fcr is set at a position indicated by E1 in the first-type operational amplifier OP1 shown in FIG. 7A, the noise at the frequency f1 increases, whereby thermal noise cannot be effectively reduced. On the other hand, when the corner frequency fcr is set at a position indicated by E2, the bias current IBD unnecessarily increases, thereby hindering a reduction in power consumption.

In this embodiment, the transistors of the first-type operational amplifier OP1 are sized so that the corner frequency fcr is set near the frequency f1. In this case, the thermal noise and the power consumption of the operational amplifier can be reduced optimally by ideally setting the corner frequency fcr to be $fcr=f1$, as indicated by E3 in FIG. 7A. However, when setting the corner frequency fcr to be $fcr=f1$, the thermal noise level may exceed the desired noise level when process variation occurs.

In FIG. 6B, the first-type operational amplifier OP1 is designed so that the relationship $f1-fcr<fcr-f2$ is satisfied, thereby causing the corner frequency fcr to be close to the frequency f1 as much as possible. This makes it possible to reduce the thermal noise and the power consumption of the operational amplifier while taking process variation into consideration.

In the second-type operational amplifier OP2 shown in FIG. 7B, when the corner frequency fcr is set at a position indicated by E4, the noise at the frequency f2 increases, whereby flicker noise cannot be effectively reduced. On the other hand, when the corner frequency fcr is set at a position indicated by E5, the WL product $W1 \times L1$ unnecessarily increases, thereby hindering a reduction in circuit area.

In this embodiment, the transistors of the second-type operational amplifier OP2 are sized so that the corner frequency fcr is set near the frequency f2. In this case, the flicker noise and the layout area of the operational amplifier can be reduced optimally by ideally setting the corner frequency fcr to be $fcr=f2$, as indicated by E6 in FIG. 7B. However, when setting the corner frequency fcr to be $fcr=f2$, the flicker noise level may exceed the desired noise level when process variation occurs.

In FIG. 6C, the second-type operational amplifier OP2 is designed so that the relationship $fcr-f2<f1-fcr$ is satisfied, thereby causing the corner frequency fcr to be close to the frequency f2 as much as possible. This makes it possible to reduce the thermal noise and the area of the operational amplifier while taking process variation into consideration.

2.4 Effective Gate Voltage

As shown in FIG. **5**C and the equation (10), flicker noise can be reduced by increasing the WL product W**1**b×L**1**b of the differential-stage transistor as much as possible and reducing the channel length L**1**b as much as possible. Therefore, it is considered that flicker noise can be efficiently reduced by sizing the transistors so that the WL ratio W**1**b/L**1**b is increased.

However, it was found that an effective gate voltage Veff decreases when increasing the WL ratio W**1**b/L**1**b to a large extent, thereby resulting in an increase in flicker noise. The effective gate voltage Veff is expressed by the following equation (17).

$$\begin{aligned} Veff &= Vgs - Vth \\ &= \left\{\frac{2 \times Ids}{\mu \times C_{OX} \times RT1b}\right\}^{\frac{1}{2}} \end{aligned} \tag{17}$$

Where, Vgs represents the gate-source voltage of the transistor, Vth represents the threshold voltage, Ids represents the drain-source current, μ represents the mobility, Cox represents the gate capacitance per unit area, and RT**1**b represents the WL ratio of the differential-stage transistor, provided that RT**1**b=W**1**b/L**1**b.

FIGS. **8**A and **8**B show measurement results of the relationship between the effective gate voltage Veff and noise (noise level Svg), for example. FIG. **8**A shows an example of an N-type transistor, and FIG. **8**B shows an example of a P-type transistor. In FIGS. **8**A and **8**B, the effective gate voltage Veff is changed by changing the noise level Vgs. Note that the drain-source voltage Vds is equal to the gate-source voltage Vgs.

As indicated by E**7** in FIG. **8**A and E**8** in FIG. **8**B, noise increases steeply when the effective gate voltage Veff decreases. This occurs due to a phenomenon in which the transistor operates in a weak inversion region when the effective gate voltage Veff as the small-signal reference voltage decreases, whereby flicker noise increases rapidly. In FIGS. **8**A and **8**B, flicker noise increases rapidly at an effective gate voltage Veff of 10 mV to 100 mV, for example. Therefore, in order to suppress an increase in flicker noise due to the operation in the weak inversion region, it is desirable to increase the effective gate voltage Veff to a value greater than 10 mV to 100 mV.

FIG. **9**A provides simulation results showing the relationship among the area, current consumption, and noise of the operational amplifier when changing the effective gate voltage Veff, wherein the X axis indicates the area (the length of one side when the operational amplifier is square), the Y axis indicates the current consumption, and the Z axis indicates the noise level.

In FIG. **9**A, the effective gate voltage Veff is changed by changing the WL ratio RT**1**b=W**1**b/L**1**b under conditions where the WL product W**1**b×L**1**b is constant. For example, the directions indicated by arrows F**1** and F**2** in FIG. **9**A are directions in which the effective gate voltage Veff decreases. The effective gate voltage Veff is reduced by increasing the WL ratio RT**1**b=W**1**b/L**1**b.

As indicated by F**1** in FIG. **9**A, the area and the current consumption of the operational amplifier decrease as the effective gate voltage Veff decreases. On the other hand, the noise changes to only a small extent.

However, the noise increases rapidly at the point F**3** in FIG. **9**A. Specifically, when the WL ratio RT**1**b=W**1**b/L**1**b exceeds a specific value, the transistor operates in the weak inversion region, as described with reference to FIGS. **8**A and **8**B, whereby flicker noise increases rapidly so that the noise of the operational amplifier increases rapidly.

At a point F**4** in FIG. **9**A, since the area and the current consumption of the operational amplifier are large although the noise is small, the area and the current are uselessly consumed.

In this embodiment, the WL ratio RT**1**b=W**1**b/L**1**b of the differential-stage transistor is determined (the range is narrowed) so that the WL ratio RT**1**b is set at the point F**3** in FIG. **9**A. For example, the WL ratio RT**1**b may be a value in the range of 50 to 200. The transistors of the operational amplifier are sized so that the WL product W**1**b×L**1**b increases and the channel length ratio L**1**b/L**3**b decreases as shown in FIG. **5**C under conditions where the WL ratio RT**1**b is determined as described above.

Specifically, the transistor is prevented from operating in the weak inversion region by satisfying the following equation (18).

$$Veff = \left\{\frac{2 \times Ids}{\mu \times C_{OX} \times RT1b}\right\}^{\frac{1}{2}} > \frac{k \times T}{q} \tag{18}$$

Where, k represents the Boltzmann constant, T represents the absolute temperature, and q (=1.602×10^{-19} coulombs) represents the amount of electronic charge. k×T/q=25.7 mV at room temperature (25°).

On the other hand, since flicker noise increases at the boundary between the weak inversion region and the strong inversion region, as shown in FIGS. **8**A and **8**B, it is necessary to take process variation into consideration. Therefore, when process variation parameter (process-dependent parameter) is referred to as P (P>1), the following equation (19) is satisfied.

$$P \times \frac{k \times T}{q} > Veff = \left\{\frac{2 \times Ids}{\mu \times C_{OX} \times RT1b}\right\}^{\frac{1}{2}} > \frac{k \times T}{q} \tag{19}$$

The process variation parameter P may be set at 3.0, for example. The process variation parameter P may be desirably a value in the range of 1.5 to 2.0.

In this embodiment, the WL ratio RT**1**b=W**1**b/L**1**b of the differential-stage transistor is determined so that the effective gate voltage Veff is a value in the range which satisfies the equation (19). The transistors of the operational amplifier are sized so that the WL product W**1**b×L**1**b increases and the channel length ratio L**1**b/L**3**b decreases under conditions where the WL ratio RT**1**b is determined as described above. It is desirable to again perform a fine adjustment by changing the WL ratio RT**1**b after determining the WL ratio RT**1**b and determining the WL product W**1**b×L**1**b and the channel length ratio L**1**b/L**3**b.

FIG. **9**B provides simulation results showing the relationship among the area, current consumption, and noise of the operational amplifier when changing the ratio L**1**b/L**3**b (L**3**b/L**1**b) which is the ratio of the gate length L**1**b of the differential-stage transistor and the gate length L**3**b of the active-load-stage transistor.

When increasing the ratio L**1**b/L**3**b (reducing the ratio L**3**b/L**1**b), as indicated by F**5** in FIG. **9**B, noise increases rapidly as indicated by F**7** from a point indicated by F**6**. In this case, the area of the operational amplifier decreases when increasing the ratio L1*b*/L3*b*, but the current consumption changes to only a small extent.

As is clear from the results shown in FIG. 9B, the ratio L1*b*/L3*b* can be optimally set by setting the ratio L1*b*/L3*b* at the point indicated by F6. Specifically, the ratio L1*b*/L3*b* may be a value in the range of 0.4 to 0.8, for example.

According to this embodiment, a reduction in noise, circuit area, and power consumption is successfully achieved in combination by sizing the transistors of the operational amplifier as described above.

For example, the reference voltage supply circuit **20** supplies the voltage AGND (analog reference voltage) to the first circuit **310** and the second circuit **320**. The voltage AGND is a voltage used as a reference for the analog circuit. The signal amplification operation of the operational amplifier is performed based on the voltage AGND. Accordingly, the reference voltage supply circuit **20** must supply the voltage AGND at a stable potential to the first circuit **310** and the second circuit **320**.

It is desirable that the first circuit **310** include the first-type operational amplifier OP**1** and the second circuit **320** include the second-type operational amplifier OP**2**. For example, the noise of the first circuit **310** can be reduced by forming the first circuit **310** using the first-type operational amplifier OP**1** mainly designed to reduce thermal noise. The noise of the second circuit **320** can be reduced by forming the second circuit **320** using the second-type operational amplifier OP**2** mainly designed to reduce flicker noise.

However, even if the first circuit **310** is formed using the first-type operational amplifier OP**1** and the second circuit **320** is formed using the second-type operational amplifier OP**2**, when thermal noise or flicker noise is superimposed on the voltage AGND supplied from the reference voltage supply circuit **20**, it becomes difficult to increase the SNR of the entire system.

For example, the frequency f**1** of the amplification target signal of the first circuit **310** which operates based on the voltage AGND supplied from the first supply circuit **21** is high, as shown in FIG. **5**A, and thermal noise predominantly occurs at the frequency f**1**, as described above. Therefore, even if the first-type operational amplifier is used for the first circuit **310**, when thermal noise is superimposed on the voltage AGND from the first supply circuit **21**, the thermal noise of the first circuit **310** increases.

In this embodiment, the first supply circuit **21** includes the reference-voltage first-type operational amplifier OP**1**, and supplies the voltage AGND using the reference-voltage first-type operational amplifier OP**1**. The reference-voltage first-type operational amplifier OP**1** is an operational amplifier mainly designed to reduce thermal noise, as described with reference to FIG. **5**C and the like. Therefore, thermal noise superimposed on an AGND line AGL**1** can be minimized, whereby an increase in thermal noise in the first circuit **310** can be prevented.

The frequency f**2** of the amplification target signal of the second circuit **320** which operates based on the voltage AGND supplied from the second supply circuit **22** is low, as shown in FIG. **5**A, and flicker noise predominantly occurs at the frequency f**2**, as described above. Therefore, even if the second-type operational amplifier is used for the second circuit **320**, when flicker noise is superimposed on the voltage AGND from the second supply circuit **22**, the flicker noise of the second circuit **320** increases.

In this embodiment, the second supply circuit **22** includes the reference-voltage second-type operational amplifier OP**2**, and supplies the voltage AGND using the reference-voltage second-type operational amplifier OP**2**. The reference-voltage second-type operational amplifier OP**2** is an operational amplifier mainly designed to reduce flicker noise, as described with reference to FIG. **5**C and the like. Therefore, flicker noise superimposed on an AGND line AGL**2** can be minimized, whereby an increase in flicker noise in the second circuit **320** can be prevented.

The voltage AGND from the first supply circuit **21** is supplied through the AGND line AGL**1** (first analog reference voltage line in a broad sense). The voltage AGND from the second supply circuit **22** is supplied through the AGND line AGL**2** (second analog reference voltage line in a broad sense). In this case, the AGND lines AGL**1** and AGL**2** are separately provided from the reference voltage supply circuit **20** to the first and second circuits **310** and **320**. Specifically, the two AGND lines AGL**1** and AGL**2** are connected with the first and second circuits **310** and **320** while being separated in the layout. This prevents a situation in which noise from the AGND line AGL**1** is transmitted to the AGND line AGL**2** or noise from the AGND line AGL**2** is transmitted to the AGND line AGL**1**.

For example, when thermal noise from the AGND line AGL**2** is transmitted to the AGND line AGL**1**, the thermal noise from the AGND line AGL**2** is transmitted to the first circuit **310**, even if the first supply circuit **21** is formed using the first-type operational amplifier OP**1** mainly designed to reduce thermal noise, whereby the SNR deteriorates. Likewise, when flicker noise from the AGND line AGL**2** is transmitted to the AGND line AGL**2**, the flicker noise from the AGL**1** is transmitted to the second circuit **320**, even if the second supply circuit **22** is formed using the second-type operational amplifier OP**2** mainly designed to reduce flicker noise, whereby the SNR deteriorates.

The above-described situation can be prevented by separately providing the AGND lines AGL**1** and AGL**2**, whereby the SNR of the entire system can be increased.

FIG. **10** shows the results when applying the method according to this embodiment to a gyrosensor detection device described later. QVAMP, DIFF, PGA, SYNCD, and FLT respectively indicate the noise levels of a Q/V conversion circuit, a differential amplifier circuit, a sensitivity adjustment circuit, a synchronous detection circuit, and a filter section.

As shown in FIG. **10**, this embodiment successfully and efficiently reduces the noise of the entire system by selectively using the operational amplifiers for the first supply circuit **21** which supplies the voltage AGND to the first circuit **310** which processes the AC signal and the second supply circuit **22** which supplies the voltage AGND to the second circuit **320** which processes the DC signal to achieve an optimum low-noise design.

2.5 Layout

A layout method for the first-type and second-type operational amplifiers OP**1** and OP**2** is described below. FIG. **11**A shows a layout example of the first-type operational amplifier OP**1**, and FIG. **11**B shows a layout example of the second-type operational amplifier OP**2**.

In FIG. **11**B, H**2** indicates the arrangement region of the differential-stage transistors M**1** and M**2** among the elements (e.g., transistor, capacitor, and resistor) of the second-type operational amplifier OP**2**. The area of the arrangement region H**2** is referred to as Sdf, and the area of the arrangement region of the elements of the second-type operational amplifier other than the differential-stage transistors M**1** and M**2** is referred to as Sre. Note that the elements other than the differential-stage transistors M**1** and M**2** refer to the transistors M**3**, M**4**, M**5**, M**6**, and M**7** other than the transistors M**1** and M2, the capacitor CF, the resistor RF, and the like shown in FIG. 4B, for example. In FIG. 11B, the relationship Sdf>Sre is satisfied. The WL product W1b×L1b can be increased by satisfying such a relationship, whereby flicker noise can be reduced.

In the first-type operational amplifier OP1 shown in FIG. 11A, since the arrangement region of the differential-stage transistors M1 and M2 is a small, as indicated by H1, the relationship Sdf>Sre is not satisfied. In the first-type operational amplifier OP1, thermal noise is reduced by sizing the transistors so that the bias current IBD=Ia increases.

In FIG. 11B, the differential-stage transistor M1 of the second-type operational amplifier OP2 includes (J) transistors TR11, TR12, TR13, and TR14 connected in parallel. Likewise, the differential-stage transistor M2 of the second-type operational amplifier OP2 includes transistors TR21, TR22, TR23, and TR24 connected in parallel. The parallel-connected transistors TR11 to TR14 and TR21 to TR24 are disposed in the arrangement region of the differential-stage transistors M1 and M2 indicated by H2.

In FIG. 11B, a direction X is the channel length direction, and a direction Y is the channel width direction. The channel length of each of the parallel-connected transistors TR11 to TR14 and TR21 to TR24 is L1b. When the number of the parallel-connected transistors TR11 to TR14 or TR21 to TR24 is J (J=4 in FIG. 11B), the channel width of each of the transistors TR11 to TR14 and TR21 to TR24 is W11b=W1b/J.

The WL ratio W1b/L1b can be increased while increasing the WL product W1b×L1b by disposing the parallel-connected transistors TR11 to TR14 and TR21 to TR24 as shown in FIG. 11B whereby flicker noise can be efficiently reduced.

In FIG. 11B, the active-load-stage transistors M3 and M4 respectively include (I) transistors TR31 and TR32 and (I) transistors TR41 and TR42 connected in parallel. The channel length of each of the parallel-connected transistors TR31 and TR32 and the parallel-connected transistors TR41 and TR42 is L3b. When the number of the parallel-connected transistors TR31 and TR32 or TR41 and TR42 is I (I=2 in FIG. 11B), the channel width of each of the transistors TR31 and TR32 and the transistors TR41 and TR42 is W33b=W3b/I.

In FIG. 11B, the J (e.g., J=4) transistors TR11 to TR14 and the J transistors TR21 to TR24 are disposed in the arrangement region of the differential-stage transistors M1 and M2 in the direction X, and the I (I<J; e.g., I=2) transistors TR31 and TR32 and the I transistors TR41 and TR42 are disposed in the arrangement region of the active-load-stage transistors M3 and M4 in the direction X. This enables the transistors TR11 to TR14 and the transistors TR21 to TR24 respectively forming the differential-stage transistors M1 and M2 and the transistors TR31 and TR32 and the transistors TR41 and TR42 respectively forming the active-load-stage transistors M3 and M4 to be efficiently disposed symmetrically in the rectangular arrangement region while satisfying the relationship L1b<L3b described with reference to FIG. 5C. This increases layout efficiency.

FIG. 12 shows a layout example of the third-type operational amplifier OP3. In FIG. 12, H3 indicates the arrangement region of the differential-stage transistors M1 and M2. In FIG. 12, since the relationship Sdf>Sre is satisfied in the same manner as in FIG. 11B, the WL ratio W1c/L1c can be increased. Therefore, flicker noise can be reduced.

In FIG. 12, the differential-stage transistors M1 and M2 respectively include parallel-connected transistors TS11 to TS14 and parallel-connected transistors TS21 to TS24. The (J) parallel-connected transistors TS11 to TS14 and the (J) parallel-connected transistors TS21 to TS24 are disposed in the arrangement region of the differential-stage transistors M1 and M2 indicated by H3.

The channel length of each of the parallel-connected transistors TS11 to TS14 and the parallel-connected transistors TS21 to TS24 is L1c, and the channel width is W11c=W1c/J.

As is clear from the comparison between FIG. 12 and FIG. 11B, the arrangement region H3 of the differential-stage transistors M1 and M2 of the third-type operational amplifier OP3 shown in FIG. 12 is further increased as compared with FIG. 11B. This realizes an operational amplifier which can further reduce flicker noise as compared with FIG. 11B.

2.6 Reference Voltage Supply Circuit

FIG. 13 shows a detailed configuration example of the reference voltage supply circuit 20. The reference voltage supply circuit 20 is not limited to the configuration shown in FIG. 13. Various modification may be made such as omitting some elements or adding another element.

The reference voltage supply circuit 20 includes the first, second, and third supply circuits 21, 22, and 23. The reference voltage supply circuit 20 also includes a reference voltage generation circuit 26.

The first supply circuit 21 (first impedance conversion circuit) performs voltage impedance conversion using the reference-voltage first-type operational amplifier OP1, for example. Specifically, the first-type operational amplifier OP1 included in the first supply circuit 21 is a voltage-follower-connected operational amplifier of which the inverting input terminal (second input terminal in a broad sense) is connected with the output terminal. The output terminal of the first-type operational amplifier OP1 is connected with the AGND line AGL1.

The second supply circuit 22 (second impedance conversion circuit) performs voltage impedance conversion using the reference-voltage second-type operational amplifier OP2, for example. Specifically, the second-type operational amplifier OP2 included in the second supply circuit 22 is a voltage-follower-connected operational amplifier of which the inverting input terminal (second input terminal) is connected with the output terminal. The output terminal of the second-type operational amplifier OP2 is connected with the AGND line AGL2.

The third supply circuit 23 is provided in the preceding stage of the first and second supply circuits 21 and 22, and supplies the output voltage V3Q to the first and second supply circuits 21 and 22. For example, the first and second supply circuits 21 and 22 subject the output voltage V3Q from the third supply circuit 23 to impedance conversion and outputs the voltage AGND.

The third supply circuit 23 includes the third-type operational amplifier OP3 described with reference to FIGS. 5C and 12. The third supply circuit 23 may include a voltage divider circuit including resistors RJ1, RJ2, and RJ3.

The reference voltage generation circuit 26 generates a reference voltage VR for generating the voltage AGND. A circuit which generates the reference voltage VR by a band gap may be employed as the reference voltage generation circuit 26, for example.

In FIG. 13, the voltage of a node NJ1 is equal to the reference voltage VR due to a virtual short circuit of the third-type operational amplifier OP3, for example. Therefore, when the resistances of the resistors RJ2 and RJ3 are respectively referred to as R2 and R3, the output voltage of the third supply circuit 23 is V3Q=VR×{(R2+R3)/R3}. The first and second supply circuits 21 and 22 subject the output voltage

V3Q (=AGND=VR×{(R2+R3)/R3}) to impedance conversion. This enables the potential of the voltage AGND to be stabilized.

The channel width and the channel length of the differential-stage transistor of the differential section of the reference-voltage third-type operational amplifier OP3 are respectively referred to as W1c and L1c, and the bias current flowing through the differential section is referred to as Ic. In this case, the relationship W1c×L1c>W1a×L1a and Ic>Ib is satisfied.

Specifically, the first supply circuit 21 receives the output voltage V3Q from the third supply circuit 23, and supplies the voltage AGND to the amplifier circuit 70. Therefore, when thermal noise is superimposed on the output voltage V3Q of the third supply circuit 23, the thermal noise superimposed on the output voltage V3Q is transmitted to the first circuit 310, even if the first-type operational amplifier OP1 mainly designed to reduce thermal noise is used as the first supply circuit 21. As a result, the SNR of the entire system deteriorates.

The second supply circuit 22 receives the output voltage V3Q from the third supply circuit 23, and supplies the voltage AGND to the filter section 110. Therefore, when flicker noise is superimposed on the output voltage V3Q of the third supply circuit 23, the flicker noise superimposed on the output voltage V3Q is transmitted to the second circuit 320, even if the second-type operational amplifier OP2 mainly designed to reduce flicker noise is used as the second supply circuit 22. As a result, the SNR of the entire system deteriorates.

The third-type operational amplifier OP3 of the third supply circuit 23 shown in FIG. 13 satisfies the relationship W1c×L1c>W1a×L1a and Ic>Ib. The relationship W1c×L1c>W1b×L1b and Ic>Ia is desirably satisfied. Therefore, the third-type operational amplifier OP3 is an operational amplifier with low thermal noise and low flicker noise. For example, the third-type operational amplifier OP3 has a large WL product and a large bias current, as shown in the layout example in FIG. 12. Therefore, the third-type operational amplifier OP3 is an operational amplifier with very low thermal noise and very low flicker noise.

As described above, thermal noise and flicker noise superimposed on the output voltage V3Q of the third supply circuit 23 can be minimized using the third-type operational amplifier OP3 with low thermal noise and low flicker noise as the third supply circuit 23. Therefore, a situation can be minimized in which thermal noise superimposed on the output voltage V3Q is transmitted to the first circuit 310 through the first supply circuit 21 or flicker noise superimposed on the output voltage V3Q is transmitted to the second circuit 320 through the second supply circuit 22, whereby the SNR of the entire system can be significantly increased.

3. Application of Gyrosensor Detection Device

3.1 Configuration of Detection Device

A case of applying the method according to this embodiment to a gyrosensor detection device is described below. FIG. 14 shows a configuration example of a detection device 30. The detection device 30 includes a driver circuit 40 and a detection circuit 60. The detection device 30 is not limited to the configuration shown in FIG. 14. Various modification may be made such as omitting some elements or adding another element. For example, the configuration of the driver circuit 40 may be omitted when a synchronization signal can be extracted based on a detection signal from a vibrator 10.

The vibrator 10 (vibrating gyroscope) as a physical quantity transducer is a piezoelectric vibrator formed of a piezoelectric material such as a crystal. FIG. 15A shows a tuning-fork piezoelectric vibrator as an example of the vibrator 10. The vibrator 10 includes driving vibrators 11 and 12 and detection vibrators 16 and 17. The driving vibrators 11 and 12 are respectively provided with driving terminals 2 and 4, and the detection vibrators 16 and 17 are respectively provided with detection terminals 6 and 8. FIG. 15A shows an example in which the vibrator 10 is a tuning-fork vibrator. Note that the vibrator 10 according to this embodiment is not limited to the structure shown in FIG. 15A. For example, the vibrator 10 may be a T-shaped vibrator, double-T-shaped vibrator, or the like. The piezoelectric material for the vibrator 10 may be a material other than a crystal. The vibrator 10 (physical quantity transducer) may be an electrostatic micro electro mechanical system (MEMS) which performs a driving/detection operation utilizing capacitance. The physical quantity transducer is an element for converting a physical quantity (indicating the degree of property of an object and expressed in defined units) into another physical quantity. As the conversion target physical quantity, a force such as Coriolis force and gravity, acceleration, mass, and the like can be given. A physical quantity obtained by conversion may be a voltage or the like in addition to current (charge).

The driver circuit 40 outputs a driving signal (driving voltage) VD to drive the vibrator 10 (physical quantity transducer in a broad sense), and receives a feedback signal VF from the vibrator 10. The driver circuit 40 thus causes the vibrator 10 to vibrate. The detection circuit 60 receives detection signals (detection current or charge) ISP and ISM from the vibrator 10 driven by the driving signal VD, and detects (extracts) a desired signal (Coriolis force signal) from the detection signals.

Specifically, the alternating-current driving signal (driving voltage) VD from the driver circuit 40 is applied to the driving terminal 2 of the driving vibrator 11 shown in FIG. 15A. This causes the driving vibrator 11 to start to vibrate due to the reverse voltage effect, and the driving vibrator 12 also starts to vibrate due to the tuning-fork vibration. A current (charge) generated by the piezoelectric effect of the driving vibrator 12 is fed back to the driver circuit 40 from the driving terminal 4 as the feedback signal VF. An oscillation loop including the vibrator 10 is thus formed.

When the driving vibrators 11 and 12 vibrate, the detection vibrators 16 and 17 vibrate in the directions shown in FIG. 15A at a vibration velocity v. A current (charge) generated by the piezoelectric effect of the detection vibrators 16 and 17 is output from the detection terminals 6 and 8 as the detection signals ISP and ISM. The detection circuit 60 receives the detection signals ISP and ISM, and detects the desired signal (desired wave) which is the signal corresponding to the Coriolis force.

Specifically, when the vibrator 10 (gyrosensor) rotates around a detection axis 19 shown in FIG. 15A, a Coriolis force Fc occurs in the directions perpendicular to the vibration directions at the vibration velocity v. FIG. 15B schematically shows the detection axis 19 shown in FIG. 15A viewed from the upper side. In FIG. 15B, when the angular velocity of the vibrator while the vibrator rotates around the detection axis 19 is referred to as ω, the mass of the vibrator is referred to as m, and the vibration velocity of the vibrator is referred to as v, the Coriolis force is expressed as $Fc=2m\cdot v\cdot\omega$. Therefore, the rotation angular velocity ω of the gyrosensor (vibrator) can be determined by causing the detection circuit 60 to detect (extract) the desired signal which is the signal corresponding to the Coriolis force.

The vibrator 10 has a driving-side resonance frequency fd and a detection-side resonance frequency fs. Specifically, the natural resonance frequency (natural resonance frequency in driving vibration mode) of the driving vibrators 11 and 12 is the frequency fd, and the natural resonance frequency (natural resonance frequency in detection vibration mode) of the detection vibrators **16** and **17** is the frequency fs. In this case, a constant frequency difference is provided between the frequencies fd and fs in a range so that the driving vibrators **11** and **12** and the detection vibrators **16** and **17** can perform the detection operation and have an appropriate intermode coupling which does not cause unnecessary resonant coupling. A detuning frequency $\Delta f=|fd-fs|$ which is the above difference in frequency is set at a value sufficiently lower than the frequencies fd and fs.

The driver circuit (oscillation circuit) **40** includes an amplifier circuit **42**, an automatic gain control (AGC) circuit **44** which performs automatic gain control, and a binarization circuit (comparator) **46**. The driver circuit **40** must maintain a constant amplitude of the driving voltage supplied to the vibrator **10** (driving vibrator) in order to maintain constant sensitivity of the gyrosensor. Therefore, the AGC circuit **44** for automatic gain adjustment is provided in the oscillation loop of the driving vibration system. Specifically, the AGC circuit **44** variably and automatically adjusts the gain so that the amplitude of the feedback signal FD (vibration velocity v of the vibrator) becomes constant. Note that the phase is adjusted so that the phase shift in the oscillation loop becomes zero degrees (0 deg). In order to enable high-speed oscillation startup, the gain in the oscillation loop is set at a value larger than unity during oscillation startup.

The amplifier circuit **42** amplifies the feedback signal FD from the vibrator **10**. Specifically, an I/V conversion circuit included in the amplifier circuit **42** converts a current (charge) as the feedback signal FD from the vibrator **10** into voltage, and outputs the voltage as a driving signal VD**2**.

The AGC circuit **44** monitors the driving-side amplified signal VD**2** which is the signal amplified by the driving-side amplifier circuit **42**, and controls the gain in the oscillation loop. The AGC circuit **44** may include a gain control amplifier (GCA) for controlling the oscillation amplitude in the oscillation loop, and a gain control circuit which outputs a control voltage for adjusting the gain of the gain control amplifier corresponding to the oscillation amplitude. The gain control circuit may include a rectifier circuit (full-wave rectifier) which converts the alternating-current driving signal VD**2** from the amplifier circuit **42** into a direct-current signal, a circuit which outputs the control voltage corresponding to the difference between the voltage of the direct-current signal from the rectifier circuit and a reference voltage, and the like.

The binarization circuit **46** binarizes the driving-side amplified signal VD**2** which is a sine wave, and outputs a synchronization signal (reference signal) CLK obtained by binarization to a synchronous detection circuit **100** of the detection circuit **60**. The binarization circuit **46** may be realized by a comparator to which the sine-wave (alternating-current) signal VD**2** from the amplifier circuit **42** is input and which outputs the rectangular-wave synchronization signal CLK. Note that another circuit may be provided between the amplifier circuit **42** and the binarization circuit **46** or between the binarization circuit **46** and the synchronous detection circuit **100**. For example, a high-pass filter, a phase-shift circuit (phase shifter), or the like may be provided.

The detection circuit **60** includes an amplifier circuit **70**, the synchronous detection circuit **100**, and a filter section **110**. Note that some of these elements may be omitted, or another element may be added.

The amplifier circuit **70** amplifies the detection signals ISP and ISM from the vibrator **10**. Specifically, Q/V conversion circuits (I/V conversion circuits) included in the amplifier circuit **70** respectively receive the signals ISP and ISM from the vibrator **10**, and convert (amplify) the charge (current) generated by the vibrator **10** into voltage.

The synchronous detection circuit (detection circuit or detector) **100** performs synchronous detection based on the synchronization signal CLK (synchronization clock signal or reference signal). A mechanical vibration leakage unnecessary signal can be removed by synchronous detection.

The filter section **110** provided in the subsequent stage of the synchronous detection circuit **100** filters a signal VS**6** obtained by synchronous detection. Specifically, the filter section **110** performs a low-pass filtering process of removing high-frequency components.

The detection signal (sensor signal) from the vibrator **10** includes a desired signal (desired wave) and an unnecessary signal (unnecessary wave) in a mixed state. Since the amplitude of the unnecessary signal is generally about 100 to 500 times the amplitude of the desired signal, a high performance is required for the detection device **30**. Examples of the unnecessary signal include an unnecessary signal caused by mechanical vibration leakage, an unnecessary signal caused by electrostatic coupling leakage, an unnecessary signal caused by the detuning frequency Δf, an unnecessary signal caused by the frequency 2fd ($2\omega d$), an unnecessary signal caused by DC offset, and the like. The unnecessary signal caused by mechanical vibration leakage occurs due to the imbalance of the shape of the vibrator **10** and the like. The unnecessary signal caused by electrostatic coupling leakage occurs when the driving signal VD shown in FIG. **14** leaks into input terminals of the signals ISP and ISM and the like through the parasitic capacitors CP and CM.

FIGS. **16**A to **16**C show Frequency spectra illustrative of unnecessary signal removal. FIG. **16**A shows the frequency spectrum before synchronous detection. As shown in FIG. **16**A, an unnecessary signal caused by DC offset exists in the detection signal before synchronous detection in the DC frequency band. An unnecessary signal caused by mechanical vibration leakage and the desired signal exist in the fd frequency band.

FIG. **16**B shows the frequency spectrum after synchronous detection. The desired signal in the fd frequency band shown in FIG. **16**A appears in the DC and 2fd frequency bands after synchronous detection, as shown in FIG. **16**B. The unnecessary signal (DC offset) in the DC frequency band shown in FIG. **16**A appears in the fd frequency band after synchronous detection, as shown in FIG. **16**B. The unnecessary signal (mechanical vibration leakage) in the fd frequency band shown in FIG. **16**A appears in the 2fd frequency band after synchronous detection, as shown in FIG. **16**B.

FIG. **16**C shows the frequency spectrum after filtering. The frequency components of the unnecessary signals in the frequency bands of the frequencies fd, 2fd, and the like can be removed by smoothing (LPF) the signal after synchronous detection using the filter section **110**.

In this embodiment, the first supply circuit **21** of the reference voltage supply circuit **20** supplies the voltage AGND (analog reference voltage) to the amplifier circuit **70** of the detection circuit **60**, and the second supply circuit **22** supplies the voltage AGND to the filter section **110** of the detection circuit **60**.

In this case, the first-type operational amplifier OP**1** included in the first supply circuit **21** is an operational amplifier of which the thermal noise at the frequency of the carrier signal (e.g., resonance frequency of the vibrator or driving-side resonance frequency) is lower than that of the second-type operational amplifier OP**2**, for example. The second-type operational amplifier OP**2** included in the second supply circuit **22** is an operational amplifier of which the flicker noise at the frequency of the desired signal (e.g., maximum frequency in the frequency band of the desired signal) is lower than that of the first-type operational amplifier OP**1**. The first-type operational amplifier OP**1** satisfies the relationship f**1**−fcr<fcr−f**2**, and the second-type operational amplifier OP**2** satisfies the relationship fcr−f**2**<f**1**−fcr, as described above. The relationship W**1***b*×L**1***b*>W**1***a*×L**1***a* and Ia>Ib is also satisfied. The synchronous detection circuit **100** may include a third-type operational amplifier OP**3**, for example. In this case, the relationship W**1***c*×L**1***c*>W**1***a*×L**1***a* and Ic>Ib is satisfied. Alternatively, the relationship W**1***c*×L**1***c*>W**1***b*×L**1***b* and Ic>Ia may be satisfied.

3.2 First Modification

FIG. **17** shows a first modification of the detection device. In the first modification, the filter section **110** includes an output circuit **116**, and the reference voltage supply circuit **20** includes a fourth supply circuit **24**.

The output circuit **116** is a circuit which subjects the output signal to impedance conversion, and functions as an output buffer. Note that the output circuit **116** may function as a postfilter.

The fourth supply circuit **24** supplies the voltage AGND (analog reference voltage) to the output circuit **116**. The fourth supply circuit **24** includes a second-type operational amplifier OP**2**.

In FIG. **17**, the voltage AGND from the first supply circuit **21** is supplied through the AGND line AGL**1** (first analog reference voltage line in a broad sense), and the voltage AGND from the second supply circuit **22** is supplied through the AGND line AGL**2** (second analog reference voltage line). The voltage AGND from the fourth supply circuit **24** is supplied to the output circuit **116** through an AGND line AGL**3** (third analog reference voltage line in a broad sense). Specifically, the voltage AGND is supplied to a preceding-stage circuit **115** (e.g., prefilter or SCF) which is a circuit of the filter section **110** other than the output circuit **116** through the AGND line AGL**2**, and the voltage AGND is supplied to the output circuit **116** through the AGND line AGL**3**.

FIG. **18** shows a layout example of the detection circuit **60**. As shown in FIG. **18**, the AGND lines AGL**1**, AGL**2**, and AGL**3** are separately provided from the reference voltage supply circuit **20** to the detection circuit **60**. Specifically, the three AGND lines AGL**1**, AGL**2**, and AGL**3** are respectively connected with the amplifier circuit **70**, the preceding-stage circuit **115** of the filter section **110**, and the output circuit **116** of the filter section **110** while being separated in the layout. This prevents a situation in which noise from the AGND line AGL**1** is transmitted to the AGND line AGL**2**, or noise from the AGND line AGL**2** is transmitted to the AGND line AGL**3**, or noise from the AGND line AGL**3** is transmitted to the AGND line AGL**1**.

Specifically, the frequency of the amplification target signal of the preceding-stage circuit **115** and the output circuit **116** of the filter section **110** is the low frequency f**2** at which flicker noise predominantly occurs. Therefore, the second-type operational amplifiers OP**2** mainly designed to reduce flicker noise are used for the second supply circuit **22** and the fourth supply circuit **24** which supply the voltage AGND to the preceding-stage circuit **115** and the output circuit **116**.

However, when the preceding-stage circuit **115** includes a switched-capacitor filter (SCF) described later, for example, the SNR may deteriorate when a clock signal used in the SCF functions as a noise source. Specifically, clock noise generated by the preceding-stage circuit **115** (SCF) may be superimposed on the output signal VSQ of the output circuit **116**. In particular, a gyrosensor detects angular velocity information by A/D converting the voltage of the output signal VSQ. Therefore, when the voltage of the output signal VSQ varies due to the clock noise, wrong angular velocity information may be detected.

In FIG. **17**, although the second and fourth supply circuits **22** and **24** use the second-type operational amplifiers OP**2**, the AGND line AGL**2** of the second supply circuit **22** and the AGND line AGL**3** of the fourth supply circuit **24** are separated in the layout. This prevents a situation in which clock noise or the like generated by the preceding-stage circuit **115** is transmitted from the AGND line AGL**2** to the AGND line AGL**3** and is superimposed on the output signal VSQ, whereby erroneous detection of angular velocity information and the like can be prevented.

FIG. **19** shows a configuration example of the reference voltage supply circuit **20** used in the first modification shown in FIG. **17**. In FIG. **19**, the fourth supply circuit **24** is additionally provided in the configuration shown in FIG. **13**. The fourth supply circuit **24** (fourth impedance conversion circuit) performs voltage impedance conversion using the reference-voltage second-type operational amplifier OP**2**, for example. Specifically, the second-type operational amplifier OP**2** included in the fourth supply circuit **24** is a voltage-follower-connected operational amplifier of which the inverting input terminal (second input terminal) is connected with the output terminal. The output terminal of the second-type operational amplifier OP**2** is connected with the AGND line AGL**3**. A situation in which noise from the AGND line AGL**2** is transmitted to the AGND line AGL**3** can be effectively prevented by providing the fourth supply circuit **24** having the impedance conversion function.

3.3 Second Modification

FIG. **20** shows a second modification of the detection device. The second modification shows a detailed configuration example of the detection circuit **60**. The detection circuit **60** shown in FIG. **20** includes the amplifier circuit **70**, a sensitivity adjustment circuit **80**, the synchronous detection circuit **100**, and the filter section **110**.

The amplifier circuit **70** includes Q/V conversion circuits **72** and **74** and a differential amplifier circuit **76**. The Q/V (I/V) conversion circuits **72** and **74** convert charge (current) generated by the vibrator **10** into voltage. The differential amplifier circuit **76** differentially amplifies output signals VS**1**P and VS**1**M from the Q/V conversion circuits **72** and **74**.

The Q/V conversion circuit **72** includes a capacitor CA**1** and a resistor RA**1** provided between nodes NA**1** and NA**2** and an operational amplifier OPA**1**, and has low-pass filter frequency characteristics. The input node NA**1** is connected with an inverting input terminal (first input terminal) of the operational amplifier OPA**1**, and the voltage AGND (reference power supply voltage) is connected with a non-inverting input terminal (second input terminal) of the operational amplifier OPA**1**. The Q/V conversion circuit **74** has the same configuration as the Q/V conversion circuit **72**.

The differential amplifier circuit **76** includes resistors RB**1**, RB**2**, RB**3**, and RB**4** and an operational amplifier OPB. The differential amplifier circuit **76** amplifies the difference between the input signals VS**1**P and VS**1**M with opposite phases by equalizing the resistance ratio of the resistors RB**1** and RB**2** and the resistance ratio of the resistors RB**3** and RB**4**. Unnecessary signals due to common mode noise, electrostatic coupling leakage, and the like input from the vibrator **10** to the Q/V conversion circuits **72** and **74** can be removed by differential amplification.

In this embodiment, the first supply circuit **21** of the reference voltage supply circuit **20** supplies the voltage AGND (analog reference voltage) to the Q/V conversion circuits **72** and **74** (first and second charge/voltage conversion circuits or first and second current/voltage conversion circuits) and the differential amplifier circuit **76** using the reference-voltage first-type operational amplifier OP**1**. It is also desirable to use the first-type operational amplifiers OP**1** as the operational amplifiers OPA**1**, OPA**2**, and OPB of the Q/v conversion circuits **72** and **74** and the differential amplifier circuit **76** shown in FIG. **20**.

Therefore, the voltage AGND can be supplied to the Q/v conversion circuits **72** and **74** and the differential amplifier circuit **76** which amplify a signal in a high frequency band (driving-side resonance frequency band) in which thermal noise predominantly occurs using the first-type operational amplifiers OP**1** mainly designed to reduce thermal noise. As a result, the thermal noise of the Q/v conversion circuits **72** and **74** and the differential amplifier circuit **76** can be reduced, whereby the SNR of the entire system can be increased.

The sensitivity adjustment circuit **80** adjusts the sensitivity (the amount of change in output voltage per unit angular velocity) by variably controlling the gain.

In FIG. **20**, the sensitivity adjustment circuit **80** is provided in the preceding stage of the synchronous detection circuit **100**. A sensitivity adjustment is performed for the signal having the frequency fd instead of the DC signal by providing the sensitivity adjustment circuit **80** (programmable gain amplifier) in the preceding stage of the synchronous detection circuit **100**. Therefore, an adverse effect of flicker noise (1/f noise) which is reduced as the frequency increases can be minimized. Moreover, since the number of circuit blocks provided in the preceding stage of the sensitivity adjustment circuit **80** is reduced in comparison with the case of providing the sensitivity adjustment circuit in the subsequent stage of the filter section **110**, deterioration in SNR which occurs when the sensitivity adjustment circuit **80** amplifies noise generated by these circuit blocks can be minimized.

The sensitivity adjustment circuit **80** shown in FIG. **20** is an example of a non-inverting amplifier circuit. Note that an inverting amplifier circuit may be used as the sensitivity adjustment circuit **80**.

In the sensitivity adjustment circuit **80**, the resistance of a variable resistor RD**2** between an output node ND**3** and an output tap QT and the resistance of a variable resistor RD**1** between the output tap QT and a node of the voltage AGND are variably controlled based on sensitivity adjustment data DPGA. This allows adjustment of the gain of the sensitivity adjustment circuit **80**, whereby the sensitivity is adjusted. For example, when the resistances of the variable resistors RD**1** and RD**2** are respectively referred to as R**1** and R**2**, the gain of the sensitivity adjustment circuit **80** (PGA) is G=(R**1**+R**2**)/R**1**.

The sensitivity adjustment circuit **80** shown in FIG. **20** operates as a programmable-gain amplifier and a high-pass filter, for example. Specifically, a capacitor CD**1**, a resistor RD**3**, and an operational amplifier OPD form a high-pass active filter. Specifically, the operational amplifier OPD functions as a buffer for the high-pass filter formed of the capacitor CD**1** and the resistor RD**3**. A programmable-gain amplifier is formed of the variable resistors RD**1** and RD**2** and the operational amplifier OPD. Specifically, the operational amplifier OPD is used in common by the high-pass active filter and the programmable-gain amplifier.

The DC component can be cut off by causing the sensitivity adjustment circuit **80** to operate as the high-pass filter, whereby a situation can be prevented in which the DC signal is amplified by the programmable-gain amplifier (PGA). Therefore, a problem can be prevented in which the programmable-gain amplifier of the sensitivity adjustment circuit **80** or the operational amplifier in the subsequent stage (e.g. operational amplifier of the synchronous detection circuit) is saturated due to overinput, whereby the output overflows. Moreover, DC noise can be removed by the high-pass filter, whereby the SNR can be increased.

In the sensitivity adjustment circuit **80**, the operational amplifier OPD is used in common by the high-pass active filter and the programmable-gain amplifier. Therefore, the number of operational amplifiers can be reduced as compared with the case of separately providing an operational amplifier for the active filter and an operational amplifier for the programmable-gain amplifier. Therefore, the circuit scale can be reduced. Moreover, since the number of circuit blocks as the noise source can be reduced, the SNR can be increased.

In this embodiment, the first supply circuit **21** of the reference voltage supply circuit **20** supplies the voltage AGND (analog reference voltage) to the sensitivity adjustment circuit **80** using the reference-voltage first-type operational amplifier OP**1** described with reference to FIGS. **5**C and **11**A.

This enables the voltage AGND to be supplied to the sensitivity adjustment circuit **80** which processes a signal in a high frequency band (driving-side resonance frequency band) in which thermal noise predominantly occurs using the first-type operational amplifier OP**1** mainly designed to reduce thermal noise. As a result, the thermal noise of the sensitivity adjustment circuit **80** can be reduced, whereby the SNR of the entire system can be increased.

The synchronous detection circuit **100** performs synchronous detection based on the synchronization signal CLK from the driver circuit **40**. The synchronous detection circuit **100** includes a switching element SE**1** ON/OFF-controlled based on the synchronization signal CLK, and a switching element SE**2** ON/OFF-controlled based on an inversion synchronization signal CLKN. The synchronous detection circuit **100** performs synchronous detection using a single balanced mixer method. A signal VS**5** is input to the switching element SE**1**, and an inversion signal VS**5**N of the signal VS**5** is input to the switching element SE**2**.

FIG. **21** shows a signal waveform example illustrative of synchronous detection. As shown in FIG. **21**, the input signal VS**5** is output to the output terminal as the signal VS**6** in a first period T**1** in which the synchronization signal CLK is set at the H level, and the inversion signal VS**5**N of the input signal VS**5** is output to the output terminal as the signal VS**6** in a second period T**2** in which the synchronization signal CLK is set at the L level. The gyrosensor output signal (desired signal) can be detected and extracted by synchronous detection. Note that the synchronous detection circuit **100** may utilize a double balanced mixer method.

In FIG. **20**, the synchronous detection circuit **100** includes an offset adjustment circuit **90** (zero-point adjustment circuit). The offset adjustment circuit **90** removes an initial offset voltage (offset voltage) of the output signal VSQ of the detection device **30**. For example, the offset adjustment circuit **90** performs an offset adjustment process so that the voltage of the output signal VSQ coincides with the reference output voltage at a typical temperature of 25° C.

The offset adjustment circuit **90** includes a D/A conversion circuit **92** and an adder circuit (adder-subtracter circuit) **94**. The D/A conversion circuit **92** converts initial offset adjustment data DDA into an analog initial offset adjustment voltage VA.

The adder circuit **94** adds the adjustment voltage VA from the D/A conversion circuit **92** to the voltage of the input signal VS**5**. The adder circuit **94** includes resistors RE**1**, RE**2**, and RE**3** respectively provided between a node NE**5** and nodes

NE6, NE1, and NE2. The adder circuit **94** also includes an operational amplifier OPE of which the inverting input terminal is connected with the node NE5 and the noninverting input terminal is connected with a node of the voltage AGND. In FIG. **20**, a modification may be made in which the offset adjustment circuit **90** is not provided in the synchronous detection circuit **100**.

With regard to the unnecessary signals described with reference to FIGS. **16**A to **16**C, an unnecessary signal caused by the detuning frequency Δf=|fd−fs| occurs when a signal having the detection-side resonance frequency fs is mixed into the gyrosensor detection signal and the resulting detection signal is synchronously detected by the synchronous detection circuit **100**. For example, the detection vibrator may be allowed to vibrate (idle) with a small amplitude at the natural resonance frequency fs in order to improve the response of the gyrosensor. Or, the detection vibrator may vibrate at the natural resonance frequency fs when external vibration from the outside of the gyrosensor is applied to the vibrator. When the detection vibrator vibrates at the frequency fs, a signal having the frequency fs is mixed into the signal VS**5** input to the synchronous detection circuit **100**. Since the synchronous detection circuit **100** performs synchronous detection based on the synchronization signal CLK having the frequency fd, an unnecessary signal having the detuning frequency Δf=|fd−fs| corresponding to the difference between the frequencies fd and fs is generated.

The detuning frequency Δf=|fd−fs| is sufficiently lower than the frequencies fd and fs. Therefore, steep attenuation characteristics shown in FIG. **22** are necessary to remove the unnecessary signal of the component having the detuning frequency Δf. Therefore, it is difficult to remove the unnecessary signal of the component having the detuning frequency Δf using only a continuous-time low-pass filter.

In order to solve the above problem, a switched-capacitor filter (SCF) **114** (discrete-time filter) is provided in the filter section **110** in FIG. **20**. The SCF **114** has frequency characteristics of removing the component having the detuning frequency Δf−|fd−fs| corresponding to the difference between the driving-side resonance frequency fd and the detection-side resonance frequency fs of the vibrator and allowing the frequency component (DC component) of the desired signal to pass through. The filter section **110** also includes a prefilter **112** provided in the preceding stage of the SCF **114**, and an output circuit **116** which is provided in the subsequent stage of the SCF **114** and functions as an output buffer and a postfilter. The prefilter **112** and the output circuit **116** are continuous-time filters.

The steep attenuation characteristics shown in FIG. **22** are easily realized by providing the SCF **114** (discrete-time filter in a broad sense) in the filter section **110**, as shown in FIG. **20**. Therefore, even if the detuning frequency Δf is extremely lower than the frequency fd, the component of the unnecessary signal in the frequency band of the detuning frequency Δf can be reliably and easily removed without adversely affecting the desired signal in the pass band.

As shown in FIG. **20**, the SCF **114** includes switched capacitor circuits **210**, **212**, and **214**, capacitors CG4, CG5, CG6, and CG7, and operational amplifiers OPG1 and OPG2. The configuration of the SCF **114** is not limited to the configuration shown in FIG. **20**. Various known configurations may be used.

When providing the SCF **114** in the filter section **110** as shown in FIG. **20**, since the SCF **114** samples the signal in discrete time, aliasing occurs which is a frequency fold-over phenomenon caused by sampling.

In order to prevent an adverse effect of such aliasing, the anti-aliasing prefilter **112** (continuous-time filter in a broad sense) is provided in the preceding stage of the SCF **114** in FIG. **20**. Specifically, when the sampling frequency is fsp (=fd), the prefilter **112** has anti-aliasing frequency characteristics of removing frequency components equal to or higher than the frequency fsp/2 (=fd/2).

In this case, the frequency band of the desired signal is fa**0** or less (i.e., the frequency of the desired signal is low), as shown in FIG. **22**, for example. On the other hand, the sampling frequency fsp of the SCF **114** is 50 to 500 times the frequency fa**0** (i.e., the sampling frequency fsp is high), for example. Therefore, steep attenuation characteristics are unnecessary when using a normal anti-aliasing prefilter.

However, it was found that a sensor processing a weak signal such as a gyrosensor cannot remove an unnecessary signal utilizing normal anti-aliasing attenuation characteristics. Specifically, the amplitude of the unnecessary signal included in the gyrosensor detection signal is about 100 to 500 times the amplitude of the desired signal, for example. Therefore, the amplitude of the unnecessary signal becomes higher than the amplitude of the desired signal (DC component) when utilizing normal anti-aliasing attenuation characteristics, whereby the SNR deteriorates due to the fold-over effect on the DC component caused by sampling of the SCF **114**, for example.

Therefore, the prefilter **112** (continuous-time filter) preferably has frequency characteristics (filtering characteristics or attenuation characteristics) of attenuating the amplitude of the unnecessary signal, which appears in the frequency band of the frequency k×fd (k is a positive integer) due to synchronous detection by the synchronous detection circuit **100**, to a value equal to or smaller than the amplitude of the desired signal (minimum resolution). The amplitude of the desired signal corresponds to the minimum resolution of the desired signal, and corresponds to degrees per second (dps). The amplitude of the desired signal is the amplitude of the desired signal in the DC frequency region.

Therefore, even if the unnecessary signal having an amplitude about 100 to 500 times the amplitude of the desired signal appears at the frequency k×fd, the frequency component of the unnecessary signal can be reliably removed using the prefilter **112**.

In this embodiment, the second supply circuit **22** of the reference voltage supply circuit **20** supplies the voltage AGND (analog reference voltage) to the prefilter **112** (continuous-time filter) and the SCF **114** (discrete-time filter) using the reference-voltage second-type operational amplifier OP2 described with reference to FIGS. **5**B, **5**C, and **11**B. The fourth supply circuit **24** described with reference to FIG. **19** supplies the voltage AGND to the output circuit **116** by using the reference-voltage second-type operational amplifier OP**2**. Specifically, the second supply circuit **22** supplies the voltage AGND to the operational amplifiers OPH, OPG**1**, and OPG**2**, and the fourth supply circuit **24** supplies the voltage AGND to the operational amplifier OP**1**. It is also desirable to use the second-type operational amplifiers as the operational amplifiers OPH, OPG**1**, OPG**2**, and OP**1**.

In FIG. **20**, the SCF **114** with steep attenuation characteristics is used to remove the unnecessary signal due to the detuning frequency. The operational amplifiers OPG**1** and OPG**2** are necessary in order to realize the SCF **114**.

In FIG. **20**, the anti-aliasing prefilter **112** is also used as a filter which removes the unnecessary signal which appears at the frequency k×fd due to synchronous detection. Therefore, a second-order active low-pass filter is used as the prefilter

112, for example. The operational amplifier OPH is required for realizing the active low-pass filter.

In FIG. 20, the output circuit 116 functions as the output buffer which subjects the output signal VSQ to impedance conversion and also functions as the postfilter for the SCF 114. The operational amplifier OP1 is required for realizing the function of the output buffer and the function of the postfilter.

As described above, the operational amplifiers OPH, OPG1, OPG2, and OP1 are provided in the filter section 110, and the SNR of the entire system deteriorates to a large extent when these operational amplifier have a high noise level.

In this embodiment, the voltage AGND can be supplied to the operational amplifiers OPH, OPG1, OPG2, and OP1 which process the signal in a low frequency band (frequency band of desired signal) in which flicker noise predominantly occurs using the second-type operational amplifiers OP2 mainly designed to reduce flicker noise. Therefore, even if these operational amplifiers are used, the flicker noise of the filter section 110 can be minimized, whereby the SNR of the entire system can be increased.

4. Electronic Instrument

FIG. 23 shows a configuration example of a gyrosensor 510 (sensor in a broad sense) including the detection device 30 according to this embodiment, and an electronic instrument 500 including the gyrosensor 510. The electronic instrument 500 and the gyrosensor 510 are not limited to the configuration shown in FIG. 23. Various modification may be made such as omitting some elements or adding another element. As the electronic instrument 500 according to this embodiment, various electronic instruments such as a digital camera, a video camera, a portable telephone, a car navigation system, a robot, a game machine, and a personal digital assistant may be considered.

The electronic instrument 500 includes the gyrosensor 510 and a processing section 520. The electronic instrument 500 may also include a memory 530, an operation section 540, and a display section 550. The processing section (e.g., CPU or MPU) 520 controls the gyrosensor 510 and the like, and controls the entire electronic instrument 500. The processing section 520 performs processes based on information (angular velocity information or physical quantity) detected by the gyrosensor 510. For example, the processing section 520 performs processes for image blur correction, position control, GPS autonomous navigation, and the like based on the detected angular velocity information. The memory (e.g. ROM or RAM) 530 stores a control program and various types of data, and functions as a work area and a data storage area. The operation section 540 allows the user to operate the electronic instrument 500, and the display section 550 displays various types of information for the user. The detection device 30 according to this embodiment allows a small sensor to be employed as the gyrosensor 510 incorporated in the electronic instrument 500. This enables a reduction in size and cost of the electronic instrument 500.

Although only some embodiments of the invention have been described in detail above, those skilled in the art would readily appreciate that many modifications are possible in the embodiments without materially departing from the novel teachings and advantages of the invention. Accordingly, such modifications are intended to be included within the scope of the invention. Any term (e.g. vibrator, gyrosensor, AGND, or SCF) cited with a different term (e.g. physical quantity transducer, sensor, analog reference voltage, or discrete-time filter) having a broader meaning or the same meaning at least once in the specification and the drawings can be replaced by the different term in any place in the specification and the drawings. The configurations of the reference voltage supply circuit, the analog circuit, the receiver device, the detection device, and the electronic instrument are not limited to those described in the above embodiments. Various modifications and variations may be made.

What is claimed is:

1. A reference voltage supply circuit comprising:

a first supply circuit that includes a reference-voltage first-type operational amplifier and supplies an analog reference voltage to a first analog reference voltage line; and

a second supply circuit that includes a reference-voltage second-type operational amplifier and supplies the analog reference voltage to a second analog reference voltage line;

when a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage first-type operational amplifier are respectively referred to as $W1a$ and $L1a$, a bias current flowing through the differential section of the reference-voltage first-type operational amplifier is referred to as Ia, a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage second-type operational amplifier are respectively referred to as $W1b$ and $L1b$, and a bias current flowing through the differential section of the reference-voltage second-type operational amplifier is referred to as Ib, $W1b \times L1b > W1a \times L1a$ and $Ia > Ib$ being satisfied.

2. The reference voltage supply circuit as defined in claim 1,

when a frequency of an amplification target signal of a first circuit to which the analog reference voltage is supplied from the first supply circuit is referred to as $f1$, a frequency of an amplification target signal of a second circuit to which the analog reference voltage is supplied from the second supply circuit is referred to as $f2$, and a corner frequency of flicker noise and thermal noise in frequency-noise characteristics is referred to as fcr, the reference-voltage first-type operational amplifier satisfying $f1 - fcr < fcr - f2$, and the reference-voltage second-type operational amplifier satisfying $fcr - f2 < f1 - fcr$.

3. The reference voltage supply circuit as defined in claim 1,

when a channel length of an active-load-stage transistor of the differential section of the reference-voltage second-type operational amplifier is referred to as $L3b$, $L1b < L3b$ being satisfied.

4. The reference voltage supply circuit as defined in claim 1,

when a WL ratio of the differential-stage transistor of the reference-voltage first-type operational amplifier is referred to as $RT1a$ and a WL ratio of an active-load-stage transistor of the reference-voltage first-type operational amplifier is referred to as $RT3a$, $RT1a > RT3a$ being satisfied.

5. The reference voltage supply circuit as defined in claim 1,

when an effective gate voltage of the differential-stage transistor of the reference-voltage second-type operational amplifier is referred to as Veff, a drain-source current is referred to as Ids, a mobility is referred to as μ, a gate capacitance per unit area is referred to as Cox, a WL ratio is referred to as $RT1b$, a Boltzmann constant is referred to as k, an absolute temperature is referred to as T, an amount of electronic charge is referred to as q, and a process variation parameter is referred to as P ($P>1$), the WL ratio RT1*b* being set at a value satisfying the relationship $P\times(k\times T/q)>Veff=\{2\times Ids/(\mu\times Cox\times RT1b)\}^{1/2}>k\times T/q$.

6. The reference voltage supply circuit as defined in claim **1**,

when the area of an arrangement region of the differential-stage transistor of the reference-voltage second-type operational amplifier is referred to as Sdf and the area of an arrangement region of the elements forming the reference-voltage second-type operational amplifier other than the differential-stage transistor of the reference-voltage second-type operational amplifier is referred to as Sre, Sdf>Sre being satisfied.

7. The reference voltage supply circuit as defined in claim **6**,

the differential-stage transistor of the reference-voltage second-type operational amplifier including J (J>2) transistors connected in parallel; and

the J transistors connected in parallel being disposed in the arrangement region of the differential-stage transistor of the reference-voltage second-type operational amplifier.

8. The reference voltage supply circuit as defined in claim **7**, further comprising:

an active-load-stage transistor of the reference-voltage second-type operational amplifier including I (J>I>2) transistors connected in parallel; and

the J transistors forming the differential-stage transistor of the reference-voltage second-type operational amplifier being arranged along a direction X, and the I transistors forming the active-load-stage transistor being arranged along the direction X on a direction Y side of the J transistors.

9. The reference voltage supply circuit as defined in claim **1**,

the first supply circuit being a circuit which performs voltage impedance conversion using the reference-voltage first-type operational amplifier; and

the second supply circuit being a circuit which performs voltage impedance conversion using the reference-voltage second-type operational amplifier.

10. The reference voltage supply circuit as defined in claim **1**, further comprising:

a third supply circuit that is provided in a preceding stage of the first and second supply circuits, includes a reference-voltage third-type operational amplifier, and supplies a voltage to the first and second supply circuits;

when a channel width and a channel length of a differential-stage transistor of a differential section of the reference-voltage third-type operational amplifier are respectively referred to as W1*c* and L1*c* and a bias current which flows through the differential section of the reference-voltage third-type operational amplifier is referred to as Ic, $W1c\times L1c>W1a\times L1a$ and Ic>Ib being satisfied.

11. The reference voltage supply circuit as defined in claim **10**,

$W1c\times L1c>W1b\times L1b$ and Ic>Ia being satisfied.

12. An analog circuit comprising:

the reference voltage supply circuit as defined in claim **1**,

a first circuit to which the analog reference voltage is supplied from the first supply circuit of the reference voltage supply circuit through the first analog reference voltage line; and

a second circuit to which the analog reference voltage is supplied from the second supply circuit of the reference voltage supply circuit through the second analog reference voltage line.

13. The analog circuit as defined in claim **12**, further comprising:

a mixer that mixes a signal with a specific frequency into a signal including a desired signal;

the first circuit being a circuit provided on a preceding stage of the mixer; and

the second circuit being a circuit provided on a subsequent stage of the mixer.

14. The analog circuit as defined in claim **13**,

the first circuit being a first amplifier circuit which amplifies an input signal; and

the reference voltage supply circuit supplying the analog reference voltage to the first amplifier circuit through the first analog reference voltage line.

15. The analog circuit as defined in claim **13**,

the second circuit being a second amplifier circuit that amplifies the mixed signal from the mixer or a filter section that filters the mixed signal from the mixer; and

the reference voltage supply circuit supplying the analog reference voltage to the second amplifier circuit or the filter section through the second analog reference voltage line.

16. An electronic instrument comprising:

the analog circuit as defined in claim **12**; and

a processing section that performs processes based on detection information of the analog circuit.

17. An electronic instrument comprising:

the analog circuit as defined in claim **13**; and

a processing section that performs processes based on detection information of the analog circuit.

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