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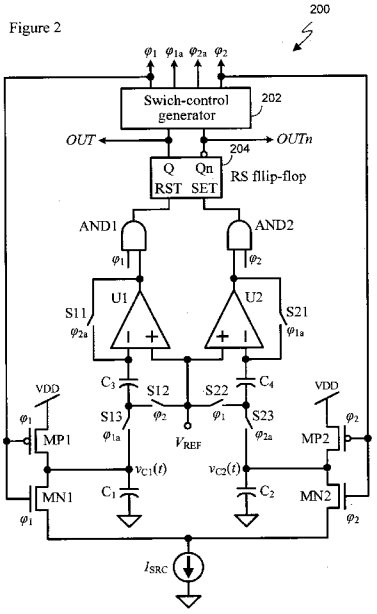
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(54) Title: A RELAXATION OSCILLATOR

Figure 2



(57) Abstract: A relaxation oscillator and a method for offset cancellation in a relaxation oscillator. The relaxation oscillator comprises two comparator units, each comparator unit comprising a comparator element and a memory element; and a switch control generator coupled to each of the comparator units; wherein each comparator unit, in a reset state, stores an input-offset voltage on the memory element under the control of the switch control generator such that, in a comparison state, the input-offset voltage is applied to both inputs of the comparator for implementing an offset-free threshold.

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A Relaxation Oscillator

FIELD OF INVENTION

The present invention relates broadly to a relaxation oscillator, and to a method for offset cancellation in a relaxation oscillator.

BACKGROUND

In a complementary metal-oxide-semiconductor (CMOS) integrated-circuit (IC) systems with extreme constrains on area and power consumption, a monolithic implementation of clock oscillator is essential.

A ring of digital logic gate with negative feed-back, (e.g. ring oscillator) is one of the possible monolithic implementation of an oscillator, and the oscillation frequency is inversely proportional to the sum of each logic gates' delay. The oscillation frequency range can cover from a few mega-hertz to giga-hertz. However, the ring oscillator suffers from huge deviation in its oscillation frequency as environmental conditions change. Therefore, the ring oscillator is almost always used with a frequency locking system such as phase-locked loop where an external reference clock is required.

For a mid-to-high frequency range, inductor-capacitor (LC) tuned oscillator is a popular choice for a time reference. Since both inductors and capacitors do not generate any intrinsic noises, the LC tuned oscillator has one of the best frequency stability. However, although modern CMOS fabrication process provides well-controlled on-chip inductance, inductors occupy significant die area that is sometimes not acceptable for an area-limited application. This becomes worse as the target oscillation frequency goes low because of the inverse proportionality between inductance and the oscillation frequency.

For a low-to-mid frequency range, a resistor-capacitor (RC) pair is another choice for a time reference. Relaxation oscillator is one of the most widely studied and

implemented oscillators that utilize readily available RC time reference on a CMOS fabrication process. Since a large RC time constant can be implemented on chip more readily than a large LC value, this oscillator occupies smaller area than LC tuned oscillator. However, monolithic relaxation oscillator circuits also suffer from large errors in oscillation period due to process and temperature variation. Beside the capacitance and resistance, the threshold value of a threshold device is also affected by process and temperature variations. An automatic offset canceling technique can be used in order to compensate for the threshold variation. However, since offset canceling techniques are based on switched-capacitor circuits, offset canceling requires an additional clock signal.

In a relaxation oscillator, a capacitor is periodically charged and discharged by a resistor (or a current source). The timing when to switch between charging and discharging is provided by threshold devices, e.g. CMOS comparators. The oscillation period is directly proportional to the capacitance-resistance product (or capacitance-to-current ratio).

Process variation affects the absolute value of the capacitance-resistance product and may cause errors as large as ±25%. However, this error can be significantly reduced if on-chip calibration for the capacitor (or resistor) is employed. Temperature variation commonly causes an increase of the capacitance-resistance product as temperature rises. This variation can be compensated for by device with a complementary temperature dependency.

A need therefore exists to provide a relaxation oscillator that seeks to address at least one of the above-mentioned problems.

SUMMARY

In accordance with a first aspect of the invention, there is provided a relaxation oscillator comprising two comparator units, each comparator unit comprising a comparator element and a memory element; and a switch control generator coupled to each of the comparator units; wherein each comparator unit, in a reset state, stores an input-offset voltage on the memory element under the control

of the switch control generator such that, in a comparison state, the input-offset voltage is applied to both inputs of the comparator for implementing an offset-free threshold.

The memory elements may comprise capacitors.

Each comparator unit may comprise an AND element coupled at respective inputs to an output of the comparator and to the switch control generator respectively, and at an output to a memory block; such that the output of the comparator is decoupled from an input of the memory block in the reset state, and coupled to the input of the memory block in the comparison state under the control of the switch signal generator.

The memory block may provide clock signals to the switch control generator based on current states of the comparator units.

The memory block may comprise an RS flip-flop.

Each comparator may comprise a feedback switchable under the control of the switch control generator such that the feedback is active in the reset state.

Each comparator unit may further comprise a switch coupled to the switch control generator, for charging of the memory element from a reference voltage, including the input-offset voltage, in the reset state.

The switch control generator may comprise a RS flip-flop with multiple delay stages along each feedback path.

In accordance with a second aspect of the invention, there is provided a method for offset cancellation in a relaxation oscillator, the method comprising the steps of for each of two comparators, storing an input-offset voltage on a memory element in a reset phase; and applying, in a comparison phase, a reference voltage, including the input-offset voltage, at a first input of the respective comparators and simultaneously applying the input-offset voltage from the memory element at a

second input of the respective comparators for implementing an offset-free threshold.

The method may further comprise decoupling an output of the respective comparators from an input of a memory block in the reset phase, and coupling the output to the input of the memory block in the comparison phase.

The method may further comprise implementing a time delay between decoupling the output of the comparators from the input of the memory block, and entering the reset state for the respective comparators.

The method may further comprise implementing a time delay between entering the comparison state for the respective comparators, and coupling the outputs of the respective comparators to the input of the memory block.

The amount of delay may be controlled by a selected number of delay stages in a switch control generator of the relaxation oscillator.

The memory block may provide clock signals for generating switch control signals based on current states of the comparators.

The method may further comprise applying a feedback across the respective comparator in the reset phase.

The method may comprise charging of the memory element from a reference voltage, including the input-offset voltage, in the reset state.

The switch control generator may comprise a RS flip-flop with two delay stages along each feedback path.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1 shows a schematic circuit diagram illustrating a conventional implementation of a relaxation oscillator.

Figure 2 shows a schematic circuit diagram of a relaxation oscillator according to an example embodiment.

Figure 3 shows a schematic circuit diagram of a switch-control generator according to an example embodiment.

Figure 4 shows graphs illustrating the input-output signal-timing diagram, according to an example embodiment.

Figure 5 shows a schematic circuit diagram of only the activated connections of the relaxation oscillator according to an example embodiment in the set stage.

Figure 6 shows a schematic circuit diagram of only the activated connections of the relaxation oscillator according to an example embodiment in the reset stage.

Figure 7 is a diagram showing simulated results of variations in the oscillation period as a function of ambient temperature comparing a relaxation oscillator according to an example embodiment, and a conventional relaxation oscillator.

Figure 8 is a graph showing peak-to-peak variations in the oscillation period as a result of process variation, as a function of temperature, comparing a relaxation oscillator according to an example embodiment, and a conventional relaxation oscillator.

Figure 9 shows a flowchart illustrating a method for offset cancellation in a relaxation oscillator, according to an example of embodiment.

Figure 10 shows a flowchart illustrating a method for the comparators to make transitions between the set stage and the reset stage depending on each capacitor's voltage, according to an example embodiment.

DETAILED DESCRIPTION

The example embodiments described can provide for cancelling errors in the oscillation period due to comparator input-offset voltages, without the need for external signals the example embodiments compensate for the threshold variation with self-clocked offset cancelling comparators.

Before description of the example embodiments, in the following a conventional implementation of a relaxation oscillator will be described with reference to Figure 1.

Figure 1 shows a conventional implementation of a relaxation oscillator 100. The two capacitors, C_1 and C_2 are alternately charged and discharged depending on the state of the RS flip-flop 102. The input-referred offset voltage of the comparators, U1 and U2 are modeled as V_{OFF1} and V_{OFF2}, respectively.

Assume that, at time t=0, C_1 is charged to VDD. Also assume that the RS flip-flop is in the *set* state at t=0. This state causes transistor MN1 to be turned on while MP1 is turned off; the voltage across C_1, $v_{C1}(t)$ decreases, starting from $v_{C1}(0)$=VDD, as C_1 is discharged by the constant current source, I_{SRC}. If we denote the time duration when the RS flip-flop is in the set state as τ_H, $v_{C1}(t)$ is found out to be as follows.

$$\begin{aligned} v_{C1}(t) &= v_{C1}(0) - \frac{1}{C_1}\int_0^t I_{SRC}\,dt \\ &= \mathrm{VDD} - \frac{I_{SRC}}{C_1}\cdot t \quad \text{for } 0 \le t < \tau_H . \end{aligned} \tag{1}$$

At the same time, MP2 is turned on while MN2 is off. This makes C_2 to be clamped to VDD. Thus the output of U2 is held low.

While continuously compared by U1, $v_{C1}(t)$ reaches the trip point of U1, i.e. $V_{REF}+V_{OFF1}$ at $t=\tau_H$ then the output of U1 goes high causing the RS flip-flop 102 to transit to the *reset* state. τ_H can be found by letting $t=\tau_H$ and $v_{C1}(t)=V_{REF}+V_{OFF1}$ into (1) and solving it for τ_H as follows.

$$\tau_H = \frac{C_1}{I_{SRC}}(VDD - V_{REF} - V_{OFF1}). \quad (2)$$

The transition of the RS flip-flop 102 to the reset state causes MP1 to be turned on while MN1 is turned off. Then $v_{C1}(t)$ is rapidly increased back to VDD making the output of U1, i.e. the RST input of the RS flip-flop 102 to be low again. At the same time, MN2 is turned on while MP2 is turned off. The voltage across C_2, $v_{C2}(t)$ decreases as C_2 is discharged by I_{SRC}. Since C_2 was charged to VDD during the previous state of the RS flip-flop 102, $v_{C2}(t)$ starts from VDD. If we denote the time duration when the RS flip-flop 102 is in the reset state as τ_L, $v_{C2}(t)$ during the reset state is defined as follows.

$$v_{C2}(t) = VDD - \frac{I_{SRC}}{C_2} \cdot t \quad \text{for } \tau_H \le t < (\tau_H + \tau_L). \quad (3)$$

While continuously compared by U2, $v_{C2}(t)$ reaches the trip point of U2, i.e. $V_{REF}+V_{OFF2}$ at $t=\tau_H+\tau_L$. τ_L can be found by letting $t=\tau_H+\tau_L$ and $v_{C2}(\tau_H+\tau_L)=V_{REF}+V_{OFF2}$ into (3) and solving it for τ_L as follows.

$$\tau_L = \frac{C_2}{I_{SRC}}(VDD - V_{REF} - V_{OFF2}). \quad (4)$$

At $t=\tau_H+\tau_L$, the output of U2 goes high causing the RS flip-flop to be set again, and completing an oscillation cycle. Therefore, the oscillation period of the relaxation oscillator 100, t_{OSC} is given as follows.

$$\begin{aligned} t_{OSC} &= t_H + t_L \\ &= \frac{C_1 + C_2}{I_{SRC}}(VDD - V_{REF}) + \frac{C_1}{I_{SRC}}V_{OFF1} + \frac{C_2}{I_{SRC}}V_{OFF2}. \end{aligned} \quad (5)$$

Figure 2 shows a schematic diagram of a relaxation oscillator 200 according to an example embodiment. C_3 and C_4 are added in addition to C_1 and C_2 to store and cancel out the input-offset voltage of each comparator U1 and U2. A switch-control generator 202 is added to generate φ_1, φ_{1a}, φ_2 and φ_{2a}.

Figure 3 shows a circuit diagram of the switch-control generator 202 and Figure 4 shows the input-output signal-timing diagram 400 of the switch-control generator 102. The switch-control generator 202 comprises a RS flip-flop 300 where two delay stages 302, 304 and 306, 308 are placed along each feedback path 310, 312. As shown in Figure 4, φ_1 and φ_{1a} do not overlap with φ_2 and φ_{2a}. Also note that φ_{1a} and φ_{2a} turn on-and-off slightly earlier than φ_1 and φ_2, respectively. With reference to Figure 2, S11 and S21 are controlled by φ_{2a} and φ_{1a}, respectively. By turning off S11 and S21 earlier than S12 and S22, charge injections from S12 and S22 can advantageously be reduced.

It is understood in the art to employ cascaded offset cancelling comparator(s) in order to further reduce charge injections. Assuming that there are two cascaded offset cancelling comparators and let φ_{1b} and φ_{2b} be the feedback control signals for the additional comparator. In this case, φ_{1b} and φ_{2b} should be turned on-and-off slightly later than φ_{1a} and φ_{2a} but earlier than φ_1 and φ_2. One can readily generate φ_{1b} and φ_{2b} by using one more delay stage along each feedback path 310, 312. This can be expanded to n-stages of cascaded comparator(s) with n+1 delay stages.

Figure 5 shows only the activated connections of the relaxation ozillator 200a when the RS flip-flop is in the set state, i.e. $Q=\varphi_1=\varphi_{1a}=high$ while $Qn=\varphi_2=\varphi_{2a}=low$. Both U1 and U2 have an input-offset voltage error that is modelled by V_{OFF1} and V_{OFF2}, respectively. It is assumed that C_1 is initially charged to VDD and C_3 to V_{OFF1}. The voltage across C_1, $v_{C1}(t)$ decreases linearly as C_1 is being discharged by the constant current source, I_{SRC}. The voltage at the inverting input of U1, $v_{IN1-}(t)$ is given by $v_{C1}(t)+V_{C3}$ where V_{C3} denotes the voltage across C_3. Since V_{C3} is assumed to be V_{OFF1}, U1 compares $v_{IN1-}(t)=v_{C1}(t)+V_{OFF1}$ with $V_{REF}+V_{OFF1}$ cancelling out V_{OFF1}. On the other hand, the voltage across C_2, $v_{C2}(t)$ is clamped to VDD. The voltage at the inverting input of U2, $v_{IN2-}(t)$ is given by $V_{REF}+V_{OFF2}$ due to the negative feedback across U2. Since the bottom-side of C_4 is connected to V_{REF}, C_4 is charged to V_{OFF2}. An AND gate, AND2, is inserted between U2 and the RS flip-flop 202. During $\varphi_2=low$, U2 is disconnected from the SET input of the RS flip-flop. This is to prevent the RS flip-flop from being set by the output of U2 when U2 is in the follower configuration.

Once the output of U1 is asserted high, the RS flip-flop 204 proceeds to the reset state. Figure 6 shows only the activated connections of the relaxation oscillator

200b in the reset state, i.e. Q=φ_1=φ_{1a}=*low* while Qn=φ_2=φ_{2a}=*high*. Just after the RS flip-flop 204 is reset by U1, C_1 is disconnected from U1, and then rapidly charged back to VDD. In order to prevent the RS flipflop 204 from being reset erroneously by charging C_1 to VDD, AND1 decouples U1 from the RS flipflop 204 at the moment when C_1 is being charged to VDD. Note that this happens before the feedback of U1 is activated by φ_{2a}. Therefore, any glitches that can be seen at the output of U1 during activation of U1's feedback are also decoupled from the RS flipflop. The negative feedback across U1 is activated, thus $v_{IN1-}(t)$ is driven to $V_{REF}+V_{OFF1}$ storing V_{OFF1} into C_3; this corresponds to the initial assumption for C_3. The AND gate, AND1, hold its output low causing the RST input of the RS flip-flop 204 to be low again. Since C_4 has been charged to V_{OFF2} during the previous state (i.e. the set state), $v_{IN2-}(t)$ is given by $v_{C2}(t)+V_{OFF2}$. Then U2 compares $v_{IN2-}(t)$ with the voltage at the non-inverting input, i.e. $V_{REF}+V_{OFF2}$. Both the inverting and non-inverting inputs of U2 have the term V_{OFF2} causing V_{OFF2} to be cancelled out during the comparison. Once $v_{IN2-}(t)$ reaches $V_{REF}+V_{OFF2}$, U2 sets the RS flip-flop 204 again by asserting its output high. This completes one oscillation cycle.

Mathematically, $v_{C1}(t)$ during the RS flip-flop 204 being in the set state can be expressed as follows.

$$v_{C1}(t) = \mathrm{VDD} - \frac{I_{SRC}}{C_1} \cdot t. \tag{6}$$

Therefore, $v_{IN1-}(t)$ during the set state becomes

$$v_{IN1-}(t) = v_{C1}(t) + V_{C3}. \tag{7}$$

Since $v_{IN1-}(t)$ is compared with $V_{REF}+V_{OFF1}$, the time duration τ_H when the RS flip-flop 204 stays in the set state can be found to be

$$\tau_H = \frac{C_1}{I_{SRC}}(\mathrm{VDD} - V_{REF} + V_{C3} - V_{OFF1}). \tag{8}$$

The time duration τ_L when the RS flip-flop 204 stays in the reset state also can be found symmetrically to be

$$\tau_L = \frac{C_2}{I_{SRC}}(VDD - V_{REF} + V_{C4} - V_{OFF2}). \quad (9)$$

Therefore, the oscillation period, t_{OSC} becomes.

$$\begin{aligned} t_{OSC} &= \tau_H + \tau_L \\ &= \frac{VDD - V_{REF}}{I_{SRC}}(C_1 + C_2) + \frac{C_1}{I_{SRC}}(V_{C3} - V_{OFF1}) + \frac{C_2}{I_{SRC}}(V_{C4} - V_{OFF2}). \end{aligned} \quad (10)$$

Since the $V_{C3}=V_{OFF1}$ and $V_{C4}=V_{OFF2}$, the second and the third term of (10) cancel out and thus we can write t_{OSC} as follows.

$$t_{OSC} = \frac{VDD - V_{REF}}{I_{SRC}}(C_1 + C_2). \quad (11)$$

In equation (11), the dependency of the oscillation period on the input-offset voltage errors, V_{OFF1} and V_{OFF2} is cancelled out, advantageously providing cancelling of errors in the oscillation period due to comparator input-offset voltages in the example embodiment. As will be appreciated by a person skill in the art, this cancellation in the example embodiment does not require any external signals, thus addressing one of the problems in existing relaxation oscillators with automatic offset cancelling techniques based on switch-capacitors circuits requiring an additional clock signal.

Figure 10 shows a flowchart 1000 illustrating a method for offset cancellation in the relaxation oscillator 200 (Figure 2), in this example embodiment. After power on at step 1002, C1 is discharged, C2 is clamped to VDD and at U2, $V_{C4}=V_{OFF2}$ during the cycle where the condition in step 1004 is not fulfilled. Once the condition in step 1004 is fulfilled, the RS flip flop is reset at step 1006. During the next cycle, where the condition in step 1008 is not fulfilled, C1 is clamped to VDD, C2 is discharged and at U1, $V_{C3}=V_{OFF1}$. Once the condition in step 1008 is fulfilled, the RS flip flop is set at step 1010, and the process loops back to step 1004.

It will be appreciated that the relaxation oscillator of example embodiments can be implemented utilizing readily available RC time reference on a CMOS fabrication

process. The proposed relaxation oscillator 200 (Figure 2) was simulated using a device model for 0.13-μm, 1.5V CMOS process and results were compared with those of a conventional relaxation oscillator. The reference capacitors, C_1 and C_2 are considered ideal in order to clearly see the effectiveness of the offset cancelling scheme in the example embodiment.

Figure 7 shows simulated results of variations in the oscillation period, t_{OSC} as ambient temperature change. t_{OSC} according to an example embodiment (curve 700) shows 65.0 PPM/°C of sensitivity to temperature whereas the conventional relaxation oscillator (curve 702) has 153.0 PPM/°C. Figure 8 shows peak-to-peak variations in the oscillation period for approximately 99.73% of possible process variation, as a function of temperature. The proposed oscillator (curve 800) shows approximately 1% of variation in oscillation period over the investigated temperature range, whereas the conventional oscillator (curve 802) shows >10% in the worst case.

Figure 9 shows a flowchart 900 illustrating a method for offset cancellation in a relaxation oscillator, according to an example embodiment. At step 902, for each of two comparators, an input-offset voltage is stored on a memory element in a reset phase. At step 904, in a comparison stage, a reference voltage, including the input-offset voltage, is applied at a first input of the respective comparator and simultaneously the input-offset voltage from the memory element is applied at a second input of the respective comparator for implementing an offset-free threshold.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. A relaxation oscillator comprising:

two comparator units, each comparator unit comprising a comparator element and a memory element; and

a switch control generator coupled to each of the comparator units;

wherein each comparator unit, in a reset state, stores an input-offset voltage on the memory element under the control of the switch control generator such that, in a comparison state, the input-offset voltage is applied to both inputs of the comparator for implementing an offset-free threshold.

2. The oscillator as claimed in claim 1, wherein the memory elements comprise capacitors.

3. The oscillator as claimed in claims 1 or 2, wherein each comparator unit comprises an AND element coupled at respective inputs to an output of the comparator and to the switch control generator respectively, and at an output to a memory block; such that the output of the comparator is decoupled from an input of the memory block in the reset state, and coupled to the input of the memory block in the comparison state under the control of the switch signal generator.

4. The oscillator as claimed in claim 3, wherein the memory block provides clock signals to the switch control generator based on current states of the comparator units.

5. The oscillator as claimed in claim 4, wherein the memory block comprises an RS flip-flop.

6. The oscillator as claimed in any one of claims 1 to 5, wherein each comparator comprises a feedback switchable under the control of the switch control generator such that the feedback is active in the reset state.

7. The oscillator as claimed in any one of claims 1 to 6, wherein each comparator unit further comprises a switch coupled to the switch control generator,

for charging of the memory element from a reference voltage, including the input-offset voltage, in the reset state.

8. The oscillator as claimed in any one of claims 1 to 7, wherein the switch control generator comprises a RS flip-flop with multiple delay stages along each feedback path.

9. A method for offset cancellation in a relaxation oscillator, the method comprising the steps of:

for each of two comparators, storing an input-offset voltage on a memory element in a reset phase; and

applying, in a comparison phase, a reference voltage, including the input-offset voltage, at a first input of the respective comparators and simultaneously applying the input-offset voltage from the memory element at a second input of the respective comparators for implementing an offset-free threshold.

10. The method as claimed in claim 9, further comprising decoupling an output of the respective comparators from an input of a memory block in the reset phase, and coupling the output to the input of the memory block in the comparison phase.

11. The method as claimed in claim 10, further comprising implementing a time delay between decoupling the output of the comparators from the input of the memory block, and entering the reset state for the respective comparators.

12. The method as claimed in claim 10, further comprising implementing a time delay between entering the comparison state for the respective comparators, and coupling the outputs of the respective comparators to the input of the memory block.

13. The method as claimed in claims 11 or 12, wherein the amount of delay is controlled by a selected number of delay stages in a switch control generator of the relaxation oscillator.

14. The method as claimed in any one of claims 10 to 13, wherein the memory block provides clock signals for generating switch control signals based on current states of the comparators.

15. The method as claimed in any one of claims 9 to 14, further comprising applying a feedback across the respective comparator in the reset phase.

16. The method as claimed in any one of claims 9 to 15, comprising charging of the memory element from a reference voltage, including the input-offset voltage, in the reset state.

17. The oscillator as claimed in any one of claims 1 to 7, wherein the switch control generator comprises a RS flip-flop with two delay stages along each feedback path.

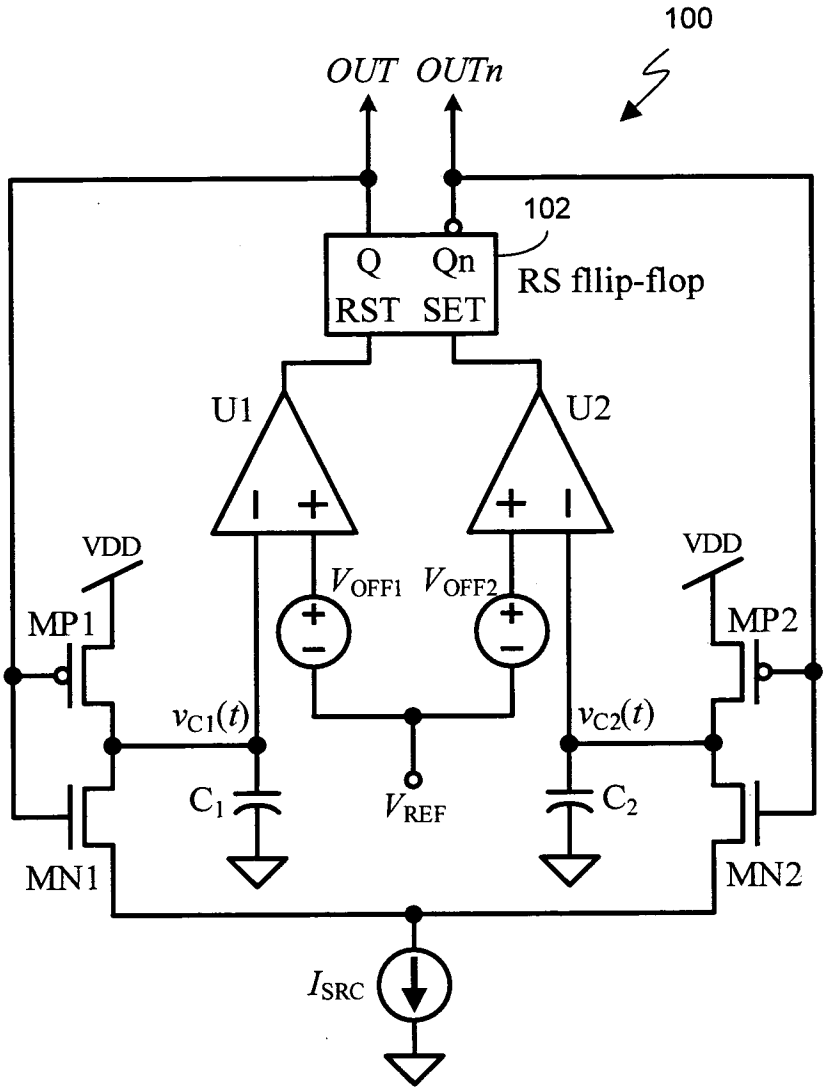

100
OUT
OUTn
102
Q
Qn
RST
SET
RS fllip-flop
U1
U2
VDD
VDD
MP1
MP2
V_{OFF1}
V_{OFF2}
$v_{C1}(t)$
$v_{C2}(t)$
C_1
C_2
V_{REF}
MN1
MN2
I_{SRC}

Figure 1

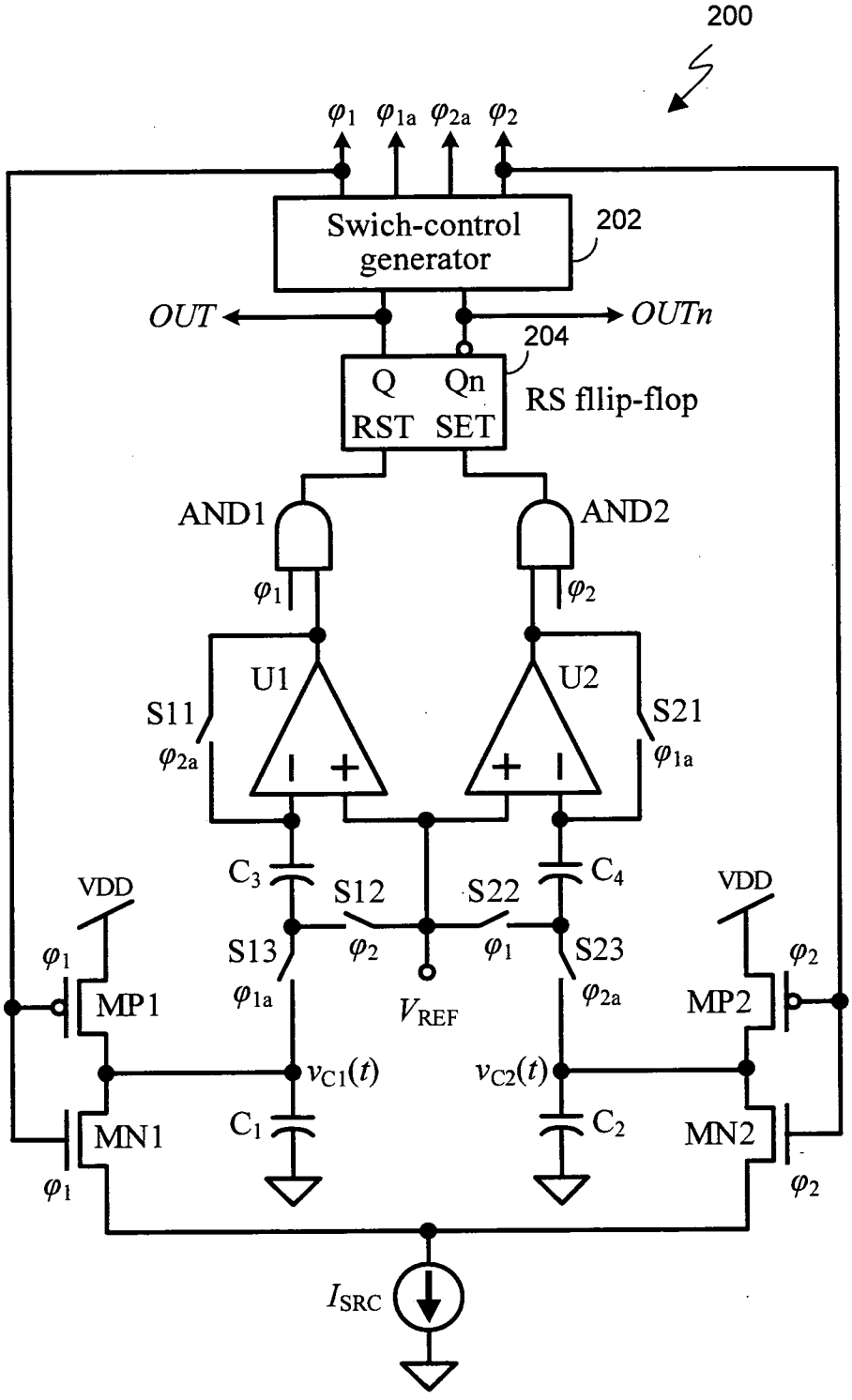

200
φ_1 φ_{1a} φ_{2a} φ_2
Swich-control generator
202
OUT
OUTn
204
Q Qn
RST SET
RS fllip-flop
AND1
AND2
φ_1
φ_2
U1
U2
S11
S21
φ_{2a}
φ_{1a}
C_3
C_4
S12
S22
VDD
VDD
S13
S23
φ_1
φ_2
φ_{1a}
φ_{2a}
MP1
MP2
V_{REF}
$v_{C1}(t)$
$v_{C2}(t)$
MN1
MN2
C_1
C_2
I_{SRC}

Figure 2

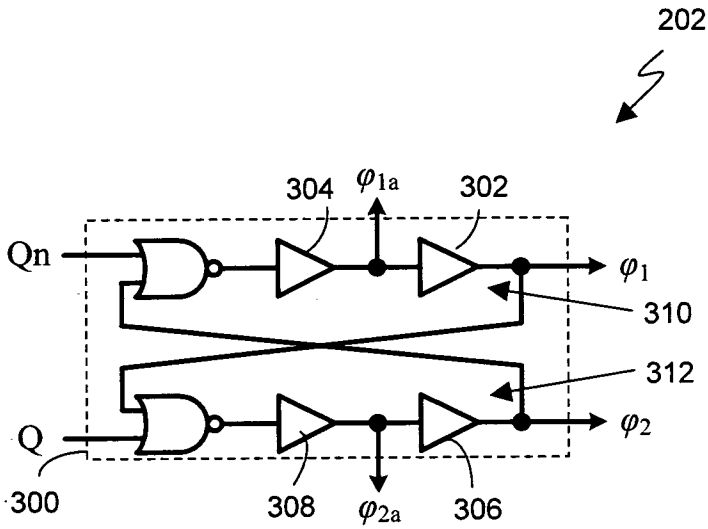

202
304
φ_{1a}
302
Qn
φ_1
310
312
Q
φ_2
300
308
φ_{2a}
306

Figure 3

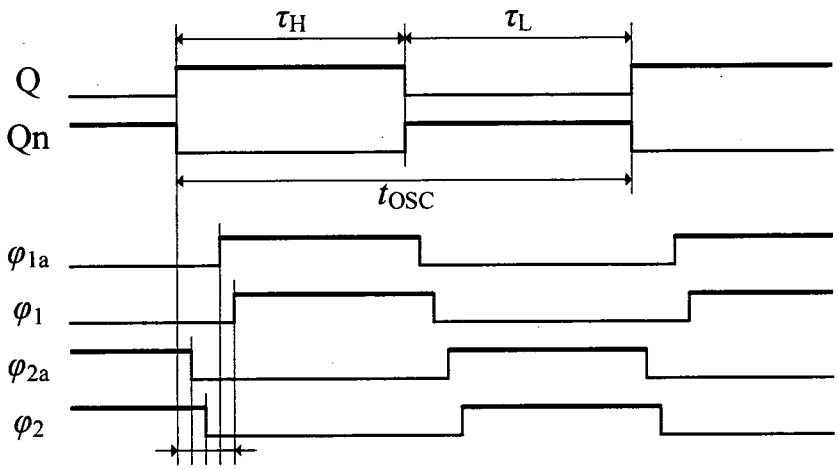


Figure 4

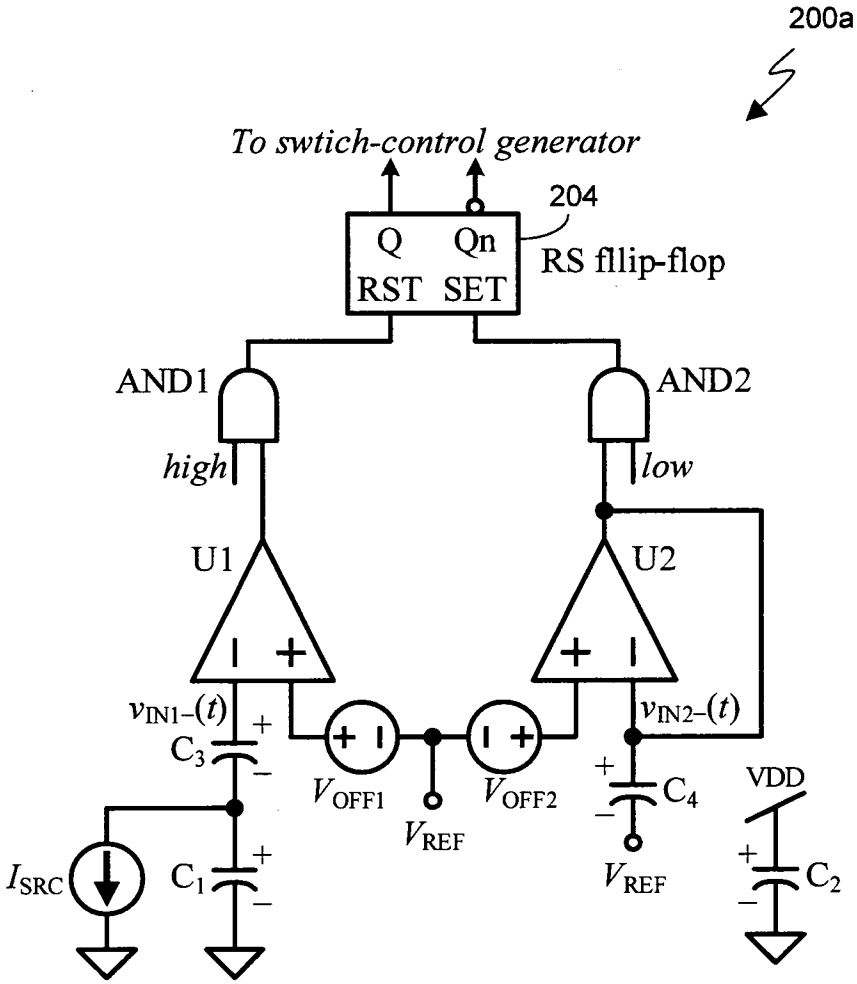

200a
To swtich-control generator
204
Q
Qn
RST
SET
RS fllip-flop
AND1
AND2
high
low
U1
U2
$v_{IN1-}(t)$
$v_{IN2-}(t)$
C_3
C_4
V_{OFF1}
V_{OFF2}
V_{REF}
V_{REF}
VDD
I_{SRC}
C_1
C_2

Figure 5

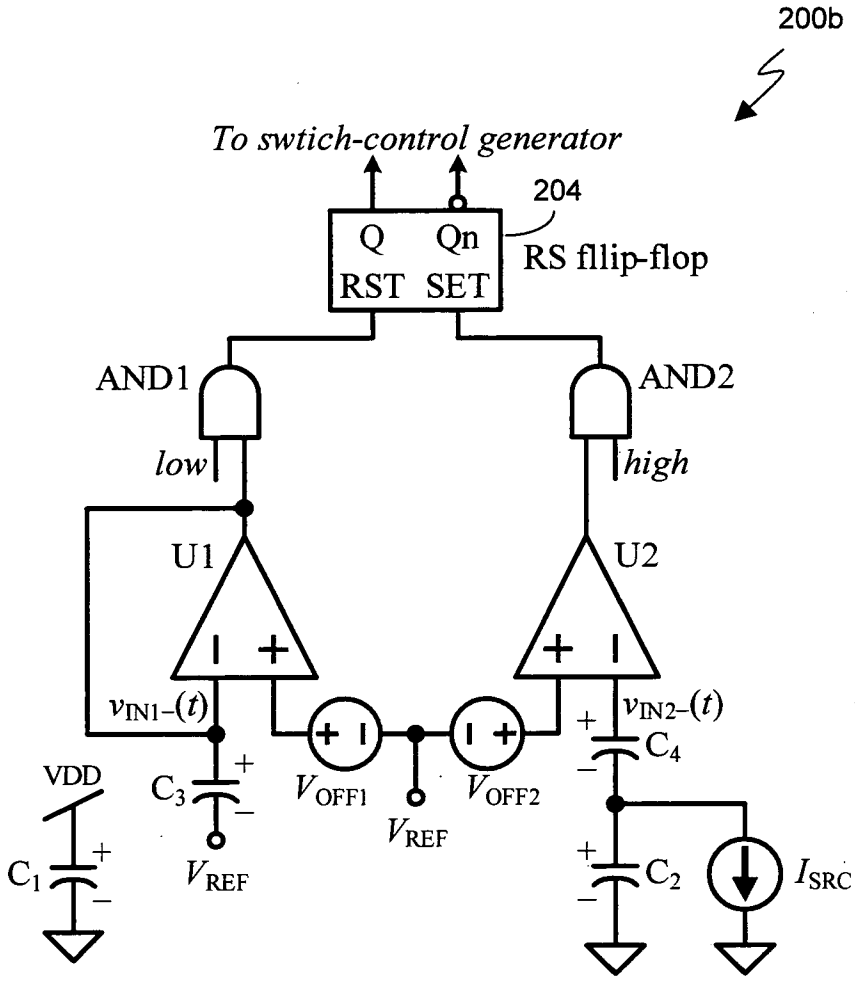

200b
To swtich-control generator
204
Q
Qn
RST
SET
RS fllip-flop
AND1
AND2
low
high
U1
U2
$v_{IN1-}(t)$
$v_{IN2-}(t)$
VDD
C_3
C_4
V_{OFF1}
V_{OFF2}
V_{REF}
V_{REF}
C_1
C_2
I_{SRC}

Figure 6

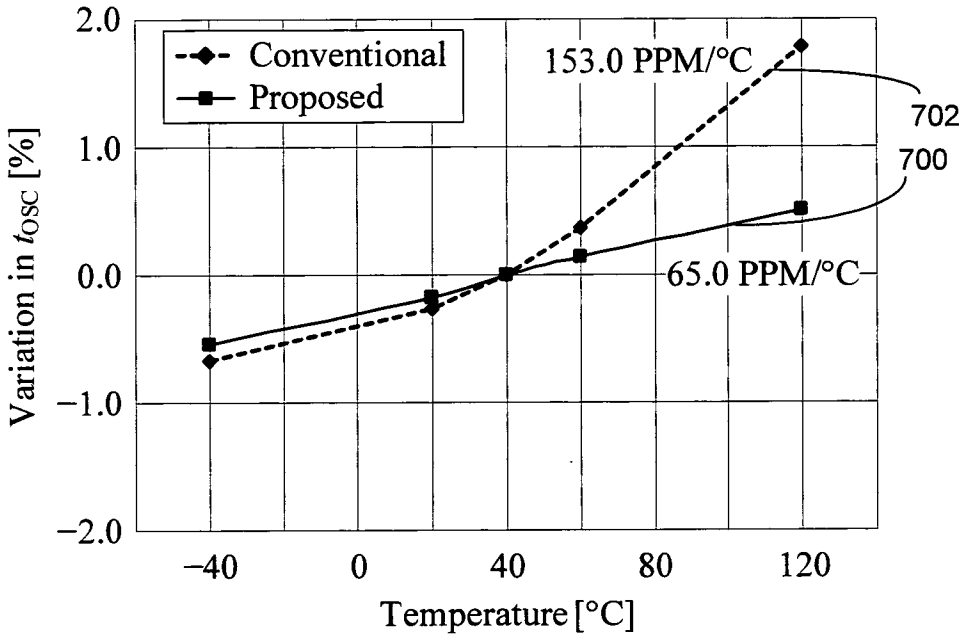

2.0
1.0
0.0
−1.0
−2.0
Variation in t_{OSC} [%]
−40
0
40
80
120
Temperature [°C]
Conventional
Proposed
153.0 PPM/°C
65.0 PPM/°C
702
700

Figure 7

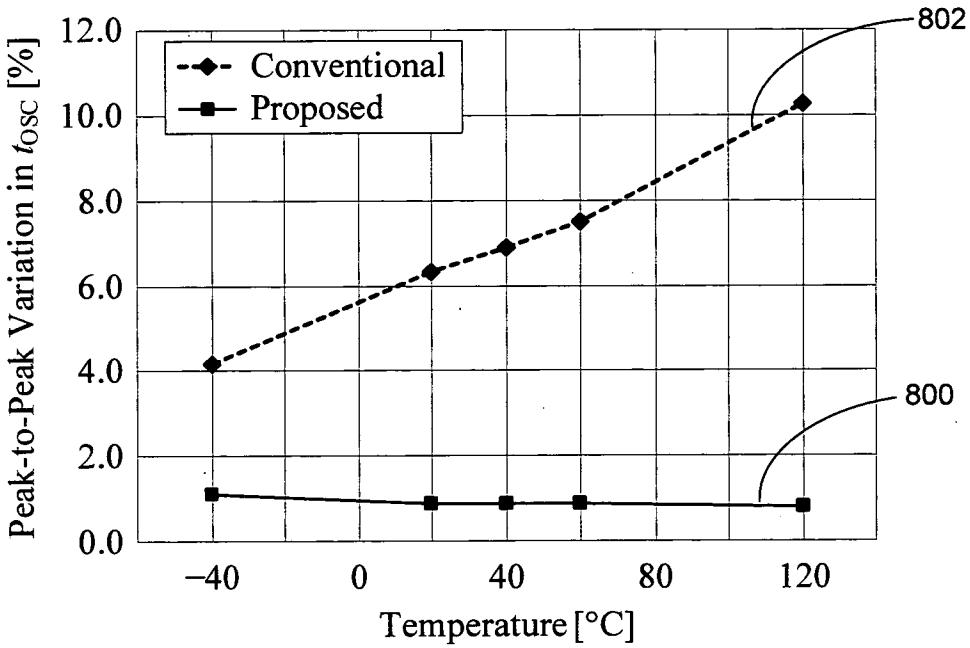

12.0
10.0
8.0
6.0
4.0
2.0
0.0
Peak-to-Peak Variation in t_{OSC} [%]
Conventional
Proposed
802
800
−40
0
40
80
120
Temperature [°C]

Figure 8

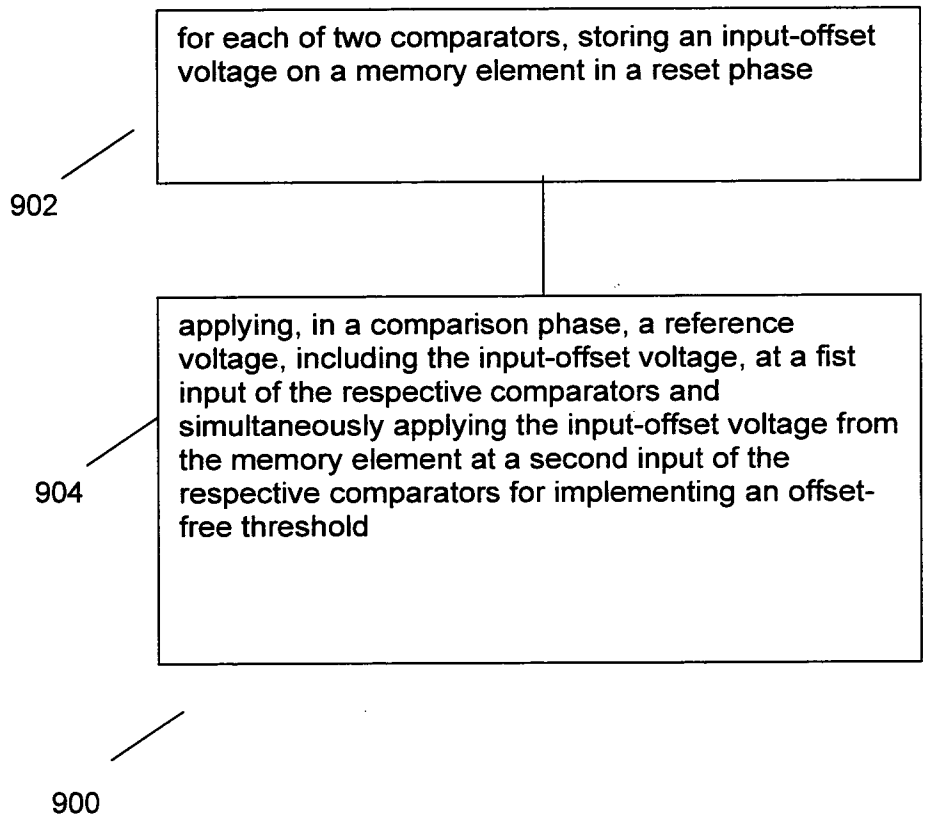

for each of two comparators, storing an input-offset voltage on a memory element in a reset phase
902
applying, in a comparison phase, a reference voltage, including the input-offset voltage, at a fist input of the respective comparators and simultaneously applying the input-offset voltage from the memory element at a second input of the respective comparators for implementing an offset-free threshold
904
900

Figure 9

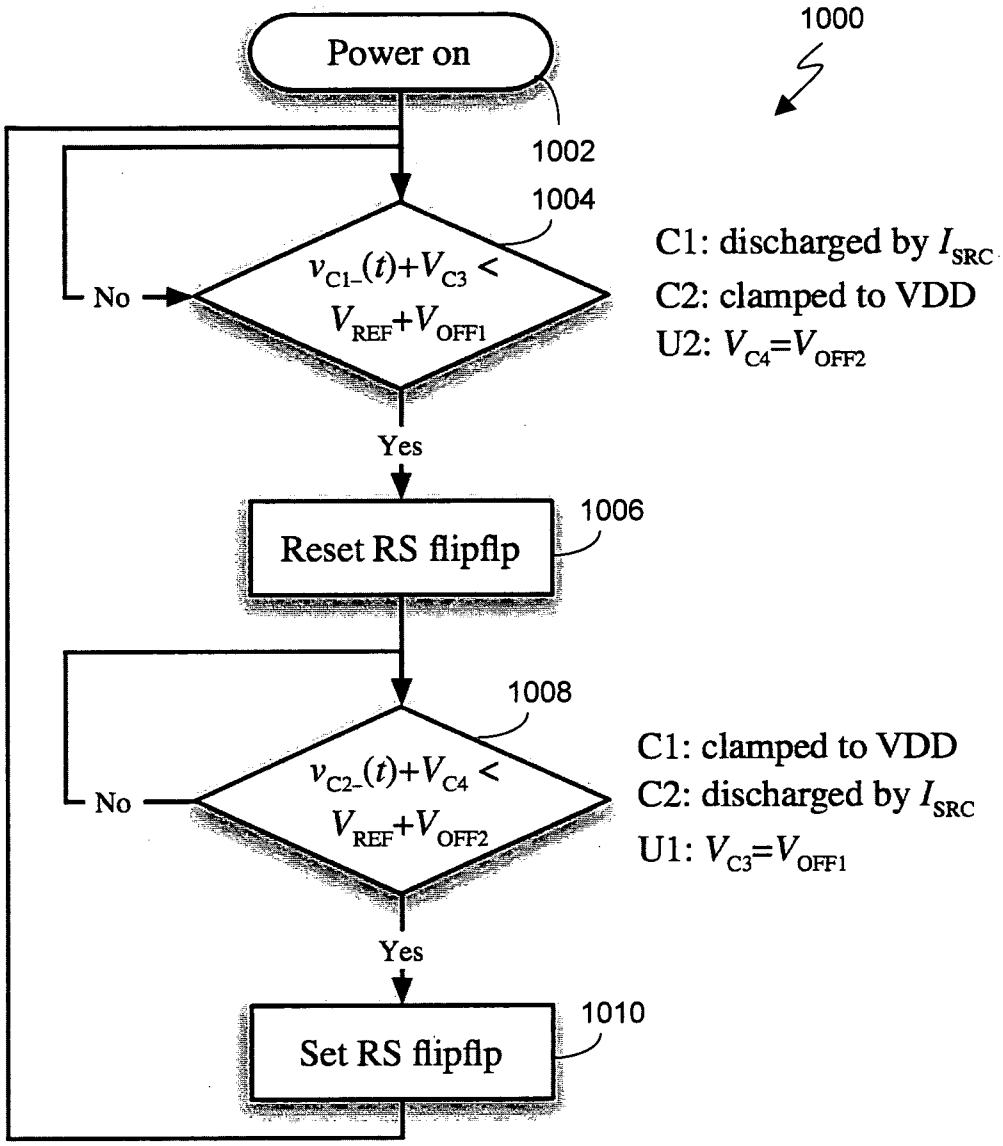

1000
Power on
1002
1004
$v_{C1}(t)+V_{C3} < V_{REF}+V_{OFF1}$
No
Yes
C1: discharged by I_{SRC}
C2: clamped to VDD
U2: $V_{C4}=V_{OFF2}$
Reset RS flipflp
1006
1008
$v_{C2}(t)+V_{C4} < V_{REF}+V_{OFF2}$
No
Yes
C1: clamped to VDD
C2: discharged by I_{SRC}
U1: $V_{C3}=V_{OFF1}$
Set RS flipflp
1010

Figure 10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000359

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H03K 3/0231 (2006.01) ***H03K 4/502*** (2006.01)
H03B 5/20 (2006.01) ***H03L 1/00*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPODOC, WPI with keywords: relaxation w oscillator?, offset 2w cancel+, comparator?, memory, switch+, control+, flip_flop, reference w voltage and similar words.
Esp@cenet, USPTO, IEEE and Google Scholar with similar keywords as above.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,356,161 B1 (NOLAN et al.) 12 March 2002 See whole document	1 – 17
A	EP 1653617 A1 (STMICROELECTRONICS S.R.L) 03 May 2006 See whole document	1 – 17
A	US 6,924,709 B2 (BASHAR) 02 August 2005 See whole document	1 – 17

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:
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"E" earlier application or patent but published on or after the international filing date
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"P" document published prior to the international filing date but later than the priority date claimed
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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 December 2008	10 DEC 2008
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. +61 2 6283 7999	Authorized officer **SHREYAS KUMAR** AUSTRALIAN PATENT OFFICE (ISO 9001 Quality Certified Service) Telephone No : +61 2 6222 3674

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2008/000359

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,565,819 A (COOPER) 15 October 1996 See whole document	1 – 17
A	US 3,873,853 (AHMED) 25 March 1975 See whole document	1 – 17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2008/000359

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	6356161	CN	1296665	CN	1535499	EP	0944169
		EP	1053596	EP	1142114	JP	11298299
		US	6020792	US	6052035	WO	0036745
		WO	0076069				
EP	1653617	US	2006103477				
US	6924709	US	2005077971				
US	5565819	EP	0780035	WO	9703497		
US	3873853	AU	72118/74	CA	1015410	CH	581352
		DE	2437867	FR	2240578	GB	1466771
		JP	50072163	NL	7410395	SE	7410113

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX